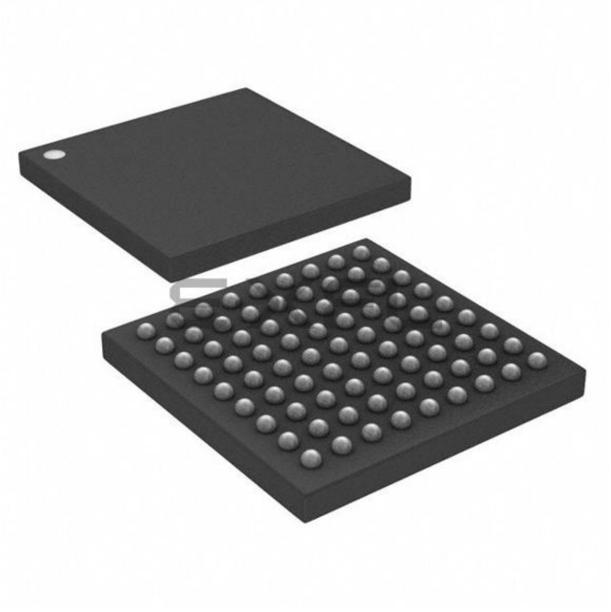
Microchip Technology - AGLN030V5-ZUCG81 Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	768
Total RAM Bits	-
Number of I/O	66
Number of Gates	30000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-20°C ~ 85°C (TJ)
Package / Case	81-WFBGA, CSBGA
Supplier Device Package	81-UCSP (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/agln030v5-zucg81

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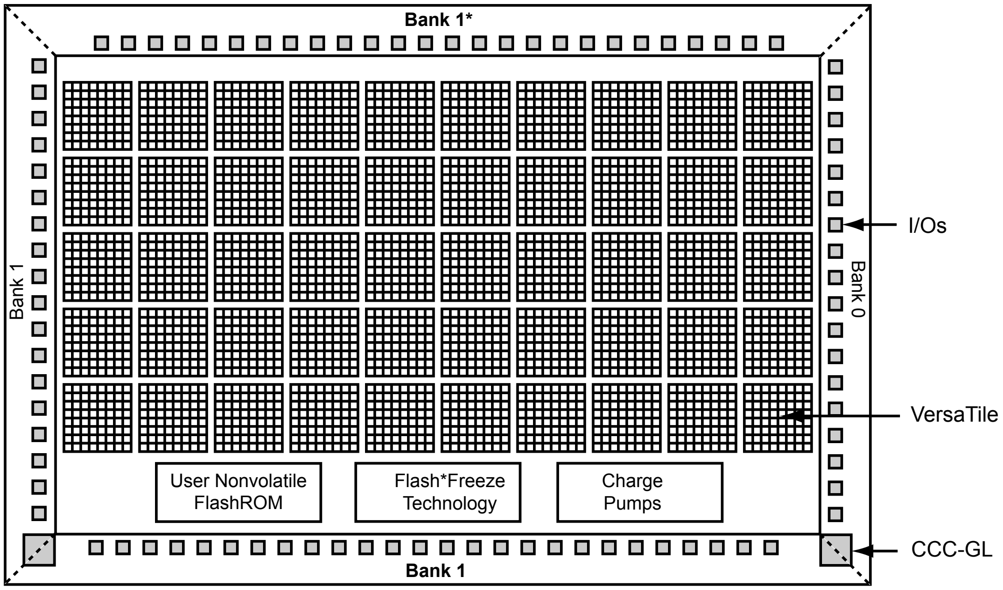


Note: **Bank 0 for the AGLN030 device*

Figure 1-1 • **IGLOO Device Architecture Overview with Two I/O Banks and No RAM (AGLN010 and AGLN030)**

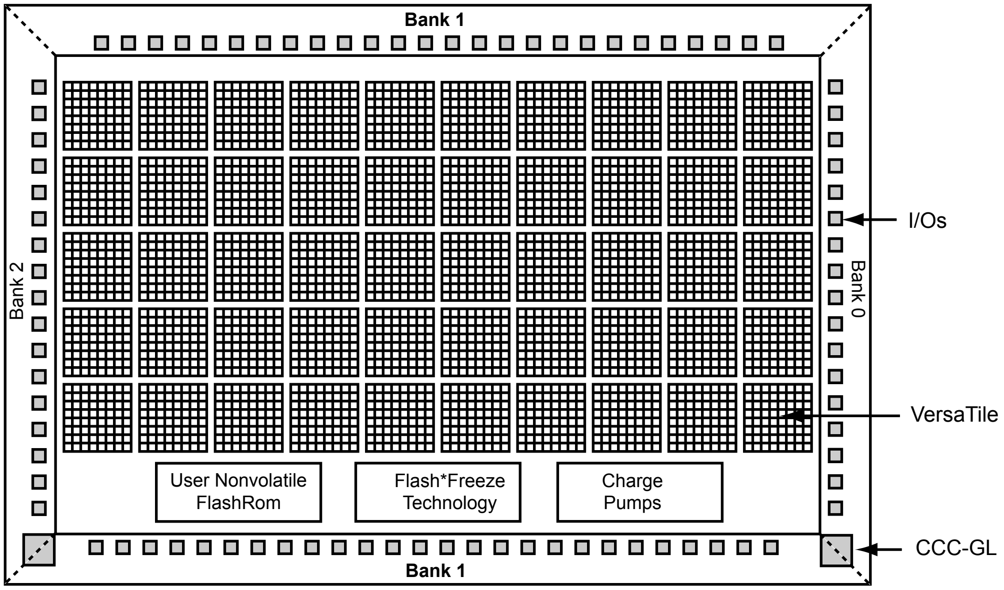


Figure 1-2 • **IGLOO Device Architecture Overview with Three I/O Banks and No RAM (AGLN015 and AGLN020)**

The inputs of the six CCC blocks are accessible from the FPGA core or from dedicated connections to the CCC block, which are located near the CCC.

The CCC block has these key features:

- Wide input frequency range (f_{IN_CCC}) = 1.5 MHz up to 250 MHz
- Output frequency range (f_{OUT_CCC}) = 0.75 MHz up to 250 MHz
- 2 programmable delay types for clock skew minimization
- Clock frequency synthesis (for PLL only)

Additional CCC specifications:

- Internal phase shift = 0°, 90°, 180°, and 270°. Output phase shift depends on the output divider configuration (for PLL only).
- Output duty cycle = 50% ± 1.5% or better (for PLL only)
- Low output jitter: worst case < 2.5% × clock period peak-to-peak period jitter when single global network used (for PLL only)
- Maximum acquisition time is 300 µs (for PLL only)
- Exceptional tolerance to input period jitter—allowable input jitter is up to 1.5 ns (for PLL only)
- Four precise phases; maximum misalignment between adjacent phases of 40 ps × 250 MHz / f_{OUT_CCC} (for PLL only)

Global Clocking

IGLOO nano devices have extensive support for multiple clocking domains. In addition to the CCC and PLL support described above, there is a comprehensive global clock distribution network.

Each VersaTile input and output port has access to nine VersaNets: six chip (main) and three quadrant global networks. The VersaNets can be driven by the CCC or directly accessed from the core via multiplexers (MUXes). The VersaNets can be used to distribute low-skew clock signals or for rapid distribution of high-fanout nets.

I/Os with Advanced I/O Standards

IGLOO nano FPGAs feature a flexible I/O structure, supporting a range of voltages (1.2 V, 1.2 V wide range, 1.5 V, 1.8 V, 2.5 V, 3.0 V wide range, and 3.3 V).

The I/Os are organized into banks with two, three, or four banks per device. The configuration of these banks determines the I/O standards supported.

Each I/O module contains several input, output, and enable registers. These registers allow the implementation of various single-data-rate applications for all versions of nano devices and double-data-rate applications for the AGLN060, AGLN125, and AGLN250 devices.

IGLOO nano devices support LVTTL and LVCMOS I/O standards, are hot-swappable, and support cold-sparing and Schmitt trigger.

Hot-swap (also called hot-plug, or hot-insertion) is the operation of hot-insertion or hot-removal of a card in a powered-up system.

Cold-sparing (also called cold-swap) refers to the ability of a device to leave system data undisturbed when the system is powered up, while the component itself is powered down, or when power supplies are floating.

Wide Range I/O Support

IGLOO nano devices support JEDEC-defined wide range I/O operation. IGLOO nano devices support both the JESD8-B specification, covering both 3 V and 3.3 V supplies, for an effective operating range of 2.7 V to 3.6 V, and JESD8-12 with its 1.2 V nominal, supporting an effective operating range of 1.14 V to 1.575 V.

Wider I/O range means designers can eliminate power supplies or power conditioning components from the board or move to less costly components with greater tolerances. Wide range eases I/O bank management and provides enhanced protection from system voltage spikes, while providing the flexibility to easily run custom voltage applications.

Table 2-4 • **Overshoot and Undershoot Limits** [1]

VCCI	Average VCCI–GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle[2]	Maximum Overshoot/ Undershoot[2]
2.7 V or less	10%	1.4 V
	5%	1.49 V
3 V	10%	1.1 V
	5%	1.19 V
3.3 V	10%	0.79 V
	5%	0.88 V
3.6 V	10%	0.45 V
	5%	0.54 V

Notes:

1. *Based on reliability requirements at 85°C.*
2. *The duration is allowed at one out of six clock cycles. If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15 V.*

I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)

Sophisticated power-up management circuitry is designed into every IGLOO nano device. These circuits ensure easy transition from the powered-off state to the powered-up state of the device. The many different supplies can power up in any sequence with minimized current spikes or surges. In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in Figure 2-1 on page 2-4.

There are five regions to consider during power-up.

IGLOO nano I/Os are activated only if ALL of the following three conditions are met:

1. VCC and VCCI are above the minimum specified trip points (Figure 2-1 and Figure 2-2 on page 2-5).
2. VCCI > VCC – 0.75 V (typical)
3. Chip is in the operating mode.

VCCI Trip Point:

Ramping up (V5 devices): 0.6 V < trip_point_up < 1.2 V
Ramping down (V5 devices): 0.5 V < trip_point_down < 1.1 V
Ramping up (V2 devices): 0.75 V < trip_point_up < 1.05 V
Ramping down (V2 devices): 0.65 V < trip_point_down < 0.95 V

VCC Trip Point:

Ramping up (V5 devices): 0.6 V < trip_point_up < 1.1 V
Ramping down (V5 devices): 0.5 V < trip_point_down < 1.0 V
Ramping up (V2 devices): 0.65 V < trip_point_up < 1.05 V
Ramping down (V2 devices): 0.55 V < trip_point_down < 0.95 V

VCC and VCCI ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- During programming, I/Os become tristated and weakly pulled up to VCCI.
- JTAG supply, PLL power supplies, and charge pump VPUMP supply have no influence on I/O behavior.

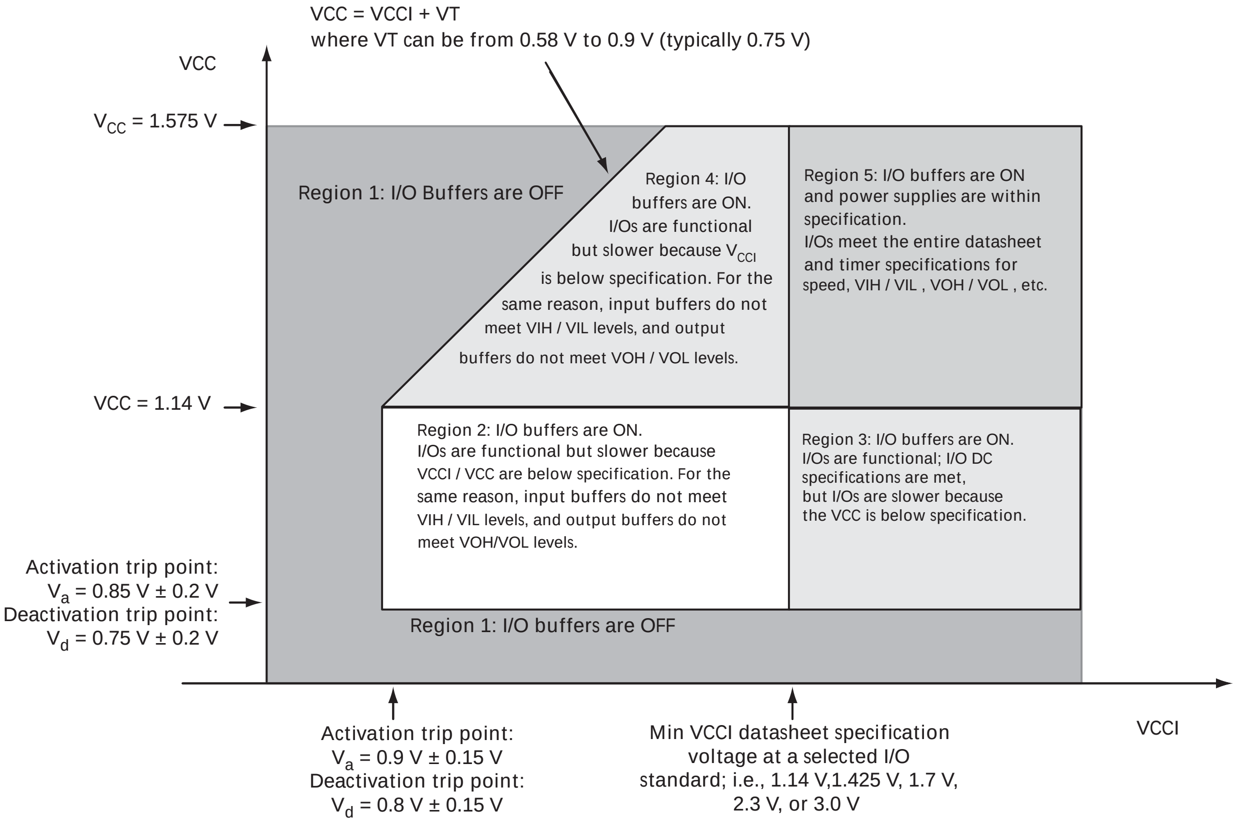


Figure 2-2 • **V2 Devices – I/O State as a Function of VCCI and VCC Voltage Levels**

Table 2-29 • I/O Weak Pull-Up/Pull-Down Resistances
Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values

	$R_{(WEAK\ PULL\text{-}UP)}$[1] (Ω)		$R_{(WEAK\ PULL\text{-}DOWN)}$[2] (Ω)	
VCCI	**Min.**	**Max.**	**Min.**	**Max.**
3.3 V	10 K	45 K	10 K	45 K
3.3 V (wide range I/Os)	10 K	45 K	10 K	45 K
2.5 V	11 K	55 K	12 K	74 K
1.8 V	18 K	70 K	17 K	110 K
1.5 V	19 K	90 K	19 K	140 K
1.2 V	25 K	110 K	25 K	150 K
1.2 V (wide range I/Os)	19 K	110 K	19 K	150 K

Notes:

1. $R_{(WEAK\ PULL\text{-}UP\text{-}MAX)} = (VCCImax - VOHspec) / I_{(WEAK\ PULL\text{-}UP\text{-}MIN)}$
2. $R_{(WEAK\ PULL\text{-}DOWN\text{-}MAX)} = (VOLspec) / I_{(WEAK\ PULL\text{-}DOWN\text{-}MIN)}$

Table 2-30 • I/O Short Currents IOSH/IOSL

	Drive Strength	**IOSL (mA)***	**IOSH (mA)***
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	25	27
	4 mA	25	27
	6 mA	51	54
	8 mA	51	54
3.3 V LVCMOS Wide Range	100 µA	Same as equivalent software default drive	
2.5 V LVCMOS	2 mA	16	18
	4 mA	16	18
	6 mA	32	37
	8 mA	32	37
1.8 V LVCMOS	2 mA	9	11
	4 mA	17	22
1.5 V LVCMOS	2 mA	13	16
1.2 V LVCMOS	1 mA	10	13
1.2 V LVCMOS Wide Range	100 µA	10	13

Note: *T_J = 100°C

Applies to 1.2 V DC Core Voltage

Table 2-38 • **3.3 V LVTTL / 3.3 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	1.55	4.09	0.26	0.97	1.36	1.10	4.16	3.91	2.19	2.64	ns
4 mA	STD	1.55	4.09	0.26	0.97	1.36	1.10	4.16	3.91	2.19	2.64	ns
6 mA	STD	1.55	3.45	0.26	0.97	1.36	1.10	3.51	3.32	2.43	3.03	ns
8 mA	STD	1.55	3.45	0.26	0.97	1.36	1.10	3.51	3.32	2.43	3.03	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-39 • **3.3 V LVTTL / 3.3 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	1.55	2.68	0.26	0.97	1.36	1.10	2.72	2.26	2.19	2.74	ns
4 mA	STD	1.55	2.68	0.26	0.97	1.36	1.10	2.72	2.26	2.19	2.74	ns
6 mA	STD	1.55	2.31	0.26	0.97	1.36	1.10	2.34	1.90	2.43	3.14	ns
8 mA	STD	1.55	2.31	0.26	0.97	1.36	1.10	2.34	1.90	2.43	3.14	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Timing Characteristics

Applies to 1.5 V DC Core Voltage

Table 2-53 • 1.8 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	0.97	5.44	0.19	1.03	1.44	0.66	5.25	5.44	1.69	1.35	ns
4 mA	STD	0.97	4.44	0.19	1.03	1.44	0.66	4.37	4.44	1.99	2.11	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-54 • 1.8 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	0.97	2.64	0.19	1.03	1.44	0.66	2.59	2.64	1.69	1.40	ns
4 mA	STD	0.97	2.08	0.19	1.03	1.44	0.66	2.12	1.95	1.99	2.19	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Applies to 1.2 V DC Core Voltage

Table 2-55 • 1.8 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	1.55	5.92	0.26	1.13	1.59	1.10	5.72	5.92	2.11	1.95	ns
4 mA	STD	1.55	4.91	0.26	1.13	1.59	1.10	4.82	4.91	2.42	2.73	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-56 • 1.8 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	1.55	3.05	0.26	1.13	1.59	1.10	3.01	3.05	2.10	2.00	ns
4 mA	STD	1.55	2.49	0.26	1.13	1.59	1.10	2.53	2.34	2.42	2.81	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

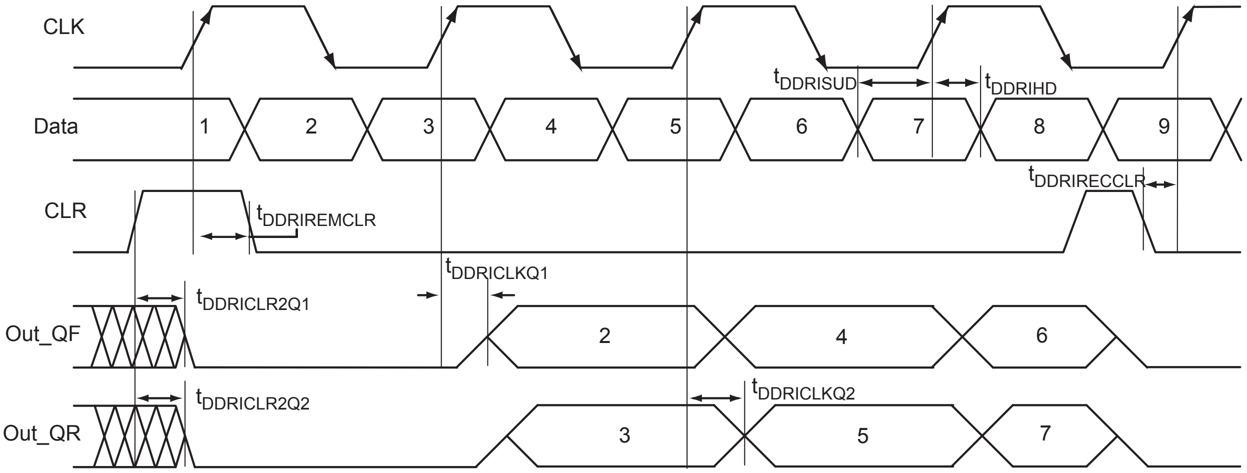


Figure 2-18 **• Input DDR Timing Diagram**

Timing Characteristics

1.5 V DC Core Voltage

Table 2-79 **• Input DDR Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.25 V

Parameter	Description	Std.	Units
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR for Input DDR	0.48	ns
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF for Input DDR	0.65	ns
$t_{DDRISUD1}$	Data Setup for Input DDR (negedge)	0.50	ns
$t_{DDRISUD2}$	Data Setup for Input DDR (posedge)	0.40	ns
$t_{DDRIHD1}$	Data Hold for Input DDR (negedge)	0.00	ns
$t_{DDRIHD2}$	Data Hold for Input DDR (posedge)	0.00	ns
$t_{DDRICLR2Q1}$	Asynchronous Clear-to-Out Out_QR for Input DDR	0.82	ns
$t_{DDRICLR2Q2}$	Asynchronous Clear-to-Out Out_QF for Input DDR	0.98	ns
$t_{DDRIREMCLR}$	Asynchronous Clear Removal Time for Input DDR	0.00	ns
$t_{DDRIRECCLR}$	Asynchronous Clear Recovery Time for Input DDR	0.23	ns
$t_{DDRIWCLR}$	Asynchronous Clear Minimum Pulse Width for Input DDR	0.19	ns
$t_{DDRICKMPWH}$	Clock Minimum Pulse Width HIGH for Input DDR	0.31	ns
$t_{DDRICKMPWL}$	Clock Minimum Pulse Width LOW for Input DDR	0.28	ns
$F_{DDRIMAX}$	Maximum Frequency for Input DDR	250.00	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

1.2 V DC Core Voltage

Table 2-83 • Output DDR Propagation Delays
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V

Parameter	Description	Std.	Units
$t_{DDROCLKQ}$	Clock-to-Out of DDR for Output DDR	1.60	ns
$t_{DDROSUD1}$	Data_F Data Setup for Output DDR	1.09	ns
$t_{DDROSUD2}$	Data_R Data Setup for Output DDR	1.16	ns
$t_{DDROHD1}$	Data_F Data Hold for Output DDR	0.00	ns
$t_{DDROHD2}$	Data_R Data Hold for Output DDR	0.00	ns
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out for Output DDR	1.99	ns
$t_{DDROREMCLR}$	Asynchronous Clear Removal Time for Output DDR	0.00	ns
$t_{DDRORECCLR}$	Asynchronous Clear Recovery Time for Output DDR	0.24	ns
$t_{DDROWCLR1}$	Asynchronous Clear Minimum Pulse Width for Output DDR	0.19	ns
$t_{DDROCKMPWH}$	Clock Minimum Pulse Width HIGH for the Output DDR	0.31	ns
$t_{DDROCKMPWL}$	Clock Minimum Pulse Width LOW for the Output DDR	0.28	ns
F_{DDOMAX}	Maximum Frequency for the Output DDR	160.00	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

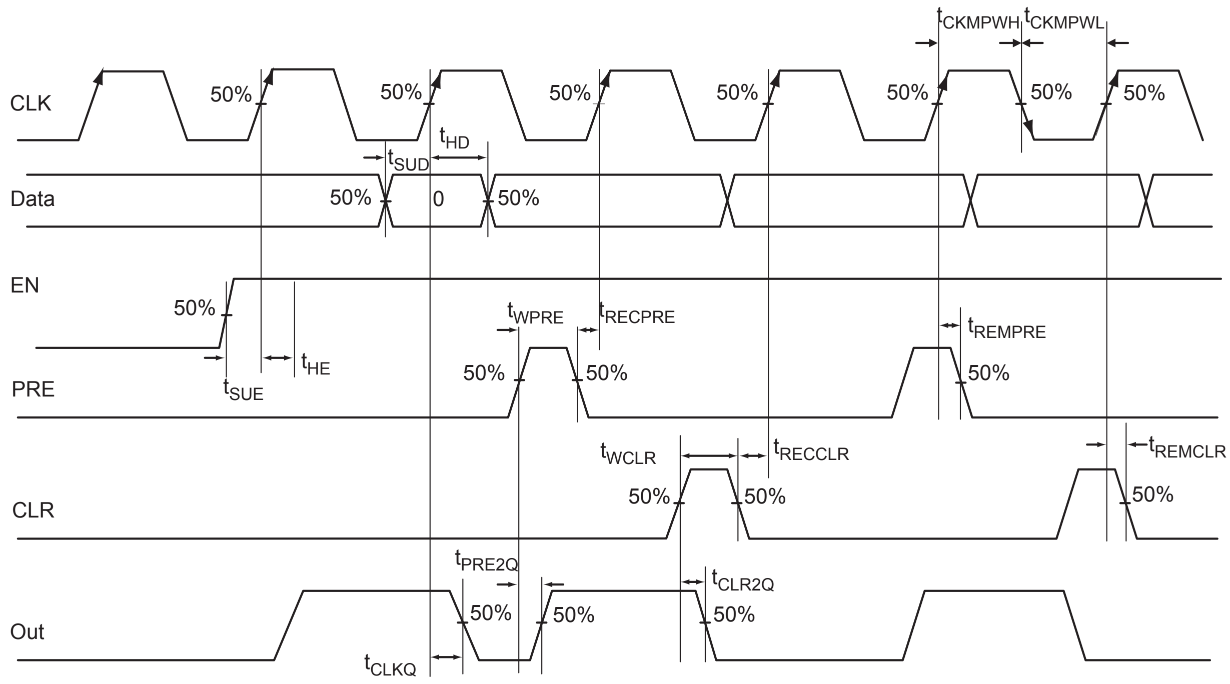


Figure 2-24 • **Timing Model and Waveforms**

Timing Characteristics

1.5 V DC Core Voltage

Table 2-86 • **Register Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	Std.	Units
t_{CLKQ}	Clock-to-Q of the Core Register	0.89	ns
t_{SUD}	Data Setup Time for the Core Register	0.81	ns
t_{HD}	Data Hold Time for the Core Register	0.00	ns
t_{SUE}	Enable Setup Time for the Core Register	0.73	ns
t_{HE}	Enable Hold Time for the Core Register	0.00	ns
t_{CLR2Q}	Asynchronous Clear-to-Q of the Core Register	0.60	ns
t_{PRE2Q}	Asynchronous Preset-to-Q of the Core Register	0.62	ns
t_{REMCLR}	Asynchronous Clear Removal Time for the Core Register	0.00	ns
t_{RECCLR}	Asynchronous Clear Recovery Time for the Core Register	0.24	ns
t_{REMPRE}	Asynchronous Preset Removal Time for the Core Register	0.00	ns
t_{RECPRE}	Asynchronous Preset Recovery Time for the Core Register	0.23	ns
t_{WCLR}	Asynchronous Clear Minimum Pulse Width for the Core Register	0.30	ns
t_{WPRE}	Asynchronous Preset Minimum Pulse Width for the Core Register	0.30	ns
t_{CKMPWH}	Clock Minimum Pulse Width HIGH for the Core Register	0.56	ns
t_{CKMPWL}	Clock Minimum Pulse Width LOW for the Core Register	0.56	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Global Resource Characteristics

AGLN125 Clock Tree Topology

Clock delays are device-specific. Figure 2-25 is an example of a global tree used for clock routing. The global tree presented in Figure 2-25 is driven by a CCC located on the west side of the AGLN125 device. It is used to drive all D-flip-flops in the device.

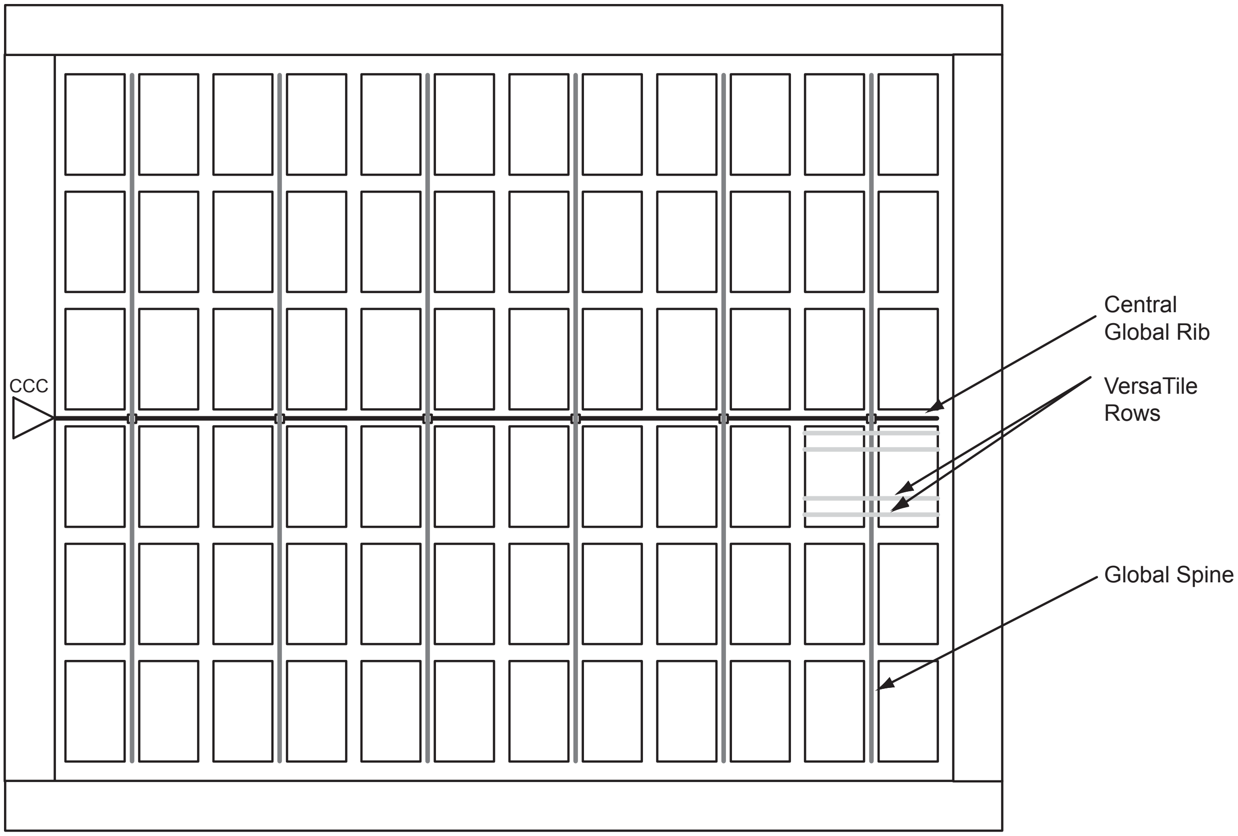


Figure 2-25 • **Example of Global Tree Use in an AGLN125 Device for Clock Routing**

Table 2-96 • AGLN020 Global Resource
Commercial-Case Conditions: T_J = 70°C, VCC = 1.14 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.81	2.26	ns
t_{RCKH}	Input High Delay for Global Clock	1.90	2.51	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.61	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

Table 2-97 • AGLN060 Global Resource
Commercial-Case Conditions: T_J = 70°C, VCC = 1.14 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	2.02	2.42	ns
t_{RCKH}	Input High Delay for Global Clock	2.09	2.65	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.56	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

Table 2-101 • IGLOO nano CCC/PLL Specification
For IGLOO nano V2 Devices, 1.2 V DC Core Supply Voltage

Parameter		Min.	Typ.	Max.	Units
Clock Conditioning Circuitry Input Frequency f_{IN_CCC}		1.5		160	MHz
Clock Conditioning Circuitry Output Frequency f_{OUT_CCC}		0.75		160	MHz
Delay Increments in Programmable Delay Blocks [1, 2]			580[3]		ps
Number of Programmable Values in Each Programmable Delay Block				32	
Serial Clock (SCLK) for Dynamic PLL [4,9]				60	
Input Cycle-to-Cycle Jitter (peak magnitude)				0.25	ns
Acquisition Time					
	LockControl = 0			300	µs
	LockControl = 1			6.0	ms
Tracking Jitter [5]					
	LockControl = 0			4	ns
	LockControl = 1			3	ns
Output Duty Cycle		48.5		51.5	%
Delay Range in Block: Programmable Delay 1 [1, 2]		2.3		20.86	ns
Delay Range in Block: Programmable Delay 2 [1, 2]		0.025		20.86	ns
Delay Range in Block: Fixed Delay [1, 2]			5.7		ns
VCO Output Peak-to-Peak Period Jitter F_{CCC_OUT} [6]		Max Peak-to-Peak Period Jitter [6,7,8]			
	SSO ≤ 2	SSO ≤ 4	SSO ≤ 8	SSO ≤ 16	
0.75 MHz to 50MHz	0.50	1.20	2.00	3.00	%
50 MHz to 100 MHz	2.50	5.00	7.00	15.00	%

Notes:

1. *This delay is a function of voltage and temperature. See Table 2-6 on page 2-6 and Table 2-7 on page 2-7 for deratings.*
2. *T_J = 25°C, V_{CC} = 1.2 V.*
3. *When the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available. Refer to the Libero SoC Online Help associated with the core for more information.*
4. *Maximum value obtained for a STD speed grade device in Worst-Case Commercial conditions. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 and Table 2-7 on page 2-7 for derating values.*
5. *Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to the PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by the period jitter parameter.*
6. *VCO output jitter is calculated as a percentage of the VCO frequency. The jitter (in ps) can be calculated by multiplying the VCO period by the % jitter. The VCO jitter (in ps) applies to CCC_OUT, regardless of the output divider settings. For example, if the jitter on VCO is 300 ps, the jitter on CCC_OUT is also 300 ps, no matter what the settings are for the output divider.*
7. *Measurements done with LVTTL 3.3 V 8 mA I/O drive strength and high slew rate. VCC/VCCPLL = 1.14 V, VCCI = 3.3 V, VQ/PQ/TQ type of packages, 20 pF load.*
8. *SSOs are outputs that are synchronous to a single clock domain and have their clock-to-out times within ±200 ps of each other. Switching I/Os are placed outside of the PLL bank. Refer to the "Simultaneously Switching Outputs (SSOs) and Printed Circuit Board Layout" section in the IGLOO nano FPGA Fabric User's Guide.*
9. *The AGLN010, AGLN015, and AGLN020 devices do not support PLLs.*

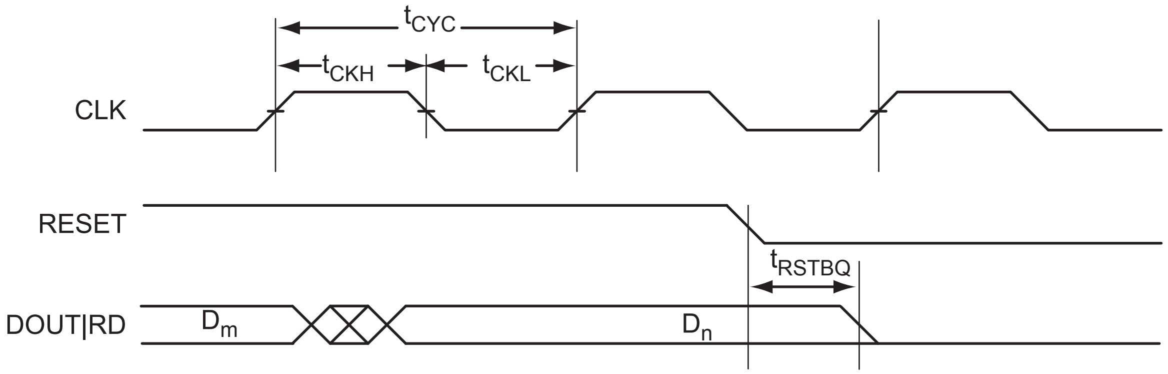
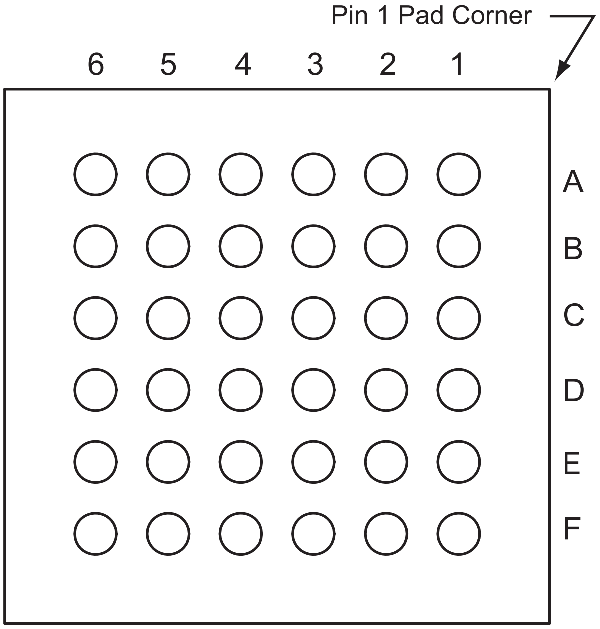


***Figure 2-32* • RAM Reset. Applicable to Both RAM4K9 and RAM512x18.**

4 – Package Pin Assignments

UC36



Note: *This is the bottom view of the package.*

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

UC81	
Pin Number	**AGLN020 Function**
A1	IO64RSB2
A2	IO54RSB2
A3	IO57RSB2
A4	IO36RSB1
A5	IO32RSB1
A6	IO24RSB1
A7	IO20RSB1
A8	IO04RSB0
A9	IO08RSB0
B1	IO59RSB2
B2	IO55RSB2
B3	IO62RSB2
B4	IO34RSB1
B5	IO28RSB1
B6	IO22RSB1
B7	IO18RSB1
B8	IO00RSB0
B9	IO03RSB0
C1	IO51RSB2
C2	IO50RSB2
C3	NC
C4	NC
C5	NC
C6	NC
C7	NC
C8	IO10RSB0
C9	IO07RSB0
D1	IO49RSB2
D2	IO44RSB2
D3	NC
D4	VCC
D5	VCCIB2
D6	GND
D7	NC
D8	IO13RSB0
D9	IO12RSB0

UC81	
Pin Number	**AGLN020 Function**
E1	GEC0/IO48RSB2
E2	GEA0/IO47RSB2
E3	NC
E4	VCCIB1
E5	VCC
E6	VCCIB0
E7	NC
E8	GDA0/IO15RSB0
E9	GDC0/IO14RSB0
F1	IO46RSB2
F2	IO45RSB2
F3	NC
F4	GND
F5	VCCIB1
F6	NC
F7	NC
F8	IO16RSB0
F9	IO17RSB0
G1	IO43RSB2
G2	IO42RSB2
G3	IO41RSB2
G4	IO31RSB1
G5	NC
G6	IO21RSB1
G7	NC
G8	VJTAG
G9	TRST
H1	IO40RSB2
H2	FF/IO39RSB1
H3	IO35RSB1
H4	IO29RSB1
H5	IO26RSB1
H6	IO25RSB1
H7	IO19RSB1
H8	TDI
H9	TDO

UC81	
Pin Number	**AGLN020 Function**
J1	IO38RSB1
J2	IO37RSB1
J3	IO33RSB1
J4	IO30RSB1
J5	IO27RSB1
J6	IO23RSB1
J7	TCK
J8	TMS
J9	VPUMP

QN68	
Pin Number	**AGLN015 Function**
1	IO60RSB2
2	IO54RSB2
3	IO52RSB2
4	IO50RSB2
5	IO49RSB2
6	GEC0/IO48RSB2
7	GEA0/IO47RSB2
8	VCC
9	GND
10	VCCIB2
11	IO46RSB2
12	IO45RSB2
13	IO44RSB2
14	IO43RSB2
15	IO42RSB2
16	IO41RSB2
17	IO40RSB2
18	FF/IO39RSB1
19	IO37RSB1
20	IO35RSB1
21	IO33RSB1
22	IO31RSB1
23	IO30RSB1
24	VCC
25	GND
26	VCCIB1
27	IO27RSB1
28	IO25RSB1
29	IO23RSB1
30	IO21RSB1
31	IO19RSB1
32	TCK
33	TDI
34	TMS
35	VPUMP

QN68	
Pin Number	**AGLN015 Function**
36	TDO
37	TRST
38	VJTAG
39	IO17RSB0
40	IO16RSB0
41	GDA0/IO15RSB0
42	GDC0/IO14RSB0
43	IO13RSB0
44	VCCIB0
45	GND
46	VCC
47	IO12RSB0
48	IO11RSB0
49	IO09RSB0
50	IO05RSB0
51	IO00RSB0
52	IO07RSB0
53	IO03RSB0
54	IO18RSB1
55	IO20RSB1
56	IO22RSB1
57	IO24RSB1
58	IO28RSB1
59	NC
60	GND
61	NC
62	IO32RSB1
63	IO34RSB1
64	IO36RSB1
65	IO61RSB2
66	IO58RSB2
67	IO56RSB2
68	IO63RSB2

VQ100	
Pin Number	AGLN250Z Function
1	GND
2	GAA2/IO67RSB3
3	IO66RSB3
4	GAB2/IO65RSB3
5	IO64RSB3
6	GAC2/IO63RSB3
7	IO62RSB3
8	IO61RSB3
9	GND
10	GFB1/IO60RSB3
11	GFB0/IO59RSB3
12	VCOMPLF
13	GFA0/IO57RSB3
14	VCCPLF
15	GFA1/IO58RSB3
16	GFA2/IO56RSB3
17	VCC
18	VCCIB3
19	GFC2/IO55RSB3
20	GEC1/IO54RSB3
21	GEC0/IO53RSB3
22	GEA1/IO52RSB3
23	GEA0/IO51RSB3
24	VMV3
25	GNDQ
26	GEA2/IO50RSB2
27	FF/GEB2/IO49RSB2
28	GEC2/IO48RSB2
29	IO47RSB2
30	IO46RSB2
31	IO45RSB2
32	IO44RSB2
33	IO43RSB2
34	IO42RSB2
35	IO41RSB2
36	IO40RSB2
37	VCC
38	GND
39	VCCIB2
40	IO39RSB2
41	IO38RSB2
42	IO37RSB2
43	GDC2/IO36RSB2
44	GDB2/IO35RSB2
45	GDA2/IO34RSB2
46	GNDQ
47	TCK
48	TDI
49	TMS
50	VMV2
51	GND
52	VPUMP
53	NC
54	TDO
55	TRST
56	VJTAG
57	GDA1/IO33RSB1
58	GDC0/IO32RSB1
59	GDC1/IO31RSB1
60	IO30RSB1
61	GCB2/IO29RSB1
62	GCA1/IO27RSB1
63	GCA0/IO28RSB1
64	GCC0/IO26RSB1
65	GCC1/IO25RSB1
66	VCCIB1
67	GND
68	VCC
69	IO24RSB1
70	GBC2/IO23RSB1
71	GBB2/IO22RSB1
72	IO21RSB1
73	GBA2/IO20RSB1
74	VMV1
75	GNDQ
76	GBA1/IO19RSB0
77	GBA0/IO18RSB0
78	GBB1/IO17RSB0
79	GBB0/IO16RSB0
80	GBC1/IO15RSB0
81	GBC0/IO14RSB0
82	IO13RSB0
83	IO12RSB0
84	IO11RSB0
85	IO10RSB0
86	IO09RSB0
87	VCCIB0
88	GND
89	VCC
90	IO08RSB0
91	IO07RSB0
92	IO06RSB0
93	GAC1/IO05RSB0
94	GAC0/IO04RSB0
95	GAB1/IO03RSB0
96	GAB0/IO02RSB0
97	GAA1/IO01RSB0
98	GAA0/IO00RSB0
99	GNDQ
100	VMV0

Revision / Version	Changes	Page
Revision 2 (Dec 2008) Product Brief Advance v0.4	The second table note in "IGLOO nano Devices" table was revised to state, "AGLN060, AGLN125, and AGLN250 in the CS81 package do not support PLLs. AGLN030 and smaller devices do not support this feature."	II
	The I/Os per package for CS81 were revised to 60 for AGLN060, AGLN125, and AGLN250 in the "I/Os Per Package"table.	II
Packaging Advance v0.3	The "UC36" pin table is new.	4-2
Revision 1 (Nov 2008) Product Brief Advance v0.3	The "Advanced I/Os" section was updated to include wide power supply voltage support for 1.14 V to 1.575 V.	I
	The AGLN030 device was added to product tables and replaces AGL030 entries that were formerly in the tables.	VI
	The "I/Os Per Package"table was updated for the CS81 package to change the number of I/Os for AGLN060, AGLN125, and AGLN250 from 66 to 64.	II
	The "Wide Range I/O Support" section is new.	1-8
	The table notes and references were revised in Table 2-2 • Recommended Operating Conditions [1]. VMV was included with VCCI and a table note was added stating, "VMV pins must be connected to the corresponding VCCI pins. See *Pin Descriptions* for further information." Please review carefully.	2-2
	VJTAG was added to the list in the table note for Table 2-9 • Quiescent Supply Current (IDD) Characteristics, IGLOO nano Flash*Freeze Mode*. Values were added for AGLN010, AGLN015, and AGLN030 for 1.5 V.	2-7
	VCCI was removed from the list in the table note for Table 2-10 • Quiescent Supply Current (IDD) Characteristics, IGLOO nano Sleep Mode*.	2-8
	Values for I_{CCA} current were updated for AGLN010, AGLN015, and AGLN030 in Table 2-12 • Quiescent Supply Current (IDD), No IGLOO nano Flash*Freeze Mode[1].	2-8
	Values for PAC1 and PAC2 were added to Table 2-15 • Different Components Contributing to Dynamic Power Consumption in IGLOO nano Devices and Table 2-17 • Different Components Contributing to Dynamic Power Consumption in IGLOO nano Devices.	2-10, 2-11
	Table notes regarding wide range support were added to Table 2-21 • Summary of Maximum and Minimum DC Input and Output Levels.	2-19
	1.2 V LVCMOS wide range values were added to Table 2-22 • Summary of Maximum and Minimum DC Input Levels and Table 2-23 • Summary of AC Measuring Points.	2-19, 2-20
	The following table note was added to Table 2-25 • Summary of I/O Timing Characteristics—Software Default Settings and Table 2-26 • Summary of I/O Timing Characteristics—Software Default Settings: "All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range, as specified in the JESD8-B specification."	2-21
	3.3 V LVCMOS Wide Range and 1.2 V Wide Range were added to Table 2-28 • I/O Output Buffer Maximum Resistances [1] andTable 2-30 • I/O Short Currents IOSH/IOSL.	2-23, 2-24