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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	LCD, PWM, WDT
Number of I/O	57
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 16x16b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9s08gw32clh

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Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://freescale.com/

The following revision history table summarizes changes contained in this document.

Rev	Date	Description of Changes
1	5/26/2010	Initial public release
2	10/29/2010	Completed all the TBDs. Updated the voltage output data in the Table 20. Changed the classification marking of $\|I_{InT}\|$ to C in the Table 8.
3	1/28/2011	Updated Table 7.

Related Documentation

Find the most current versions of all documents at: http://www.freescale.com

Reference Manual (MC9S08GW64RM)

Contains extensive product information including modes of operation, memory, resets and interrupts, register definition, port pins, CPU, and all module information.

1 Devices in the MC9S08GW64 Series

Table 1 summarizes the feature set available in the MC9S08GW64 series of MCUs.

Table 1. MC9S08GW64 Series Features by MCU and Package

Feature	MC9S08GW64		MC9S08GW32	
Package	**80-pin LQFP**	**64-pin LQFP**	**80-pin LQFP**	**64-pin LQFP**
FLASH	65,536 Bytes		32,768 Bytes	
RAM	4,032 Bytes		2,048 Bytes	
ADC0[1] Single-ended Channels	7-ch	7-ch	7-ch	7-ch
ADC0 Differential Channels[2]	1	0	1	0
ADC1 Single-ended Channels	7-ch	7-ch	7-ch	7-ch
ADC1 Differential Channels	1	1	1	1
BKPT	yes		yes	
ICS	yes		yes	
IIC	yes		yes	
IRQ	yes		yes	
IRTC	yes		yes	
KBI	8-ch		8-ch	
MTIM8	2		2	
MTIM16	yes		yes	
PCNT	yes		yes	
PCRC	yes		yes	
PDB	yes		yes	
PRACMP	3		3	
SCI	4		4	
SPI	3		3	
FTM	2-ch		2-ch	
LCD	8×36 4×40	8×24 4×28	8×36 4×40	8×24 4×28
VREFO	yes	yes	yes	yes
XOSC	2		2	
I/O pins[3]	57	45	57	45

2 Pin Assignments

This section shows the pin assignments for the MC9S08GW64 series devices.

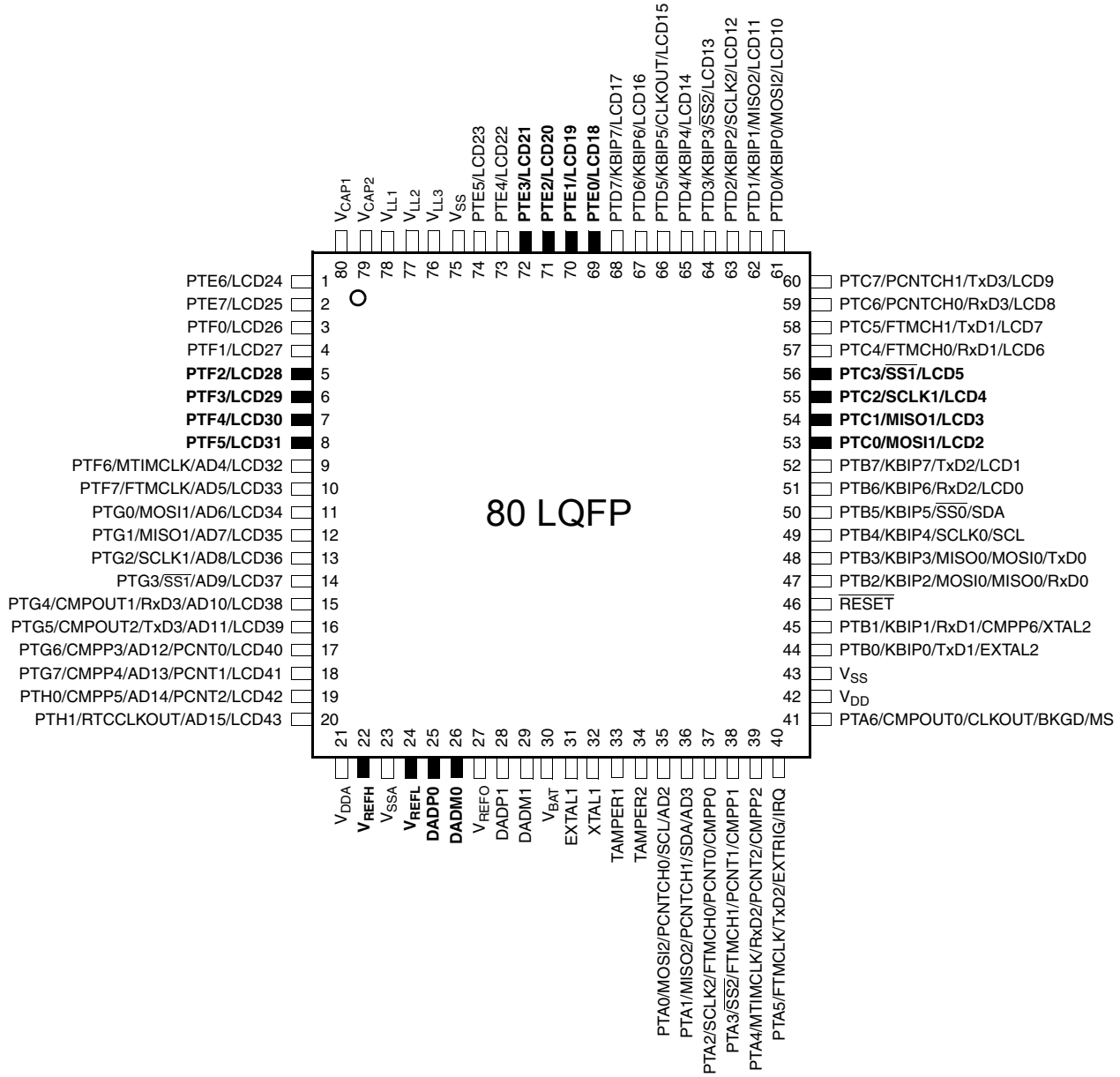


Figure 2. MC9S08GW64 Series in 80-Pin LQFP Package

Table 2. Pin Availability by Package Pin-Count (continued)

80	64	Port Pin	Default func	Alt 1	Alt 2	Alt3	Alt4
7		PTF4	PTF4	LCD30			
8		PTF5	PTF5	LCD31			
9	5	PTF6	PTF6	MTIMCLK	AD4	LCD32	
10	6	PTF7	PTF7	FTMCLK	AD5	LCD33	
11	7	PTG0	PTG0	MOSI1	AD6	LCD34	
12	8	PTG1	PTG1	MISO1	AD7	LCD35	
13	9	PTG2	PTG2	SCLK1	AD8	LCD36	
14	10	PTG3	PTG3	$\overline{SS1}$	AD9	LCD37	
15	11	PTG4	PTG4	CMPOUT1	RxD3	AD10	LCD38
16	12	PTG5	PTG5	CMPOUT2	TxD3	AD11	LCD39
17	13	PTG6	PTG6	CMPP3	AD12	PCNT0	LCD40
18	14	PTG7	PTG7	CMPP4	AD13	PCNT1	LCD41
19	15	PTH0	PTH0	CMPP5	AD14	PCNT2	LCD42
20	16	PTH1	PTH1	RTCCLKOUT	AD15	LCD43	
21	17	V_{DDA}	V_{DDA}				
22		V_{REFH}	V_{REFH}				
23	18	V_{SSA}	V_{SSA}				
24		V_{REFL}	V_{REFL}				
25		DADP0	DADP0				
26		DADM0	DADM0				
27	19	V_{REFO}	V_{REFO}				
28	20	DADP1	DADP1				
29	21	DADM1	DADM1				
30	22	V_{BAT}	V_{BAT}				
31	23	EXTAL1	EXTAL1				
32	24	XTAL1	XTAL1				
33	25	TAMPER1[1]	TAMPER1				
34	26	TAMPER2	TAMPER2				
35	27	PTA0	PTA0	MOSI2	PCNTCH0	SCL	AD2
36	28	PTA1	PTA1	MISO2	PCNTCH1	SDA	AD3
37	29	PTA2	PTA2	SCLK2	FTMCH0	PCNT0	CMPP0
38	30	PTA3	PTA3	$\overline{SS2}$	FTMCH1	PCNT1	CMPP1
39	31	PTA4	PTA4	MTIMCLK	RxD2	PCNT2	CMPP2
40	32	PTA5[2]	PTA5	FTMCLK	TxD2	EXTRIG	IRQ
41	33	PTA6[3]	BKGD/MS	CMPOUT0	CLKOUT	BKGD/MS	

Table 2. Pin Availability by Package Pin-Count (continued)

80	64	Port Pin	Default func	Alt 1	Alt 2	Alt3	Alt4
77	61	V_{LL2}	V_{LL2}				
78	62	V_{LL1}	V_{LL1}				
79	63	V_{CAP2}	V_{CAP2}				
80	64	V_{CAP1}	V_{CAP1}				

1 TAMPER0 pin is dedicatedly used for Battery Removal Tamper and not exposed on any SoC pins.

2 PTA5 is with double drive strength.

3 PTA6 is an output-only pin when it is configured as GPIO.

4 PTB2, PTB3 and PTB4 are compatible with 5 V devices with a pullup device.

3 Electrical Characteristics

3.1 Introduction

This section contains electrical and timing specifications for the MC9S08GW64 sries of microcontrollers available at the time of publication.

3.2 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 3. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

3.3 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 4 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this

high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pull-up resistor associated with the pin is enabled.

Table 4. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to +3.8	V
Maximum current into V_{DD}	I_{DD}	120	mA
Digital input voltage	V_{In}	–0.3 to V_{DD} + 0.3	V
Instantaneous maximum current Single pin limit (applies to all port pins except PTA5 and PTB1)[1, 2, 3]	I_D	± 25	mA
Instantaneous maximum current Single pin limit (applies to PTA5 and PTB1)[1,2,3]	I_D	± 50	mA
Storage temperature range	T_{stg}	–55 to 150	°C

1 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

2 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

3 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low (which would reduce overall power consumption).

3.4 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 5. Thermal Characteristics

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	T_A	T_L to T_H –40 to 85	°C
Maximum junction temperature	T_J	95	°C
Thermal resistance Single-layer board			
80-pin LQFP	θ_{JA}	61	°C/W
64-pin LQFP		70	
Thermal resistance Four-layer board			
80-pin LQFP	θ_{JA}	48	°C/W
64-pin LQFP		52	

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad \textit{Eqn. 1}$$

where:

T_A = Ambient temperature, °C
θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W
$P_D = P_{int} + P_{I/O}$
$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power
$P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad \textit{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273°C) + \theta_{JA} \times (P_D)^2 \quad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

3.5 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, normal handling precautions should be taken to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits. During the device qualification, ESD stresses were performed for the human body model (HBM), the machine model (MM) and the charge device model (CDM).

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless instructed otherwise in the device specification.

Table 6. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body Model	Series resistance	R1	1500	Ω
	Storage capacitance	C	100	pF
	Number of pulses per pin	—	3	
Charge Device Model	Series resistance	R1	0	Ω
	Storage capacitance	C	200	pF
	Number of pulses per pin	—	3	
Latch-up	Minimum input voltage limit		–2.5	V
	Maximum input voltage limit		7.5	V

Table 8. DC Characteristics (continued)

Num	C	Characteristic		Symbol	Condition	Min	Typ[1]	Max	Unit
5	C	Output low voltage	All non-LCD pins low-drive strength	V_{OL}	V_{DD} > 1.8 V, I_{Load} = 0.6 mA	—	—	0.5	V
	P		All non-LCD pins high-drive strength		V_{DD} > 2.7 V, I_{Load} = 10 mA	—	—	0.5	
	C				V_{DD} > 1.8 V, I_{Load} = 3 mA	—	—	0.5	
6	C	Output low voltage	All LCD/GPIO pins low-drive strength	V_{OL}	V_{DD} > 1.8 V, I_{Load} = 0.5 mA	—	—	0.5	V
	P		All LCD/GPIO pins high-drive strength		V_{DD} > 2.7 V, I_{Load} = 3 mA	—	—	0.5	
	C				V_{DD} > 1.8 V, I_{Load} = 1 mA	—	—	0.5	
7	D	Output low current	Max total I_{OL} for all ports	I_{OLT}		—	—	100	mA
8	P	Input high voltage	all digital inputs	V_{IH}	V_{DD} > 2.7 V	0.70 x V_{DD}	—	—	V
	C				V_{DD} > 1.8 V	0.85 x V_{DD}	—	—	
9	P	Input low voltage	all digital inputs	V_{IL}	V_{DD} > 2.7 V	—	—	0.35 x V_{DD}	
	C				V_{DD} > 1.8 V	—	—	0.30 x V_{DD}	
10	C	Input hysteresis	all digital inputs	V_{hys}		0.06 x V_{DD}	—	—	mV
11	P	Input leakage current	all input only pins (per pin)	$\lvert I_{In} \rvert$	V_{In} = V_{DD} or V_{SS}	—	0.025	1	μA
12	P	Hi-Z (off-state) leakage current	all input/output (per pin)	$\lvert I_{OZ} \rvert$	V_{In} = V_{DD} or V_{SS}	—	0.025	1	μA
13	C	Total leakage current[2]	Total leakage current for all pins	$\lvert I_{InT} \rvert$	V_{In} = V_{DD} or V_{SS}	—	—	2	μA
14	P	Pullup, Pulldown resistors	all digital inputs, when enabled	R_{PU}, R_{PD}		17.5	—	52.5	kΩ
15	P	Pullup, Pulldown resistors	all digital inputs, when enabled	R_{PU}, R_{PD}		17.5	—	52.5	kΩ
16	D	DC injection current [3, 4, 5]	Single pin limit	I_{IC}	V_{IN} < V_{SS}, V_{IN} > V_{DD}	–0.2	—	0.2	mA
			Total MCU limit, includes sum of all stressed pins			–5	—	5	mA
17	C	Input Capacitance, all pins		C_{In}		—	—	8	pF
18	C	RAM retention voltage		V_{RAM}		—	0.6	1.0	V
19	C	iRTC RAM retention voltage		V_{iRAM}		—	1.05	—	V
20	C	POR re-arm voltage[6]		V_{POR}		0.9	1.4	2.0	V
21	D	POR re-arm time		t_{POR}		10	—	—	μs

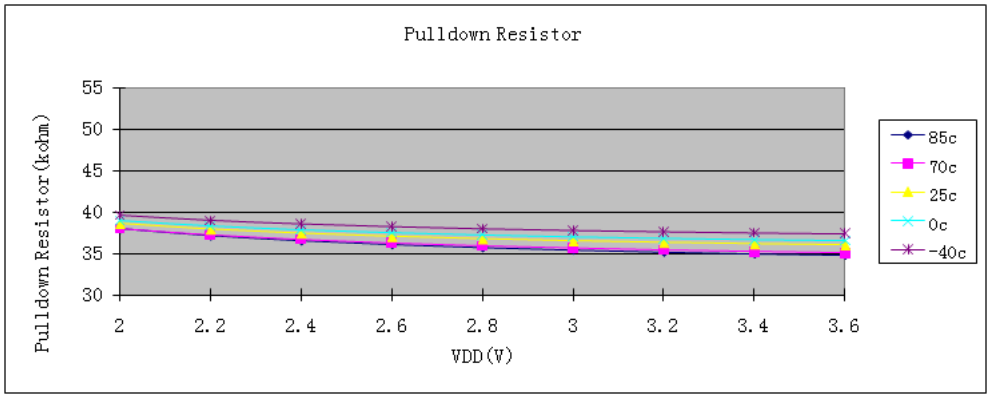
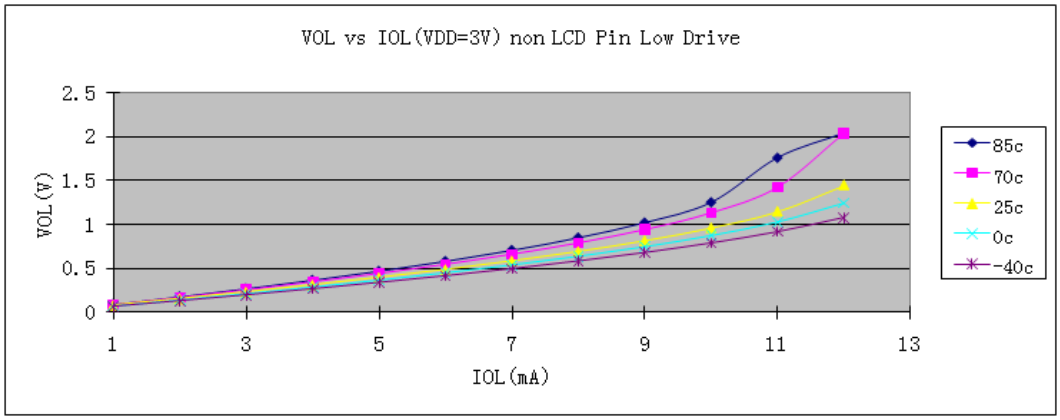


Figure 5. Non LCD pins I/O Pulldown Typical Resistor Values



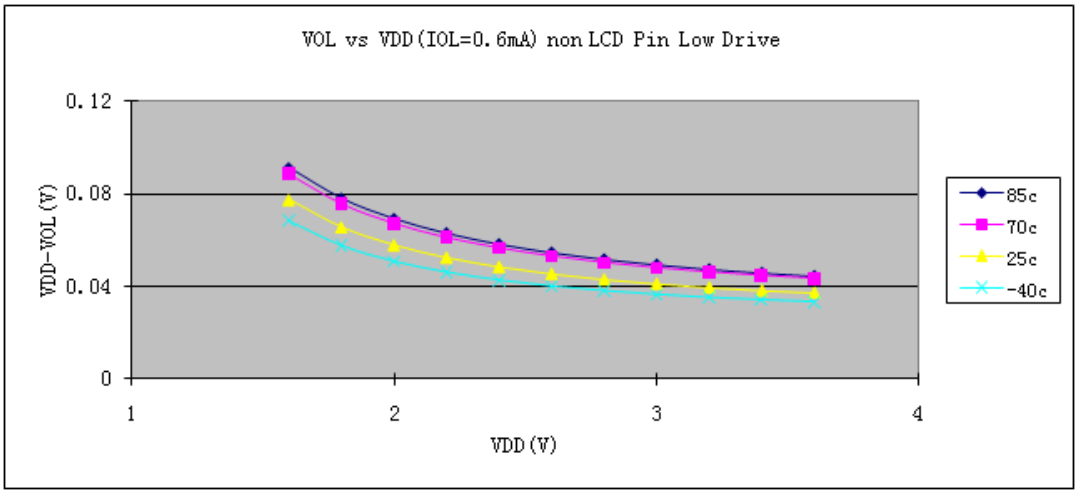
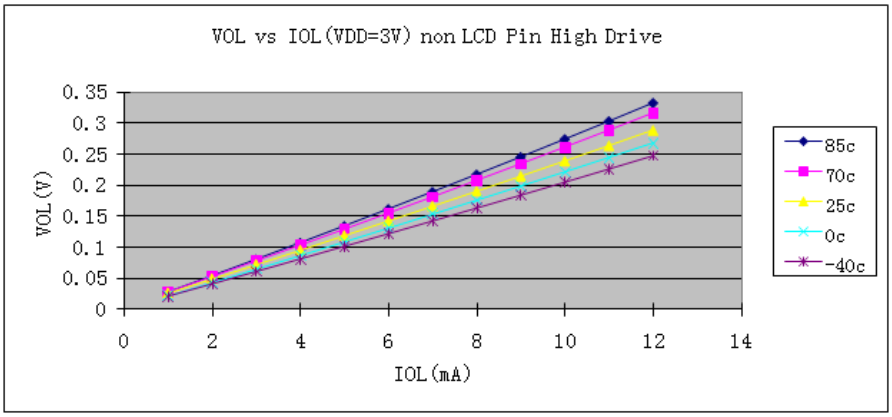


Figure 6. Typical Low-Side Driver (Sink) Characteristics(Non LCD pins) — Low Drive (PTxDSn = 0)



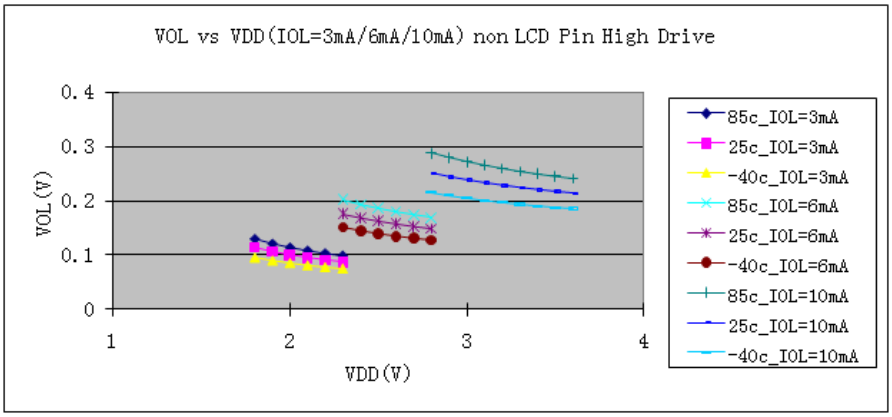


Figure 7. Typical Low-Side Driver (Sink) Characteristics(Non LCD pins) — High Drive (PTxDSn = 1)

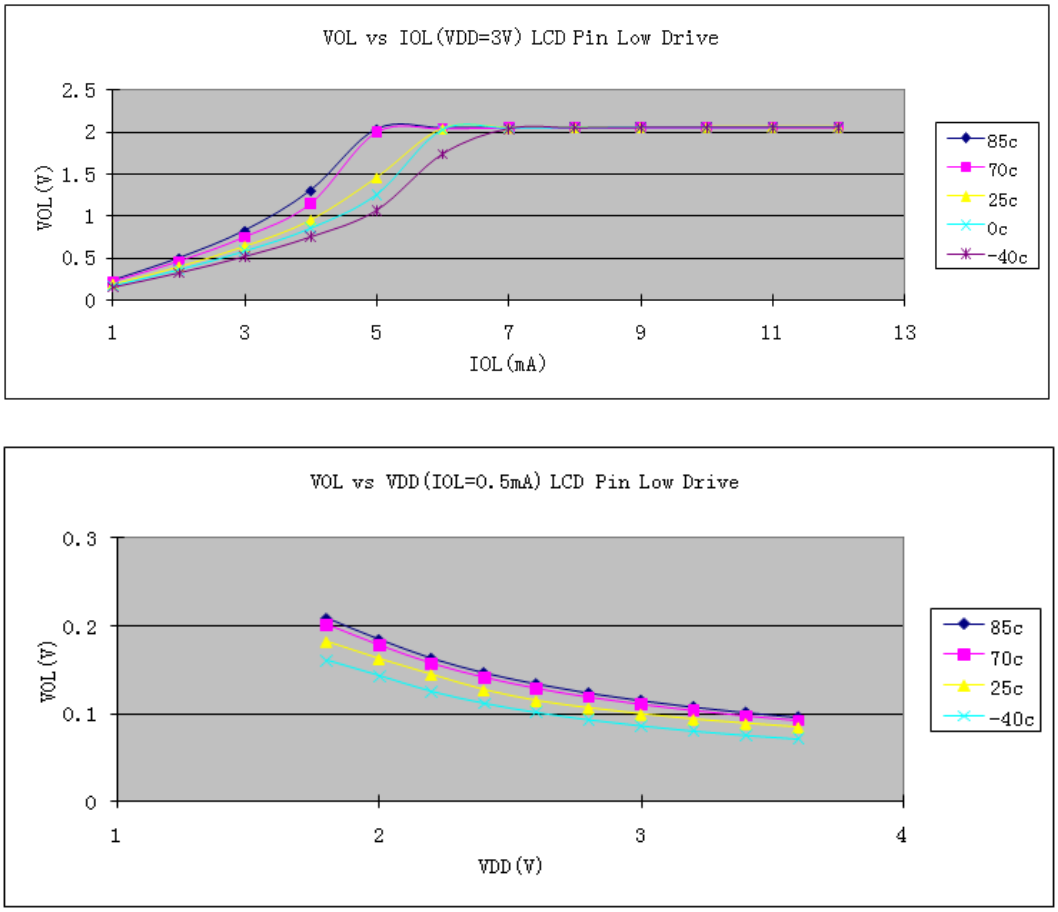
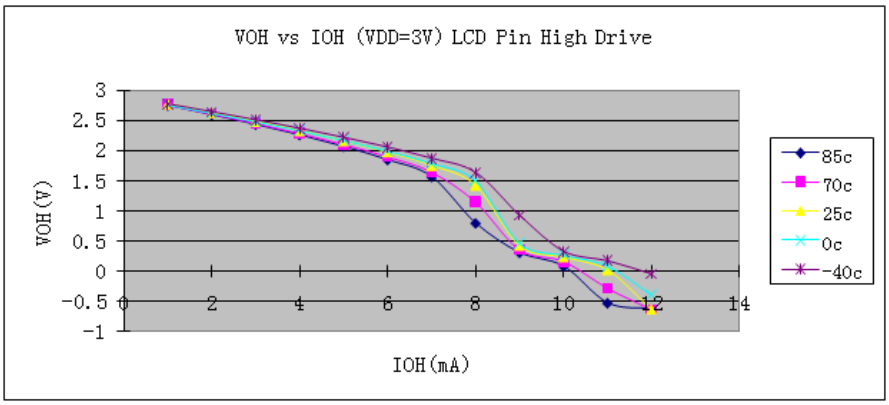


Figure 10. Typical Low-Side Driver (Sink) Characteristics(LCD/GPIO pins) — Low Drive (PTxDSn = 0)



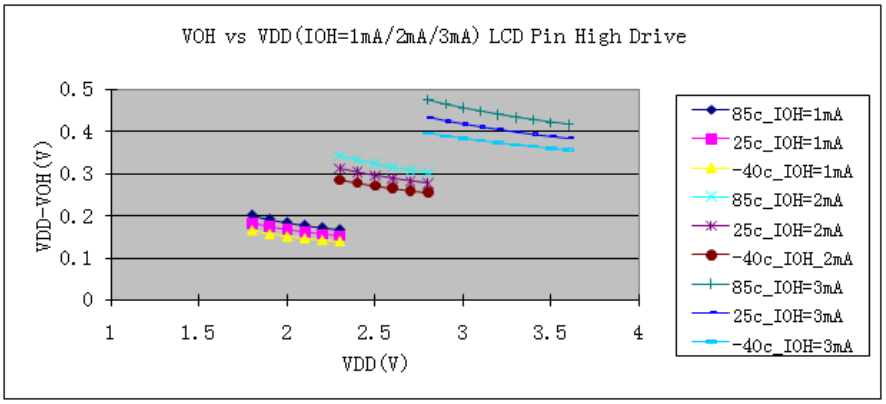


Figure 13. Typical High-Side (Source) Characteristics(LCD/GPIO pins) — High Drive (PTxDSn = 1)

3.7 Supply Current Characteristics

This section includes information about power supply current in various operating modes.

Table 9. Supply Current Characteristics

Num	C	Parameter	Symbol	Bus Freq	V_{DD} (V)	Typ[1]	Max	Unit	Temp (°C)
1	C	Run supply current FEI mode, all modules on, running from Flash	RI_{DD}	20 MHz	3	17.4	20.5	mA	–40 to 85°C
	T			2 MHz		2.6	—		
2	C	Run supply current FEI mode, all modules off, running from Flash	RI_{DD}	20 MHz	3	10.5	—	mA	–40 to 85°C
	T			2 MHz		1.6	—		
3	T	Run supply current LPRS=0, all modules off, running from Flash	RI_{DD}	16 kHz FBILP	3	158	—	µA	–40 to 85°C
	T			16 kHz FBELP		148	—		
4	T	Run supply current LPRS=1, all modules off; running from Flash	RI_{DD}	16 kHz FBILP	3	160	—	µA	–40 to 85°C
	T			16 kHz FBELP		23	—		

Table 9. Supply Current Characteristics

Num	C	Parameter	Symbol	Bus Freq	V_{DD} (V)	Typ[1]	Max	Unit	Temp (°C)
5	T	Run supply current LPRS=1, all modules off; running from RAM	RI_{DD}	16 kHz FBILP	3	137	—	μA	–40 to 85°C
	T			16 kHz FBELP		8	—		
6	C	Wait mode supply current, all modules off	WI_{DD}	20 MHz	3	5.4	7.5	mA	–40 to 85°C
	C			2 MHz		1.1	—		
7	T	Wait mode supply current LPRS = 0, all modules off	WI_{DD}	16 kHz FBILP	3	131	—	μA	–40 to 85°C
	T			16 kHz FBELP	3	123	—	μA	–40 to 85°C
8	T	Wait mode supply current LPRS = 1, all modules off	WI_{DD}	16 kHz FBILP	3	159	—	μA	–40 to 85°C
	T			16 kHz FBELP	3	5.6	—	μA	–40 to 85°C
9	C	Stop2 mode supply current	$S2I_{DD}$	N/A	3	330	1000	nA	–40 to 25°C
						1622	—		70°C
						6000	—		85°C
	C			N/A	2	—	—		–40 to 25°C
						—	—		70°C
						—	—		85°C
10	C	Stop3 mode supply current No clocks active	$S3I_{DD}$	N/A	3	474	1100	nA	–40 to 25°C
						2608	—		70°C
						9000	—		85°C
	C			N/A	2	—	—		–40 to 25°C
						—	—		70°C
						—	—		85°C

[1] Typical values are measured at 25°C. Characterized, not tested.

Table 10. Stop Mode Adders (V_{DD}=3V, V_{DDA}=V_{DD})

Num	C	Parameter	Condition	Temperature (°C)				Units
				-40	25	70	85	
1	C	LPO		100	100	150	175	nA
2	C	ERREFSTEN	RANGE = HGO = 0	600	737	830	863	nA
3	C	IREFSTEN[1]		—	73	80	92	μA
4	C	LVD[1]	LVDSE = 1	110	112	112	113	μA
5	C	PRACMP[1]	Not using the bandgap (BGBE = 0), PRG enabled	30	35	40	55	μA

Table 10. Stop Mode Adders (continued)(V_{DD}=3V, V_{DDA}=V_{DD})

Num	C	Parameter	Condition	Temperature (°C)				Units
				-40	25	70	85	
6	C	VREFO	Not using the bandgap (BGBE = 0), in tight regulation mode	264	286	296	298	μA
7	C	IRTC		1.4	1.65	2.01	2.27	μA
8	C	ADC[1]	ADLPC = ADLSMP = 1 Not using the bandgap (BGBE = 0), single conversion	78.1	88.5	92.6	93.6	μA
9	C	LCD	VIREG enabled for Contrast control, 1/8 Duty cycle, 8x24 configuration for driving 192 Segments, 32Hz frame rate, No LCD glass connected.	0.67	0.88	3.74	7.16	μA
10	C	PCNT[1]	32KHz clock, without PWM output	33	47	67	77	nA
11	C	PCNT[1]	32KHz clock, with PWM output	40	50	63	77	nA

[1] Not available in stop2 mode.

3.8 External Oscillator (XOSCVLP) Characteristics

Reference Figure 14 and Figure 15 for crystal or resonator circuits.

Table 11. XOSCVLP and ICS Specifications (Temperature Range = –40 to 85°C Ambient)

Num	C	Characteristic	Symbol	Min	Typ[1]	Max	Unit
1	C	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1) Low range (RANGE = 0) High range (RANGE = 1), high gain (HGO = 1) High range (RANGE = 1), low power (HGO = 0)	 f_{lo} f_{hi} f_{hi}	 32 1 1	 — — —	 38.4 16 8	 kHz MHz MHz
2	D	Load capacitors Low range (RANGE=0), low power (HGO=0) Other oscillator settings	C_1,C_2	See Note [2] See Note [3]			
3	D	Feedback resistor Low range, low power (RANGE=0, HGO=0)[2] Low range, high gain (RANGE=0, HGO=1) High range (RANGE=1, HGO=X)	R_F	 — — —	 — 10 1	 — — —	MΩ
4	D	Series resistor — Low range, low power (RANGE = 0, HGO = 0)[2] Low range, high gain (RANGE = 0, HGO = 1) High range, low power (RANGE = 1, HGO = 0) High range, high gain (RANGE = 1, HGO = 1) ≥ 8 MHz 4 MHz 1 MHz	R_S	 — — — — — —	 — 100 0 0 0 0	 — — — 0 10 20	kΩ
5	C	Crystal start-up time [4] Low range, low power Low range, high gain High range, low power High range, high gain	 t_{CSTL} t_{CSTH} 	 — — — —	 600 400 5 15	 — — — —	ms
6	D	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1) FEE mode FBE or FBELP mode	f_{extal}	0.03125 0	—	20 20	MHz MHz

1 Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

2 Load capacitors (C_1,C_2), feedback resistor (R_F) and series resistor (R_S) are incorporated internally when RANGE=HGO=0.

3 See crystal or resonator manufacturer's recommendation.

4 Proper PC board layout procedures must be followed to achieve specifications.

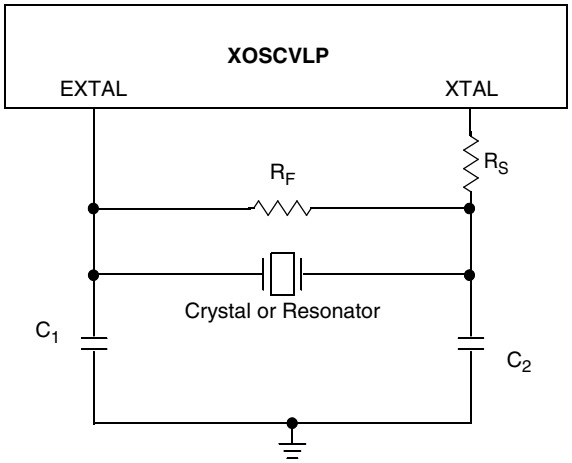


Figure 14. Typical Crystal or Resonator Circuit: High Range and Low Range/High Gain

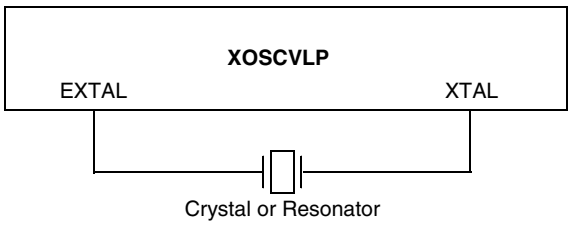


Figure 15. Typical Crystal or Resonator Circuit: Low Range/Low Power

3.9 Internal Clock Source (ICS) Characteristics

Table 12. ICS Frequency Specifications (Temperature Range = –40 to 85°C Ambient)

Num	C	Characteristic	Symbol	Min	Typ[1]	Max	Unit
1	P	Average internal reference frequency — factory trimmed at VDD = 3.6 V and temperature = 25 °C	f_{int_ft}	—	32.768	—	kHz
2	P	Average internal reference frequency - trimmed	f_{int_t}	31.25	—	39.063	kHz
3	T	Internal reference start-up time	t_{IRST}	—	—	6	µs
4	P	DCO output frequency range - untrimmed	f_{dco_ut}	12.8	16.8	21.33	MHz
5	P	DCO output frequency range - trimmed	f_{dco_t}	16	—	20	MHz
6	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM)	$\Delta f_{dco\_res\_t}$	—	± 0.1	± 0.2	$\%f_{dco}$
7	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)	$\Delta f_{dco\_res\_t}$	—	± 0.2	± 0.4	$\%f_{dco}$
8	C	Total deviation from trimmed DCO output frequency over voltage and temperature	Δf_{dco_t}	—	+ 0.5 -1.0	± 2	$\%f_{dco}$

3.10.1 Control Timing

Table 13. Control Timing

Num	C	Rating	Symbol	Min	Typ[1]	Max	Unit
1	D	Bus frequency (t_{cyc} = 1/f_{Bus})	f_{Bus}	dc	—	20	MHz
2	D	Internal low power oscillator period	t_{LPO}	700	—	1300	μs
3	D	External reset pulse width[2]	t_{extrst}	100	—	—	ns
4	D	Reset low drive	t_{rstdrv}	34 x t_{cyc}	—	—	ns
5	D	BKGD/MS setup time after issuing background debug force reset to enter user or BDM modes	t_{MSSU}	500	—	—	ns
6	D	BKGD/MS hold time after issuing background debug force reset to enter user or BDM modes [3]	t_{MSH}	100	—	—	μs
7	D	IRQ pulse width Asynchronous path[2] Synchronous path[4]	t_{ILIH}, t_{IHIL}	 100 1.5 x t_{cyc}	 — —	 — —	ns
8	D	Keyboard interrupt pulse width Asynchronous path[2] Synchronous path[4]	t_{ILIH}, t_{IHIL}	 100 1.5 x t_{cyc}	 — —	 — —	ns
9	C	Port rise and fall time — Non-LCD Pins Low output drive (PTxDS = 0) (load = 50 pF)[5, 6] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	 — —	 16 23	 — —	ns
		Port rise and fall time — Non-LCD Pins High output drive (PTxDS = 1) (load = 50 pF)[5, 6] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	 — —	 5 9	 — —	ns
10	C	Voltage Regulator Recovery time	t_{VRR}	—	6	10	us

1 Typical values are based on characterization data at V_{DD} = 3.0 V, 25°C unless otherwise stated.

2 This is the shortest pulse that is guaranteed to be recognized as a reset pin request.

3 To enter BDM mode following a POR, BKGD/MS should be held low during the power-up and for a hold time of t_{MSH} after V_{DD} rises above V_{LVD}.

4 This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized.

5 Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40°C to 85°C.

6 Except for LCD pins in Open Drain mode.

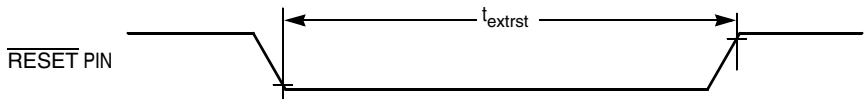


Figure 17. Reset Timing

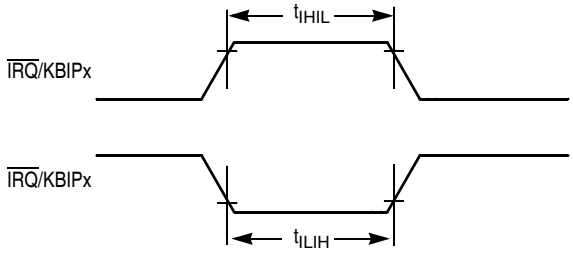


Figure 18. IRQ/KBIPx Timing

3.10.2 Timer (TPM/FTM) Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 14. TPM Input Timing

No.	C	Function	Symbol	Min	Max	Unit
1	D	External clock frequency	f_{TCLK}	0	$f_{Bus}/4$	Hz
2	D	External clock period	t_{TCLK}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

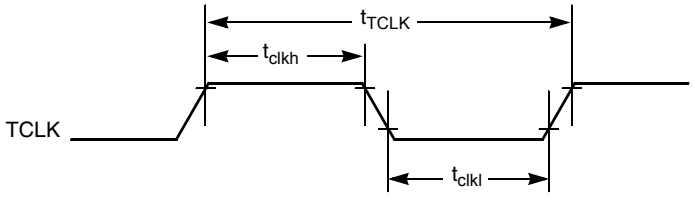
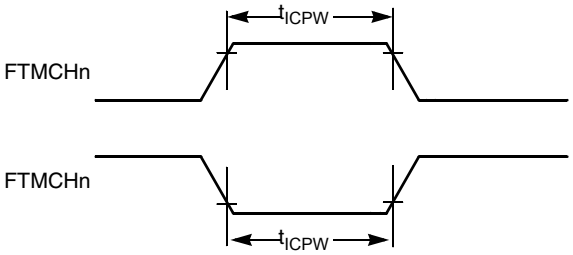


Figure 19. Timer External Clock



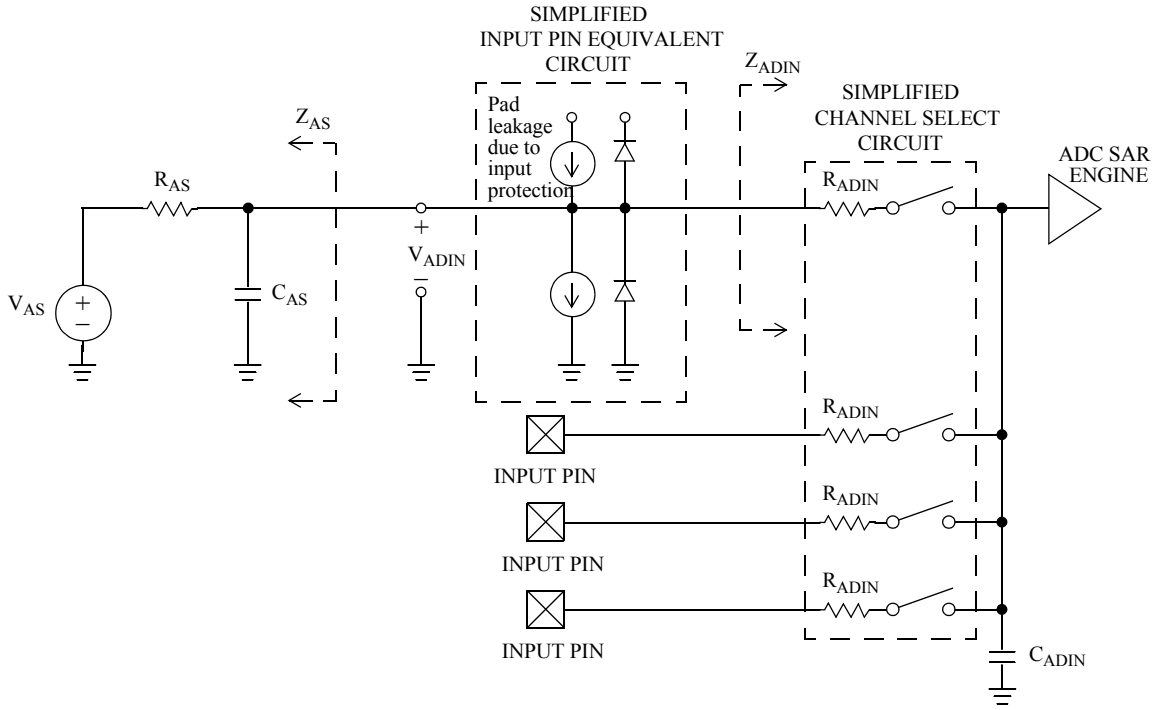


Figure 24. ADC Input Impedance Equivalency Diagram

Table 18. 16-bit ADC Characteristics full operating range($V_{REFH} = V_{DDAD}$, $V_{REFL} = V_{SSAD}$, $F_{ADCK} \leq 10MHz$)

Characteristic	Conditions[1]	C	Symb	Min	Typ[2]	Max	Unit	Comment
Supply Current	ADLPC = 1, ADHSC = 0	T	I_{DDA}	—	215	—	μA	ADLSMP = 0 ADCO = 1
	ADLPC = 0, ADHSC = 0			—	540	—		
	ADLPC=0, ADHSC=1			—	610	—		
Supply Current	Stop, Reset, Module Off	C	I_{DDA}	—	0.072	—	μA	
ADC Asynchronous Clock Source	ADLPC = 1, ADHSC = 0	P	f_{ADACK}	—	2.4	—	MHz	$t_{ADACK} = 1/f_{ADACK}$
	ADLPC = 0, ADHSC = 0			—	5.2	—		
	ADLPC = 0, ADHSC = 1			—	6.2	—		
Sample Time	See reference manual for sample times							
Conversion Time	See reference manual for conversion times							

1 All accuracy numbers assume the ADC is calibrated with $V_{REFH} = V_{DDAD}$

2 Typical values assume V_{DDAD} = 3.0V, Temp = 25°C, f_{ADCK} = 2.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

Table 19. 16-bit ADC Characteristics($V_{REFH} = V_{DDAD} \geq 2.7V$, $V_{REFL} = V_{SSAD}$, $F_{ADCK} \leq 4MHz$, ADHSC=1)

Characteristic	Conditions[1]	C	Symb	Min	Typ[2]	Max	Unit	Comment
Total Unadjusted Error	16-bit differential mode 16-bit single-ended mode	T	TUE	— —	±16 ±20	+24/-24 +32/-20	LSB[3]	32x Hardware Averaging (AVGE = %1 AVGS = %11)
	13-bit differential mode 12-bit single-ended mode	T		— —	±1.5 ±1.75	±2.0 ±2.5		
	11-bit differential mode 10-bit single-ended mode	T		— —	±0.7 ±0.8	±1.0 ±1.25		
	9-bit differential mode 8-bit single-ended mode	T		— —	±0.5 ±0.5	±1.0 ±1.0		
Differential Non-Linearity	16-bit differential mode 16-bit single-ended mode	T	DNL	— —	±2.5 ±2.5	±3 ±3	LSB[2]	
	13-bit differential mode 12-bit single-ended mode	T		— —	±0.7 ±0.7	±1 ±1		
	11-bit differential mode 10-bit single-ended mode	T		— —	±0.5 ±0.5	±0.75 ±0.75		
	9-bit differential mode 8-bit single-ended mode	T		— —	±0.2 ±0.2	±0.5 ±0.5		
Integral Non-Linearity	16-bit differential mode 16-bit single-ended mode	T	INL	— —	±6.0 ±10.0	±12.0 ±16.0	LSB[2]	
	13-bit differential mode 12-bit single-ended mode	T		— —	±1.0 ±1.0	±2.0 ±2.0		
	11-bit differential mode 10-bit single-ended mode	T		— —	±0.5 ±0.5	±1.0 ±1.0		
	9-bit differential mode 8-bit single-ended mode	T		— —	±0.3 ±0.3	±0.5 ±0.5		
Zero-Scale Error	16-bit differential mode 16-bit single-ended mode	T	E_{ZS}	— —	±4.0 ±4.0	+16/0 +16/-38	LSB[2]	$V_{ADIN} = V_{SSAD}$
	13-bit differential mode 12-bit single-ended mode	T		— —	±0.7 ±0.7	±2.0 ±2.0		
	11-bit differential mode 10-bit single-ended mode	T		— —	±0.4 ±0.4	±1.0 ±1.0		
	9-bit differential mode 8-bit single-ended mode	T		— —	±0.2 ±0.2	±0.5 ±0.5		