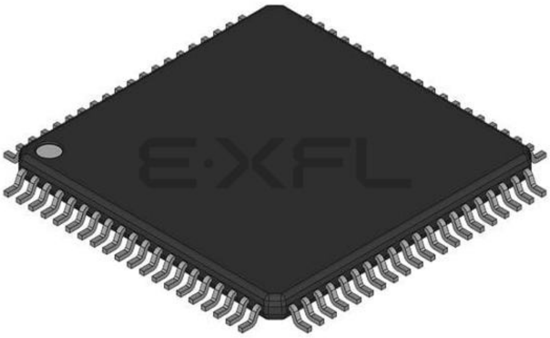

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	LCD, PWM, WDT
Number of I/O	45
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 16x16b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9s08gw64clk

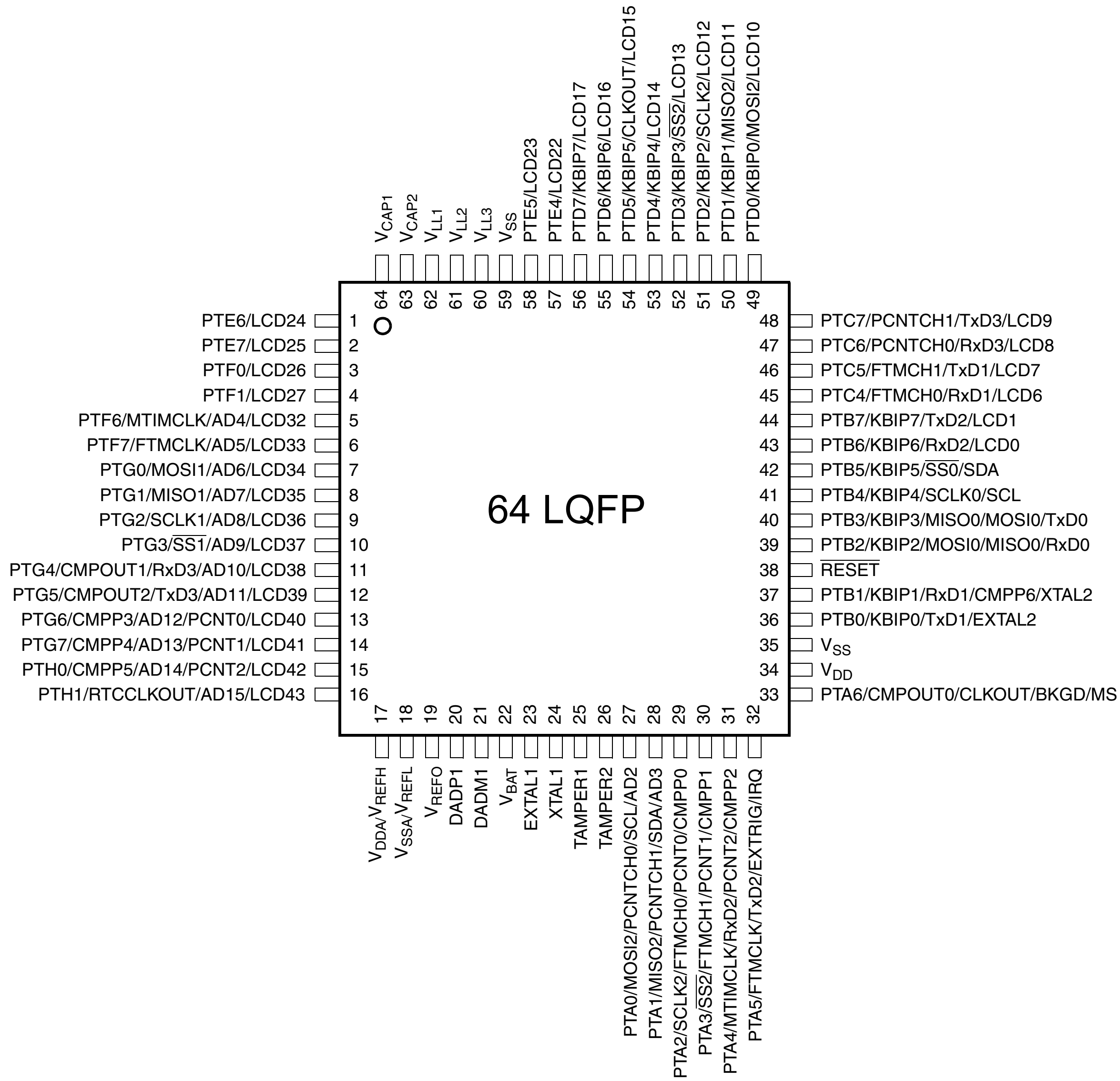


Figure 3. MC9S08GW64 Series in 64-Pin LQFP Package

Table 2. Pin Availability by Package Pin-Count

80	64	Port Pin	Default func	Alt 1	Alt 2	Alt3	Alt4
1	1	PTE6	PTE6		LCD24		
2	2	PTE7	PTE7		LCD25		
3	3	PTF0	PTF0	LCD26			
4	4	PTF1	PTF1	LCD27			
5		PTF2	PTF2	LCD28			
6		PTF3	PTF3	LCD29			

Table 2. Pin Availability by Package Pin-Count (continued)

80	64	Port Pin	Default func	Alt 1	Alt 2	Alt3	Alt4
7		PTF4	PTF4	LCD30			
8		PTF5	PTF5	LCD31			
9	5	PTF6	PTF6	MTIMCLK	AD4	LCD32	
10	6	PTF7	PTF7	FTMCLK	AD5	LCD33	
11	7	PTG0	PTG0	MOSI1	AD6	LCD34	
12	8	PTG1	PTG1	MISO1	AD7	LCD35	
13	9	PTG2	PTG2	SCLK1	AD8	LCD36	
14	10	PTG3	PTG3	$\overline{SS1}$	AD9	LCD37	
15	11	PTG4	PTG4	CMPOUT1	RxD3	AD10	LCD38
16	12	PTG5	PTG5	CMPOUT2	TxD3	AD11	LCD39
17	13	PTG6	PTG6	CMPP3	AD12	PCNT0	LCD40
18	14	PTG7	PTG7	CMPP4	AD13	PCNT1	LCD41
19	15	PTH0	PTH0	CMPP5	AD14	PCNT2	LCD42
20	16	PTH1	PTH1	RTCCLKOUT	AD15	LCD43	
21	17	V_{DDA}	V_{DDA}				
22		V_{REFH}	V_{REFH}				
23	18	V_{SSA}	V_{SSA}				
24		V_{REFL}	V_{REFL}				
25		DADP0	DADP0				
26		DADM0	DADM0				
27	19	V_{REFO}	V_{REFO}				
28	20	DADP1	DADP1				
29	21	DADM1	DADM1				
30	22	V_{BAT}	V_{BAT}				
31	23	EXTAL1	EXTAL1				
32	24	XTAL1	XTAL1				
33	25	TAMPER1[1]	TAMPER1				
34	26	TAMPER2	TAMPER2				
35	27	PTA0	PTA0	MOSI2	PCNTCH0	SCL	AD2
36	28	PTA1	PTA1	MISO2	PCNTCH1	SDA	AD3
37	29	PTA2	PTA2	SCLK2	FTMCH0	PCNT0	CMPP0
38	30	PTA3	PTA3	$\overline{SS2}$	FTMCH1	PCNT1	CMPP1
39	31	PTA4	PTA4	MTIMCLK	RxD2	PCNT2	CMPP2
40	32	PTA5[2]	PTA5	FTMCLK	TxD2	EXTRIG	IRQ
41	33	PTA6[3]	BKGD/MS	CMPOUT0	CLKOUT	BKGD/MS	

Table 2. Pin Availability by Package Pin-Count (continued)

80	64	Port Pin	Default func	Alt 1	Alt 2	Alt3	Alt4
42	34	V_{DD}	V_{DD}				
43	35	V_{SS}	V_{SS}				
44	36	PTB0	PTB0	KBIP0	TxD1	EXTAL2	
45	37	PTB1[1]	PTB1	KBIP1	RxD1	CMPP6	XTAL2
46	38	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$				
47	39	PTB2	PTB2	KBIP2	MOSI0	MISO0	RxD0
48	40	PTB3[4]	PTB3	KBIP3	MISO0	MOSI0	TxD0
49	41	PTB4[3]	PTB4	KBIP4	SCLK0	SCL	
50	42	PTB5[3]	PTB5	KBIP5	$\overline{\text{SS0}}$	SDA	
51	43	PTB6	PTB6	KBIP6	RxD2	LCD0	
52	44	PTB7	PTB7	KBIP7	TxD2	LCD1	
53		PTC0	PTC0	MOSI1	LCD2		
54		PTC1	PTC1	MISO1	LCD3		
55		PTC2	PTC2	SCLK1	LCD4		
56		PTC3	PTC3	$\overline{\text{SS1}}$	LCD5		
57	45	PTC4	PTC4	FTMCH0	RxD1	LCD6	
58	46	PTC5	PTC5	FTMCH1	TxD1	LCD7	
59	47	PTC6	PTC6	PCNTCH0	RxD3	LCD8	
60	48	PTC7	PTC7	PCNTCH1	TxD3	LCD9	
61	49	PTD0	PTD0	KBIP0	MOSI2	LCD10	
62	50	PTD1	PTD1	KBIP1	MISO2	LCD11	
63	51	PTD2	PTD2	KBIP2	SCLK2	LCD12	
64	52	PTD3	PTD3	KBIP3	$\overline{\text{SS2}}$	LCD13	
65	53	PTD4	PTD4	KBIP4	LCD14		
66	54	PTD5	PTD5	KBIP5	CLKOUT	LCD15	
67	55	PTD6	PTD6	KBIP6	LCD16		
68	56	PTD7	PTD7	KBIP7	LCD17		
69		PTE0	PTE0	LCD18			
70		PTE1	PTE1	LCD19			
71		PTE2	PTE2	LCD20			
72		PTE3	PTE3	LCD21			
73	57	PTE4	PTE4		LCD22		
74	58	PTE5	PTE5		LCD23		
75	59	V_{SS}	V_{SS}				
76	60	V_{LL3}	V_{LL3}				

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \qquad \textit{Eqn. 1}$$

where:

T_A = Ambient temperature, °C
θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W
$P_D = P_{int} + P_{I/O}$
$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power
$P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \qquad \textit{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273°C) + \theta_{JA} \times (P_D)^2 \qquad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

3.5 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, normal handling precautions should be taken to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits. During the device qualification, ESD stresses were performed for the human body model (HBM), the machine model (MM) and the charge device model (CDM).

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless instructed otherwise in the device specification.

Table 6. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body Model	Series resistance	R1	1500	Ω
	Storage capacitance	C	100	pF
	Number of pulses per pin	—	3	
Charge Device Model	Series resistance	R1	0	Ω
	Storage capacitance	C	200	pF
	Number of pulses per pin	—	3	
Latch-up	Minimum input voltage limit		–2.5	V
	Maximum input voltage limit		7.5	V

Table 7. ESD and Latch-Up Protection Characteristics

No.	Rating[1]	Symbol	Min	Max	Unit
1	Human body model (HBM)	V_{HBM}	±2000	—	V
2	Machine Model (MM)	V_{MM}	±200	—	V
3	Charge device model (CDM)	V_{CDM}	±500	—	V
4	Latch-up current at T_A = 85°C (applies to all pins except pin 31EXTAL1 and pin 30 XTAL1 in 80-pin package, applies to all pins except pin 23 EXTAL1 and pin 24 XTAL1 in 64-pin package)	I_{LAT}	±100[2]	—	mA
	Latch-up current at T_A = 85°C (applies to pin 31EXTAL1 and pin 30 XTAL1 in 80-pin package, applies to pin 23 EXTAL1 and pin 24 XTAL1 in 64-pin package)	I_{LAT}	±62[3]	—	mA

1 Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

2 These pins meet JESD78A Class II (section 1.2) Level A (section 1.3) requirement of ±100mA.

3 This pin meets JESD78A Class II (section 1.2) Level B (section 1.3) characterization to ±62mA.

3.6 DC Characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 8. DC Characteristics

Num	C	Characteristic		Symbol	Condition	Min	Typ[1]	Max	Unit
1		Operating Voltage				1.8		3.6	V
2	C	Output high voltage	All non-LCD pins low-drive strength	V_{OH}	V_{DD} >1.8 V I_{Load} = –0.6 mA	V_{DD} – 0.5	—	—	V
	P		All non-LCD pins high-drive strength		V_{DD} > 2.7 V I_{Load} = –10 mA	V_{DD} – 0.5	—	—	
	C				V_{DD} > 1.8 V I_{Load} = –3 mA	V_{DD} – 0.5	—	—	
3	C	Output high voltage	All LCD/GPIO pins low-drive strength	V_{OH}	V_{DD} >1.8 V I_{Load} = –0.5 mA	V_{DD} – 0.5	—	—	V
	P		All LCD/GPIO pins high-drive strength		V_{DD} > 2.7 V I_{Load} = –2.5 mA	V_{DD} – 0.5	—	—	
	C				V_{DD} > 1.8 V I_{Load} = –1 mA	V_{DD} – 0.5	—	—	
4	D	Output high current	Max total I_{OH} for all ports	I_{OHT}		—	—	100	mA

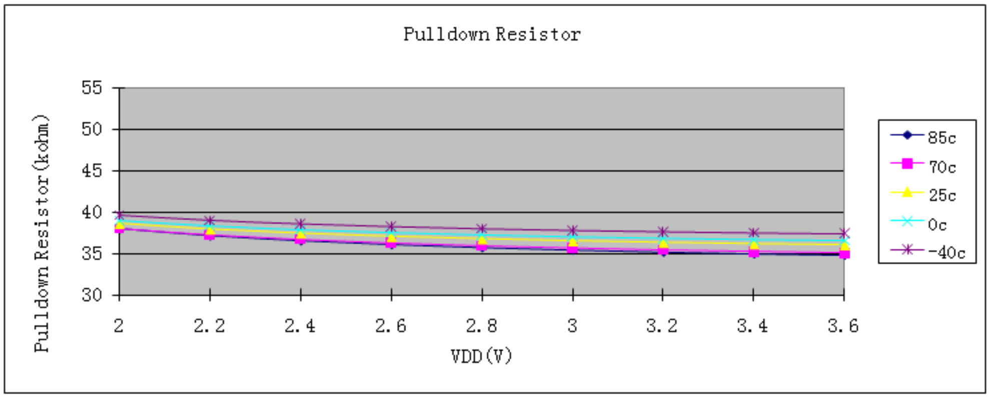
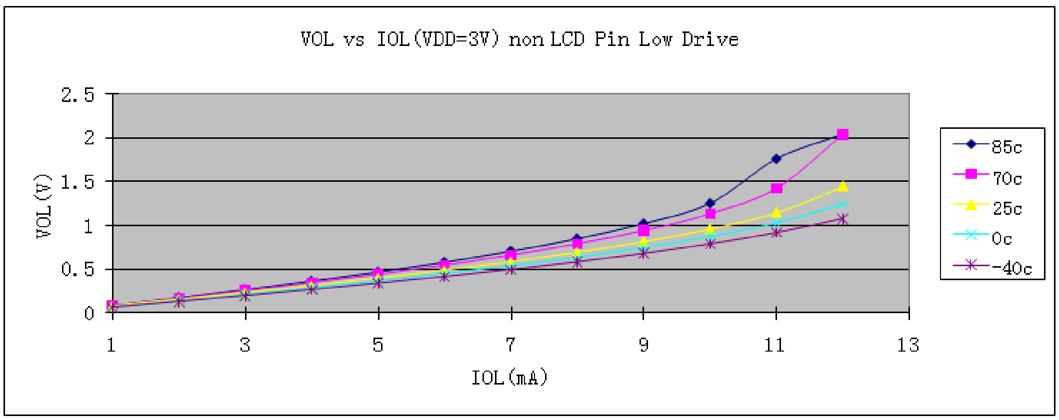


Figure 5. Non LCD pins I/O Pulldown Typical Resistor Values



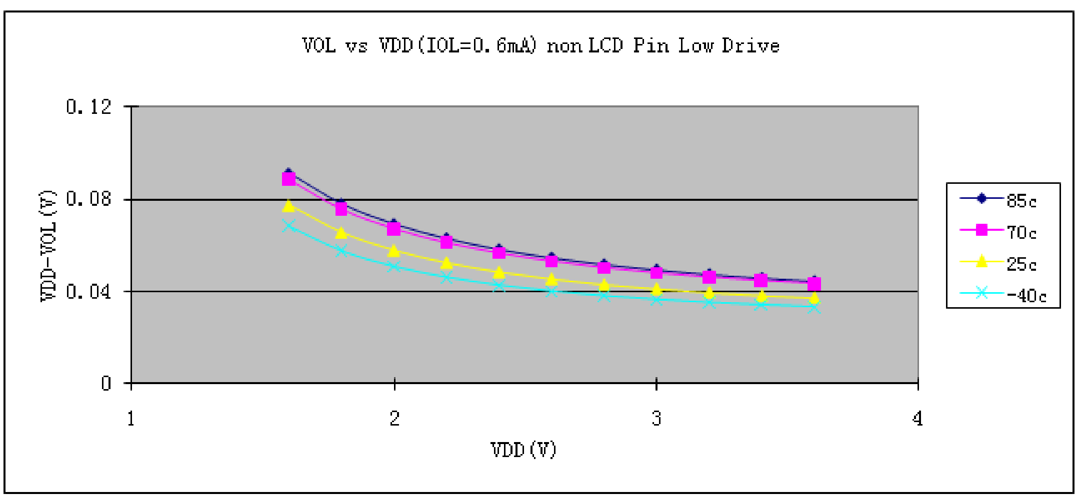
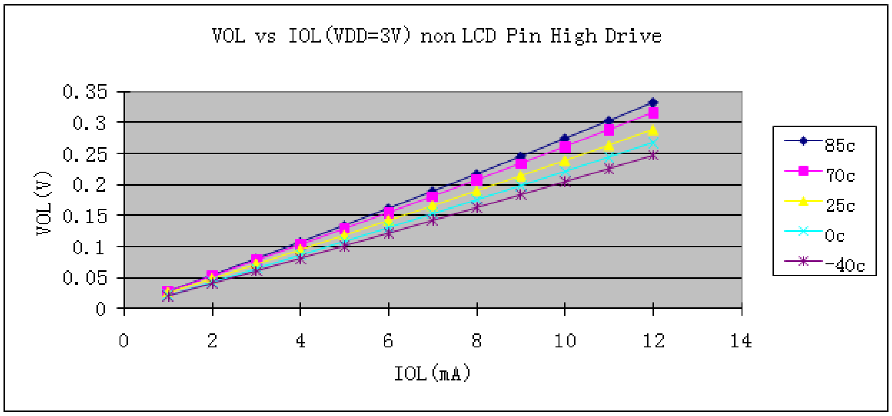


Figure 6. Typical Low-Side Driver (Sink) Characteristics(Non LCD pins) — Low Drive (PTxDSn = 0)



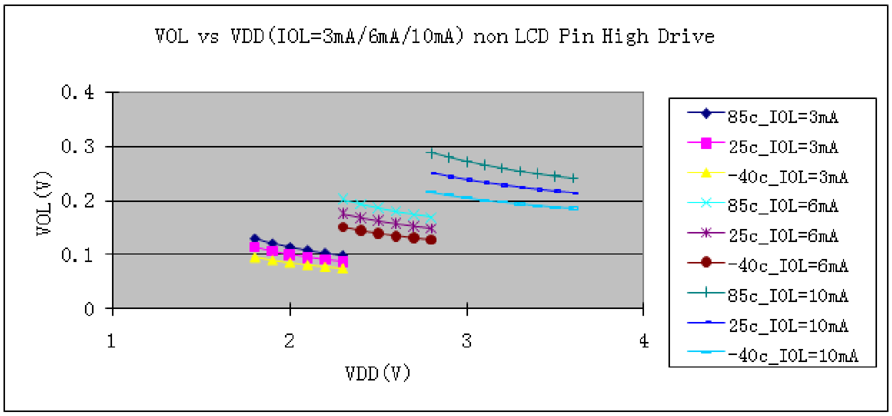


Figure 7. Typical Low-Side Driver (Sink) Characteristics(Non LCD pins) — High Drive (PTxDSn = 1)

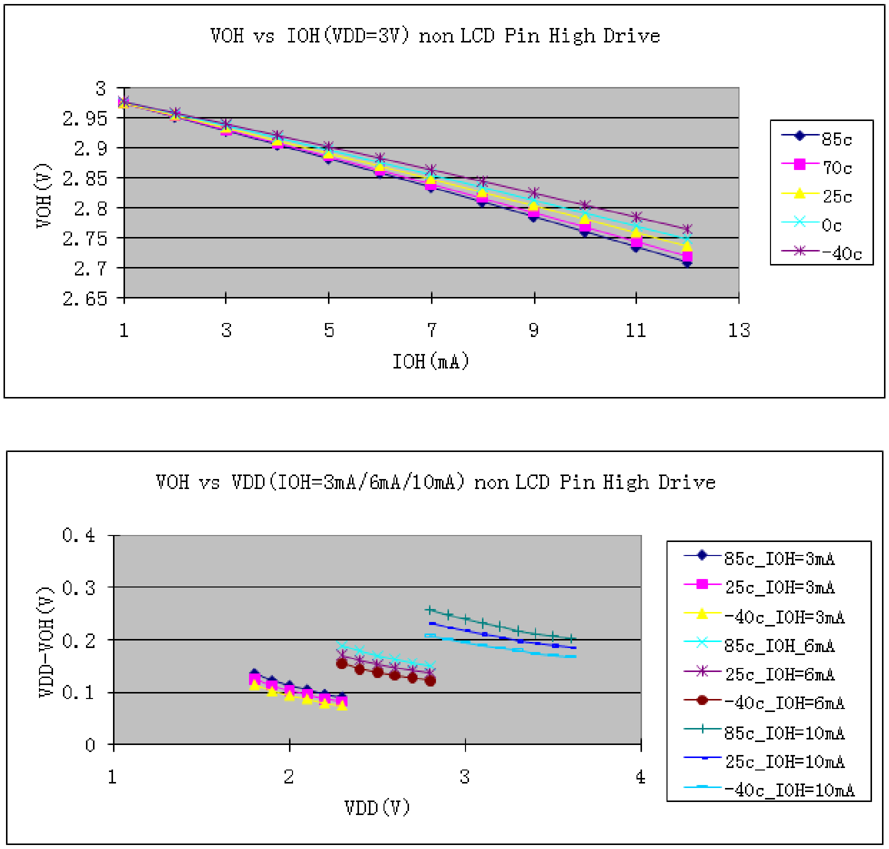


Figure 9. Typical High-Side (Source) Characteristics(Non LCD pins) — High Drive (PTxDSn = 1)

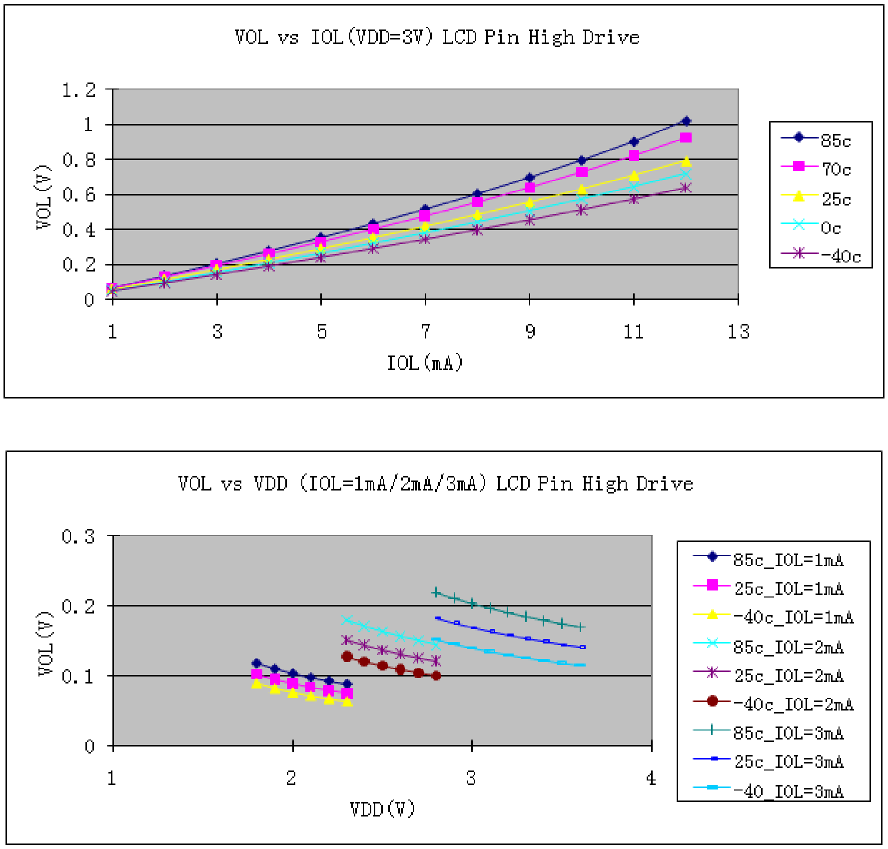


Figure 11. Typical Low-Side Driver (Sink) Characteristics(LCD/GPIO pins) — High Drive (PTxDSn = 1)

Table 9. Supply Current Characteristics

Num	C	Parameter	Symbol	Bus Freq	V_{DD} (V)	Typ[1]	Max	Unit	Temp (°C)
5	T	Run supply current LPRS=1, all modules off; running from RAM	RI_{DD}	16 kHz FBILP	3	137	—	µA	–40 to 85°C
	T			16 kHz FBELP		8	—		
6	C	Wait mode supply current, all modules off	WI_{DD}	20 MHz	3	5.4	7.5	mA	–40 to 85°C
	C			2 MHz		1.1	—		
7	T	Wait mode supply current LPRS = 0, all modules off	WI_{DD}	16 kHz FBILP	3	131	—	µA	–40 to 85°C
	T			16 kHz FBELP	3	123	—	µA	–40 to 85°C
8	T	Wait mode supply current LPRS = 1, all modules off	WI_{DD}	16 kHz FBILP	3	159	—	µA	–40 to 85°C
	T			16 kHz FBELP	3	5.6	—	µA	–40 to 85°C
9	C	Stop2 mode supply current	$S2I_{DD}$	N/A	3	330	1000	nA	–40 to 25°C
						1622	—		70°C
						6000	—		85°C
	C			N/A	2	—	—		–40 to 25°C
						—	—		70°C
						—	—		85°C
10	C	Stop3 mode supply current No clocks active	$S3I_{DD}$	N/A	3	474	1100	nA	–40 to 25°C
						2608	—		70°C
						9000	—		85°C
	C			N/A	2	—	—		–40 to 25°C
						—	—		70°C
						—	—		85°C

[1] Typical values are measured at 25°C. Characterized, not tested.

Table 10. Stop Mode Adders (V_{DD}=3V, V_{DDA}=V_{DD})

Num	C	Parameter	Condition	Temperature (°C)				Units
				-40	25	70	85	
1	C	LPO		100	100	150	175	nA
2	C	ERREFSTEN	RANGE = HGO = 0	600	737	830	863	nA
3	C	IREFSTEN[1]		—	73	80	92	µA
4	C	LVD[1]	LVDSE = 1	110	112	112	113	µA
5	C	PRACMP[1]	Not using the bandgap (BGBE = 0), PRG enabled	30	35	40	55	µA

3.8 External Oscillator (XOSCVLP) Characteristics

Reference Figure 14 and Figure 15 for crystal or resonator circuits.

Table 11. XOSCVLP and ICS Specifications (Temperature Range = –40 to 85°C Ambient)

Num	C	Characteristic	Symbol	Min	Typ[1]	Max	Unit
1	C	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1) Low range (RANGE = 0) High range (RANGE = 1), high gain (HGO = 1) High range (RANGE = 1), low power (HGO = 0)	 f_{lo} f_{hi} f_{hi}	 32 1 1	 — — —	 38.4 16 8	 kHz MHz MHz
2	D	Load capacitors Low range (RANGE=0), low power (HGO=0) Other oscillator settings	C_1, C_2	See Note [2] See Note [3]			
3	D	Feedback resistor Low range, low power (RANGE=0, HGO=0)[2] Low range, high gain (RANGE=0, HGO=1) High range (RANGE=1, HGO=X)	R_F	 — — —	 — 10 1	 — — —	MΩ
4	D	Series resistor — Low range, low power (RANGE = 0, HGO = 0)[2] Low range, high gain (RANGE = 0, HGO = 1) High range, low power (RANGE = 1, HGO = 0) High range, high gain (RANGE = 1, HGO = 1) ≥ 8 MHz 4 MHz 1 MHz	R_S	 — — — — — —	 — 100 0 0 0 0	 — — — 0 10 20	kΩ
5	C	Crystal start-up time [4] Low range, low power Low range, high gain High range, low power High range, high gain	t_{CSTL} t_{CSTH}	 — — — —	 600 400 5 15	 — — — —	ms
6	D	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1) FEE mode FBE or FBELP mode	f_{extal}	 0.03125 0	 — —	 20 20	 MHz MHz

[1] Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.
[2] Load capacitors (C_1, C_2), feedback resistor (R_F) and series resistor (R_S) are incorporated internally when RANGE=HGO=0.
[3] See crystal or resonator manufacturer's recommendation.
[4] Proper PC board layout procedures must be followed to achieve specifications.

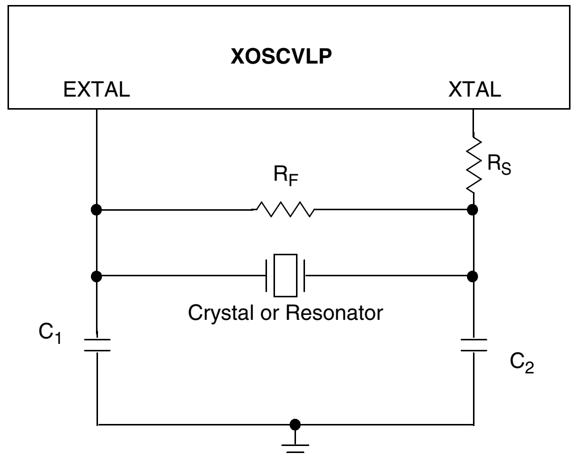


Figure 14. Typical Crystal or Resonator Circuit: High Range and Low Range/High Gain

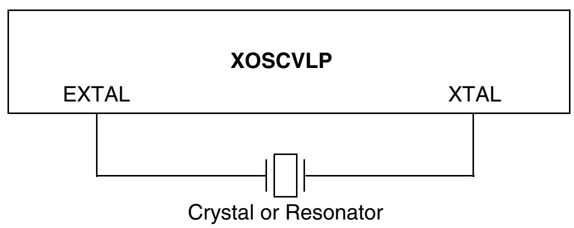


Figure 15. Typical Crystal or Resonator Circuit: Low Range/Low Power

3.9 Internal Clock Source (ICS) Characteristics

Table 12. ICS Frequency Specifications (Temperature Range = –40 to 85°C Ambient)

Num	C	Characteristic	Symbol	Min	Typ[1]	Max	Unit
1	P	Average internal reference frequency — factory trimmed at VDD = 3.6 V and temperature = 25 °C	f_{int_ft}	—	32.768	—	kHz
2	P	Average internal reference frequency - trimmed	f_{int_t}	31.25	—	39.063	kHz
3	T	Internal reference start-up time	t_{IRST}	—	—	6	μs
4	P	DCO output frequency range - untrimmed	f_{dco_ut}	12.8	16.8	21.33	MHz
5	P	DCO output frequency range - trimmed	f_{dco_t}	16	—	20	MHz
6	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM)	$\Delta f_{dco\_res\_t}$	—	± 0.1	± 0.2	$\%f_{dco}$
7	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)	$\Delta f_{dco\_res\_t}$	—	± 0.2	± 0.4	$\%f_{dco}$
8	C	Total deviation from trimmed DCO output frequency over voltage and temperature	Δf_{dco_t}	—	+ 0.5 -1.0	± 2	$\%f_{dco}$

3.10.1 Control Timing

Table 13. Control Timing

Num	C	Rating	Symbol	Min	Typ[1]	Max	Unit
1	D	Bus frequency (t_{cyc} = 1/f_{Bus})	f_{Bus}	dc	—	20	MHz
2	D	Internal low power oscillator period	t_{LPO}	700	—	1300	μs
3	D	External reset pulse width[2]	t_{extrst}	100	—	—	ns
4	D	Reset low drive	t_{rstdrv}	34 x t_{cyc}	—	—	ns
5	D	BKGD/MS setup time after issuing background debug force reset to enter user or BDM modes	t_{MSSU}	500	—	—	ns
6	D	BKGD/MS hold time after issuing background debug force reset to enter user or BDM modes [3]	t_{MSH}	100	—	—	μs
7	D	IRQ pulse width Asynchronous path[2] Synchronous path[4]	t_{ILIH}, t_{IHIL}	 100 1.5 x t_{cyc}	 — —	 — —	ns
8	D	Keyboard interrupt pulse width Asynchronous path[2] Synchronous path[4]	t_{ILIH}, t_{IHIL}	 100 1.5 x t_{cyc}	 — —	 — —	ns
9	C	Port rise and fall time — Non-LCD Pins Low output drive (PTxDS = 0) (load = 50 pF)[5, 6] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	 — —	 16 23	 — —	ns
		Port rise and fall time — Non-LCD Pins High output drive (PTxDS = 1) (load = 50 pF)[5, 6] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	 — —	 5 9	 — —	ns
10	C	Voltage Regulator Recovery time	t_{VRR}	—	6	10	us

1. Typical values are based on characterization data at V_{DD} = 3.0 V, 25°C unless otherwise stated.
2. This is the shortest pulse that is guaranteed to be recognized as a reset pin request.
3. To enter BDM mode following a POR, BKGD/MS should be held low during the power-up and for a hold time of t_{MSH} after V_{DD} rises above V_{LVD}.
4. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized.
5. Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40°C to 85°C.
6. Except for LCD pins in Open Drain mode.

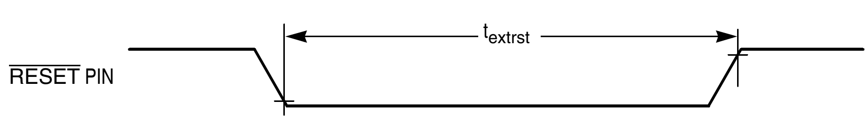


Figure 17. Reset Timing

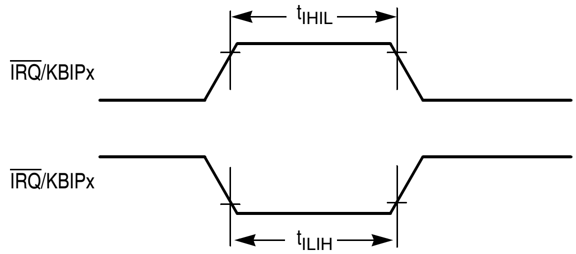


Figure 18. $\overline{IRQ}$/KBIPx Timing

3.10.2 Timer (TPM/FTM) Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 14. TPM Input Timing

No.	C	Function	Symbol	Min	Max	Unit
1	D	External clock frequency	f_{TCLK}	0	$f_{Bus}/4$	Hz
2	D	External clock period	t_{TCLK}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

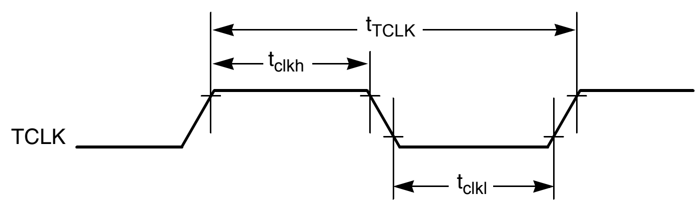
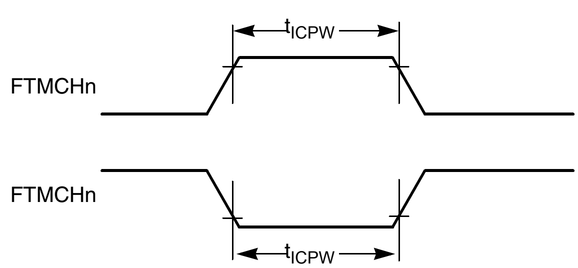


Figure 19. Timer External Clock



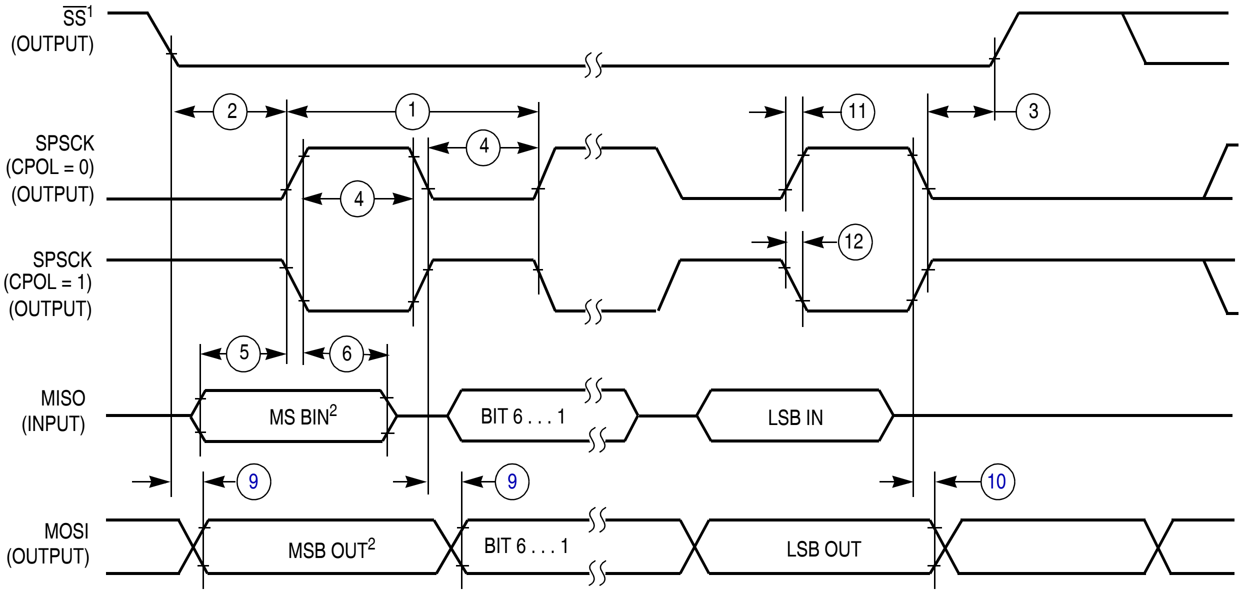
3.10.3 SPI Timing

Table 15 and Figure 20 through Figure 23 describe the timing requirements for the SPI system[1,2].

Table 15. SPI Timing

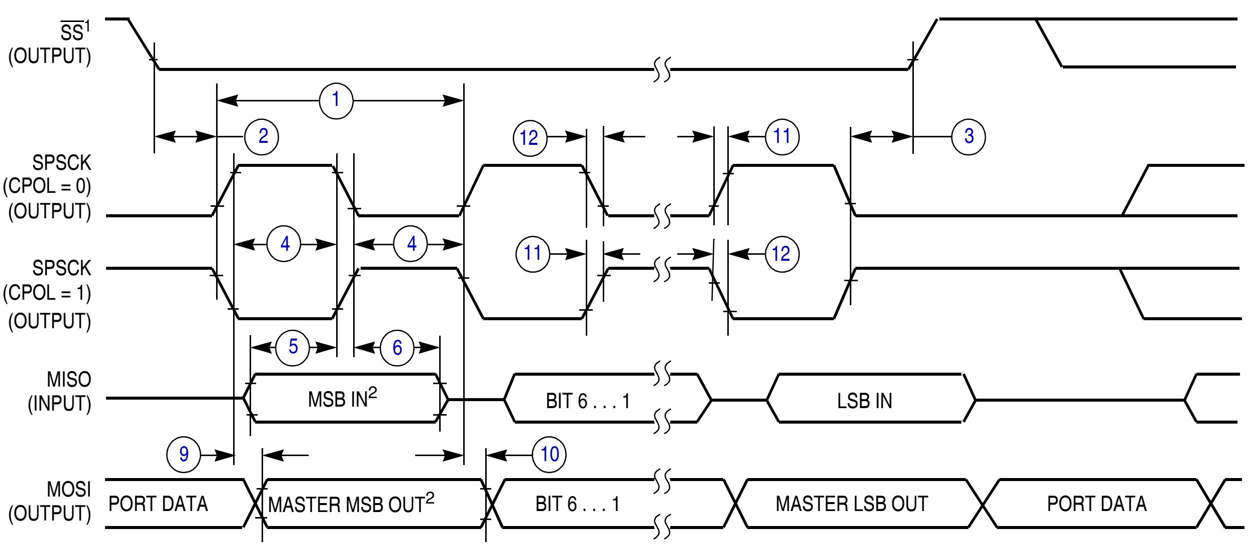
No.	C	Function	Symbol	Min	Max	Unit
—	D	Operating frequency Master Slave	f_{op}	 $f_{Bus}/2048$ 0	 $f_{Bus}/2$ $f_{Bus}/4$	Hz
1	D	SPSCK period Master Slave	t_{SPSCK}	 2 4	 2048 —	 t_{cyc} t_{cyc}
2	D	Enable lead time Master Slave	t_{Lead}	 1/2 1	 — —	 t_{SPSCK} t_{cyc}
3	D	Enable lag time Master Slave	t_{Lag}	 1/2 1	 — —	 t_{SPSCK} t_{cyc}
4	D	Clock (SPSCK) high or low time Master Slave	t_{WSPSCK}	 $t_{cyc} - 30$ $t_{cyc} - 30$	 1024 t_{cyc} —	 ns ns
5	D	Data setup time (inputs) Master Slave	t_{SU}	 30 30	 — —	 ns ns
6	D	Data hold time (inputs) Master Slave	t_{HI}	 0 25	 — —	 ns ns
7	D	Slave access time	t_a	—	1	t_{cyc}
8	D	Slave MISO disable time	t_{dis}	—	1	t_{cyc}
9	D	Data valid (after SPSCK edge) Master Slave	t_v	 — —	 60 60	 ns ns
10	D	Data hold time (outputs) Master Slave	t_{HO}	 0 0	 — —	 ns ns
11	D	Rise time Input Output	 t_{RI} t_{RO}	 — —	 $t_{cyc} - 25$ 25	 ns ns
12	D	Fall time Input Output	 t_{FI} t_{FO}	 — —	 $t_{cyc} - 25$ 25	 ns ns

1.There is 20 pF load on the SPI ports.
2.There are three types of SPI ports in MC9S08GW64 Series. They are ports for AMR, ports shared with LCD pads and normal ports. This timing is for normal ports condition.



NOTES:
1. SS output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 20. SPI Master Timing (CPHA = 0)



NOTES:
1. $\overline{SS}$ output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 21. SPI Master Timing (CPHA =1)

3.11 Analog Comparator (PRACMP) Electricals

Table 16. PRACMP Electrical Specifications

N	C	Characteristic	Symbol	Min	Typical	Max	Unit
1	D	Supply voltage	V_{PWR}	1.8	—	3.6	V
2	C	Supply current (active) (PRG enabled)	I_{DDACT1}	—	—	60	µA
3	C	Supply current (active) (PRG disabled)	I_{DDACT2}	—	—	40	µA
4	C	Supply current (ACMP and PRG all disabled)	I_{DDDIS}	—	—	2	nA
5	D	Analog input voltage	VAIN	V_{SS} – 0.3	—	V_{DD}	V
6	C	Analog input offset voltage	VAIO	—	5	40	mV
7	C	Analog comparator hysteresis	V_H	3.0	—	20.0	mV
8	P	Analog input leakage current	I_{ALKG}	—	—	1	nA
9	C	Analog comparator initialization delay	tAINIT	—	—	1.0	µs
10	C	Programmable reference generator inputs	$V_{In1}(V_{DD})$	1.8	—	V_{DD}	V
11	C	Programmable reference generator inputs	$V_{In2}(V_{DD25})$	1.8	—	2.75	V
12	C	Programmable reference generator setup delay	t_{PRGST}	—	—	—	ns
13	C	Programmable reference generator step size	Vstep	–0.25	1	0.25	LSB
14	C	Programmable reference generator voltage range	Vprgout	$V_{In}/32$	—	V_{in}	V

3.12 ADC Characteristics

These specs all assume seperate V_{DDAD} supply for ADC and isolated pad segment for ADC supplies and differential inputs.. Spec's should be de-rated for $V_{REFH} = V_{bg}$ condition.

Table 17. 16-bit ADC Operating Conditions

Num	Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
1	Supply voltage	Absolute	V_{DDA}	1.8	—	3.6	V	
2		Delta to V_{DD} (V_{DD}–V_{DDA})[2]	ΔV_{DDA}	–100	0	100	mV	
3	Ground voltage	Delta to V_{SS} (V_{SS}–V_{SSA})[2]	ΔV_{SSA}	–100	0	100	mV	
4	Ref Voltage High		V_{REFH}	1.15	V_{DDA}	V_{DDA}	V	

Table 17. 16-bit ADC Operating Conditions

Num	Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
5	Ref Voltage Low		V_{REFL}	V_{SSA}	V_{SSA}	V_{SSA}	V	
6	Input Voltage		V_{ADIN}	V_{REFL}	—	V_{REFH}	V	
7	Input Capacitance	16-bit modes 8/10/12-bit modes	C_{ADIN}	—	8 4	10 5	pF	
8	Input Resistance		R_{ADIN}	—	2	5	kΩ	
9	Analog Source Resistance	16 bit modes f_{ADCK} > 8MHz 4MHz < f_{ADCK} < 8MHz f_{ADCK} < 4MHz	R_{AS}	— — —	— — —	0.5 1 2	kΩ	External to MCU Assumes ADLSMP=0
10		13/12 bit modes f_{ADCK} > 8MHz 4MHz < f_{ADCK} < 8MHz f_{ADCK} < 4MHz		— — —	— — —	1 2 5		
11		11/10 bit modes f_{ADCK} > 8MHz 4MHz < f_{ADCK} < 8MHz f_{ADCK} < 4MHz		— — —	— — —	2 5 10		
12		9/8 bit modes f_{ADCK} > 8MHz f_{ADCK} < 8MHz		— —	— —	5 10		
13	ADC Conversion Clock Freq.	ADLPC = 0, ADHSC = 1	f_{ADCK}	1.0	—	10	MHz	
14		ADLPC = 0, ADHSC = 0		1.0	—	5		
15		ADLPC = 1, ADHSC = 0		1.0	—	2.5		

[1] Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

[2] DC potential difference.

Table 19. 16-bit ADC Characteristics($V_{REFH} = V_{DDAD} \geq 2.7V$, $V_{REFL} = V_{SSAD}$, $F_{ADCK} \leq 4MHz$, ADHSC=1)

Characteristic	Conditions[1]	C	Symb	Min	Typ[2]	Max	Unit	Comment
Total Unadjusted Error	16-bit differential mode 16-bit single-ended mode	T	TUE	— —	±16 ±20	+24/-24 +32/-20	LSB[3]	32x Hardware Averaging (AVGE = %1 AVGS = %11)
	13-bit differential mode 12-bit single-ended mode	T		— —	±1.5 ±1.75	±2.0 ±2.5		
	11-bit differential mode 10-bit single-ended mode	T		— —	±0.7 ±0.8	±1.0 ±1.25		
	9-bit differential mode 8-bit single-ended mode	T		— —	±0.5 ±0.5	±1.0 ±1.0		
Differential Non-Linearity	16-bit differential mode 16-bit single-ended mode	T	DNL	— —	±2.5 ±2.5	±3 ±3	LSB[2]	
	13-bit differential mode 12-bit single-ended mode	T		— —	±0.7 ±0.7	±1 ±1		
	11-bit differential mode 10-bit single-ended mode	T		— —	±0.5 ±0.5	±0.75 ±0.75		
	9-bit differential mode 8-bit single-ended mode	T		— —	±0.2 ±0.2	±0.5 ±0.5		
Integral Non-Linearity	16-bit differential mode 16-bit single-ended mode	T	INL	— —	±6.0 ±10.0	±12.0 ±16.0	LSB[2]	
	13-bit differential mode 12-bit single-ended mode	T		— —	±1.0 ±1.0	±2.0 ±2.0		
	11-bit differential mode 10-bit single-ended mode	T		— —	±0.5 ±0.5	±1.0 ±1.0		
	9-bit differential mode 8-bit single-ended mode	T		— —	±0.3 ±0.3	±0.5 ±0.5		
Zero-Scale Error	16-bit differential mode 16-bit single-ended mode	T	E_{ZS}	— —	±4.0 ±4.0	+16/0 +16/-38	LSB[2]	$V_{ADIN} = V_{SSAD}$
	13-bit differential mode 12-bit single-ended mode	T		— —	±0.7 ±0.7	±2.0 ±2.0		
	11-bit differential mode 10-bit single-ended mode	T		— —	±0.4 ±0.4	±1.0 ±1.0		
	9-bit differential mode 8-bit single-ended mode	T		— —	±0.2 ±0.2	±0.5 ±0.5		

Table 19. 16-bit ADC Characteristics($V_{REFH} = V_{DDAD} \geq 2.7V$, $V_{REFL} = V_{SSAD}$, $F_{ADCK} \leq 4MHz$, ADHSC=1)

Characteristic	Conditions[1]	C	Symb	Min	Typ[2]	Max	Unit	Comment
Full-Scale Error	16-bit differential mode 16-bit single-ended mode	T	E_{FS}	— —	+8/0 +12/0	+24/0 +24/0	LSB[2]	$V_{ADIN} = V_{DDAD}$
	13-bit differential mode 12-bit single-ended mode	T		— —	±0.7 ±0.7	±2.0 ±2.5		
	11-bit differential mode 10-bit single-ended mode	T		— —	±0.4 ±0.4	±1.0 ±1.0		
	9-bit differential mode 8-bit single-ended mode	T		— —	±0.2 ±0.2	±0.5 ±0.5		
Quantization Error	16 bit modes	D	E_Q	—	-1 to 0	—	LSB[2]	
	≤13 bit modes			—	—	±0.5		
Effective Number of Bits	16 bit differential mode Avg = 32 Avg = 16 Avg = 8 Avg = 4 Avg = 1	C	ENOB	 — — — — —	 13.5 13.4 13.2 13 12.6	 — — — — —	Bits	For ADC_DIV=1, ADC_CLK=10 MHz.
	16 bit single-ended mode Avg = 32 Avg = 16 Avg = 8 Avg = 4 Avg = 1			 — — — — —	 12.39 12.34 12.13 11.94 11.4	 — — — — —		
Signal to Noise plus Distortion	See ENOB		SINAD	$SINAD = 6.02 \cdot ENOB + 1.76$			dB	
Total Harmonic Distortion	16-bit differential mode Avg = 32	C	THD	—	—	—	dB	
	16-bit single-ended mode Avg = 32	D		—	—	—		
Spurious Free Dynamic Range	16-bit differential mode Avg = 32	C	SFDR	91.0	96.5	—	dB	
	16-bit single-ended mode Avg = 32	D		—	—	—		
Input Leakage Error	all modes	D	E_{IL}	$I_{In} * R_{AS}$			mV	I_{In} = leakage current (refer to DC characteristics)
Temp Sensor Slope	–40°C–25°C	D	m	—	1.646	—	mV/°C	
	25°C–125°C			—	1.769	—		
Temp Sensor Voltage	25°C	D	V_{TEMP25}	—	966	—	mV	