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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	LCD, PWM, WDT
Number of I/O	45
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 16x16b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s08gw64clkr

Table of Contents

Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://freescale.com/

The following revision history table summarizes changes contained in this document.

Rev	Date	Description of Changes
1	5/26/2010	Initial public release
2	10/29/2010	Completed all the TBDs. Updated the voltage output data in the Table 20. Changed the classification marking of $\|I_{InT}\|$ to C in the Table 8.
3	1/28/2011	Updated Table 7.

Related Documentation

Find the most current versions of all documents at: http://www.freescale.com

Reference Manual (MC9S08GW64RM)

Contains extensive product information including modes of operation, memory, resets and interrupts, register definition, port pins, CPU, and all module information.

1 Devices in the MC9S08GW64 Series

Table 1 summarizes the feature set available in the MC9S08GW64 series of MCUs.

Table 1. MC9S08GW64 Series Features by MCU and Package

Feature	MC9S08GW64		MC9S08GW32	
Package	**80-pin LQFP**	**64-pin LQFP**	**80-pin LQFP**	**64-pin LQFP**
FLASH	65,536 Bytes		32,768 Bytes	
RAM	4,032 Bytes		2,048 Bytes	
ADC0[1] Single-ended Channels	7-ch	7-ch	7-ch	7-ch
ADC0 Differential Channels[2]	1	0	1	0
ADC1 Single-ended Channels	7-ch	7-ch	7-ch	7-ch
ADC1 Differential Channels	1	1	1	1
BKPT	yes		yes	
ICS	yes		yes	
IIC	yes		yes	
IRQ	yes		yes	
IRTC	yes		yes	
KBI	8-ch		8-ch	
MTIM8	2		2	
MTIM16	yes		yes	
PCNT	yes		yes	
PCRC	yes		yes	
PDB	yes		yes	
PRACMP	3		3	
SCI	4		4	
SPI	3		3	
FTM	2-ch		2-ch	
LCD	8×36 4×40	8×24 4×28	8×36 4×40	8×24 4×28
VREFO	yes	yes	yes	yes
XOSC	2		2	
I/O pins[3]	57	45	57	45

1 There are two 16-bit ADC modules, so two parallel conversions at two channels can be made simultaneously.
2 Each differential channel consists of two pins (DADPx and DADMx).
3 The I/O pins include one output-only pin.

The block diagram in Figure 1 shows the structure of the MC9S08GW64 series MCUs.

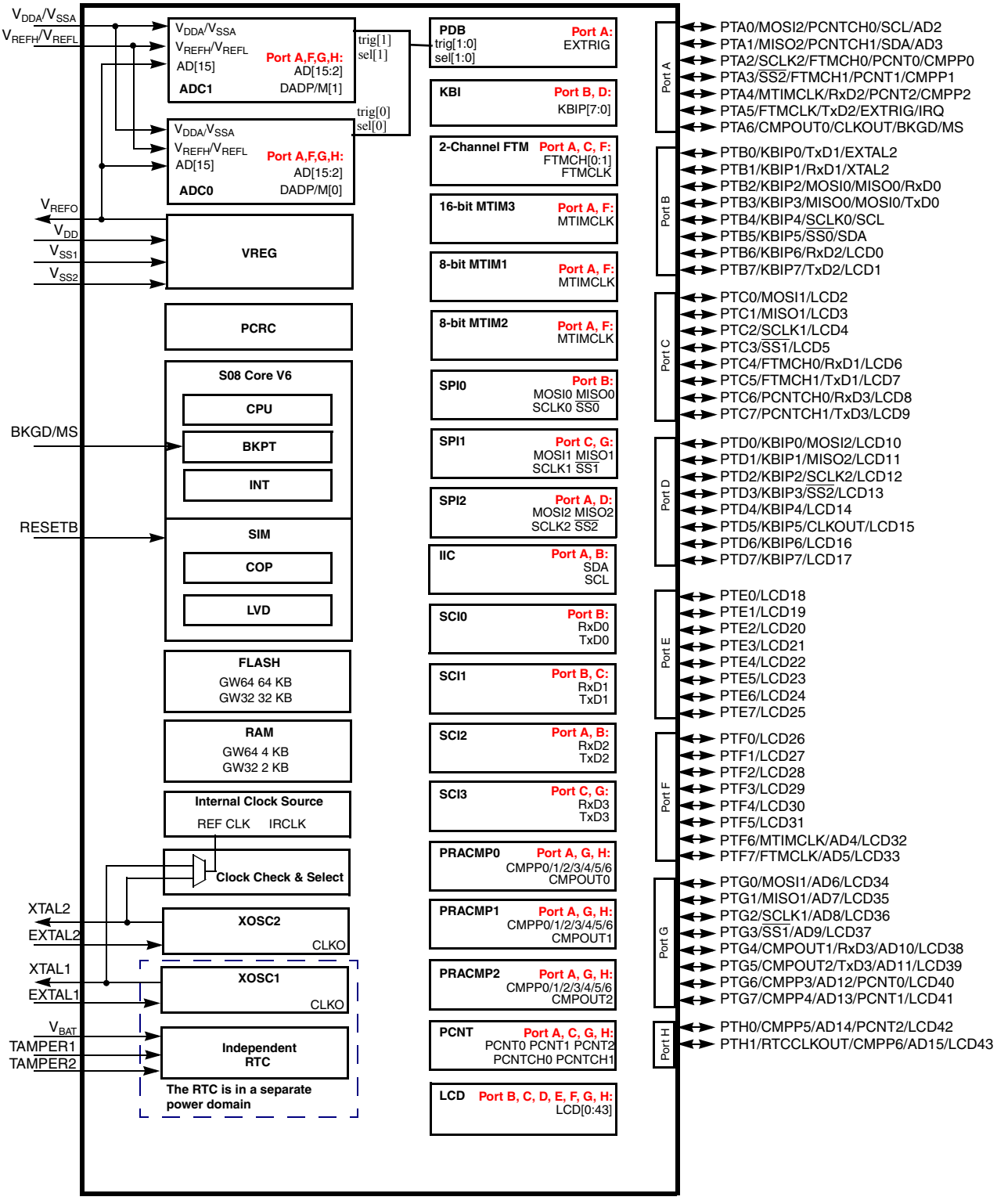


Figure 1. MC9S08GW64 Series Block Diagram

2 Pin Assignments

This section shows the pin assignments for the MC9S08GW64 series devices.

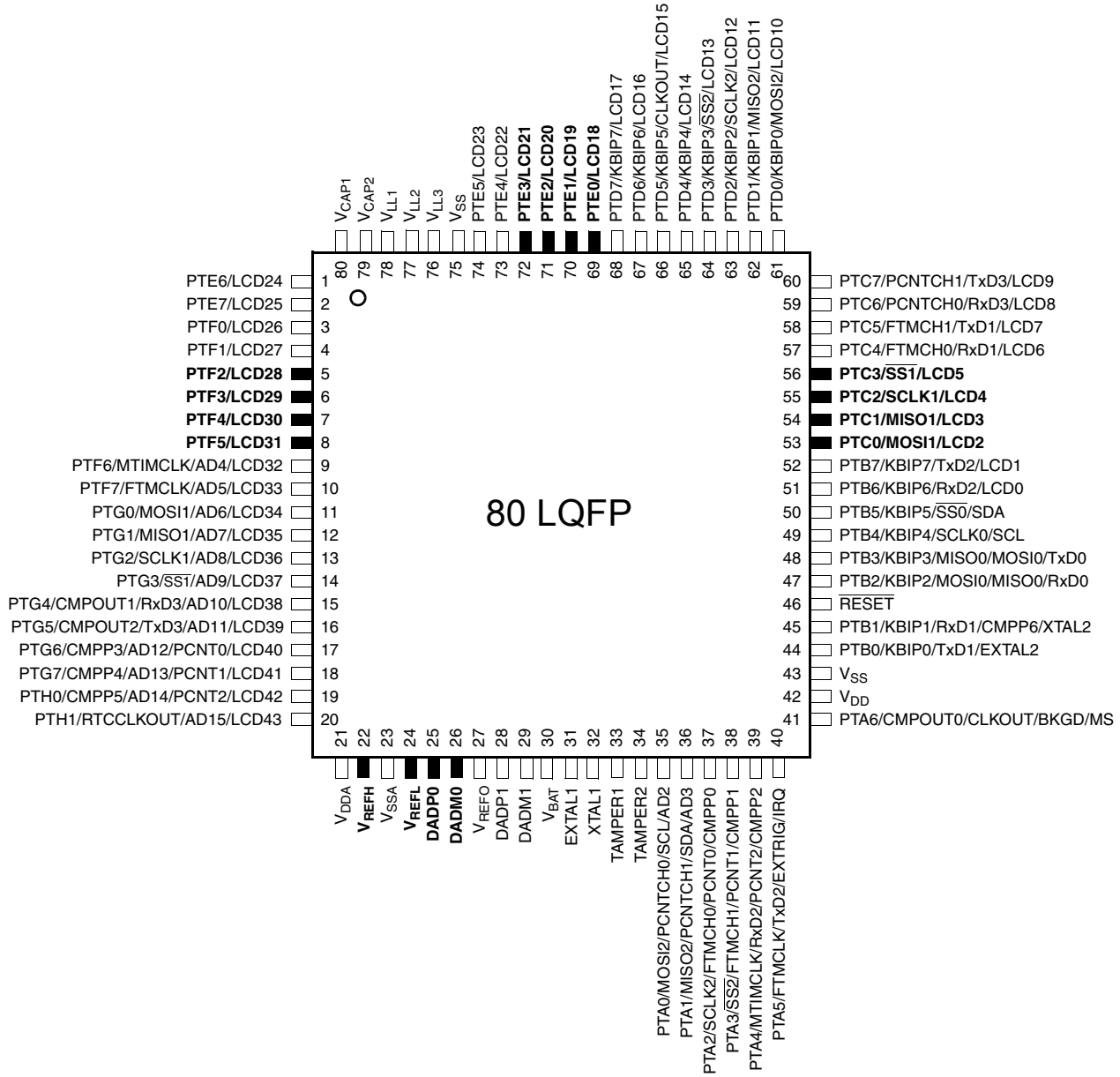


Figure 2. MC9S08GW64 Series in 80-Pin LQFP Package

Table 2. Pin Availability by Package Pin-Count (continued)

80	64	Port Pin	Default func	Alt 1	Alt 2	Alt3	Alt4
7		PTF4	PTF4	LCD30			
8		PTF5	PTF5	LCD31			
9	5	PTF6	PTF6	MTIMCLK	AD4	LCD32	
10	6	PTF7	PTF7	FTMCLK	AD5	LCD33	
11	7	PTG0	PTG0	MOSI1	AD6	LCD34	
12	8	PTG1	PTG1	MISO1	AD7	LCD35	
13	9	PTG2	PTG2	SCLK1	AD8	LCD36	
14	10	PTG3	PTG3	$\overline{SS1}$	AD9	LCD37	
15	11	PTG4	PTG4	CMPOUT1	RxD3	AD10	LCD38
16	12	PTG5	PTG5	CMPOUT2	TxD3	AD11	LCD39
17	13	PTG6	PTG6	CMPP3	AD12	PCNT0	LCD40
18	14	PTG7	PTG7	CMPP4	AD13	PCNT1	LCD41
19	15	PTH0	PTH0	CMPP5	AD14	PCNT2	LCD42
20	16	PTH1	PTH1	RTCCLKOUT	AD15	LCD43	
21	17	V_{DDA}	V_{DDA}				
22		V_{REFH}	V_{REFH}				
23	18	V_{SSA}	V_{SSA}				
24		V_{REFL}	V_{REFL}				
25		DADP0	DADP0				
26		DADM0	DADM0				
27	19	V_{REFO}	V_{REFO}				
28	20	DADP1	DADP1				
29	21	DADM1	DADM1				
30	22	V_{BAT}	V_{BAT}				
31	23	EXTAL1	EXTAL1				
32	24	XTAL1	XTAL1				
33	25	TAMPER1[1]	TAMPER1				
34	26	TAMPER2	TAMPER2				
35	27	PTA0	PTA0	MOSI2	PCNTCH0	SCL	AD2
36	28	PTA1	PTA1	MISO2	PCNTCH1	SDA	AD3
37	29	PTA2	PTA2	SCLK2	FTMCH0	PCNT0	CMPP0
38	30	PTA3	PTA3	$\overline{SS2}$	FTMCH1	PCNT1	CMPP1
39	31	PTA4	PTA4	MTIMCLK	RxD2	PCNT2	CMPP2
40	32	PTA5[2]	PTA5	FTMCLK	TxD2	EXTRIG	IRQ
41	33	PTA6[3]	BKGD/MS	CMPOUT0	CLKOUT	BKGD/MS	

Table 7. ESD and Latch-Up Protection Characteristics

No.	Rating[1]	Symbol	Min	Max	Unit
1	Human body model (HBM)	V_{HBM}	±2000	—	V
2	Machine Model (MM)	V_{MM}	±200	—	V
3	Charge device model (CDM)	V_{CDM}	±500	—	V
4	Latch-up current at T_A = 85°C (applies to all pins except pin 31EXTAL1 and pin 30 XTAL1 in 80-pin package, applies to all pins except pin 23 EXTAL1 and pin 24 XTAL1 in 64-pin package)	I_{LAT}	±100[2]	—	mA
	Latch-up current at T_A = 85°C (applies to pin 31EXTAL1 and pin 30 XTAL1 in 80-pin package, applies to pin 23 EXTAL1 and pin 24 XTAL1 in 64-pin package)	I_{LAT}	±62[3]	—	mA

1 Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

2 These pins meet JESD78A Class II (section 1.2) Level A (section 1.3) requirement of ±100mA.

3 This pin meets JESD78A Class II (section 1.2) Level B (section 1.3) characterization to ±62mA.

3.6 DC Characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 8. DC Characteristics

Num	C	Characteristic		Symbol	Condition	Min	Typ[1]	Max	Unit
1		Operating Voltage				1.8		3.6	V
2	C	Output high voltage	All non-LCD pins low-drive strength	V_{OH}	V_{DD} >1.8 V, I_{Load} = –0.6 mA	V_{DD} – 0.5	—	—	V
	P		All non-LCD pins high-drive strength		V_{DD} > 2.7 V, I_{Load} = –10 mA	V_{DD} – 0.5	—	—	
	C				V_{DD} > 1.8 V, I_{Load} = –3 mA	V_{DD} – 0.5	—	—	
3	C	Output high voltage	All LCD/GPIO pins low-drive strength	V_{OH}	V_{DD} >1.8 V, I_{Load} = –0.5 mA	V_{DD} – 0.5	—	—	V
	P		All LCD/GPIO pins high-drive strength		V_{DD} > 2.7 V, I_{Load} = –2.5 mA	V_{DD} – 0.5	—	—	
	C				V_{DD} > 1.8 V, I_{Load} = –1 mA	V_{DD} – 0.5	—	—	
4	D	Output high current	Max total I_{OH} for all ports	I_{OHT}		—	—	100	mA

Table 8. DC Characteristics (continued)

Num	C	Characteristic		Symbol	Condition	Min	Typ[1]	Max	Unit
22	C	Low-voltage detection threshold	High range — V_{DD} falling	V_{LVDH}		2.11	2.16	2.22	V
			High range — V_{DD} rising			2.16	2.23	2.27	
23	C	Low-voltage detection threshold	Low range — V_{DD} falling	V_{LVDL}		1.80	1.85	1.91	V
			Low range — V_{DD} rising			1.86	1.92	1.99	
24	C	Low-voltage warning threshold	V_{DD} falling, LVWV = 1	V_{LVWH}		2.36	2.46	2.56	V
			V_{DD} rising, LVWV = 1			2.52	2.49	2.71	
25	C	Low-voltage warning	V_{DD} falling, LVWV = 0	V_{LVWL}		2.10	2.16	2.23	V
			V_{DD} rising, LVWV = 0			2.15	2.23	2.26	
26	C	Low-voltage inhibit reset/recover hysteresis		V_{hys}		—	80	—	mV
27	P	Bandgap Voltage Reference[7]		V_{BG}		1.15	1.17	1.19	V

1 Typical values are measured at 25°C. Characterized, not tested

2 Total leakage current is the sum value for all GPIO pins. This leakage current is not distributed evenly across all pins but characterization data shows that individual pin leakage current maximums are less than 250nA.

3 All functional non-supply pins, except for PTB2 are internally clamped to V_{SS} and V_{DD}.

4 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

5 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If the positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure that external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

6 POR will occur below the minimum voltage.

7 Factory trimmed at V_{DD} = 3.0 V, Temp = 25°C

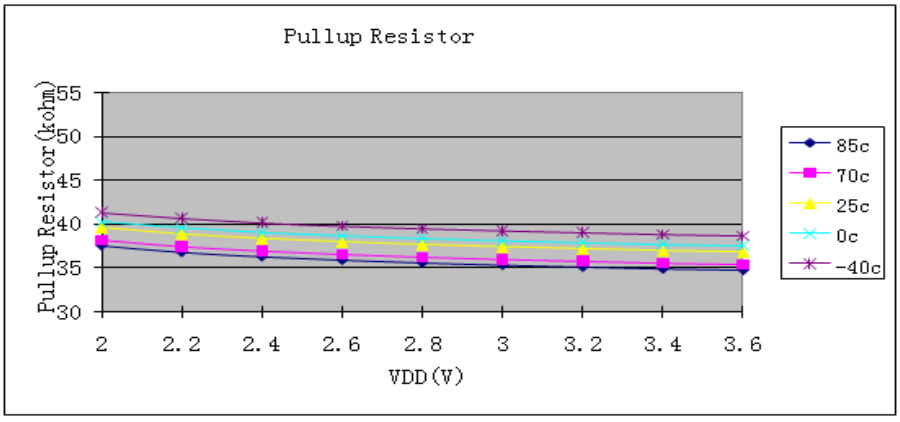


Figure 4. Non LCD pins I/O Pullup Typical Resistor Values

Table 9. Supply Current Characteristics

Num	C	Parameter	Symbol	Bus Freq	V_{DD} (V)	Typ[1]	Max	Unit	Temp (°C)
5	T	Run supply current LPRS=1, all modules off; running from RAM	RI_{DD}	16 kHz FBILP	3	137	—	μA	–40 to 85°C
	T			16 kHz FBELP		8	—		
6	C	Wait mode supply current, all modules off	WI_{DD}	20 MHz	3	5.4	7.5	mA	–40 to 85°C
	C			2 MHz		1.1	—		
7	T	Wait mode supply current LPRS = 0, all modules off	WI_{DD}	16 kHz FBILP	3	131	—	μA	–40 to 85°C
	T			16 kHz FBELP	3	123	—	μA	–40 to 85°C
8	T	Wait mode supply current LPRS = 1, all modules off	WI_{DD}	16 kHz FBILP	3	159	—	μA	–40 to 85°C
	T			16 kHz FBELP	3	5.6	—	μA	–40 to 85°C
9	C	Stop2 mode supply current	$S2I_{DD}$	N/A	3	330	1000	nA	–40 to 25°C
						1622	—		70°C
						6000	—		85°C
	C			N/A	2	—	—		–40 to 25°C
						—	—		70°C
						—	—		85°C
10	C	Stop3 mode supply current No clocks active	$S3I_{DD}$	N/A	3	474	1100	nA	–40 to 25°C
						2608	—		70°C
						9000	—		85°C
	C			N/A	2	—	—		–40 to 25°C
						—	—		70°C
						—	—		85°C

[1] Typical values are measured at 25°C. Characterized, not tested.

Table 10. Stop Mode Adders (V_{DD}=3V, V_{DDA}=V_{DD})

Num	C	Parameter	Condition	Temperature (°C)				Units
				-40	25	70	85	
1	C	LPO		100	100	150	175	nA
2	C	ERREFSTEN	RANGE = HGO = 0	600	737	830	863	nA
3	C	IREFSTEN[1]		—	73	80	92	μA
4	C	LVD[1]	LVDSE = 1	110	112	112	113	μA
5	C	PRACMP[1]	Not using the bandgap (BGBE = 0), PRG enabled	30	35	40	55	μA

3.8 External Oscillator (XOSCVLP) Characteristics

Reference Figure 14 and Figure 15 for crystal or resonator circuits.

Table 11. XOSCVLP and ICS Specifications (Temperature Range = –40 to 85°C Ambient)

Num	C	Characteristic	Symbol	Min	Typ[1]	Max	Unit
1	C	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1) Low range (RANGE = 0) High range (RANGE = 1), high gain (HGO = 1) High range (RANGE = 1), low power (HGO = 0)	 f_{lo} f_{hi} f_{hi}	 32 1 1	 — — —	 38.4 16 8	 kHz MHz MHz
2	D	Load capacitors Low range (RANGE=0), low power (HGO=0) Other oscillator settings	C_1,C_2	See Note [2] See Note [3]			
3	D	Feedback resistor Low range, low power (RANGE=0, HGO=0)[2] Low range, high gain (RANGE=0, HGO=1) High range (RANGE=1, HGO=X)	R_F	 — — —	 — 10 1	 — — —	MΩ
4	D	Series resistor — Low range, low power (RANGE = 0, HGO = 0)[2] Low range, high gain (RANGE = 0, HGO = 1) High range, low power (RANGE = 1, HGO = 0) High range, high gain (RANGE = 1, HGO = 1) ≥ 8 MHz 4 MHz 1 MHz	R_S	 — — — — — —	 — 100 0 0 0 0	 — — — 0 10 20	kΩ
5	C	Crystal start-up time [4] Low range, low power Low range, high gain High range, low power High range, high gain	 t_{CSTL} t_{CSTH} 	 — — — —	 600 400 5 15	 — — — —	ms
6	D	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1) FEE mode FBE or FBELP mode	f_{extal}	0.03125 0	—	20 20	MHz MHz

1 Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

2 Load capacitors (C_1,C_2), feedback resistor (R_F) and series resistor (R_S) are incorporated internally when RANGE=HGO=0.

3 See crystal or resonator manufacturer's recommendation.

4 Proper PC board layout procedures must be followed to achieve specifications.

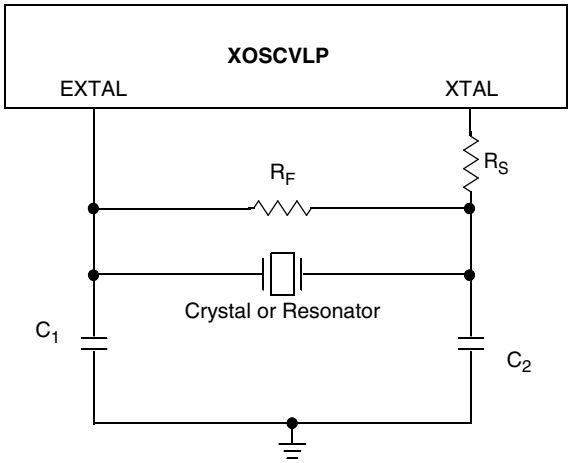


Figure 14. Typical Crystal or Resonator Circuit: High Range and Low Range/High Gain

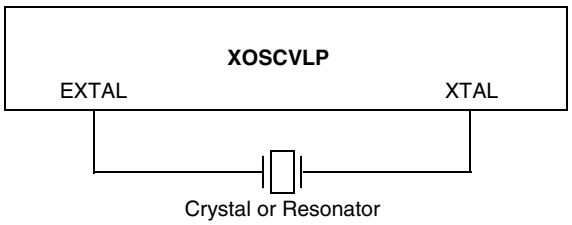


Figure 15. Typical Crystal or Resonator Circuit: Low Range/Low Power

3.9 Internal Clock Source (ICS) Characteristics

Table 12. ICS Frequency Specifications (Temperature Range = –40 to 85°C Ambient)

Num	C	Characteristic	Symbol	Min	Typ[1]	Max	Unit
1	P	Average internal reference frequency — factory trimmed at VDD = 3.6 V and temperature = 25 °C	f_{int_ft}	—	32.768	—	kHz
2	P	Average internal reference frequency - trimmed	f_{int_t}	31.25	—	39.063	kHz
3	T	Internal reference start-up time	t_{IRST}	—	—	6	µs
4	P	DCO output frequency range - untrimmed	f_{dco_ut}	12.8	16.8	21.33	MHz
5	P	DCO output frequency range - trimmed	f_{dco_t}	16	—	20	MHz
6	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM)	$\Delta f_{dco\_res\_t}$	—	± 0.1	± 0.2	$\%f_{dco}$
7	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)	$\Delta f_{dco\_res\_t}$	—	± 0.2	± 0.4	$\%f_{dco}$
8	C	Total deviation from trimmed DCO output frequency over voltage and temperature	Δf_{dco_t}	—	+ 0.5 -1.0	± 2	$\%f_{dco}$

Table 12. ICS Frequency Specifications (Temperature Range = –40 to 85°C Ambient) (continued)

Num	C	Characteristic	Symbol	Min	Typ[1]	Max	Unit
9	C	Total deviation from trimmed DCO output frequency over fixed voltage and temperature range of 0°C to 70 °C	Δf_{dco_t}	—	± 0.5	± 1	$\%f_{dco}$
10	C	FLL acquisition time [2]	$t_{Acquire}$	—	—	1	ms
11	C	Long term jitter of DCO output clock (averaged over 2-ms interval) [3]	C_{Jitter}	—	0.02	0.2	$\%f_{dco}$

1 Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

2 This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

3 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{Bus}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in the crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

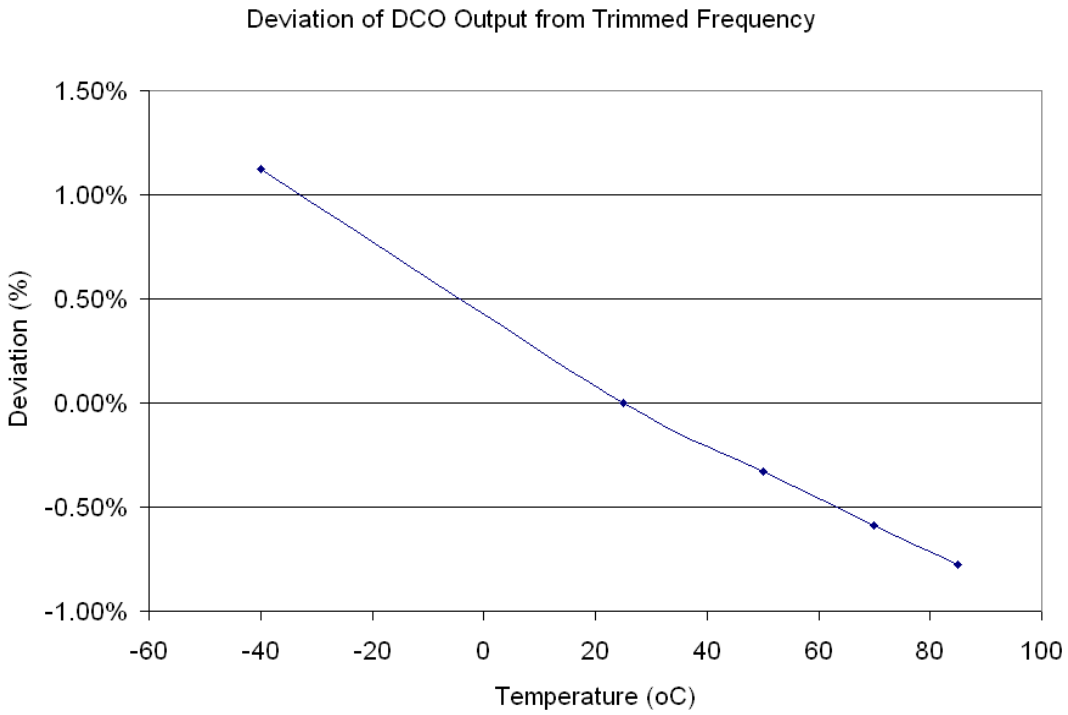


Figure 16. Deviation of DCO Output from Trimmed Frequency (20 MHz, 3.0 V)

3.10 AC Characteristics

This section describes timing characteristics for each peripheral system.

3.10.1 Control Timing

Table 13. Control Timing

Num	C	Rating	Symbol	Min	Typ[1]	Max	Unit
1	D	Bus frequency (t_{cyc} = 1/f_{Bus})	f_{Bus}	dc	—	20	MHz
2	D	Internal low power oscillator period	t_{LPO}	700	—	1300	μs
3	D	External reset pulse width[2]	t_{extrst}	100	—	—	ns
4	D	Reset low drive	t_{rstdrv}	34 x t_{cyc}	—	—	ns
5	D	BKGD/MS setup time after issuing background debug force reset to enter user or BDM modes	t_{MSSU}	500	—	—	ns
6	D	BKGD/MS hold time after issuing background debug force reset to enter user or BDM modes [3]	t_{MSH}	100	—	—	μs
7	D	IRQ pulse width Asynchronous path[2] Synchronous path[4]	t_{ILIH}, t_{IHIL}	 100 1.5 x t_{cyc}	 — —	 — —	ns
8	D	Keyboard interrupt pulse width Asynchronous path[2] Synchronous path[4]	t_{ILIH}, t_{IHIL}	 100 1.5 x t_{cyc}	 — —	 — —	ns
9	C	Port rise and fall time — Non-LCD Pins Low output drive (PTxDS = 0) (load = 50 pF)[5, 6] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	 — —	 16 23	 — —	ns
		Port rise and fall time — Non-LCD Pins High output drive (PTxDS = 1) (load = 50 pF)[5, 6] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	 — —	 5 9	 — —	ns
10	C	Voltage Regulator Recovery time	t_{VRR}	—	6	10	us

1 Typical values are based on characterization data at V_{DD} = 3.0 V, 25°C unless otherwise stated.

2 This is the shortest pulse that is guaranteed to be recognized as a reset pin request.

3 To enter BDM mode following a POR, BKGD/MS should be held low during the power-up and for a hold time of t_{MSH} after V_{DD} rises above V_{LVD}.

4 This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized.

5 Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40°C to 85°C.

6 Except for LCD pins in Open Drain mode.

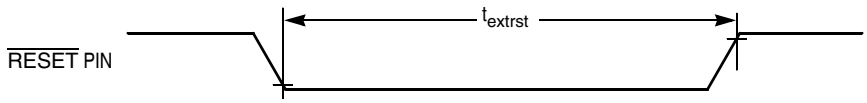
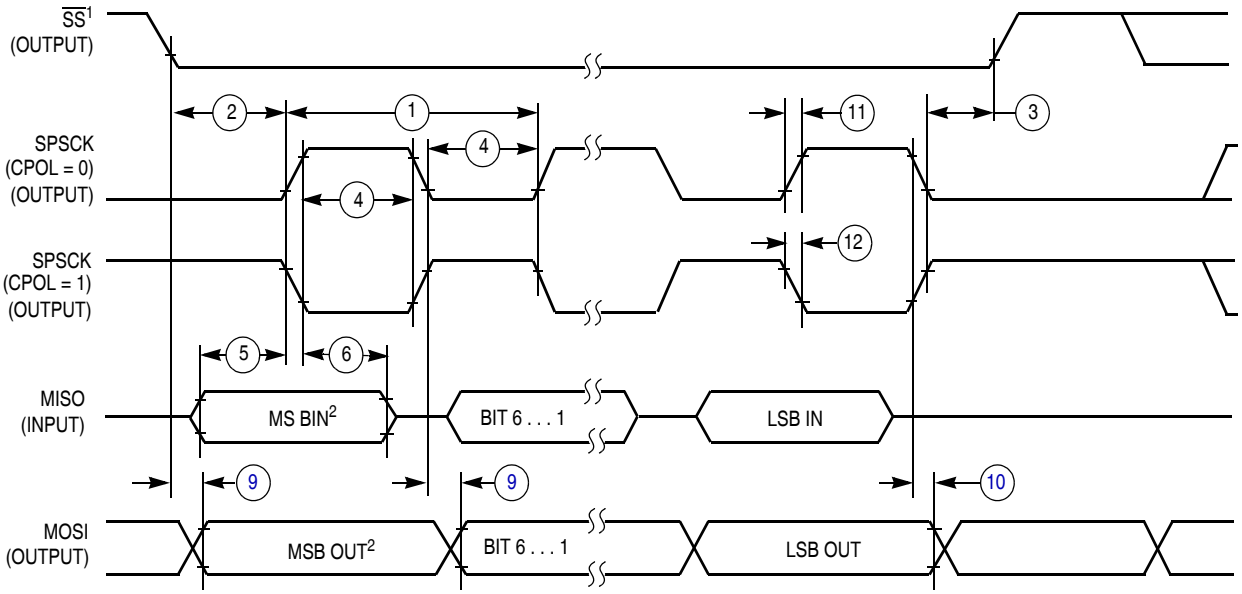


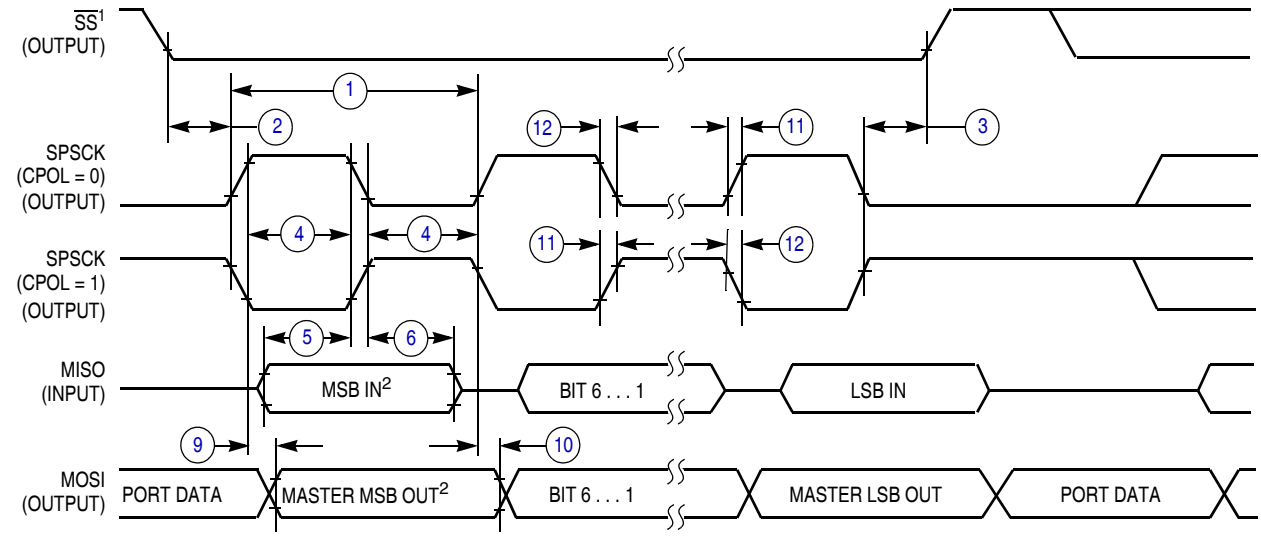
Figure 17. Reset Timing



NOTES:

1. SS output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 20. SPI Master Timing (CPHA = 0)



NOTES:

1. SS output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 21. SPI Master Timing (CPHA =1)

Table 17. 16-bit ADC Operating Conditions

Num	Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
5	Ref Voltage Low		V_{REFL}	V_{SSA}	V_{SSA}	V_{SSA}	V	
6	Input Voltage		V_{ADIN}	V_{REFL}	—	V_{REFH}	V	
7	Input Capacitance	16-bit modes 8/10/12-bit modes	C_{ADIN}	— —	8 4	10 5	pF	
8	Input Resistance		R_{ADIN}	—	2	5	kΩ	
9	Analog Source Resistance	16 bit modes f_{ADCK} > 8MHz 4MHz < f_{ADCK} < 8MHz f_{ADCK} < 4MHz	R_{AS}	— — —	— — —	0.5 1 2	kΩ	External to MCU Assumes ADLSMP=0
10		13/12 bit modes f_{ADCK} > 8MHz 4MHz < f_{ADCK} < 8MHz f_{ADCK} < 4MHz		— — —	— — —	1 2 5		
11		11/10 bit modes f_{ADCK} > 8MHz 4MHz < f_{ADCK} < 8MHz f_{ADCK} < 4MHz		— — —	— — —	2 5 10		
12		9/8 bit modes f_{ADCK} > 8MHz f_{ADCK} < 8MHz		— —	— —	5 10		
13	ADC Conversion Clock Freq.	ADLPC = 0, ADHSC = 1	f_{ADCK}	1.0	—	10	MHz	
14		ADLPC = 0, ADHSC = 0		1.0	—	5		
15		ADLPC = 1, ADHSC = 0		1.0	—	2.5		

1 Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 DC potential difference.

Table 19. 16-bit ADC Characteristics($V_{REFH} = V_{DDAD} \geq 2.7V$, $V_{REFL} = V_{SSAD}$, $F_{ADCK} \leq 4MHz$, ADHSC=1)

Characteristic	Conditions[1]	C	Symb	Min	Typ[2]	Max	Unit	Comment
Total Unadjusted Error	16-bit differential mode 16-bit single-ended mode	T	TUE	— —	±16 ±20	+24/-24 +32/-20	LSB[3]	32x Hardware Averaging (AVGE = %1 AVGS = %11)
	13-bit differential mode 12-bit single-ended mode	T		— —	±1.5 ±1.75	±2.0 ±2.5		
	11-bit differential mode 10-bit single-ended mode	T		— —	±0.7 ±0.8	±1.0 ±1.25		
	9-bit differential mode 8-bit single-ended mode	T		— —	±0.5 ±0.5	±1.0 ±1.0		
Differential Non-Linearity	16-bit differential mode 16-bit single-ended mode	T	DNL	— —	±2.5 ±2.5	±3 ±3	LSB[2]	
	13-bit differential mode 12-bit single-ended mode	T		— —	±0.7 ±0.7	±1 ±1		
	11-bit differential mode 10-bit single-ended mode	T		— —	±0.5 ±0.5	±0.75 ±0.75		
	9-bit differential mode 8-bit single-ended mode	T		— —	±0.2 ±0.2	±0.5 ±0.5		
Integral Non-Linearity	16-bit differential mode 16-bit single-ended mode	T	INL	— —	±6.0 ±10.0	±12.0 ±16.0	LSB[2]	
	13-bit differential mode 12-bit single-ended mode	T		— —	±1.0 ±1.0	±2.0 ±2.0		
	11-bit differential mode 10-bit single-ended mode	T		— —	±0.5 ±0.5	±1.0 ±1.0		
	9-bit differential mode 8-bit single-ended mode	T		— —	±0.3 ±0.3	±0.5 ±0.5		
Zero-Scale Error	16-bit differential mode 16-bit single-ended mode	T	E_{ZS}	— —	±4.0 ±4.0	+16/0 +16/-38	LSB[2]	$V_{ADIN} = V_{SSAD}$
	13-bit differential mode 12-bit single-ended mode	T		— —	±0.7 ±0.7	±2.0 ±2.0		
	11-bit differential mode 10-bit single-ended mode	T		— —	±0.4 ±0.4	±1.0 ±1.0		
	9-bit differential mode 8-bit single-ended mode	T		— —	±0.2 ±0.2	±0.5 ±0.5		

Table 19. 16-bit ADC Characteristics($V_{REFH} = V_{DDAD} \geq 2.7V$, $V_{REFL} = V_{SSAD}$, $F_{ADCK} \leq 4MHz$, ADHSC=1)

Characteristic	Conditions[1]	C	Symb	Min	Typ[2]	Max	Unit	Comment
Full-Scale Error	16-bit differential mode 16-bit single-ended mode	T	E_{FS}	— —	+8/0 +12/0	+24/0 +24/0	LSB[2]	$V_{ADIN} = V_{DDAD}$
	13-bit differential mode 12-bit single-ended mode	T		— —	±0.7 ±0.7	±2.0 ±2.5		
	11-bit differential mode 10-bit single-ended mode	T		— —	±0.4 ±0.4	±1.0 ±1.0		
	9-bit differential mode 8-bit single-ended mode	T		— —	±0.2 ±0.2	±0.5 ±0.5		
Quantization Error	16 bit modes	D	E_Q	—	-1 to 0	—	LSB[2]	
	≤13 bit modes			—	—	±0.5		
Effective Number of Bits	16 bit differential mode Avg = 32 Avg = 16 Avg = 8 Avg = 4 Avg = 1	C	ENOB	 — — — — —	 13.5 13.4 13.2 13 12.6	 — — — — —	Bits	For ADC_DIV=1, ADC_CLK=10 MHz.
	16 bit single-ended mode Avg = 32 Avg = 16 Avg = 8 Avg = 4 Avg = 1			 — — — — —	 12.39 12.34 12.13 11.94 11.4	 — — — — —		
Signal to Noise plus Distortion	See ENOB		SINAD	$SINAD = 6.02 \cdot ENOB + 1.76$			dB	
Total Harmonic Distortion	16–bit differential mode Avg = 32	C	THD	—	—	—	dB	
	16–bit single-ended mode Avg = 32	D		—	—	—		
Spurious Free Dynamic Range	16–bit differential mode Avg = 32	C	SFDR	 91.0	 96.5	 —	dB	
	16–bit single-ended mode Avg = 32	D		—	—	—		
Input Leakage Error	all modes	D	E_{IL}	$I_{In} * R_{AS}$			mV	I_{In} = leakage current (refer to DC characteristics)
Temp Sensor Slope	–40°C–25°C	D	m	—	1.646	—	mV/°C	
	25°C–125°C			—	1.769	—		
Temp Sensor Voltage	25°C	D	V_{TEMP25}	—	966	—	mV	

1 All accuracy numbers assume the ADC is calibrated with V_{REFH}=V_{DDAD}

2 Typical values assume V_{DDAD} = 3.0 V, Temp = 25 °C, f_{ADCK}=2.0MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

3 1 LSB = (V_{REFH}–V_{REFL})/2^N

3.13 VREF Characteristics

Table 20. Electrical specifications

Num	C	Characteristic	Symbol	Min	Max	Unit
1	P	Supply voltage	V_{DD}	1.80	3.60	V
2	P	Operating temperature range	T_{op}	–40	85	C
3	C	Maximum Load			10	mA
		Operation across Temperature				
4	P	Voltage output room temperature	Untrimmed	1.070–1.3		V
5	P	Voltage output room temperature	Factory trimmed[1]	1.180–1.22		V
6	C	–40 °C	Factory trimmed	1.19–1.200		V
7	C	85 °C	Factory trimmed	1.185–1.200		V
		Load Bandwidth				
8	C	Load Regulation Mode = 10 at 1mA load	Mode = 10	20	100	μV/mA
9	C	Line Regulation (Power Supply Rejection)	DC	±0.1 from room temp voltage		mV
			AC	–60		dB
		Power Consumption				
10	C	Powered down Current (Stop Mode, VREFEN = 0, VRSTEN = 0)	I		100	μA
11	C	Bandgap only (Mode[1:0] 00)	I		75	μA
12	C	Low Power buffer (Mode[1:0] 01)	I		125	μA
13	C	Tight Regulation buffer (Mode[1:0] 10)	I		1.1	mA
14	C	Low Power and Tight Regulation (Mode[1:0] 11)	I		1.15	mA

1 Factory trim is performed at the room temperature.

[2] These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

[3] The program and erase currents are additional to the standard run I_{DD}. These values are measured at room temperatures with V_{DD} = 3.0 V, bus frequency = 4.0 MHz.

[4] Typical endurance for FLASH was evaluated for this product family on the 9S12Dx64. For additional information on how Freescale defines typical endurance, please refer to Engineering Bulletin EB619, *Typical Endurance for Nonvolatile Memory*.

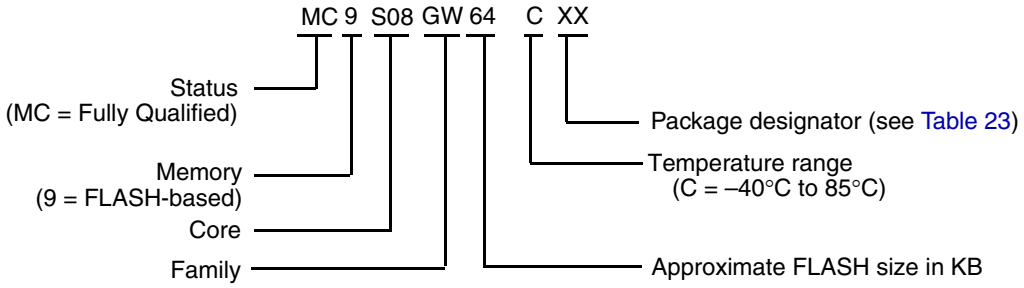
[5] Typical data retention values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale defines typical data retention, please refer to Engineering Bulletin EB618, *Typical Data Retention for Nonvolatile Memory.*

4 Ordering Information

This section contains the ordering information and the device numbering system for the MC9S08GW64 Series.

4.1 Device Numbering System

Example of the device numbering system:



5 Package Information and Mechanical Drawings

Table 23 provides the available package types and their document numbers. The latest package outline/mechanical drawings are available on the MC9S08GW64 Series Product Summary pages at http://www.freescale.com.

To view the latest drawing, either:

- Click on the appropriate link in Table 23, or
- Open a browser to the Freescale® website (http://www.freescale.com), and enter the appropriate document number (from Table 23) in the "Enter Keyword" search box at the top of the page.

Table 23. Package Descriptions

Pin Count	Package Type	Abbreviation	Designator	Case No.	Document No.
80	Low Quad Flat Package	LQFP	LK	917A	98ASS23237W
64	Low Quad Flat Package	LQFP	LH	840F	98ASS23234W

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