



Welcome to [E-XFL.COM](#)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Discontinued at Digi-Key
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	I ² C, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	39
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f563t4edfm-v0

Table 1.2 Comparison of Functions for Different Packages

Functions			RX63T Group						
Package			144 Pins	120 Pins	112 Pins	100 Pins	64 Pins	48 Pins	
External bus			16 bits				—		
External address space			1 Mbyte × 4 areas				—		
DMA	DMA controller (DMACA)		Ch. 0 to 3						
	Data transfer controller (DTCa)		Supported						
Interrupt controller (ICUb)	NMI pin		Supported						
	IRQ pin		Supported (x 8)				Supported (x 6)		
Timers	Multi-function timer pulse unit 3 (MTU3)* ¹		Ch. 0 to 7						
	General PWM timer (GPT)* ¹	Generation of delays in PWM, not supported	Ch. 0 to 7				Ch. 0 to 3		
		Generation of delays in PWM, supported	Ch. 0 to 3				—		
	Port output enable 3 (POE3)		Supported (POE pins × 6)			Supported (POE pins × 5)	Supported (POE pins × 4)		
	Compare match timer (CMT)		Ch. 0 to 3						
	Watchdog timer (WDTA)		Supported						
	Independent watchdog timer (IWDTa)		Supported						
	Communication function	USB2.0 host/function module (USBa)		Ch. 0		—			
Serial communications interfaces (SClC)		Ch. 0 to 3			Ch. 0 to 2	Ch. 0, 1			
Serial communications interfaces (SCId)		Ch. 12							
I ² C bus interfaces (RIIC)		Ch. 0, 1		Ch. 0					
Serial peripheral interfaces (RSPI)		Ch. 0, 1				Ch. 0			
CAN module (CAN) (as an optional function)* ¹		Ch. 0				—			
12-bit A/D converter (S12ADB)			4 channels × 2 units				8 channels × 1 unit (AN000 to 007)	8 channels × 1 unit (AN000 to 004, 007)	
			Three-channel simultaneous sampling function		2 units			1 unit	
			Programmable gain amplifier		3 channels × 2 units			—	
			Window comparator		3 channels × 2 units			3 channels × 1 unit	
10-bit A/D converter (ADA)			20 channels	12 channels			—		
D/A converter (DAa)			Ch. 0, 1				—		
Clock Frequency Accuracy Measurement Circuit			Supported						
Digital power supply controller (DPC)* ²			Supported				Not supported		

Note 1. For the MTU3 and GPT, the number of pins will differ with the package. See the list of pins and pin functions for details.

In addition, the CAN module is an optional function. For details, see Table 1.3.

Note 2. Not provided for the product ID code O.

Table 1.4 Pin Functions (5/5)

Classifications	Pin Name	I/O	Description
I/O ports	P00 to P05	I/O	6-bit input/output pins
	P10 to P14	I/O	5-bit input/output pins
	P20 to P26	I/O	7-bit input/output pins
	P30 to P35	I/O	6-bit input/output pins
	P40 to P47	Input	8-bit input pins
	P50 to P57	Input	8-bit input pins
	P60 to P65	Input	6-bit input pins
	P70 to P76	I/O	7-bit input/output pins
	P80 to P82	I/O	3-bit input/output pins
	P90 to P96	I/O	7-bit input/output pins
	PA0 to PA6	I/O	7-bit input/output pins
	PB0 to PB7	I/O	8-bit input/output pins
	PC0 to PC5	Input	6-bit input pins
	PD0 to PD7	I/O	8-bit input/output pins
	PE0, PE1, PE3 to PE5	I/O	6-bit input/output pins
	PE2	Input	1-bit input pin
	PF0 to PF4	I/O	5-bit input/output pins
	PG0 to PG6	I/O	7-bit input/output pins

Table 1.5 List of Pins and Pin Functions (144-Pin LQFP) (4/4)

Pin Number 144-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3, GPT, POE3, CAC)	Communications (SCIc, SCId, RSPI, RIIC, CAN, USB)	Interrupt	S12ADB, AD, DA
110		P60	A5				AN0
111		P57					AN13
112		P56					AN12
113		P55					AN11/DA1
114		P54					AN10/ DA0
115		P53	A6				AN9
116		P52	A7				AN8
117		P51					AN7
118		P50					AN6
119		P47					AN103/ CVREFH
120		P46					AN102
121		P45					AN101
122		P44					AN100
123		P43					AN003/ CVREFL
124		P42					AN002
125		P41					AN001
126		P40					AN000
127	AVCC0						
128	VREFH0						
129	VREFL0						
130	AVSS0						
131		P82	WAIT#	MTIC5U	SCK12	IRQ3	
132		P81	A8	MTIC5V	TXD12/SMOSI12/ SSDA12/TXD12/ SIOX12		
133	VSS						
134		P80	A9	MTIC5W	RXD12/SMISO12/ SSCL12/RXD12	IRQ5	
135		P12	CS3#		USB0_DPRPD		
136		P11	ALE	MTCLKC		IRQ1-DS	
137		P10		MTCLKD		IRQ0-DS	
138		P05	CS2#/WAIT#				
139	VCC						
140		P04					
141					USB0_DPUPE		
142	VSS_USB						
143					USB0_DM		
144					USB0_DP		

Note 1. Available for use as SCI pin only in boot mode.

Table 1.10 List of Pins and Pin Functions (48-Pin LQFP) (1/2)

Pin Number 64-Pin LQFP	Power Supply Clock System Control	I/O Port	POE3	Timer (MTU3, GPT, CAC)	Communications		Interrupt	S12ADB
					(SC1c, SC1d)	(RSPI, RIIC)		
1	MD FINED							
2	RES#							
3	XTAL							
4	VSS							
5	EXTAL							
6	VCC							
7		PE2	POE10#				NMI	
8	TRST#	PD7		GTIOC0A	CTS0# RTS0# SS0#			
9	TMS	PD6		GTIOC0B				
10	TDI	PD5		GTIOC1A	RXD1 SMISO1 SSCL1			
11	TCK FINEC	PD4		GTIOC1B	SCK1			
12	TDO	PD3		GTIOC2A	TXD1 SMOSI1 SSDA1			
13		PB6		GTIOC2B	RXD12 SMISO12 SSCL12 RXDX12			
14		PB5	POE11#		TXD12 SMOSI12 SSDA12 TXDX12 SIOX12		IRQ0	
15	VCC							
16		PB4	POE8#	GTETRQ	CTS12# RTS12# SS12#		IRQ3-DS	
17	VSS							
18		PB3		MTIOC0A MTCLKA CACREF	SCK0			
19		PB2		MTIOC0B MTCLKB	TXD0 SMOSI0 SSDA0	SDA		
20		PB1		MTIOC0C	RXD0 SMISO0 SSCL0	SCL		
21		PB0		MTIOC0D		MOSIA		
22		PA3		MTIOC2A		SSLA0		
23		PA2		MTIOC2B		SSLA1		
24		P76		MTIOC4D GTIOC2B MTIOC7D				
25		P75		MTIOC4C GTIOC1B MTIOC7C				

Table 4.1 List of I/O Registers (Address Order) (6/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK $\geq$ PCLK	ICLK $<$ PCLK		
0008 7098h	ICU	Interrupt Request Register 152	IR152	8	8	2 ICLK		ICUb	
0008 7099h	ICU	Interrupt Request Register 153	IR153	8	8	2 ICLK			
0008 709Ah	ICU	Interrupt Request Register 154	IR154	8	8	2 ICLK			
0008 709Bh	ICU	Interrupt Request Register 155	IR155	8	8	2 ICLK			
0008 709Ch	ICU	Interrupt Request Register 156	IR156	8	8	2 ICLK			
0008 709Dh	ICU	Interrupt Request Register 157	IR157	8	8	2 ICLK			
0008 709Eh	ICU	Interrupt Request Register 158	IR158	8	8	2 ICLK			
0008 70A1h	ICU	Interrupt Request Register 161	IR161	8	8	2 ICLK			
0008 70A2h	ICU	Interrupt Request Register 162	IR162	8	8	2 ICLK			
0008 70A3h	ICU	Interrupt Request Register 163	IR163	8	8	2 ICLK			
0008 70A4h	ICU	Interrupt Request Register 164	IR164	8	8	2 ICLK			
0008 70A5h	ICU	Interrupt Request Register 165	IR165	8	8	2 ICLK			
0008 70A6h	ICU	Interrupt Request Register 166	IR166	8	8	2 ICLK			
0008 70A7h	ICU	Interrupt Request Register 167	IR167	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70A8h	ICU	Interrupt Request Register 168	IR168	8	8	2 ICLK			
0008 70A9h	ICU	Interrupt Request Register 169	IR169	8	8	2 ICLK			
0008 70AAh	ICU	Interrupt Request Register 170	IR170	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70ABh	ICU	Interrupt Request Register 171	IR171	8	8	2 ICLK			
0008 70ACh	ICU	Interrupt Request Register 172	IR172	8	8	2 ICLK			
0008 70ADh	ICU	Interrupt Request Register 173	IR173	8	8	2 ICLK			
0008 70AEh	ICU	Interrupt Request Register 174	IR174	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70AFh	ICU	Interrupt Request Register 175	IR175	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70B0h	ICU	Interrupt Request Register 176	IR176	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70B1h	ICU	Interrupt Request Register 177	IR177	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70B2h	ICU	Interrupt Request Register 178	IR178	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70B3h	ICU	Interrupt Request Register 179	IR179	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70B4h	ICU	Interrupt Request Register 180	IR180	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70B5h	ICU	Interrupt Request Register 181	IR181	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70B6h	ICU	Interrupt Request Register 182	IR182	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70B7h	ICU	Interrupt Request Register 183	IR183	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70B8h	ICU	Interrupt Request Register 184	IR184	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70B9h	ICU	Interrupt Request Register 185	IR185	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70BAh	ICU	Interrupt Request Register 186	IR186	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70BBh	ICU	Interrupt Request Register 187	IR187	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70BCh	ICU	Interrupt Request Register 188	IR188	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70BDh	ICU	Interrupt Request Register 189	IR189	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70BEh	ICU	Interrupt Request Register 190	IR190	8	8	2 ICLK			Not present in versions with 112, 100, 64 or 48 pins.
0008 70BFh	ICU	Interrupt Request Register 191	IR191	8	8	2 ICLK			Not present in versions with 112, 100, 64 or 48 pins.

Table 4.1 List of I/O Registers (Address Order) (13/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK $\geq$ PCLK	ICLK $<$ PCLK		
0008 739Ah	ICU	Interrupt Source Priority Register 154	IPR154	8	8	2 ICLK		ICUB	
0008 739Eh	ICU	Interrupt Source Priority Register 158	IPR158	8	8	2 ICLK			
0008 73A1h	ICU	Interrupt Source Priority Register 161	IPR161	8	8	2 ICLK			
0008 73A3h	ICU	Interrupt Source Priority Register 163	IPR163	8	8	2 ICLK			
0008 73A5h	ICU	Interrupt Source Priority Register 165	IPR165	8	8	2 ICLK			
0008 73A6h	ICU	Interrupt Source Priority Register 166	IPR166	8	8	2 ICLK			
0008 73ABh	ICU	Interrupt Source Priority Register 171	IPR171	8	8	2 ICLK			
0008 73ACh	ICU	Interrupt Source Priority Register 172	IPR172	8	8	2 ICLK			
0008 73ADh	ICU	Interrupt Source Priority Register 173	IPR173	8	8	2 ICLK			
0008 73AEh	ICU	Interrupt Source Priority Register 174	IPR174	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 73B1h	ICU	Interrupt Source Priority Register 177	IPR177	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 73B4h	ICU	Interrupt Source Priority Register 180	IPR180	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 73B7h	ICU	Interrupt Source Priority Register 183	IPR183	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 73B9h	ICU	Interrupt Source Priority Register 185	IPR185	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 73BCh	ICU	Interrupt Source Priority Register 188	IPR188	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 73BEh	ICU	Interrupt Source Priority Register 190	IPR190	8	8	2 ICLK			Not present in versions with 112, 100, 64 or 48 pins.
0008 73C2h	ICU	Interrupt Source Priority Register 194	IPR194	8	8	2 ICLK			
0008 73C6h	ICU	Interrupt Source Priority Register 198	IPR198	8	8	2 ICLK			
0008 73C7h	ICU	Interrupt Source Priority Register 199	IPR199	8	8	2 ICLK			
0008 73C8h	ICU	Interrupt Source Priority Register 200	IPR200	8	8	2 ICLK			
0008 73C9h	ICU	Interrupt Source Priority Register 201	IPR201	8	8	2 ICLK			
0008 73D6h	ICU	Interrupt Source Priority Register 214	IPR214	8	8	2 ICLK			
0008 73D9h	ICU	Interrupt Source Priority Register 217	IPR217	8	8	2 ICLK			
0008 73DCh	ICU	Interrupt Source Priority Register 220	IPR220	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 73DFh	ICU	Interrupt Source Priority Register 223	IPR223	8	8	2 ICLK			Not present in versions with 100, 64 or 48 pins.
0008 73E2h	ICU	Interrupt Source Priority Register 226	IPR226	8	8	2 ICLK			
0008 73E5h	ICU	Interrupt Source Priority Register 229	IPR229	8	8	2 ICLK			
0008 73E8h	ICU	Interrupt Source Priority Register 232	IPR232	8	8	2 ICLK			
0008 73EBh	ICU	Interrupt Source Priority Register 235	IPR235	8	8	2 ICLK			
0008 73EEh	ICU	Interrupt Source Priority Register 238	IPR238	8	8	2 ICLK			
0008 73F1h	ICU	Interrupt Source Priority Register 241	IPR241	8	8	2 ICLK			
0008 73F4h	ICU	Interrupt Source Priority Register 244	IPR244	8	8	2 ICLK			
0008 73F7h	ICU	Interrupt Source Priority Register 247	IPR247	8	8	2 ICLK			
0008 73FAh	ICU	Interrupt Source Priority Register 250	IPR250	8	8	2 ICLK			
0008 7400h	ICU	DMAC Activation Request Select Register 0	DMRSR0	8	8	2 ICLK			
0008 7404h	ICU	DMAC Activation Request Select Register 1	DMRSR1	8	8	2 ICLK			
0008 7408h	ICU	DMAC Activation Request Select Register 2	DMRSR2	8	8	2 ICLK			
0008 740Ch	ICU	DMAC Activation Request Select Register 3	DMRSR3	8	8	2 ICLK			
0008 7500h	ICU	IRQ Control Register 0	IRQCR0	8	8	2 ICLK			
0008 7501h	ICU	IRQ Control Register 1	IRQCR1	8	8	2 ICLK			
0008 7502h	ICU	IRQ Control Register 2	IRQCR2	8	8	2 ICLK			
0008 7503h	ICU	IRQ Control Register 3	IRQCR3	8	8	2 ICLK			
0008 7504h	ICU	IRQ Control Register 4	IRQCR4	8	8	2 ICLK			
0008 7505h	ICU	IRQ Control Register 5	IRQCR5	8	8	2 ICLK			
0008 7506h	ICU	IRQ Control Register 6	IRQCR6	8	8	2 ICLK			Not present in versions with 64 or 48 pins.

Table 4.1 List of I/O Registers (Address Order) (20/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 9873h	AD	A/D Sampling State Register 1	ADSSTR1	8	8	2, 3 PCLKB	2 ICLK	AD	Not present in versions with 64 or 48 pins.
0008 9874h	AD	A/D Sampling State Register 2	ADSSTR2	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9875h	AD	A/D Sampling State Register 3	ADSSTR3	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9876h	AD	A/D Sampling State Register 4	ADSSTR4	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9877h	AD	A/D Sampling State Register 5	ADSSTR5	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9878h	AD	A/D Sampling State Register 6	ADSSTR6	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9879h	AD	A/D Sampling State Register 7	ADSSTR7	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 987Dh	AD	Digital Power Supply Control Circuit Output Register	ADDPCONR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64, or 48 pins.
0008 A000h	SCI0	Serial Mode Register	SMR	8	8	2, 3 PCLKB	2 ICLK	SCIc, SCId	
0008 A001h	SCI0	Bit Rate Register	BRR	8	8	2, 3 PCLKB	2 ICLK		
0008 A002h	SCI0	Serial Control Register	SCR	8	8	2, 3 PCLKB	2 ICLK		
0008 A003h	SCI0	Transmit Data Register	TDR	8	8	2, 3 PCLKB	2 ICLK		
0008 A004h	SCI0	Serial Status Register	SSR	8	8	2, 3 PCLKB	2 ICLK		
0008 A005h	SCI0	Receive Data Register	RDR	8	8	2, 3 PCLKB	2 ICLK		
0008 A006h	SCI0	Smart Card Mode Register	SCMR	8	8	2, 3 PCLKB	2 ICLK		
0008 A007h	SCI0	Serial Extended Mode Register	SEMR	8	8	2, 3 PCLKB	2 ICLK		
0008 A008h	SCI0	Noise Filter Setting Register	SNFR	8	8	2, 3 PCLKB	2 ICLK		
0008 A009h	SCI0	I ² C Mode Register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK		
0008 A00Ah	SCI0	I ² C Mode Register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK		
0008 A00Bh	SCI0	I ² C Mode Register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK		
0008 A00Ch	SCI0	I ² C Status Register	SISR	8	8	2, 3 PCLKB	2 ICLK		
0008 A00Dh	SCI0	SPI Mode Register	SPMR	8	8	2, 3 PCLKB	2 ICLK		
0008 A020h	SCI1	Serial Mode Register	SMR	8	8	2, 3 PCLKB	2 ICLK		
0008 A021h	SCI1	Bit Rate Register	BRR	8	8	2, 3 PCLKB	2 ICLK		
0008 A022h	SCI1	Serial Control Register	SCR	8	8	2, 3 PCLKB	2 ICLK		
0008 A023h	SCI1	Transmit Data Register	TDR	8	8	2, 3 PCLKB	2 ICLK		
0008 A024h	SCI1	Serial Status Register	SSR	8	8	2, 3 PCLKB	2 ICLK		
0008 A025h	SCI1	Receive Data Register	RDR	8	8	2, 3 PCLKB	2 ICLK		
0008 A026h	SCI1	Smart Card Mode Register	SCMR	8	8	2, 3 PCLKB	2 ICLK		
0008 A027h	SCI1	Serial Extended Mode Register	SEMR	8	8	2, 3 PCLKB	2 ICLK		
0008 A028h	SCI1	Noise Filter Setting Register	SNFR	8	8	2, 3 PCLKB	2 ICLK		
0008 A029h	SCI1	I ² C Mode Register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK		
0008 A02Ah	SCI1	I ² C Mode Register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK		
0008 A02Bh	SCI1	I ² C Mode Register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK		
0008 A02Ch	SCI1	I ² C Status Register	SISR	8	8	2, 3 PCLKB	2 ICLK		
0008 A02Dh	SCI1	SPI Mode Register	SPMR	8	8	2, 3 PCLKB	2 ICLK		
0008 A040h	SCI2	Serial Mode Register	SMR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 A041h	SCI2	Bit Rate Register	BRR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 A042h	SCI2	Serial Control Register	SCR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 A043h	SCI2	Transmit Data Register	TDR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 A044h	SCI2	Serial Status Register	SSR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 A045h	SCI2	Receive Data Register	RDR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 A046h	SCI2	Smart Card Mode Register	SCMR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.

Table 4.1 List of I/O Registers (Address Order) (24/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 C086h	PORT3	Open Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK	I/O Ports	Not present in versions with 144, 120, 112, or 100 pins.
0008 C087h	PORT3	Open Drain Control Register 1	ODR1	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64 or 48 pins.
0008 C090h	PORT8	Open Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C092h	PORT9	Open Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 144, 120, 112, 100 or 48 pins.
0008 C093h	PORT9	Open Drain Control Register 1	ODR1	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 48 pins.
0008 C094h	PORTA	Open Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C095h	PORTA	Open Drain Control Register 1	ODR1	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C096h	PORTB	Open Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK		
0008 C097h	PORTB	Open Drain Control Register 1	ODR1	8	8	2, 3 PCLKB	2 ICLK		
0008 C09Ah	PORTD	Open Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK		
0008 C09Bh	PORTD	Open Drain Control Register 1	ODR1	8	8	2, 3 PCLKB	2 ICLK		
0008 C09Eh	PORTF	Open Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 100, 64, or 48 pins.
0008 C0A0h	PORTG	Open Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 100, 64, or 48 pins.
0008 C0A1h	PORTG	Open Drain Control Register 1	ODR1	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 100, 64, or 48 pins.
0008 C0F2h	PORT	Driving Ability Control Register 1	DSCR1	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C0F3h	PORT	Driving Ability Control Register 2	DSCR2	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C100h	MPC	CS Output Enable Register	PFCSE	8	8	2, 3 PCLKB	2 ICLK	MPC	Not present in versions with 64 or 48 pins.
0008 C102h	MPC	CS Output Pin Select Register 0	PFCSS0	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C104h	MPC	Address Output Enable Register 0	PFAOE0	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C105h	MPC	Address Output Enable Register 1	PFAOE1	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C106h	MPC	External Bus Control Register 0	PFBCR0	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C107h	MPC	External Bus Control Register 1	PFBCR1	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C114h	MPC	USB0 Control Register	PFUSB0	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
0008 C11Fh	MPC	Write-Protect Register	PWPR	8	8	2, 3 PCLKB	2 ICLK		
0008 C140h	MPC	P00 Pin Function Control Register	P00PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 48 pins.
0008 C141h	MPC	P01 Pin Function Control Register	P01PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 48 pins.
0008 C142h	MPC	P02 Pin Function Control Register	P02PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 C143h	MPC	P03 Pin Function Control Register	P03PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 C148h	MPC	P10 Pin Function Control Register	P10PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 48 pins.
0008 C149h	MPC	P11 Pin Function Control Register	P11PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 48 pins.
0008 C14Ah	MPC	P12 Pin Function Control Register	P12PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 100, 64, or 48 pins.
0008 C14Bh	MPC	P13 Pin Function Control Register	P13PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 112, 100, 64, or 48 pins.

Table 4.1 List of I/O Registers (Address Order) (26/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 C174h	MPC	P64 Pin Function Control Register	P64PFS	8	8	2, 3 PCLKB	2 ICLK	MPC	Not present in versions with 64 or 48 pins.
0008 C175h	MPC	P65 Pin Function Control Register	P65PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C178h	MPC	P70 Pin Function Control Register	P70PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C179h	MPC	P71 Pin Function Control Register	P71PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C17Ah	MPC	P72 Pin Function Control Register	P72PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C17Bh	MPC	P73 Pin Function Control Register	P73PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C17Ch	MPC	P74 Pin Function Control Register	P74PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C17Dh	MPC	P75 Pin Function Control Register	P75PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C17Eh	MPC	P76 Pin Function Control Register	P76PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C180h	MPC	P80 Pin Function Control Register	P80PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C181h	MPC	P81 Pin Function Control Register	P81PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C182h	MPC	P82 Pin Function Control Register	P82PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C188h	MPC	P90 Pin Function Control Register	P90PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C189h	MPC	P91 Pin Function Control Register	P91PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 48 pins.
0008 C18Ah	MPC	P92 Pin Function Control Register	P92PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 48 pins.
0008 C18Bh	MPC	P93 Pin Function Control Register	P93PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 48 pins.
0008 C18Ch	MPC	P94 Pin Function Control Register	P94PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 48 pins.
0008 C18Dh	MPC	P95 Pin Function Control Register	P95PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C18Eh	MPC	P96 Pin Function Control Register	P96PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C190h	MPC	PA0 Pin Function Control Register	PA0PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C191h	MPC	PA1 Pin Function Control Register	PA1PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C192h	MPC	PA2 Pin Function Control Register	PA2PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C193h	MPC	PA3 Pin Function Control Register	PA3PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C194h	MPC	PA4 Pin Function Control Register	PA4PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 48 pins.
0008 C195h	MPC	PA5 Pin Function Control Register	PA5PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 48 pins.
0008 C196h	MPC	PA6 Pin Function Control Register	PA6PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64 or 48 pins.
0008 C198h	MPC	PB0 Pin Function Control Register	PB0PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C199h	MPC	PB1 Pin Function Control Register	PB1PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C19Ah	MPC	PB2 Pin Function Control Register	PB2PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C19Bh	MPC	PB3 Pin Function Control Register	PB3PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C19Ch	MPC	PB4 Pin Function Control Register	PB4PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C19Dh	MPC	PB5 Pin Function Control Register	PB5PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C19Eh	MPC	PB6 Pin Function Control Register	PB6PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C19Fh	MPC	PB7 Pin Function Control Register	PB7PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 48 pins.
0008 C1A0h	MPC	PC0 Pin Function Control Register	PC0PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 C1A1h	MPC	PC1 Pin Function Control Register	PC1PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 C1A2h	MPC	PC2 Pin Function Control Register	PC2PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64, or 48 pins.

Table 4.1 List of I/O Registers (Address Order) (33/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK $\geq$ PCLK	ICLK $<$ PCLK		
000A 0092h	USB0	PIPE1 Transaction Counter Register	PIPE1TRN	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than $1 + 9 / (\text{frequency ratio of ICLK} / \text{PCLKB})^{*1}$	USBa	Not present in versions with 112, 100, 64, or 48 pins.
000A 0094h	USB0	PIPE2 Transaction Counter Enable Register	PIPE2TRE	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than $1 + 9 / (\text{frequency ratio of ICLK} / \text{PCLKB})^{*1}$		Not present in versions with 112, 100, 64, or 48 pins.
000A 0096h	USB0	PIPE2 Transaction Counter Register	PIPE2TRN	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than $1 + 9 / (\text{frequency ratio of ICLK} / \text{PCLKB})^{*1}$		Not present in versions with 112, 100, 64, or 48 pins.
000A 0098h	USB0	PIPE3 Transaction Counter Enable Register	PIPE3TRE	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than $1 + 9 / (\text{frequency ratio of ICLK} / \text{PCLKB})^{*1}$		Not present in versions with 112, 100, 64, or 48 pins.
000A 009Ah	USB0	PIPE3 Transaction Counter Register	PIPE3TRN	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than $1 + 9 / (\text{frequency ratio of ICLK} / \text{PCLKB})^{*1}$		Not present in versions with 112, 100, 64, or 48 pins.
000A 009Ch	USB0	PIPE4 Transaction Counter Enable Register	PIPE4TRE	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than $1 + 9 / (\text{frequency ratio of ICLK} / \text{PCLKB})^{*1}$		Not present in versions with 112, 100, 64, or 48 pins.
000A 009Eh	USB0	PIPE4 Transaction Counter Register	PIPE4TRN	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than $1 + 9 / (\text{frequency ratio of ICLK} / \text{PCLKB})^{*1}$		Not present in versions with 112, 100, 64, or 48 pins.
000A 00A0h	USB0	PIPE5 Transaction Counter Enable Register	PIPE5TRE	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than $1 + 9 / (\text{frequency ratio of ICLK} / \text{PCLKB})^{*1}$		Not present in versions with 112, 100, 64, or 48 pins.
000A 00A2h	USB0	PIPE5 Transaction Counter Register	PIPE5TRN	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than $1 + 9 / (\text{frequency ratio of ICLK} / \text{PCLKB})^{*1}$		Not present in versions with 112, 100, 64, or 48 pins.
000C 1200h	MTU3	Timer Control Register	TCR	8	8, 16, 32	4, 5 PCLKA	2, 3 ICLK	MTU3	
000C 1201h	MTU4	Timer Control Register	TCR	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1202h	MTU3	Timer Mode Register 1	TMDR1	8	8, 16	4, 5 PCLKA	2, 3 ICLK		
000C 1203h	MTU4	Timer Mode Register 1	TMDR1	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1204h	MTU3	Timer I/O Control Register H	TIORH	8	8, 16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1205h	MTU3	Timer I/O Control Register L	TIORL	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1206h	MTU4	Timer I/O Control Register H	TIORH	8	8, 16	4, 5 PCLKA	2, 3 ICLK		
000C 1207h	MTU4	Timer I/O Control Register L	TIORL	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1208h	MTU3	Timer Interrupt Enable Register	TIER	8	8, 16	4, 5 PCLKA	2, 3 ICLK		
000C 1209h	MTU4	Timer Interrupt Enable Register	TIER	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 120Ah	MTU	Timer Output Master Enable Register A	TOERA	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 120Dh	MTU	Timer Gate Control Register A	TGCRA	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 120Eh	MTU	Timer Output Control Register 1A	TOCR1A	8	8, 16	4, 5 PCLKA	2, 3 ICLK		

5.3.4 Control Signal Timing

Table 5.11 Control Signal Timing

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
NMI pulse width	t_{NMIW}	200	—	—	ns	$t_c(PCLK) \times 2 \leq 200$ ns, Figure 5.11
		$t_c(PCLK) \times 2$	—	—	ns	$t_c(PCLK) > 200$ ns, Figure 5.11
IRQ pulse width	t_{IRQW}	200	—	—	ns	$t_c(PCLK) \leq 200$ ns, Figure 5.12
		$t_c(PCLK) \times 2$	—	—	ns	$t_c(PCLK) > 200$ ns, Figure 5.12

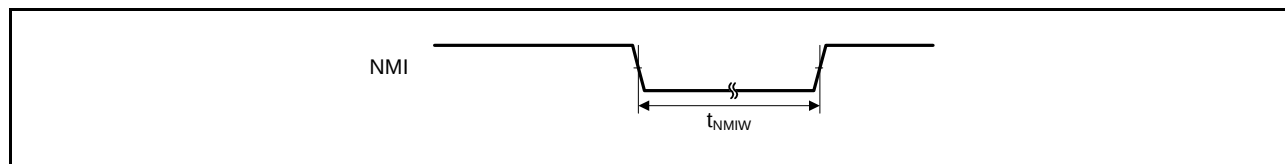


Figure 5.11 NMI Interrupt Input Timing

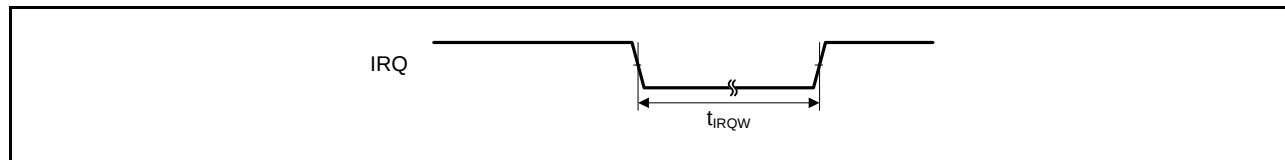


Figure 5.12 IRQ Interrupt Input Timing

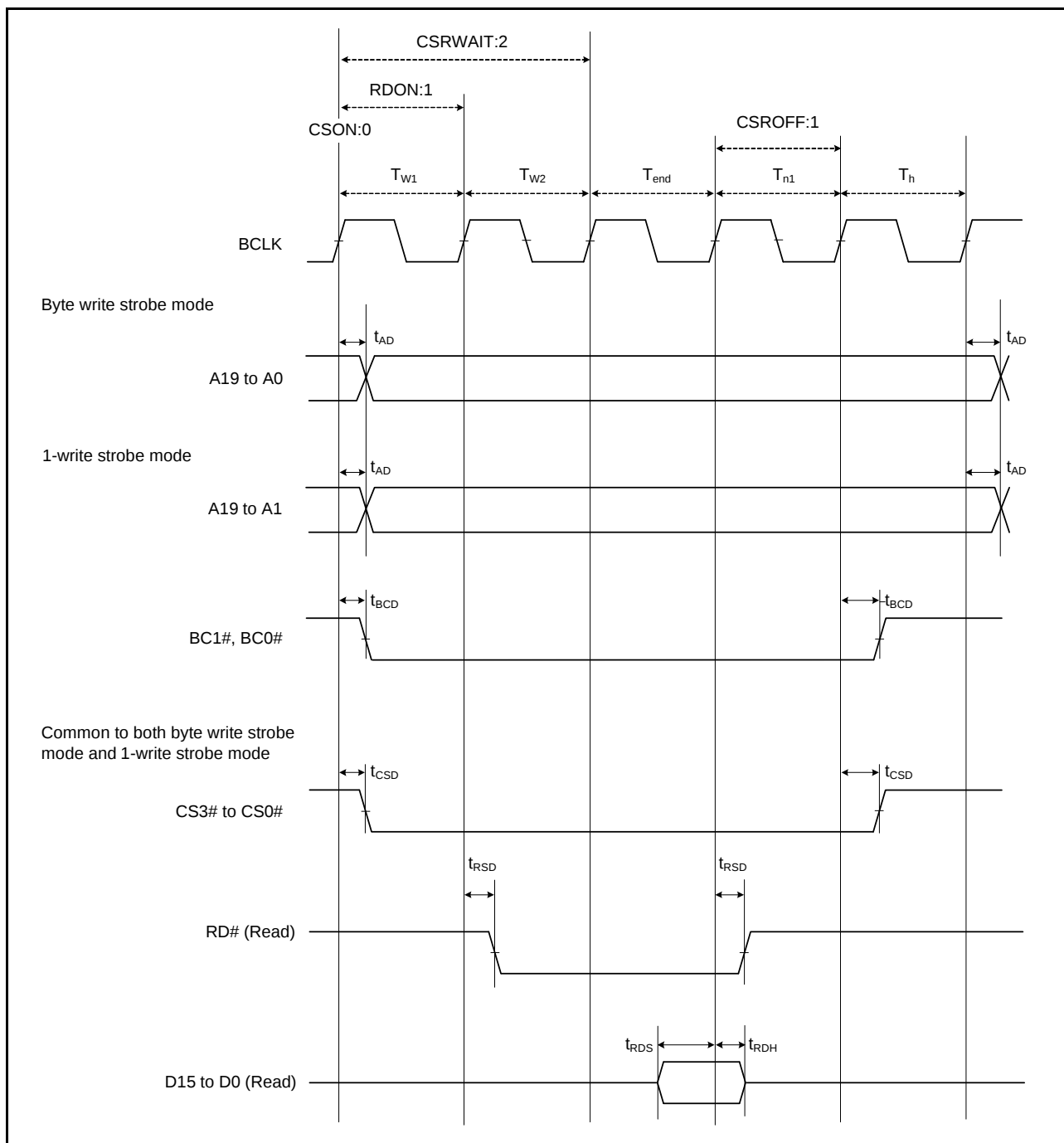


Figure 5.13 External Bus Timing/Normal Read Cycle (Bus Clock Synchronized)

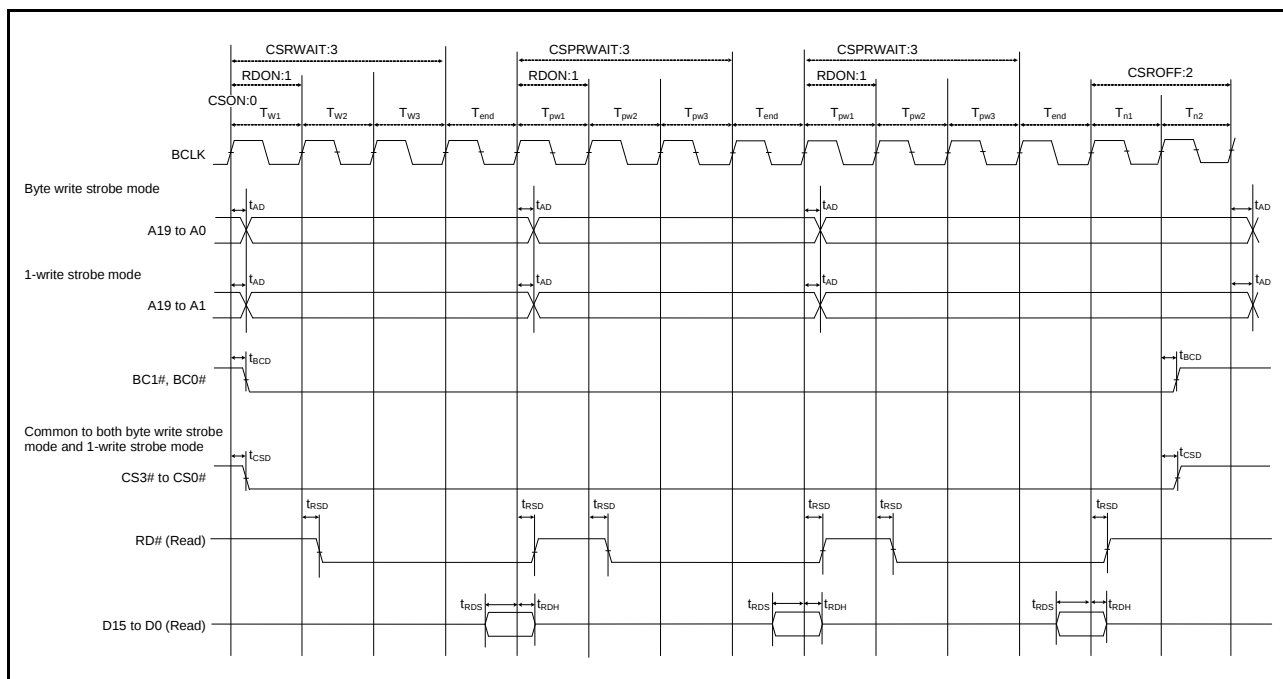


Figure 5.15 External Bus Timing/Page Read Cycle (Bus Clock Synchronized)

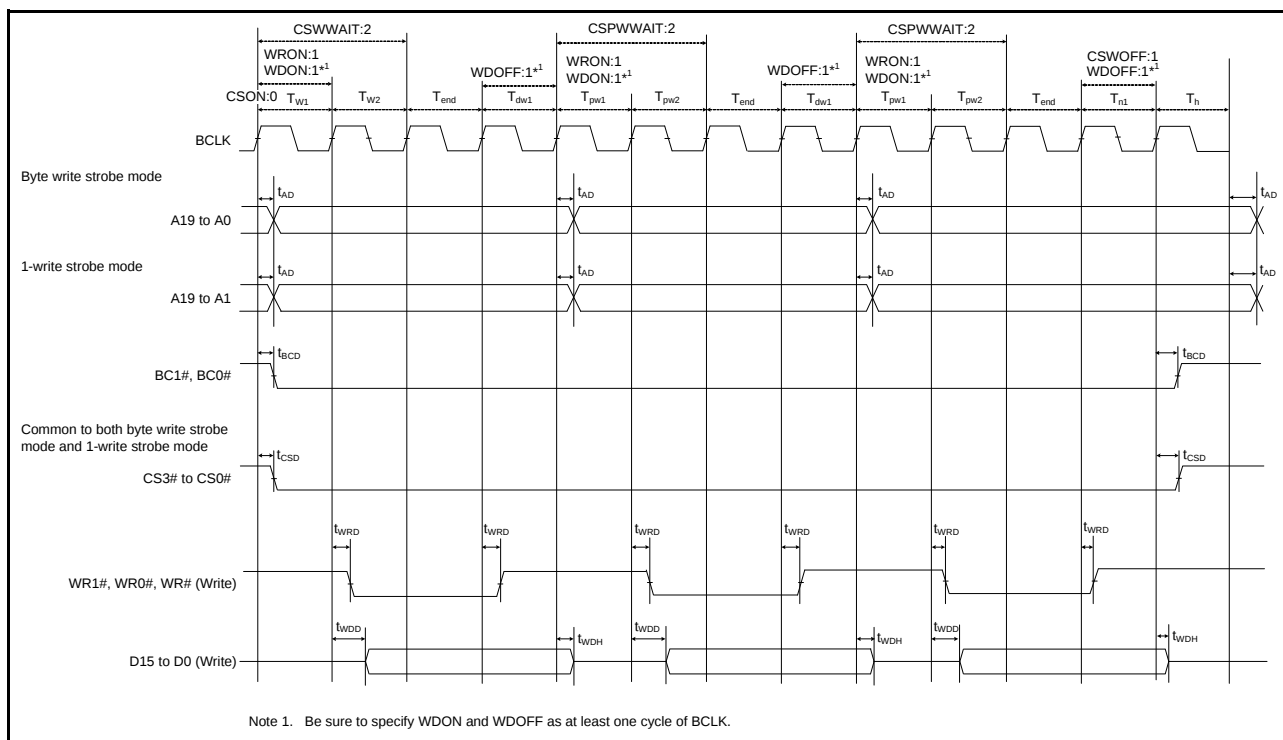


Figure 5.16 External Bus Timing/Page Write Cycle (Bus Clock Synchronized)

Table 5.16 Timing of On-Chip Peripheral Modules (6)

Note: Common standard values for conditions not given in the table are listed as "Condition 1" to "Condition 3" below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

T_a = T_{opr}. T_a is common to conditions 1 to 3.

Item		Symbol	Min.*1, *2	Max.	Unit	Test Conditions
Simple IIC (Standard-mode)	SCL, SDA input rise time	t _{Sr}	—	1000	ns	Figure 5.36
	SCL, SDA input fall time	t _{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t _{SP}	0	4 × t _{Pcyc}	ns	
	Data input setup time	t _{SDAS}	250	—	ns	
	Data input hold time	t _{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C _b	—	400	pF	
Simple IIC (Fast-mode)	SCL, SDA input rise time	t _{Sr}	20 + 0.1C _b	300	ns	
	SCL, SDA input fall time	t _{Sf}	20 + 0.1C _b	300	ns	
	SCL, SDA input spike pulse removal time	t _{SP}	0	4 × t _{Pcyc}	ns	
	Data input setup time	t _{SDAS}	100	—	ns	
	Data input hold time	t _{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C _b	—	400	pF	

Note 1. The value in parentheses is used when ICMR3.NF[1:0] are set to 11b while a digital filter is enabled with ICFER.NFE = 1.

Note 2. C_b indicates the total capacity of the bus line.

Note 3. t_{Pcyc}: PCLK cycle

5.3.7 Timing of PWM Delay Generation Circuit

Table 5.17 Timing of the PWM Delay Generation Circuit

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

T_a = T_{opr}. T_a is common to conditions 1 to 3.

Item	Symbol	Typ.	Max.	Unit	Test Conditions
Resolution	—	312.5	—	ps	PCLKA = 100 MHz
DNL*1	—	±2.0	—	LSB	

Note 1. This value is correct when the difference between each code and the next is a resolution of one bit (1 LSB).

Table 5.20 10-Bit A/D Conversion Characteristics (2)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: $V_{CC} = PLLVCC = VCC_USB = 2.7$ to 3.6 V, $VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0$ V
 $AVCC0 = AVCC = VREF = 3.0$ to 3.6 V, $VREFH0 = 3.0$ V to $AVCC0$

Condition 2: $V_{CC} = PLLVCC = VCC_USB = 2.7$ to 3.6 V, $VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0$ V
 $AVCC0 = AVCC = VREF = 4.0$ to 5.5 V, $VREFH0 = 4.0$ V to $AVCC0$

Condition 3: $V_{CC} = PLLVCC = 4.0$ to 5.5 V, $VCC_USB = 3.0$ to 3.6 V, $VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0$ V
 $AVCC0 = AVCC = VREF = 4.0$ to 5.5 V, $VREFH0 = 4.0$ V to $AVCC0$

$T_a = T_{opr}$ is common to conditions 1 to 3.

Item			Min.	Typ.	Max.	Unit	Test Conditions
Resolution			10	10	10	Bit	
Conversion time*1 (Operation at ADCLK = 50 MHz)	Without 0.1-μF external capaci- tor Permissible sig- nal source impedance (max.) = 1 kΩ	AN0 to AN7	0.8	—	—	μs	Sampling in 15 states
		Other channels	1.0	—	—	μs	Sampling in 25 states
Analog input capacitance			—	—	6	pF	
Integral nonlinearity error			—	—	±2.0	LSB	
Offset error			—	—	±2.0	LSB	
Full-scale error			—	—	±3.0	LSB	
Quantization error			—	±0.5	—	LSB	
Absolute accuracy			—	—	±4.0	LSB	

Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Table 5.23 Characteristics of the Programmable Gain Amplifier

Note: Common standard values for conditions not given in the table are listed as "Condition 1" to "Condition 3" below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$ T_a is common to conditions 1 to 3.

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Analog input capacitance		C_{in}	—	—	8	pF	
Input offset voltage		V_{off}	—	—	8	mV	
Input voltage range (V_{in})	Gain $\times$ 2.000	V_{in}	$0.050 \times AV_{cc}$	—	$0.450 \times AV_{cc}$	V	
	Gain $\times$ 2.500		$0.047 \times AV_{cc}$	—	$0.360 \times AV_{cc}$		
	Gain $\times$ 3.077		$0.045 \times AV_{cc}$	—	$0.292 \times AV_{cc}$		
	Gain $\times$ 3.636		$0.042 \times AV_{cc}$	—	$0.247 \times AV_{cc}$		
	Gain $\times$ 4.000		$0.040 \times AV_{cc}$	—	$0.212 \times AV_{cc}$		
	Gain $\times$ 4.444		$0.036 \times AV_{cc}$	—	$0.191 \times AV_{cc}$		
	Gain $\times$ 5.000		$0.033 \times AV_{cc}$	—	$0.170 \times AV_{cc}$		
	Gain $\times$ 5.714		$0.031 \times AV_{cc}$	—	$0.148 \times AV_{cc}$		
	Gain $\times$ 6.667		$0.029 \times AV_{cc}$	—	$0.127 \times AV_{cc}$		
	Gain $\times$ 10.000		$0.025 \times AV_{cc}$	—	$0.08 \times AV_{cc}$		
	Gain $\times$ 13.333		$0.023 \times AV_{cc}$	—	$0.06 \times AV_{cc}$		
Slew rate		SR	10	—	—	V/ μ s	
Gain error	Gain $\times$ 2.000	—	—	—	1	%	
	Gain $\times$ 2.500		—	—	1		
	Gain $\times$ 3.077		—	—	1		
	Gain $\times$ 3.636		—	—	1.5		
	Gain $\times$ 4.000		—	—	1.5		
	Gain $\times$ 4.444		—	—	2		
	Gain $\times$ 5.000		—	—	2		
	Gain $\times$ 5.714		—	—	2		
	Gain $\times$ 6.667		—	—	3		
	Gain $\times$ 10.000		—	—	4		
	Gain $\times$ 13.333		—	—	4		

5.10 E² Flash Characteristics

Table 5.31 E² Flash Characteristics (1)

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Temperature range for the programming/erasure operation: T_a = T_{opr}. T_a is common to conditions 1 to 3.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Reprogram/erase cycle*1	N _{DPEC}	100000	—	—	Times	
Data hold time	t _{DDRP}	30*2	—	—	Year	T _a = +85°C

Note 1. Definition of reprogram/erase cycle:

The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 100000), erasing can be performed n times for each block. For instance, when 128-byte programming is performed 16 times for different addresses in 2-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. The value is obtained from the reliability test.

Table 5.32 E² Flash Characteristics (2)

Note: Common standard values for conditions not given in the table are listed as "Condition 1" to "Condition 3" below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Temperature range for the programming/erasure operation: T_a = T_{opr}. T_a is common to conditions 1 to 3.

Item		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time N _{DPEC} ≤ 100 times	2 bytes	t _{DP2}	—	0.7	6	—	0.25	2	ms
Programming time N _{DPEC} > 100 times	2 bytes	t _{DP2}	—	0.7	6	—	0.25	2	ms
Erasure time N _{DPEC} ≤ 100 times	32 bytes	t _{DE32}	—	4	40	—	2	20	ms
Erasure time N _{DPEC} > 100 times	32 bytes	t _{DE32}	—	7	40	—	4	20	ms
Blank check time	2 bytes	t _{DBC2}	—	—	100	—	—	30	μs
Suspend delay time during programming		t _{DSPD}	—	—	250	—	—	120	μs
First suspend delay time during erasing (in suspend priority mode)		t _{DSESD1}	—	—	250	—	—	120	μs
Second suspend delay time during erasing (in suspend priority mode)		t _{DSESD2}	—	—	500	—	—	300	μs
Suspend delay time during erasing (in erasure priority mode)		t _{DSEED}	—	—	500	—	—	300	μs

6.3.5 Timing of On-Chip Peripheral Modules

Table 6.11 Timing of On-Chip Peripheral Modules (1)

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
I/O ports	Input data pulse width		t _{PRW}	1.5	—	t _{Pcyc}	Figure 6.12
MTU3	Input capture input pulse width	Single-edge setting	t _{TICW}	3	—	t _{PAcyc}	Figure 6.13
		Both-edge setting		5	—		
	Timer clock pulse width	Single-edge setting	t _{TCKWH} , t _{TCKWL}	3	—	t _{PAcyc}	Figure 6.14
		Both-edge setting		5	—		
		Phase counting mode		5	—		
POE3	POE# input pulse width		t _{POEW}	1.5	—	t _{Pcyc}	Figure 6.16
GPT	Input capture input pulse width	Single-edge setting	t _{GTICW}	3	—	t _{PAcyc}	Figure 6.15
		Both-edge setting		5	—		
	External trigger input pulse width	Single-edge setting	t _{OTETW}	3	—	t _{PAcyc}	Figure 6.18
		Both-edge setting		5	—		
SCI	Input clock cycle	Asynchronous	t _{Scyc}	4	—	t _{Pcyc}	Figure 6.17
		Clock synchronous		6	—		
	Input clock pulse width		t _{SCKW}	0.4	0.6	t _{Scyc}	
	Input clock rise time		t _{SCKr}	—	20	ns	
	Input clock fall time		t _{SCKf}	—	20	ns	
	Output clock cycle	Asynchronous	t _{Scyc}	16	—	t _{Pcyc}	
		Clock synchronous		4	—		
	Output clock pulse width		t _{SCKW}	0.4	0.6	t _{Scyc}	
	Output clock rise time		t _{SCKr}	—	20	ns	
	Output clock fall time		t _{SCKf}	—	20	ns	
	Transmit data delay time	Clock synchronous	t _{TXD}	—	40	ns	Figure 6.18
	Receive data setup time	Clock synchronous	t _{RXS}	40	—	ns	
	Receive data hold time	Clock synchronous	t _{RXH}	40	—	ns	
A/D converter	12-bit A/D converter trigger input pulse width		t _{TRGW}	1.5	—	t _{Pcyc}	Figure 6.19

Note 1. t_{Pcyc}: PCLK cycle, t_{PAcyc}: PCLKA cycle

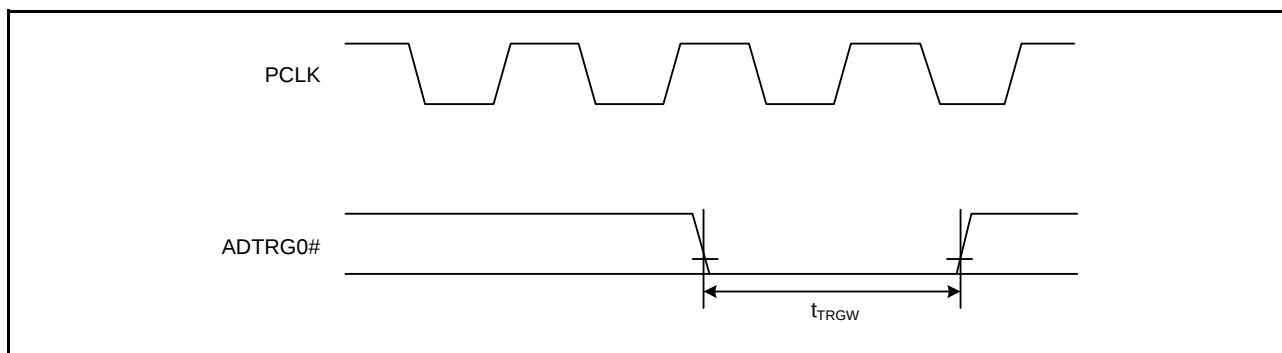


Figure 6.19 AD Converter External Trigger Input Timing

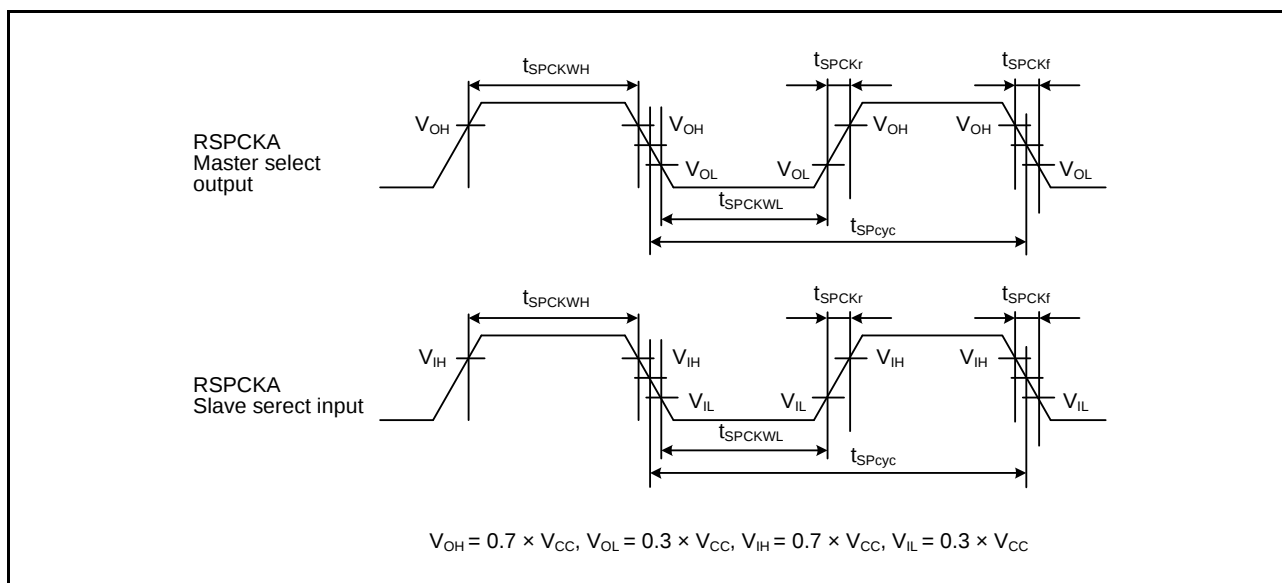


Figure 6.20 RSPCKA Clock Timing and Simple SPI Clock Timing

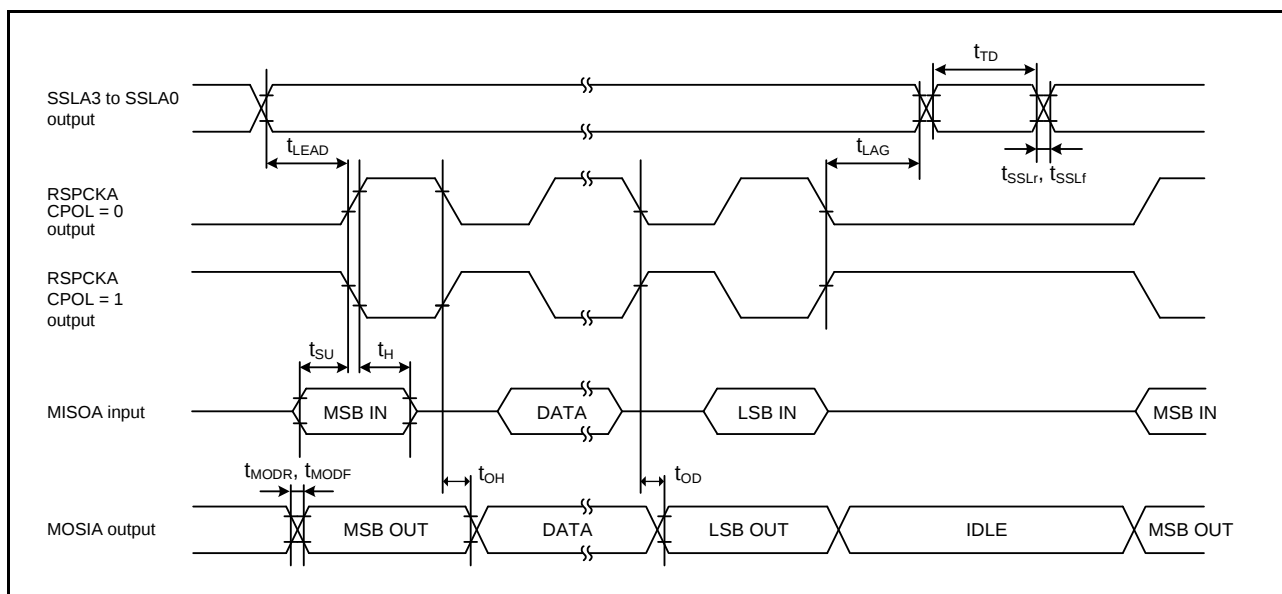


Figure 6.21 RSPCKA Timing (Master, CPHA = 0) and Simple SPI Timing (Master, CKPH = 1)

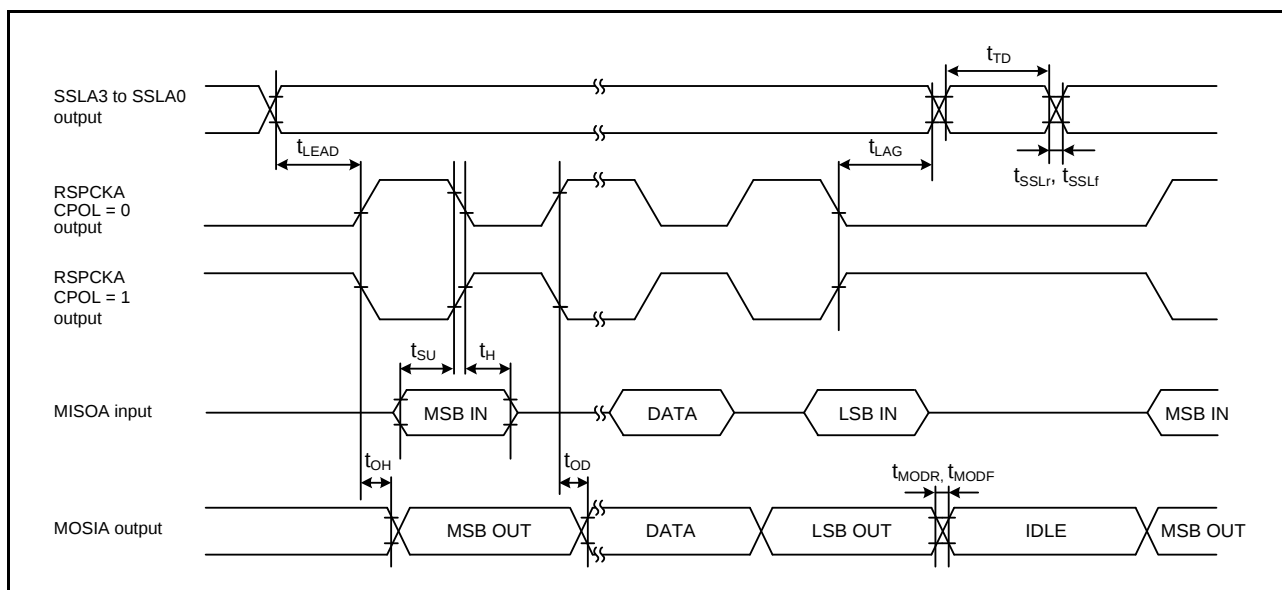


Figure 6.22 RSPI Timing (Master, CPHA = 1) and Simple SPI Timing (Master, CKPH = 0)

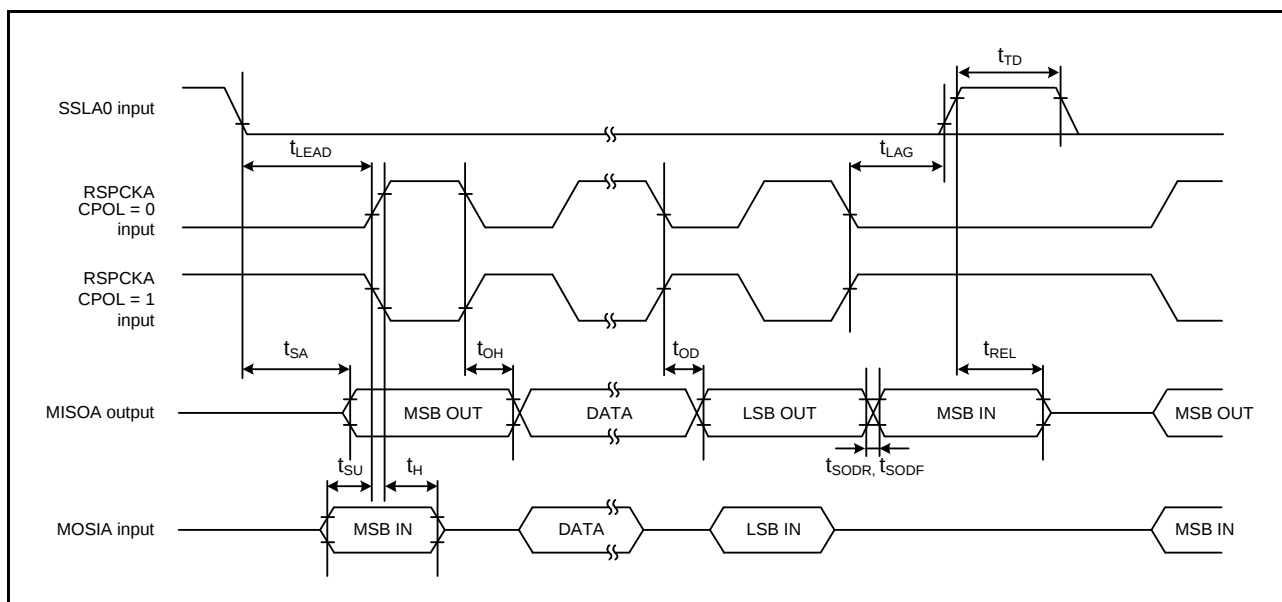


Figure 6.23 RSPI Timing (Slave, CPHA = 0) and Simple SPI Timing (Slave, CKPH = 1)