Renesas Electronics America Inc - R5F563T5EDFL#V0 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	25
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f563t5edfl-v0

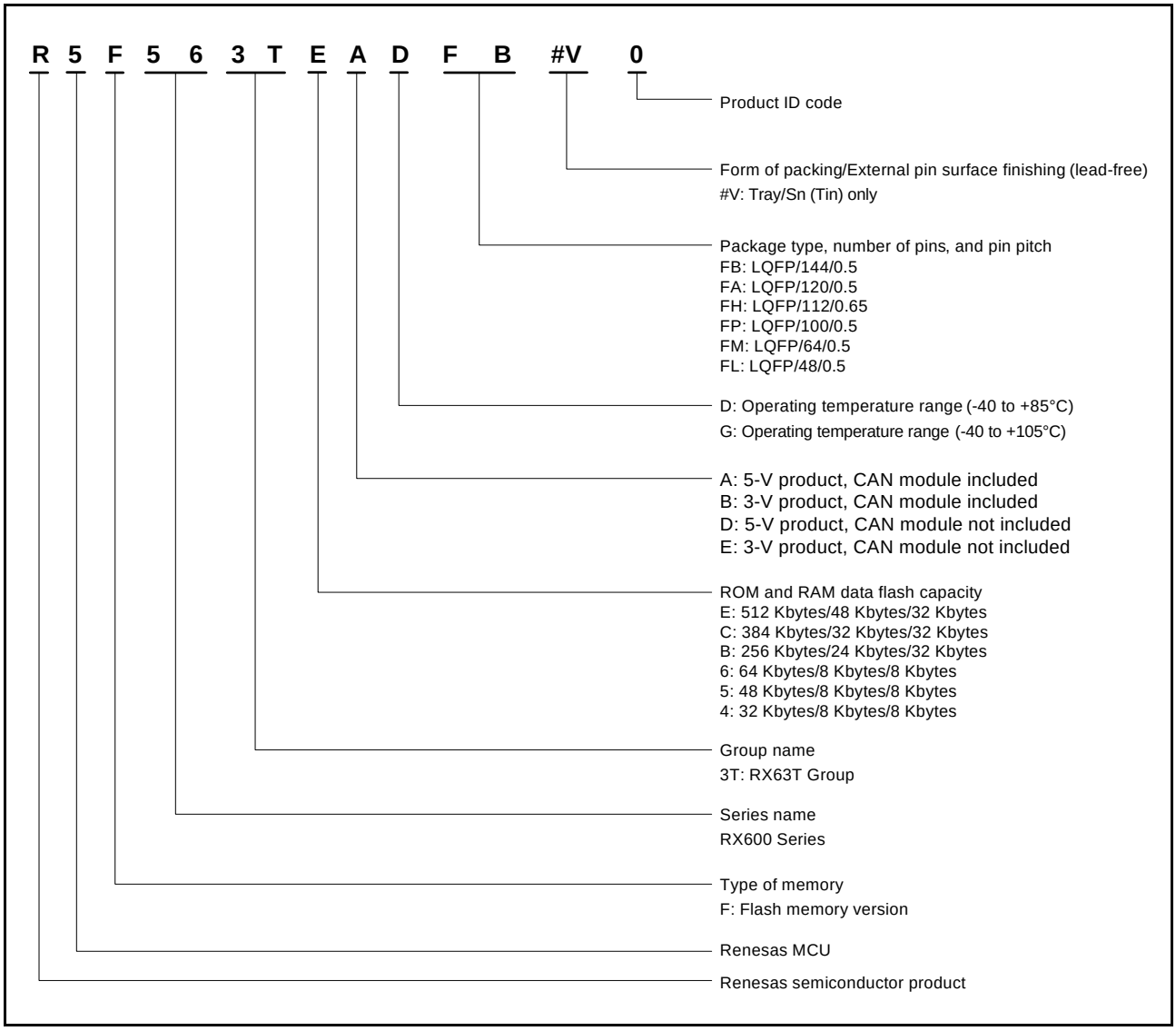

Figure 1.1 How to Read the Product Part Number

Table 1.5 List of Pins and Pin Functions (144-Pin LQFP) (1/4)

Pin Number 144-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3, GPT, POE3, CAC)	Communications (SCIc, SCId, RSPI, RIIC, CAN, USB)	Interrupt	S12ADB, AD, DA
1	VCC_USB						
2		PE5	BCLK		USB0_VBUS	IRQ0	
3	EMLE						
4	TRSYNC	P03			RXD2/SMISO2/SSCL2	IRQ7	
5	TRDATA3	P02			TXD2/SMOSI2/SSDA2		
6	VSS						
7		P01	RD#		CTS0#/RTS0#/SS0#/ USB0_DRPD		
8	VCL						
9		P00	CS1#	CACREF			
10	MD/FINED						
11		PE4	A10	POE10#/MTCLKC		IRQ1	
12		PE3	A11	POE11#/MTCLKD		IRQ2-DS	
13	TRDATA2	P14			SCK2		
14	VCC						
15		P13			CTS2#/RTS2#/SS2#/ USB0_VBUSEN		
16	RES#						
17	XTAL						
18	VSS						
19	EXTAL						
20	VCC						
21		PE2		POE10#		NMI	
22		PE1	WR0#/WR#		CTS12#/RTS12#/ SS12#/SSLA3/SSLB3/ USB0_OVRCURA		
23		PE0	WR1#/BC1#/ WAIT#		SSLA2/SSLB2/CRX1/ USB0_OVRCURB	IRQ7	
24		PD7		GTIOC0A	CTS0#/RTS0#/SS0#/ SSLA1/SSLB1/CTX1		
25		PD6		GTIOC0B	SSLA0/SSLB0		
26		PD5		GTIOC1A	RXD1/SMISO1/SSCL1	IRQ6	
27	VSS						
28		PD4		GTIOC1B	SCK1		
29		PD3		GTIOC2A	TXD1/SMOSI1/SSDA1		
30		PD2	CS2#	GTIOC2B	MOSIA/MOSIB/ USB0_ID		
31		PD1	CS0#	GTIOC3A	MISOA/MISOB/ USB0_EXICEN		
32		PD0	A12	GTIOC3B	RSPCKA/RSPCKB		
33		PF4	CS3#				
34		PF3			TXD1/SMOSI1/SSDA1		
35		PF2	CS1#		RXD1/SMISO1/SSCL1	IRQ5	
36	TRST#	PF1					
37	TMS	PF0					
38		PB7	A19		SCK12		

Table 1.5 List of Pins and Pin Functions (144-Pin LQFP) (4/4)

Pin Number 144-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3, GPT, POE3, CAC)	Communications (SCIc, SCId, RSPI, RIIC, CAN, USB)	Interrupt	S12ADB, AD, DA
110		P60	A5				AN0
111		P57					AN13
112		P56					AN12
113		P55					AN11/DA1
114		P54					AN10/ DA0
115		P53	A6				AN9
116		P52	A7				AN8
117		P51					AN7
118		P50					AN6
119		P47					AN103/ CVREFH
120		P46					AN102
121		P45					AN101
122		P44					AN100
123		P43					AN003/ CVREFL
124		P42					AN002
125		P41					AN001
126		P40					AN000
127	AVCC0						
128	VREFH0						
129	VREFL0						
130	AVSS0						
131		P82	WAIT#	MTIC5U	SCK12	IRQ3	
132		P81	A8	MTIC5V	TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12		
133	VSS						
134		P80	A9	MTIC5W	RXD12/SMISO12/ SSCL12/RXDX12	IRQ5	
135		P12	CS3#		USB0_DPRPD		
136		P11	ALE	MTCLKC		IRQ1-DS	
137		P10		MTCLKD		IRQ0-DS	
138		P05	CS2#/WAIT#				
139	VCC						
140		P04					
141					USB0_DPUPE		
142	VSS_USB						
143					USB0_DM		
144					USB0_DP		

Note 1. Available for use as SCI pin only in boot mode.

Table 1.7 List of Pins and Pin Functions (112-Pin LQFP) (4/4)

Pin Number 112-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3, GPT, POE3, CAC)	Communications (SCIc, SCId, RSPI, RIIC, CAN)	Interrupt	S12ADB, AD, DA
110		P10		MTCLKD		IRQ0-DS	
111	TRST#	P05	WAIT#/CS2#				
112	TMS	P04					

Note 1. Available for use as SCI pin only in boot mode.

Table 4.1 List of I/O Registers (Address Order) (4/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 7010h	ICU	Interrupt Request Register 016	IR016	8	8	2 ICLK		ICUb	
0008 7015h	ICU	Interrupt Request Register 021	IR021	8	8	2 ICLK			
0008 7017h	ICU	Interrupt Request Register 023	IR023	8	8	2 ICLK			
0008 701Bh	ICU	Interrupt Request Register 027	IR027	8	8	2 ICLK			
0008 701Ch	ICU	Interrupt Request Register 028	IR028	8	8	2 ICLK			
0008 701Dh	ICU	Interrupt Request Register 029	IR029	8	8	2 ICLK			
0008 701Eh	ICU	Interrupt Request Register 030	IR030	8	8	2 ICLK			
0008 701Fh	ICU	Interrupt Request Register 031	IR031	8	8	2 ICLK			
0008 7021h	ICU	Interrupt Request Register 033	IR033	8	8	2 ICLK			Not present in versions with 112, 100, 64 or 48 pins.
0008 7022h	ICU	Interrupt Request Register 034	IR034	8	8	2 ICLK			Not present in versions with 112, 100, 64 or 48 pins.
0008 7023h	ICU	Interrupt Request Register 035	IR035	8	8	2 ICLK			Not present in versions with 112, 100, 64 or 48 pins.
0008 7024h	ICU	Interrupt Request Register 036	IR036	8	8	2 ICLK			
0008 7025h	ICU	Interrupt Request Register 037	IR037	8	8	2 ICLK			
0008 7026h	ICU	Interrupt Request Register 038	IR038	8	8	2 ICLK			
0008 7027h	ICU	Interrupt Request Register 039	IR039	8	8	2 ICLK			
0008 7028h	ICU	Interrupt Request Register 040	IR040	8	8	2 ICLK			
0008 7029h	ICU	Interrupt Request Register 041	IR041	8	8	2 ICLK			
0008 702Ah	ICU	Interrupt Request Register 042	IR042	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 702Bh	ICU	Interrupt Request Register 043	IR043	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 702Ch	ICU	Interrupt Request Register 044	IR044	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 702Dh	ICU	Interrupt Request Register 045	IR045	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 702Eh	ICU	Interrupt Request Register 046	IR046	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 702Fh	ICU	Interrupt Request Register 047	IR047	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7030h	ICU	Interrupt Request Register 048	IR048	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7031h	ICU	Interrupt Request Register 049	IR049	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7032h	ICU	Interrupt Request Register 050	IR050	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7033h	ICU	Interrupt Request Register 051	IR051	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7034h	ICU	Interrupt Request Register 052	IR052	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7035h	ICU	Interrupt Request Register 053	IR053	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7036h	ICU	Interrupt Request Register 054	IR054	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7037h	ICU	Interrupt Request Register 055	IR055	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7038h	ICU	Interrupt Request Register 056	IR056	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7039h	ICU	Interrupt Request Register 057	IR057	8	8	2 ICLK			
0008 703Ah	ICU	Interrupt Request Register 058	IR058	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 703Bh	ICU	Interrupt Request Register 059	IR059	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 703Ch	ICU	Interrupt Request Register 060	IR060	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 703Dh	ICU	Interrupt Request Register 061	IR061	8	8	2 ICLK			Not present in versions with 64 or 48 pins.

Table 4.1 List of I/O Registers (Address Order) (7/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 70C0h	ICU	Interrupt Request Register 192	IR192	8	8	2 ICLK		ICUb	Not present in versions with 112, 100, 64 or 48 pins.
0008 70C1h	ICU	Interrupt Request Register 193	IR193	8	8	2 ICLK			Not present in versions with 112, 100, 64 or 48 pins.
0008 70C2h	ICU	Interrupt Request Register 194	IR194	8	8	2 ICLK			
0008 70C3h	ICU	Interrupt Request Register 195	IR195	8	8	2 ICLK			
0008 70C4h	ICU	Interrupt Request Register 196	IR196	8	8	2 ICLK			
0008 70C5h	ICU	Interrupt Request Register 197	IR197	8	8	2 ICLK			
0008 70C6h	ICU	Interrupt Request Register 198	IR198	8	8	2 ICLK			
0008 70C7h	ICU	Interrupt Request Register 199	IR199	8	8	2 ICLK			
0008 70C8h	ICU	Interrupt Request Register 200	IR200	8	8	2 ICLK			
0008 70C9h	ICU	Interrupt Request Register 201	IR201	8	8	2 ICLK			
0008 70D6h	ICU	Interrupt Request Register 214	IR214	8	8	2 ICLK			
0008 70D7h	ICU	Interrupt Request Register 215	IR215	8	8	2 ICLK			
0008 70D8h	ICU	Interrupt Request Register 216	IR216	8	8	2 ICLK			
0008 70D9h	ICU	Interrupt Request Register 217	IR217	8	8	2 ICLK			
0008 70DAh	ICU	Interrupt Request Register 218	IR218	8	8	2 ICLK			
0008 70DBh	ICU	Interrupt Request Register 219	IR219	8	8	2 ICLK			
0008 70DCh	ICU	Interrupt Request Register 220	IR220	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70DDh	ICU	Interrupt Request Register 221	IR221	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70DEh	ICU	Interrupt Request Register 222	IR222	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70DFh	ICU	Interrupt Request Register 223	IR223	8	8	2 ICLK			Not present in versions with 100, 64 or 48 pins.
0008 70E0h	ICU	Interrupt Request Register 224	IR224	8	8	2 ICLK			Not present in versions with 100, 64 or 48 pins.
0008 70E1h	ICU	Interrupt Request Register 225	IR225	8	8	2 ICLK			Not present in versions with 100, 64 or 48 pins.
0008 70E2h	ICU	Interrupt Request Register 226	IR226	8	8	2 ICLK			
0008 70E3h	ICU	Interrupt Request Register 227	IR227	8	8	2 ICLK			
0008 70E4h	ICU	Interrupt Request Register 228	IR228	8	8	2 ICLK			
0008 70E5h	ICU	Interrupt Request Register 229	IR229	8	8	2 ICLK			
0008 70E6h	ICU	Interrupt Request Register 230	IR230	8	8	2 ICLK			
0008 70E7h	ICU	Interrupt Request Register 231	IR231	8	8	2 ICLK			
0008 70E8h	ICU	Interrupt Request Register 232	IR232	8	8	2 ICLK			
0008 70E9h	ICU	Interrupt Request Register 233	IR233	8	8	2 ICLK			
0008 70EAh	ICU	Interrupt Request Register 234	IR234	8	8	2 ICLK			
0008 70EBh	ICU	Interrupt Request Register 235	IR235	8	8	2 ICLK			
0008 70ECh	ICU	Interrupt Request Register 236	IR236	8	8	2 ICLK			
0008 70EEh	ICU	Interrupt Request Register 238	IR238	8	8	2 ICLK			
0008 70EFh	ICU	Interrupt Request Register 239	IR239	8	8	2 ICLK			
0008 70F0h	ICU	Interrupt Request Register 240	IR240	8	8	2 ICLK			
0008 70F1h	ICU	Interrupt Request Register 241	IR241	8	8	2 ICLK			
0008 70F2h	ICU	Interrupt Request Register 242	IR242	8	8	2 ICLK			
0008 70F4h	ICU	Interrupt Request Register 244	IR244	8	8	2 ICLK			
0008 70F5h	ICU	Interrupt Request Register 245	IR245	8	8	2 ICLK			
0008 70F6h	ICU	Interrupt Request Register 246	IR246	8	8	2 ICLK			
0008 70F7h	ICU	Interrupt Request Register 247	IR247	8	8	2 ICLK			
0008 70F8h	ICU	Interrupt Request Register 248	IR248	8	8	2 ICLK			
0008 70FAh	ICU	Interrupt Request Register 250	IR250	8	8	2 ICLK			
0008 70FBh	ICU	Interrupt Request Register 251	IR251	8	8	2 ICLK			
0008 70FCh	ICU	Interrupt Request Register 252	IR252	8	8	2 ICLK			

Table 4.1 List of I/O Registers (Address Order) (10/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 71BBh	ICU	DTC Activation Enable Register 187	DTCER187	8	8	2 ICLK		ICUb	Not present in versions with 64 or 48 pins.
0008 71BCh	ICU	DTC Activation Enable Register 188	DTCER188	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 71BDh	ICU	DTC Activation Enable Register 189	DTCER189	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 71BFh	ICU	DTC Activation Enable Register 191	DTCER191	8	8	2 ICLK			Not present in versions with 112, 100, 64 or 48 pins.
0008 71C0h	ICU	DTC Activation Enable Register 192	DTCER192	8	8	2 ICLK			Not present in versions with 112, 100, 64 or 48 pins.
0008 71C3h	ICU	DTC Activation Enable Register 195	DTCER195	8	8	2 ICLK			
0008 71C4h	ICU	DTC Activation Enable Register 196	DTCER196	8	8	2 ICLK			
0008 71C6h	ICU	DTC Activation Enable Register 198	DTCER198	8	8	2 ICLK			
0008 71C7h	ICU	DTC Activation Enable Register 199	DTCER199	8	8	2 ICLK			
0008 71C8h	ICU	DTC Activation Enable Register 200	DTCER200	8	8	2 ICLK			
0008 71C9h	ICU	DTC Activation Enable Register 201	DTCER201	8	8	2 ICLK			
0008 71D6h	ICU	DTC Activation Enable Register 214	DTCER214	8	8	2 ICLK			
0008 71D7h	ICU	DTC Activation Enable Register 215	DTCER215	8	8	2 ICLK			
0008 71D9h	ICU	DTC Activation Enable Register 217	DTCER217	8	8	2 ICLK			
0008 71DAh	ICU	DTC Activation Enable Register 218	DTCER218	8	8	2 ICLK			
0008 71DCh	ICU	DTC Activation Enable Register 220	DTCER220	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 71DDh	ICU	DTC Activation Enable Register 221	DTCER221	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 71DFh	ICU	DTC Activation Enable Register 223	DTCER223	8	8	2 ICLK			Not present in versions with 100, 64 or 48 pins.
0008 71E0h	ICU	DTC Activation Enable Register 224	DTCER224	8	8	2 ICLK			Not present in versions with 100, 64 or 48 pins.
0008 71E2h	ICU	DTC Activation Enable Register 226	DTCER226	8	8	2 ICLK			
0008 71E3h	ICU	DTC Activation Enable Register 227	DTCER227	8	8	2 ICLK			
0008 71E4h	ICU	DTC Activation Enable Register 228	DTCER228	8	8	2 ICLK			
0008 71E5h	ICU	DTC Activation Enable Register 229	DTCER229	8	8	2 ICLK			
0008 71E6h	ICU	DTC Activation Enable Register 230	DTCER230	8	8	2 ICLK			
0008 71E7h	ICU	DTC Activation Enable Register 231	DTCER231	8	8	2 ICLK			
0008 71E8h	ICU	DTC Activation Enable Register 232	DTCER232	8	8	2 ICLK			
0008 71E9h	ICU	DTC Activation Enable Register 233	DTCER233	8	8	2 ICLK			
0008 71EAh	ICU	DTC Activation Enable Register 234	DTCER234	8	8	2 ICLK			
0008 71EBh	ICU	DTC Activation Enable Register 235	DTCER235	8	8	2 ICLK			
0008 71ECh	ICU	DTC Activation Enable Register 236	DTCER236	8	8	2 ICLK			
0008 71EEh	ICU	DTC Activation Enable Register 238	DTCER238	8	8	2 ICLK			
0008 71EFh	ICU	DTC Activation Enable Register 239	DTCER239	8	8	2 ICLK			
0008 71F0h	ICU	DTC Activation Enable Register 240	DTCER240	8	8	2 ICLK			
0008 71F1h	ICU	DTC Activation Enable Register 241	DTCER241	8	8	2 ICLK			
0008 71F2h	ICU	DTC Activation Enable Register 242	DTCER242	8	8	2 ICLK			
0008 71F4h	ICU	DTC Activation Enable Register 244	DTCER244	8	8	2 ICLK			
0008 71F5h	ICU	DTC Activation Enable Register 245	DTCER245	8	8	2 ICLK			
0008 71F6h	ICU	DTC Activation Enable Register 246	DTCER246	8	8	2 ICLK			
0008 71F7h	ICU	DTC Activation Enable Register 247	DTCER247	8	8	2 ICLK			
0008 71F8h	ICU	DTC Activation Enable Register 248	DTCER248	8	8	2 ICLK			
0008 71FAh	ICU	DTC Activation Enable Register 250	DTCER250	8	8	2 ICLK			
0008 71FBh	ICU	DTC Activation Enable Register 251	DTCER251	8	8	2 ICLK			
0008 7202h	ICU	Interrupt Request Enable Register 02	IER02	8	8	2 ICLK			
0008 7203h	ICU	Interrupt Request Enable Register 03	IER03	8	8	2 ICLK			
0008 7204h	ICU	Interrupt Request Enable Register 04	IER04	8	8	2 ICLK			
0008 7205h	ICU	Interrupt Request Enable Register 05	IER05	8	8	2 ICLK			

Table 4.1 List of I/O Registers (Address Order) (23/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 C02Ah	PORTA	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports	
0008 C02Bh	PORTB	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK		
0008 C02Dh	PORTD	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK		
0008 C02Eh	PORTE	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C02Fh	PORTF	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 100, 64, or 48 pins.
0008 C030h	PORTG	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 100, 64, or 48 pins.
0008 C040h	PORT0	Port Input Data Register	PIDR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 48 pins.
0008 C041h	PORT1	Port Input Data Register	PIDR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 48 pins.
0008 C042h	PORT2	Port Input Data Register	PIDR	8	8	2, 3 PCLKB	2 ICLK		
0008 C043h	PORT3	Port Input Data Register	PIDR	8	8	2, 3 PCLKB	2 ICLK		
0008 C044h	PORT4	Port Input Data Register	PIDR	8	8	2, 3 PCLKB	2 ICLK		
0008 C045h	PORT5	Port Input Data Register	PIDR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C046h	PORT6	Port Input Data Register	PIDR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C047h	PORT7	Port Input Data Register	PIDR	8	8	2, 3 PCLKB	2 ICLK		
0008 C048h	PORT8	Port Input Data Register	PIDR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C049h	PORT9	Port Input Data Register	PIDR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 48 pins.
0008 C04Ah	PORTA	Port Input Data Register	PIDR	8	8	2, 3 PCLKB	2 ICLK		
0008 C04Bh	PORTB	Port Input Data Register	PIDR	8	8	2, 3 PCLKB	2 ICLK		
0008 C04Ch	PORTC	Port Input Data Register	PIDR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 C04Dh	PORTD	Port Input Data Register	PIDR	8	8	2, 3 PCLKB	2 ICLK		
0008 C04Eh	PORTE	Port Input Data Register	PIDR	8	8	2, 3 PCLKB	2 ICLK		
0008 C04Fh	PORTF	Port Input Data Register	PIDR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 100, 64, or 48 pins.
0008 C050h	PORTG	Port Input Data Register	PIDR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 100, 64, or 48 pins.
0008 C060h	PORT0	Port Mode Register	PMR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 48 pins.
0008 C061h	PORT1	Port Mode Register	PMR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 48 pins.
0008 C062h	PORT2	Port Mode Register	PMR	8	8	2, 3 PCLKB	2 ICLK		
0008 C063h	PORT3	Port Mode Register	PMR	8	8	2, 3 PCLKB	2 ICLK		
0008 C067h	PORT7	Port Mode Register	PMR	8	8	2, 3 PCLKB	2 ICLK		
0008 C068h	PORT8	Port Mode Register	PMR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C069h	PORT9	Port Mode Register	PMR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 48 pins.
0008 C06Ah	PORTA	Port Mode Register	PMR	8	8	2, 3 PCLKB	2 ICLK		
0008 C06Bh	PORTB	Port Mode Register	PMR	8	8	2, 3 PCLKB	2 ICLK		
0008 C06Dh	PORTD	Port Mode Register	PMR	8	8	2, 3 PCLKB	2 ICLK		
0008 C06Eh	PORTE	Port Mode Register	PMR	8	8	2, 3 PCLKB	2 ICLK		
0008 C06Fh	PORTF	Port Mode Register	PMR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 100, 64, or 48 pins.
0008 C070h	PORTG	Port Mode Register	PMR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 100, 64, or 48 pins.
0008 C080h	PORT0	Open Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64 or 48 pins.
0008 C084h	PORT2	Open Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C085h	PORT2	Open Drain Control Register 1	ODR1	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 112 or 100 pins.

Table 4.1 List of I/O Registers (Address Order) (33/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
000A 0092h	USB0	PIPE1 Transaction Counter Register	PIPE1TRN	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1	USBa	Not present in versions with 112, 100, 64, or 48 pins.
000A 0094h	USB0	PIPE2 Transaction Counter Enable Register	PIPE2TRE	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 0096h	USB0	PIPE2 Transaction Counter Register	PIPE2TRN	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 0098h	USB0	PIPE3 Transaction Counter Enable Register	PIPE3TRE	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 009Ah	USB0	PIPE3 Transaction Counter Register	PIPE3TRN	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 009Ch	USB0	PIPE4 Transaction Counter Enable Register	PIPE4TRE	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 009Eh	USB0	PIPE4 Transaction Counter Register	PIPE4TRN	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 00A0h	USB0	PIPE5 Transaction Counter Enable Register	PIPE5TRE	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 00A2h	USB0	PIPE5 Transaction Counter Register	PIPE5TRN	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000C 1200h	MTU3	Timer Control Register	TCR	8	8, 16, 32	4, 5 PCLKA	2, 3 ICLK	MTU3	
000C 1201h	MTU4	Timer Control Register	TCR	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1202h	MTU3	Timer Mode Register 1	TMDR1	8	8, 16	4, 5 PCLKA	2, 3 ICLK		
000C 1203h	MTU4	Timer Mode Register 1	TMDR1	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1204h	MTU3	Timer I/O Control Register H	TIORH	8	8, 16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1205h	MTU3	Timer I/O Control Register L	TIORL	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1206h	MTU4	Timer I/O Control Register H	TIORH	8	8, 16	4, 5 PCLKA	2, 3 ICLK		
000C 1207h	MTU4	Timer I/O Control Register L	TIORL	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1208h	MTU3	Timer Interrupt Enable Register	TIER	8	8, 16	4, 5 PCLKA	2, 3 ICLK		
000C 1209h	MTU4	Timer Interrupt Enable Register	TIER	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 120Ah	MTU	Timer Output Master Enable Register A	TOERA	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 120Dh	MTU	Timer Gate Control Register A	TGCRA	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 120Eh	MTU	Timer Output Control Register 1A	TOCR1A	8	8, 16	4, 5 PCLKA	2, 3 ICLK		

Table 4.1 List of I/O Registers (Address Order) (37/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
000C 2006h	GPT	General PWM Timer Hardware Source Clear Control Register	GTHCCR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK	GPT	
000C 2008h	GPT	General PWM Timer Hardware Start Source Select Register	GTHSSR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 200Ah	GPT	General PWM Timer Hardware Stop/Clear Source Select Register	GTHPSR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 200Ch	GPT	General PWM Timer Write-Protection Register	GTWP	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 200Eh	GPT	General PWM Timer Sync Register	GTSYNC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2010h	GPT	General PWM Timer External Trigger Input Interrupt Register	GTETINT	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2014h	GPT	General PWM Timer Buffer Operation Disable Register	GTBDR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2018h	GPT	General PWM Timer Start Write-Protection Register	GTSWP	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2080h	GPT	LOCO Count Control Register	LCCR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2082h	GPT	LOCO Count Status Register	LCST	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2084h	GPT	LOCO Count Value Register	LCNT	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2086h	GPT	LOCO Count Result Average Register	LCNTA	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2088h	GPT	LOCO Count Result Register 0	LCNT00	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 208Ah	GPT	LOCO Count Result Register 1	LCNT01	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 208Ch	GPT	LOCO Count Result Register 2	LCNT02	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 208Eh	GPT	LOCO Count Result Register 3	LCNT03	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2090h	GPT	LOCO Count Result Register 4	LCNT04	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2092h	GPT	LOCO Count Result Register 5	LCNT05	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2094h	GPT	LOCO Count Result Register 6	LCNT06	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2096h	GPT	LOCO Count Result Register 7	LCNT07	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2098h	GPT	LOCO Count Result Register 8	LCNT08	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 209Ah	GPT	LOCO Count Result Register 9	LCNT09	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 209Ch	GPT	LOCO Count Result Register 10	LCNT10	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 209Eh	GPT	LOCO Count Result Register 11	LCNT11	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 20A0h	GPT	LOCO Count Result Register 12	LCNT12	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 20A2h	GPT	LOCO Count Result Register 13	LCNT13	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 20A4h	GPT	LOCO Count Result Register 14	LCNT14	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 20A6h	GPT	LOCO Count Result Register 15	LCNT15	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 20A8h	GPT	LOCO Count Upper Permissible Deviation Register	LCNTDU	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 20AAh	GPT	LOCO Count Lower Permissible Deviation Register	LCNTDL	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2100h	GPT0	General PWM Timer I/O Control Register	GTIOR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2102h	GPT0	General PWM Timer Interrupt Output Setting Register	GTINTAD	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2104h	GPT0	General PWM Timer Control Register	GTCR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2106h	GPT0	General PWM Timer Buffer Enable Register	GTBER	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2108h	GPT0	General PWM Timer Count Direction Register	GTUDC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 210Ah	GPT0	General PWM Timer Interrupt, A/D Converter Start Request Skipping Setting Register	GTITC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 210Ch	GPT0	General PWM Timer Status Register	GTST	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 210Eh	GPT0	General PWM Timer Counter	GTCNT	16	16	2 to 5 PCLKA	2, 3 ICLK		
000C 2110h	GPT0	General PWM Timer Compare Capture Register A	GTCCRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2112h	GPT0	General PWM Timer Compare Capture Register B	GTCCRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2114h	GPT0	General PWM Timer Compare Capture Register C	GTCCRC	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2116h	GPT0	General PWM Timer Compare Capture Register D	GTCCRD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2118h	GPT0	General PWM Timer Compare Capture Register E	GTCCRE	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		

Table 4.1 List of I/O Registers (Address Order) (39/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
000C 21A6h	GPT1	A/D Converter Start Request Timing Buffer Register A	GTADTBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK	GPT	
000C 21A8h	GPT1	A/D Converter Start Request Timing Double-Buffer Register A	GTADTDBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 21ACh	GPT1	A/D Converter Start Request Timing Register B	GTADTRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 21AEh	GPT1	A/D Converter Start Request Timing Buffer Register B	GTADTBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 21B0h	GPT1	A/D Converter Start Request Timing Double-Buffer Register B	GTADTDBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 21B4h	GPT1	General PWM Timer Output Negate Control Register	GTONCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 21B6h	GPT1	General PWM Timer Dead Time Control Register	GTDTCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 21B8h	GPT1	General PWM Timer Dead Time Value Register U	GTDVU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 21BAh	GPT1	General PWM Timer Dead Time Value Register D	GTDVD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 21BCh	GPT1	General PWM Timer Dead Time Buffer Register U	GTDBU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 21BEh	GPT1	General PWM Timer Dead Time Buffer Register D	GTDBD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 21C0h	GPT1	General PWM Timer Output Protection Function Status Register	GTSOS	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 21C2h	GPT1	General PWM Timer Output Protection Function Temporary Release Register	GTSOTR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2200h	GPT2	General PWM Timer I/O Control Register	GTIOR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2202h	GPT2	General PWM Timer Interrupt Output Setting Register	GTINTAD	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2204h	GPT2	General PWM Timer Control Register	GTCR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2206h	GPT2	General PWM Timer Buffer Enable Register	GTBER	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2208h	GPT2	General PWM Timer Count Direction Register	GTUDC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 220Ah	GPT2	General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register	GTITC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 220Ch	GPT2	General PWM Timer Status Register	GTST	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 220Eh	GPT2	General PWM Timer Counter	GTCNT	16	16	2 to 5 PCLKA	2, 3 ICLK		
000C 2210h	GPT2	General PWM Timer Compare Capture Register A	GTCCRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2212h	GPT2	General PWM Timer Compare Capture Register B	GTCCRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2214h	GPT2	General PWM Timer Compare Capture Register C	GTCCRC	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2216h	GPT2	General PWM Timer Compare Capture Register D	GTCCRD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2218h	GPT2	General PWM Timer Compare Capture Register E	GTCCRE	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 221Ah	GPT2	General PWM Timer Compare Capture Register F	GTCCRF	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 221Ch	GPT2	General PWM Timer Cycle Setting Register	GTPR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 221Eh	GPT2	General PWM Timer Cycle Setting Buffer Register	GTPBR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2220h	GPT2	General PWM Timer Cycle Setting Double-Buffer Register	GTPDBR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2224h	GPT2	A/D Converter Start Request Timing Register A	GTADTRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2226h	GPT2	A/D Converter Start Request Timing Buffer Register A	GTADTBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2228h	GPT2	A/D Converter Start Request Timing Double-Buffer Register A	GTADTDBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 222Ch	GPT2	A/D Converter Start Request Timing Register B	GTADTRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 222Eh	GPT2	A/D Converter Start Request Timing Buffer Register B	GTADTBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		

Table 5.4 DC Characteristics (3)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

The following relation applies when the USB is in use under condition 1 or condition 2: Vcc = PLLVcc = Vcc_USB = 3.0 to 3.6 V.

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Supply current *1	During operation	Max. *2	I_{CC}*3	—	—	70	mA	ICLK = 100 MHz PCLKA = 100 MHz PCLKB = 50 MHz PCLKC = 100 MHz PCLKD = 50 MHz FCLK = 50 MHz
		Normal *4		—	40	—		
		Increased by BGO operation *5		—	15	—		
	Sleep mode				40	55		
	All-module-clock-stop mode *6				20	30		
	During standby	Software standby mode		—	0.10	3	mA	
		Deep software standby mode		—	20	60	µA	
Analog power supply current	During 12-bit A/D conversion (per unit)		AI_{CC0}	—	1.5	4.2	mA	
	Programmable gain amplifier (per channel)			—	1	1.5	mA	
	Window comparator (per channel)			—	0.5	0.7	mA	
	Waiting for 12-bit A/D conversion (all units)			—	0.1	8	µA	
	During 10-bit A/D conversion (per channel)		AI_{CC}	—	0.9	1.4	mA	
	During D/A conversion (per unit)				0.1	4	µA	
	Waiting for 10-bit A/D, D/A conversion (all units)			—	0.1	4	µA	
Reference power supply current	During 12-bit A/D conversion (per unit)		AI_{REFH0}	—	1.6	2.5	mA	
	Waiting for 12-bit A/D conversion (all units)			—	0.1	1.5	µA	
	During 10-bit A/D conversion (per channel)		AI_{REF}	—	0.2	0.3	mA	
	During D/A conversion (per unit)				1	1.5	mA	
	Waiting for 10-bit A/D, D/A conversion (all units)			—	0.1	1.2	µA	
VCC rising gradient			SV_{CC}	—	—	20	ms/V	

Note 1. Supply current values are with all output pins unloaded.
Note 2. Measured with clocks supplied to the peripheral functions. This does not include the BGO operation.
Note 3. I_{CC} depends on f (ICLK) as follows. (ICLK: PCLK = 8:4)
I_{CC} max = 0.6 × f + 10 (max)
I_{CC} typ = 0.3 × f + 10 (normal)
I_{CC} max = 0.45 × f + 10 (sleep mode)
Note 4. Measured with clocks not supplied to the peripheral functions. This does not include the BGO operation.
Note 5. Incremented if data is written to or erased from the on-chip ROM or on-chip data-flash memory for data storage during the program execution.
Note 6. The values are for reference.

5.3.4 Control Signal Timing

Table 5.11 Control Signal Timing

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
NMI pulse width	t_{NMIW}	200	—	—	ns	t_c(PCLK) × 2 ≤ 200 ns, Figure 5.11
		t_c(PCLK) × 2	—	—	ns	t_c(PCLK) > 200 ns, Figure 5.11
IRQ pulse width	t_{IRQW}	200	—	—	ns	t_c(PCLK) ≤ 200 ns, Figure 5.12
		t_c(PCLK) × 2	—	—	ns	t_c(PCLK) > 200 ns, Figure 5.12

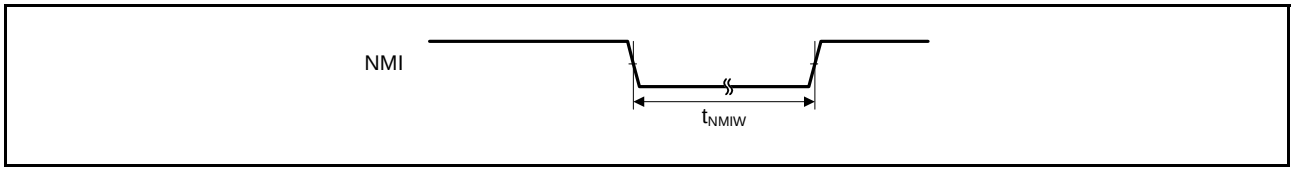

Figure 5.11 NMI Interrupt Input Timing

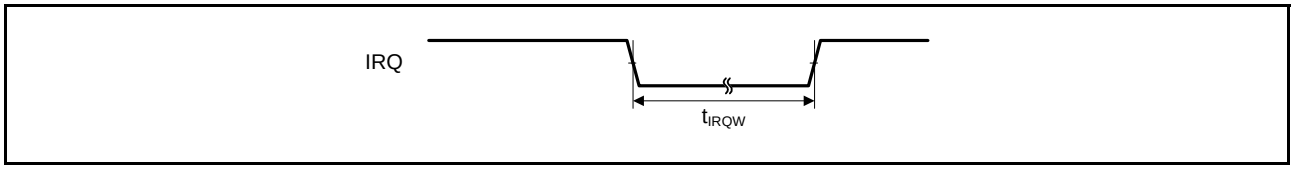

Figure 5.12 IRQ Interrupt Input Timing

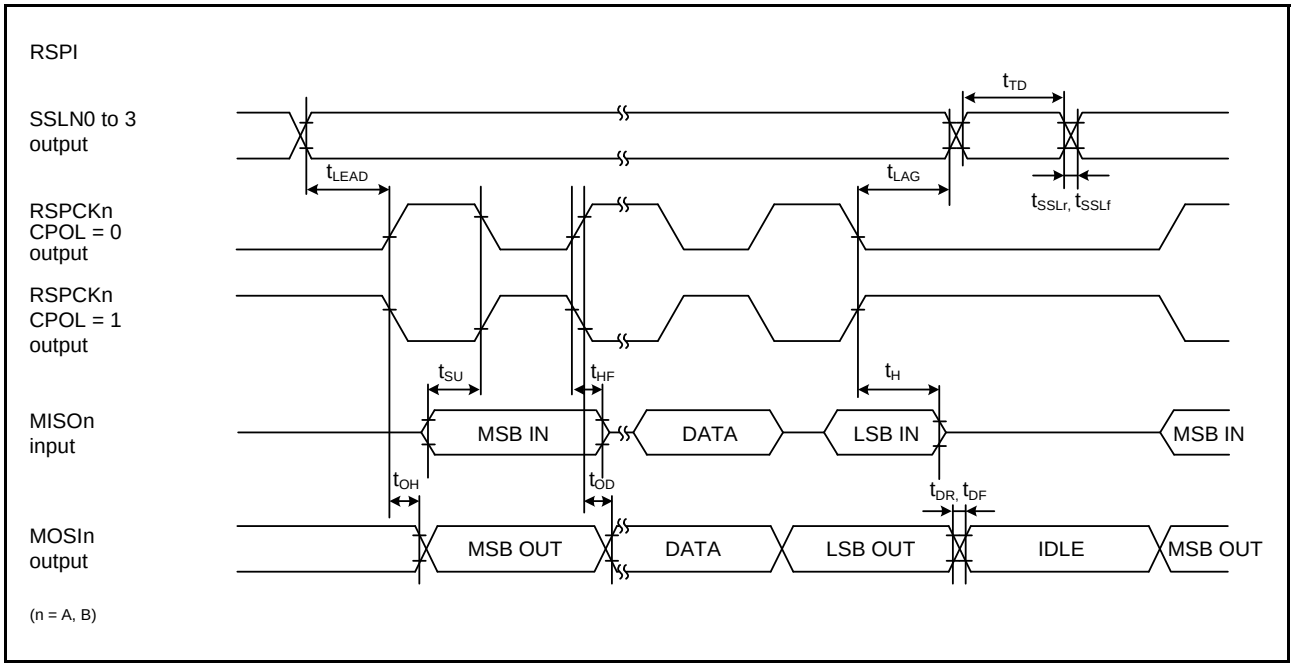

Figure 5.33 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKB Division Ratio Set to 1/2)

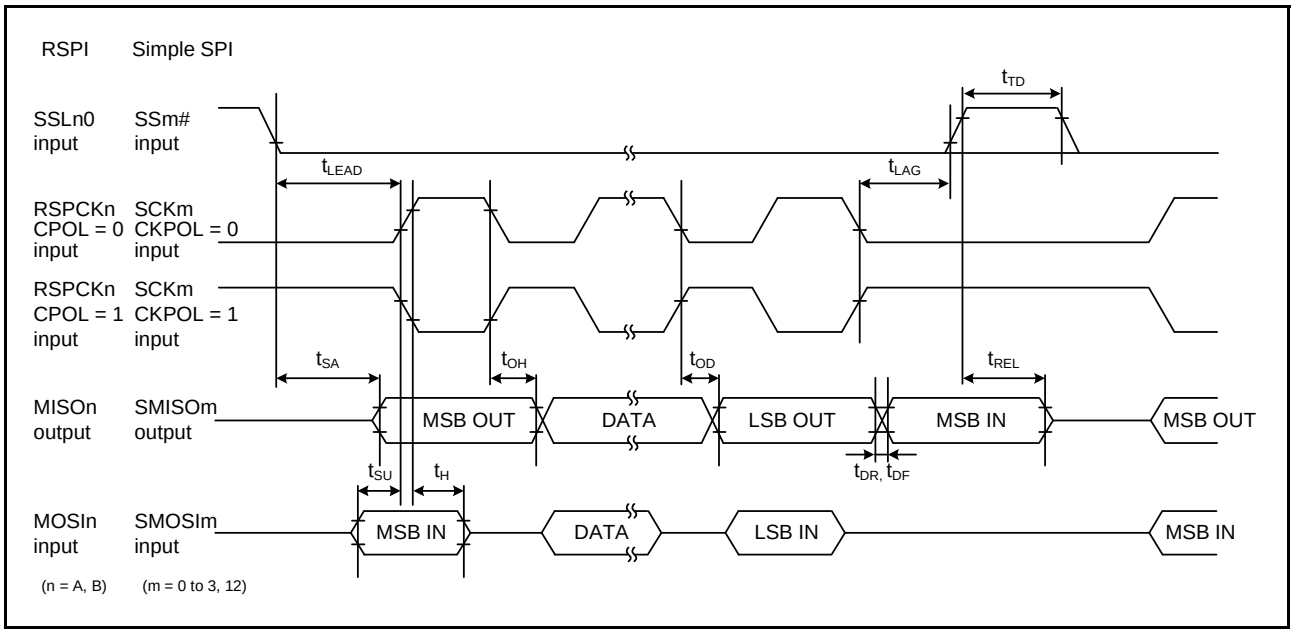

Figure 5.34 RSPI Timing (Slave, CPHA = 0) and Simple SPI Timing (Slave, CKPH = 1)

Table 5.21 12-Bit A/D Conversion Characteristics (1)

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

$T_a = T_{opr}$

Item		Min.	Typ.	Max.	Unit	Test Conditions
Resolution		12	12	12	Bit	
Conversion time*1 (ADCLK = 25 MHz)	Without 0.1-µF external capacitor Permissible signal source impedance (max.) = 1.0 kΩ	2.0	—	—	µs	Sampling in 20 states
Analog input capacitance		—	—	8	pF	
Sample and hold circuit in use	Integral nonlinearity error	—	—	±4.0	LSB	AVin = 0.25 to AV_{REFH}–0.25
	Offset error	—	—	±4.0	LSB	
	Full-scale error	—	—	±4.0	LSB	
	Quantization error	—	±0.5	—	LSB	
	Absolute accuracy	—	—	±8.0	LSB	
Sample and hold circuit not in use	Integral nonlinearity error	—	—	±3.0	LSB	AVin = AV_{REFL} to AV_{REFH}
	Offset error	—	—	±3.0	LSB	
	Full-scale error	—	—	±3.0	LSB	
	Quantization error	—	±0.5	—	LSB	
	Absolute accuracy	—	—	±6.0	LSB	

Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Table 5.22 12-Bit A/D Conversion Characteristics (2)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” and “Condition 2” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 2: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. T_a is common to conditions 2 and 3.

Item		Min.	Typ.	Max.	Unit	Test Conditions
Resolution		12	12	12	Bit	
Conversion time*1 (ADCLK = 50 MHz)	Without 0.1-µF external capacitor Permissible signal source impedance (max.) = 1.0 kΩ	1.0	—	—	µs	Sampling in 20 states
Analog input capacitance		—	—	6	pF	
Sample and hold circuit in use	Integral nonlinearity error	—	—	±6.0	LSB	AVin = 0.25 to AV_{REFH}–0.25
	Offset error	—	—	±6.0	LSB	
	Full-scale error	—	—	±6.0	LSB	
	Quantization error	—	±0.5	—	LSB	
	Absolute accuracy	—	—	±8.0	LSB	
Sample and hold circuit not in use	Integral nonlinearity error	—	—	±3.0	LSB	AVin = AV_{REFL} to AV_{REFH}
	Offset error	—	—	±3.0	LSB	
	Full-scale error	—	—	±3.0	LSB	
	Quantization error	—	±0.5	—	LSB	
	Absolute accuracy	—	—	±6.0	LSB	

Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Table 5.24 Comparator Characteristics

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Analog input capacitance	C_{in}	—	—	8	pF	
REFH pin offset voltage	V_{off}	—	—	5	mV	
REFL pin offset voltage		—	—	5	mV	
REFH input voltage range	V_{in}	1.7	—	AVcc – 0.3	V	
REFL input voltage range		0.3	—	AVcc – 1.7	V	
REFH reply time	t_{CR}	—	—	500	ns	VI = VREF±25mV
REFL reply time	t_{CF}	—	—	500	ns	

Table 5.27 Power-on Reset Circuit and Voltage Detection Circuit Characteristics (2)

Condition: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0
$T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	V_{POR}	3.6	3.8	4.0	V	Figure 5.41
	Voltage detection circuit (LVD0)	V_{DET0}	4.0	4.2	4.4		Figure 5.42
	Voltage detection circuit (LVD1)*1	V_{DET1_8}	4.59	4.77	4.95		Figure 5.43
		V_{DET1_9}	4.05	4.23	4.41		
		V_{DET1_A}	4.32	4.50	4.68		
	Voltage detection circuit (LVD2)*2	V_{DET2_8}	4.59	4.77	4.95		Figure 5.44
		V_{DET2_9}	4.05	4.23	4.41		
		V_{DET2_A}	4.32	4.50	4.68		
Internal reset time	Power-on reset (POR)	t_{POR}		9.7		ms	Figure 5.41
	Voltage detection circuit (LVD0)	t_{LVD0}		9.7			Figure 5.42
	Voltage detection circuit (LVD1)	t_{LVD1}		0.9			Figure 5.43
	Voltage detection circuit (LVD2)	t_{LVD2}		0.9			Figure 5.44
Minimum VCC down time*3		t_{VOFF}	200	—	—	µs	Figure 5.41 to Figure 5.44
Response delay time		t_{DET}			200	µs	
LVD operation stabilization time (after LVD is enabled)		$Td_{(E-A)}$			3	µs	Figure 5.41 to Figure 5.44
Hysteresis width (LVD1 and LVD2)		V_{LVH}		80		mV	

Note 1. # in symbol $V_{DET1\_\#}$ indicates the value of the LVDLVLR.LVD1LVL[3:0] bits.
Note 2. # in symbol $V_{DET2\_\#}$ indicates the value of the LVDLVLR.LVD2LVL[3:0] bits.
Note 3. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{DET1}, and V_{DET2} for the POR/ LVD.

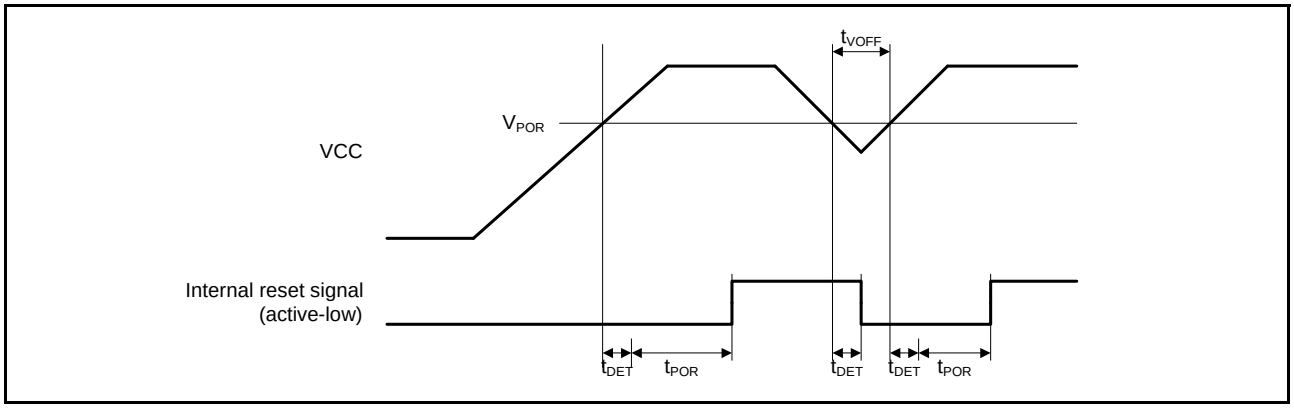

Figure 5.39 Power-on Reset Timing

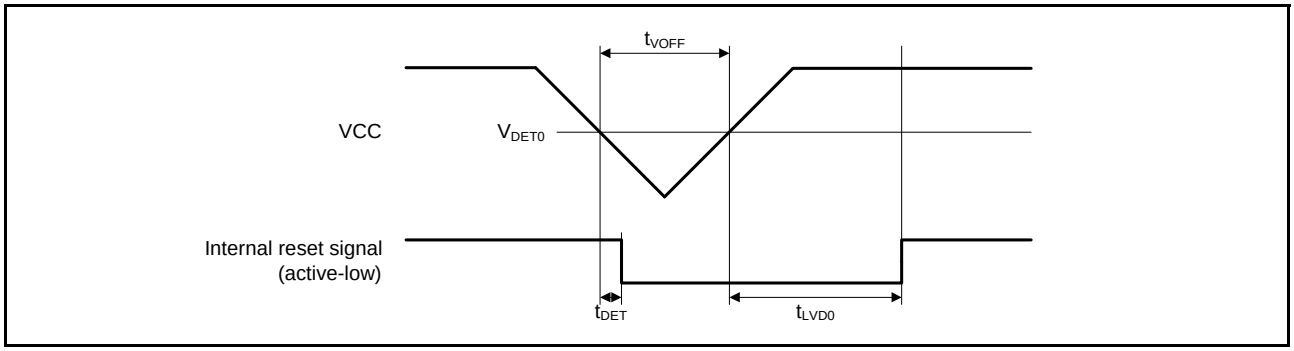

Figure 5.40 Voltage Detection Circuit Timing (V_{DET0})

6.3 AC Characteristics

Table 6.6 Operation Frequency Value

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item		Symbol	Min.	Typ	Max.	Unit
Operation frequency	System clock (ICLK)	f	—	—	100	MHz
	Peripheral module clock PCLK		—	—	50	
	Timer module clock (PCLKA)		—	—	100	
	S12AD clock (PCLKD)		—	—	50	
	Flash clock (FCLK)		—*1	—	50	

Note 1. The FCLK must run at a frequency of at least 4 MHz when changing the ROM or E2 DataFlash memory contents.

6.3.1 Clock Timing

Table 6.7 Clock Timing

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item		Symbol	Min	Typ	Max.	Unit	Test Conditions
EXTAL external clock input cycle time		t_{EXcyc}	50	—	—	ns	Figure 6.1
EXTAL external clock input high pulse width		t_{EXH}	20	—	—	ns	
EXTAL external clock input low pulse width		t_{EXL}	20	—	—	ns	
EXTAL external clock rising time		t_{EXr}	—	—	5	ns	
EXTAL external clock falling time		t_{EXf}	—	—	5	ns	
EXTAL external clock input wait time*1		t_{EXWT}	1	—	—	ms	
Main clock oscillator oscillation frequency		f_{MAIN}	4	—	16	MHz	
Main clock oscillation stabilization time (crystal)		$t_{MAINOSC}$	—	—	—*2	ms	Figure 6.2
Main clock oscillation stabilization wait time (crystal)		$t_{MAINOSCWT}$	—	—	—*3	ms	
LOCO, IWDTCLK clock cycle time		t_{cyc}	6.96	8	9.4	µs	
LOCO, IWDTCLK clock oscillation frequency		f_{LOCO}	106.25	125	143.75	kHz	
LOCO, IWDTCLK clock oscillation stabilization wait time		t_{LOCOWT}	—	—	20	µs	Figure 6.2
PLL clock oscillation stabilization time	PLL operation started after main clock oscillation has settled	t_{PLL1}	—	—	500	µs	Figure 6.4
PLL clock oscillation stabilization wait time		t_{PLLWT1}	—	—	—*4	ms	
PLL clock oscillation stabilization time PLL	PLL operation started before main clock oscillation has settled	t_{PLL2}	—	—	$t_{MAINOSC}$ + t_{PLL1}	ms	Figure 6.5
PLL clock oscillation stabilization wait time		t_{PLLWT2}	—	—	—*4	ms	

Note 1. This is the time until the clock is used after clearing the main clock oscillator stop bit (MOSCCR.MOSTP) to 0 (selecting operation).
Note 2. When using a main clock, ask the manufacturer of the oscillator to evaluate its oscillation. Refer to the results of evaluation provided by the manufacturer for the oscillation stabilization time.
Note 3. This is calculated from the formula below, where n is the number of cycles set by the MOSCWTCR.MSTS[4:0] bits.

$$t_{MAINOSCWT} = t_{MAINOSC} + \frac{n + 16384}{f_{MAIN}}$$

Table 6.15 Timing of On-Chip Peripheral Modules (5)

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item		Symbol	Min.*1, *2	Max.	Unit	Test Conditions
Simple IIC (Standard-mode)	SCL, SDAinput rise time	t_{Sr}	—	1000	ns	Figure 6.25
	SCL, SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	4 × t_{IICcyc}	ns	
	Data input setup time	t_{SDAS}	250	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
Simple IIC (Fast-mode)	SCL, SDA input rise time	t_{Sr}	20 + 0.1C_b	300	ns	
	SCL, SDA input fall time	t_{Sf}	20 + 0.1C_b	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	4 × t_{IICcyc}	ns	
	Data input setup time	t_{SDAS}	100	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note 1. The value in parentheses is used when ICMR3.NF[1:0] are set to 11b while a digital filter is enabled with ICFER.NFE = 1.
Note 2. Cb indicates the total capacity of the bus line.

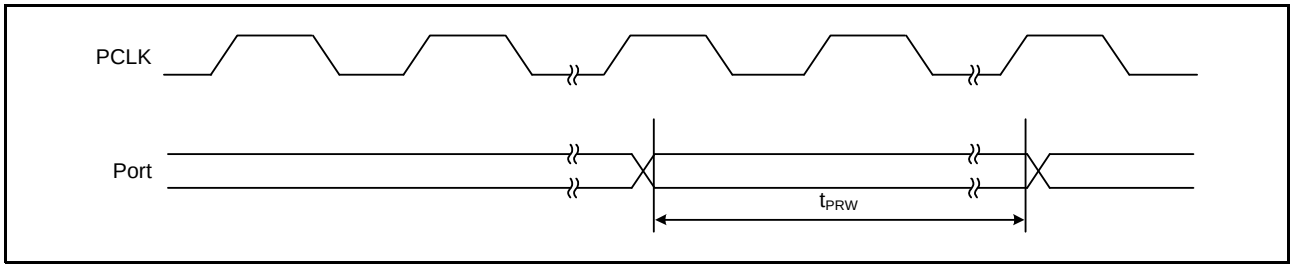

Figure 6.12 I/O port Input Timing

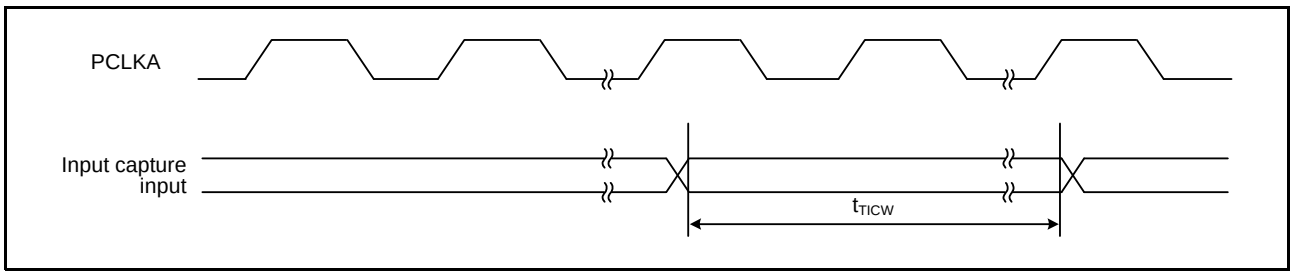

Figure 6.13 MTU3 Input/Output Timing

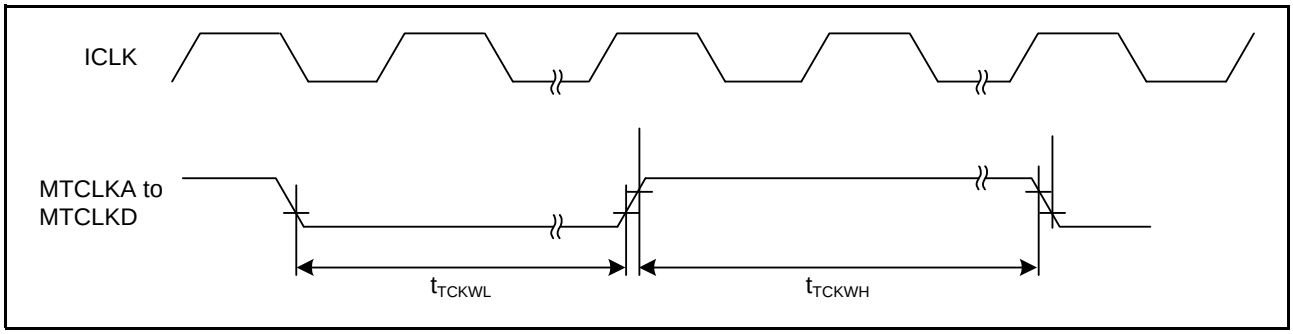

Figure 6.14 MTU3 Clock Input Timing

6.8 E^2 DataFlash Characteristic

Table 6.22 E^2 DataFlash (Flash Memory for Data Storage) Characteristics (1)

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0
Temperature range for the programming/erasure operation: $T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Reprogram/erase cycle*1	N_{DPEC}	100000	—	—	Times	
Data hold time	t_{DDRP}	30*2	—	—	Year	Ta = +85°C

Note 1. Definition of reprogram/erase cycle:
The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 128-byte programming is performed 16 times for different addresses in 2-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).
Note 2. The value is obtained from the reliability test.

Table 6.23 E^2 DataFlash (Flash Memory for Data Storage) Characteristics (2)

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item		Symbol	min	typ	max	Unit	Test Condition
Programming time	2 bytes	t_{DP2}	—	0.25	2	ms	FCLK = 50 MHz
Erasure time	32 bytes	t_{DE32}	—	2	20	ms	FCLK = 50 MHz $N_{DPEC} \leq 100$
	32 bytes	t_{DE32}	—	4	20	ms	FCLK = 50 MHz $N_{DPEC} > 100$
Blank check time	2 bytes	t_{DBC2}	—	—	30	µs	FCLK = 50 MHz
Suspend delay time during programming		t_{DSPD}	—	—	120	µs	Figure 6.31 PCLKB = 50 MHz
First suspend delay time during erasing (in suspend priority mode)		t_{DSESD1}	—	—	120	µs	
Second suspend delay time during erasing (in suspend priority mode)		t_{DSESD2}	—	—	300	µs	
Suspend delay time during erasing (in erasure priority mode)		t_{DSEED}	—	—	300	µs	