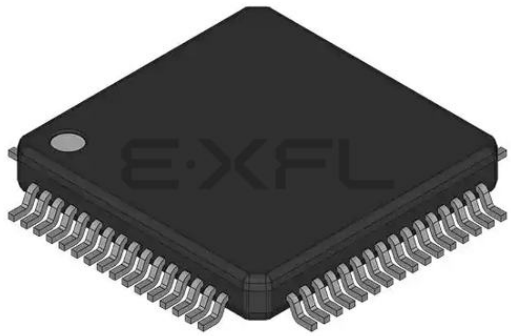
Renesas Electronics America Inc - R5F563T6EDFM#V0 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	39
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f563t6edfm-v0

Table 1.1 Outline of Specifications (4/7)

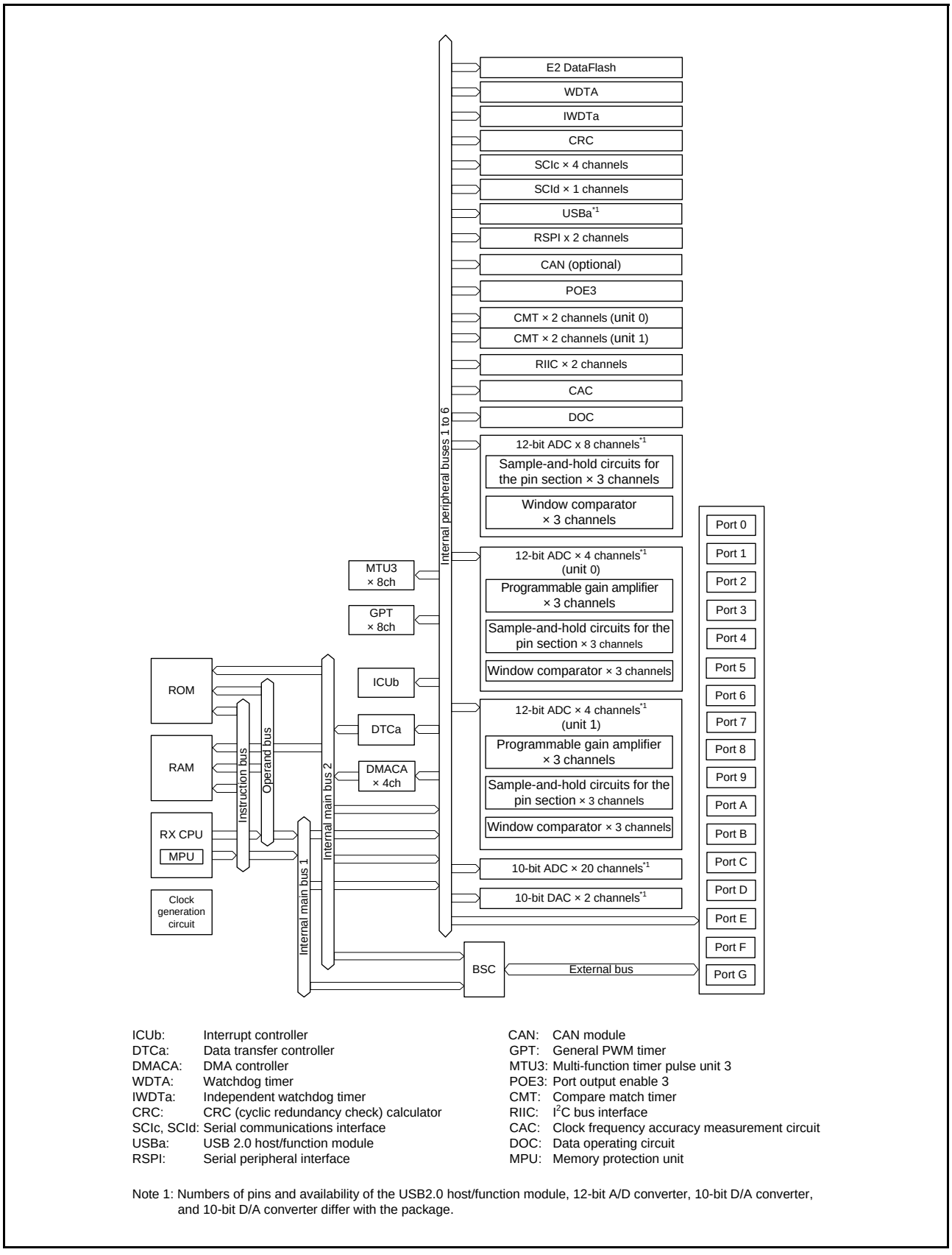
Classification	Module/Function	Description
Timers	General PWM timer (GPT)	• 16 bits x 8 channels • Counting up or down (saw-wave), counting up and down (triangle-wave) selectable for all channels • Select from among four count clocks (PCLKA/1, PCLKA/4, PCLKA/8, and PCLKA/16) for each channel • 2 input/output pins per channel • 2 output compare/input capture registers per channel • For the 2 output compare/input capture registers of each channel, 4 registers are provided as buffer registers and are capable of operating as comparison registers when buffering is not in use. • In output compare operation, buffer switching can be at peaks or troughs, enabling the generation of laterally asymmetrically PWM waveforms. • Registers for setting up frame intervals on each channel (with capability for generating interrupts on overflow or underflow) • Synchronizable operation of the several counters • Modes of synchronized operation (synchronized, or displaced by desired times for phase shifting) • Generation of dead times in PWM operation • Through combination of three counters, generation of automatic three-phase PWM waveforms incorporating dead times • Starting, clearing, and stopping counters in response to external or internal triggers • Internal trigger sources: Output of the internal comparator detection, software, and compare-match • The main clock can be used as a counter clock for measuring the timing of the edges of signals produced by frequency-dividing the dedicated clock signal for the IWDT (to detect abnormal oscillation). • A PWM delay with an accuracy of up to 1/32 times the period of the system clock (ICLK) can be generated to control the timing with which signals from the two PWM output pins from each of channels 0 to 3 rise and fall.
	Compare match timer (CMT)	• (16 bits × 2 channels) × 2 units • Select from among four internal clock signals (PCLK/8, PCLK/32, PCLK/128, PCLK/512)
	Watchdog timer (WDTA)	• 14 bits × 1 channel • Select from among 6 counter-input clock signals (PCLK/4, PCLK/64, PCLK/128, PCLK/512, PCLK/2048, PCLK/8192)
	Independent watchdog timer (IWDTa)	• 14 bits × 1 channel • Counter-input clock: Dedicated on-chip oscillator • Dedicated clock/1, dedicated clock/16, dedicated clock/32, dedicated clock/64, dedicated clock/128, dedicated clock/256
Communication function	USB 2.0 host/function module (USBa)	• Includes a UDC (USB Device Controller) and transceiver for USB 2.0 • Single port • Compliance with the USB 2.0 specification • Transfer rate: Full speed (12 Mbps) • Self-power mode and bus power mode are selectable • Supports the OTG (On-The-Go) • Incorporates 2 Kbytes of RAM as a transfer buffer
	Serial communications interfaces (SCIc, SCId)	• 5 channels (SCIc: 4 channels + SCId: 1 channel) • SCIc Serial communications modes: Asynchronous, clock synchronous, and smart-card interface Multi-processor function On-chip baud rate generator allows selection of the desired bit rate Choice of LSB-first or MSB-first transfer Simple I^2C Simple SPI • SCId (The following functions are added to SCIc) Supports the serial communications protocol, which contains the start frame and information frame Supports the LIN format

Table 1.1 Outline of Specifications (6/7)

Classification Module/Function	Description
12-bit A/D converter (S12ADB) [64- and 48-pin versions]	• 12 bits (8 channels x 1 unit) • 12-bit resolution • Conversion time 1.0 µs per channel (S12ADB clock: PCLKD (A/D conversion clock: ADCLK) = 50 MHz • Operating modes Scan mode (single scan mode / continuous scan mode / group scan mode) Group A priority control (group scan mode only) • Sample-and-hold function A common sample-and-hold circuit for units is included Separate sample-and-hold circuits are also included (three channels per unit) • Self-diagnosis function Three analog input voltages (VREFL0, VREFH0 × 1/2, VREFH0) can be generated internally by the self-diagnosis function. • Double trigger mode (double the results of A/D conversion) • Three ways to start A/D conversion Conversion can be started by software, a conversion start trigger from a timer (MTU3 or GPT), or an external trigger signal. • Window comparators (three channels per unit)
10-bit A/D converter (ADA)	10 bits (20 channels × 1 unit) • 10-bit resolution • Conversion time 0.5 µs per channel (A/D conversion clock ADCLK = 100 MHz) • Two operating modes Single mode, scan mode • Scan mode Single-cycle scan mode Continuous scan mode • Sample-and-hold function A common sample-and-hold circuit for units is included • Three ways to start A/D conversion Conversion can be started by software, a conversion start trigger from a timer (MTU3 or GPT), or an external trigger signal. • 8-bit precision output 2-bit right shifting for output of conversion results is selectable. • Self-diagnostic function The self-diagnostic function internally generates three analog input voltages (AVSS, VREF x 1/2, VREF)
D/A converter (DAa)	• 2 channels • 10-bit resolution • Output voltage: 0 V to VREF
CRC calculator (CRC)	• CRC code generation for arbitrary amounts of data in 8-bit units • Select any of three generating polynomials: $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$. • Generation of CRC codes for use with LSB-first or MSB-first communications is selectable
Data operating circuit (DOC)	• Comparison, addition, and subtraction of 16-bit data
Digital power supply controller (DPC)	• Control parameters calculation unit of the digital switch-mode power supply systems. • Adopt robust control algorithm with high control stability • Results of measurement by the 10-bit A/D converter can be used in calculating the control parameters.
Operating frequency	Up to 100 MHz
Power supply voltage [144-, 120-, 112- and 100-pin versions]	• 3-V product VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V AVCC0 = AVCC = VREF = 3.0 to 3.6 V, or 4.0 to 5.5 V VREFH0 = 3.0 to AVCC0, or 4.0 to AVCC0 • 5-V product VCC = PLLVCC = 4.0 to 5.5 V VCC_USB = 3.0 to 3.6 V AVCC0 = AVCC = VREF = 4.0 to 5.5 V VREFH0 = 4.0 to AVCC0
Power supply voltage [64- and 48-pin versions]	VCC = 2.7 to 3.6 V, AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

1.3 Block Diagram

Figure 1.2 shows a block diagram.



ICUb: Interrupt controller
DTCa: Data transfer controller
DMACA: DMA controller
WDTA: Watchdog timer
IWDTa: Independent watchdog timer
CRC: CRC (cyclic redundancy check) calculator
SCIc, SCId: Serial communications interface
USBa: USB 2.0 host/function module
RSPI: Serial peripheral interface
CAN: CAN module
GPT: General PWM timer
MTU3: Multi-function timer pulse unit 3
POE3: Port output enable 3
CMT: Compare match timer
RIIC: I^2C bus interface
CAC: Clock frequency accuracy measurement circuit
DOC: Data operating circuit
MPU: Memory protection unit

Note 1: Numbers of pins and availability of the USB2.0 host/function module, 12-bit A/D converter, 10-bit D/A converter, and 10-bit D/A converter differ with the package.

Figure 1.2 Block Diagram

Table 1.4 Pin Functions (2/5)

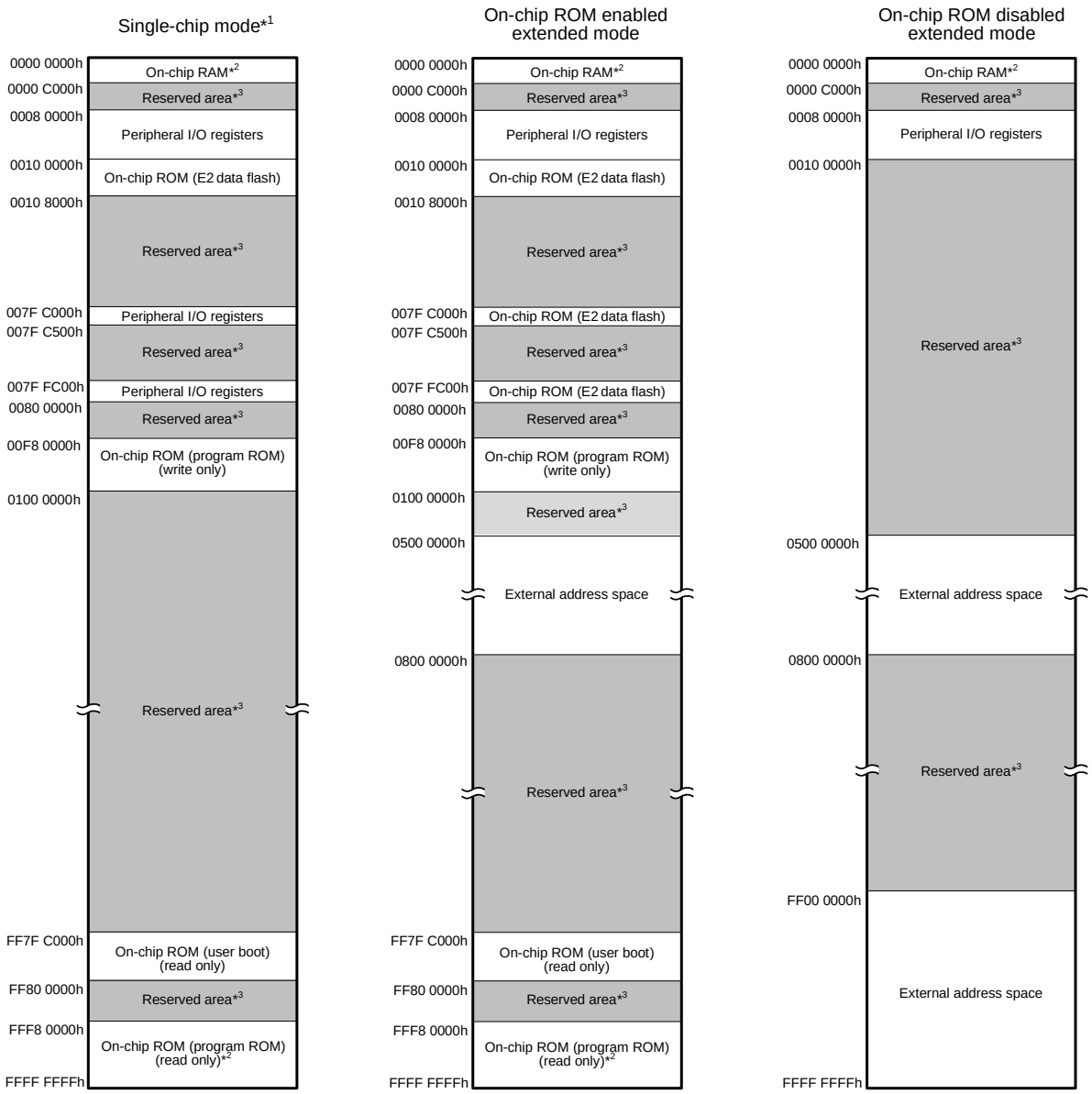
Classifications	Pin Name	I/O	Description
Interrupt	NMI	Input	Non-maskable interrupt request pin
	IRQ0 to IRQ7	Input	Maskable interrupt request pin
Multi-function timer pulse unit 3	MTIOC0A, MTIOC0B MTIOC0C, MTIOC0D	I/O	The TGRA0 to TGRD0 input capture input/output compare output/ PWM output pins
	MTIOC1A, MTIOC1B	I/O	The TGRA1 and TGRB1 input capture input/output compare output/ PWM output pins
	MTIOC2A, MTIOC2B	I/O	The TGRA2 and TGRB2 input capture input/output compare output/ PWM output pins
	MTIOC3A, MTIOC3B MTIOC3C, MTIOC3D	I/O	The TGRA3 to TGRD3 input capture input/output compare output/ PWM output pins
	MTIOC4A, MTIOC4B MTIOC4C, MTIOC4D	I/O	The TGRA4 to TGRD4 input capture input/output compare output/ PWM output pins
	MTIC5U, MTIC5V MTIC5W	Input	The TGRU5, TGRV5, and TGRW5 input capture input/dead time compensation input pins
	MTIOC6A, MTIOC6B MTIOC6C, MTIOC6D	I/O	The TGRA6 to TGRD6 input capture input/output compare output/ PWM output pins
	MTIOC7A, MTIOC7B MTIOC7C, MTIOC7D	I/O	The TGRA7 to TGRD7 input capture input/output compare output/ PWM output pins
	MTCLKA, MTCLKB MTCLKC, MTCLKD	Input	Input pins for external clock
Port output enable 3	POE0#, POE4# POE8#, POE10# POE11#, POE12#	Input	Input pins for request signals to place the MTU/GPT large-current pins in the high impedance state
General PWM timer	GTIOC0A, GTIOC0B	I/O	The GPT0.GTGRA and GPT0.GTGRB input capture input/output compare output/PWM output pins.
	GTIOC1A, GTIOC1B	I/O	The GPT1.GTGRA and GPT1.GTGRB input capture input/output compare output/PWM output pins.
	GTIOC2A, GTIOC2B	I/O	The GPT2.GTGRA and GPT2.GTGRB input capture input/output compare output/PWM output pins.
	GTIOC3A, GTIOC3B	I/O	The GPT3.GTGRA and GPT3.GTGRB input capture input/output compare output/PWM output pins.
	GTETRG0	Input	External trigger input pin for the GPT0 to GPT3
	GTIOC4A, GTIOC4B	I/O	The GPT4.GTGRA and GPT4.GTGRB input capture input/output compare output/PWM output pins.
	GTIOC5A, GTIOC5B	I/O	The GPT5.GTGRA and GPT5.GTGRB input capture input/output compare output/PWM output pins.
	GTIOC6A, GTIOC6B	I/O	The GPT6.GTGRA and GPT6.GTGRB input capture input/output compare output/PWM output pins.
	GTIOC7A, GTIOC7B	I/O	The GPT7.GTGRA and GPT7.GTGRB input capture input/output compare output/PWM output pins.
	GTETRG1	Input	External trigger input pin for the GPT4 to GPT7

Table 1.6 List of Pins and Pin Functions (120-Pin LQFP) (2/4)

Pin Number 120-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3, GPT, POE3, CAC)	Communications (SCIc, SCId, RSPI, RIIC, CAN, USB)	Interrupt	S12ADB, AD, DA
37	PLLVSS						
38		PB3	A15	MTIOC0A/CACREF	SCK0		
39		PB2		MTIOC0B	TXD0/SMOSI0/ SSDA0/SDA0		
40		PB1		MTIOC0C	RXD0/SMISO0/ SSCL0/SCL0	IRQ4	
41		PB0	A14	MTIOC0D	MOSIA/MOSIB		
42		PA5		MTIOC1A	RXD0/SMISO0/ SSCL0/ MISOA/MISOB		ADTRG1#
43		PA4		MTIOC1B	TXD0/SMOSI0/ SSDA0/RSPCKA/ RSPCKB		ADTRG0#
44		PA3		MTIOC2A	SCK0/SSLA0/SSLB0		
45		PA2		MTIOC2B	RXD2/SMISO2/ SSCL2/ SSLA1/SSLB1		
46		PA1		MTIOC6A	TXD2/SMOSI2/ SSDA2/SSLA2/SSLB2		
47		PA0		MTIOC6C	SCK2/SSLA3/SSLB3		
48	VCC						
49		P96	A13	POE4#	RXD1/SMISO1/SSCL1	IRQ4-DS	
50		PG6	CS2#		SCK1		
51	VSS						
52		P95		MTIOC6B/GTIOC4A	TXD1/SMOSI1/SSDA1		
53		P94		MTIOC7A/GTIOC5A	CTS1#/RTS1#/SS1#		
54		P93		MTIOC7B/GTIOC6A	CTS2#/RTS2#/SS2#		
55		P92		MTIOC6D/GTIOC4B			
56		P91		MTIOC7C/GTIOC5B			
57		P90		MTIOC7D/GTIOC6B			
58	TRCLK	PG5		POE12#	SCK3		ADTRG#
59	TRDATA3	PG4		GTIOC6B	RXD3/SMISO3/SSCL3	IRQ6	
60	TRDATA2	PG3		GTIOC6A	TXD3/SMOSI3/SSDA3		
61	TRDATA1	PG2			SCK2	IRQ2	
62	TRDATA0	PG1		GTIOC7B	RXD2/SMISO2/SSCL2	IRQ1	
63	TRSYNC	PG0		GTIOC7A	TXD2/SMOSI2/SSDA2	IRQ0	
64		P76	D0/[A0/D0]	MTIOC4D/GTIOC2B			
65		P75	D1/[A1/D1]	MTIOC4C/GTIOC1B			
66		P74	D2/[A2/D2]	MTIOC3D/GTIOC0B			
67		P73	D3/[A3/D3]	MTIOC4B/GTIOC2A			
68		P72	D4/[A4/D4]	MTIOC4A/GTIOC1A			
69		P71	D5/[A5/D5]	MTIOC3B/GTIOC0A			
70		P70	D6/[A6/D6]	POE0#	CTS1#/RTS1#/SS1#	IRQ5-DS	
71		P33	D7/[A7/D7]	MTIOC3A/MTCLKA	SSLA3/SSLB3		
72		P32	D8/[A8/D8]	MTIOC3C/MTCLKB	SSLA2/SSLB2		
73	VCC						
74		P31	D9/[A9/D9]	MTIOC0A/MTCLKC	SSLA1/SSLB1		

Table 1.8 List of Pins and Pin Functions (100-Pin LQFP) (2/3)

Pin Number 100-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3, GPT, POE3, CAC)	Communications (SCIc, SCId, RSPI, RIIC, CAN)	Interrupt	S12ADB, AD, DA
37		PA4		MTIOC1B	TXD0/SMOSI0/ SSDA0/ RSPCKA/RSPCKB		ADTRG0#
38		PA3		MTIOC2A	SCK0/SSLA0/SSLB0		
39		PA2		MTIOC2B	RXD2/SMISO2/ SSCL2/ SSLA1/SSLB1		
40		PA1		MTIOC6A	TXD2/SMOSI2/ SSDA2/ SSLA2/SSLB2		
41		PA0		MTIOC6C	SCK2/SSLA3/SSLB3		
42	VCC						
43		P96	A13	POE4#	RXD1/SMISO1/SSCL1	IRQ4-DS	
44	VSS						
45		P95		MTIOC6B/GTIOC4A	TXD1/SMOSI1/SSDA1		
46		P94		MTIOC7A/GTIOC5A	CTS1#/RTS1#/SS1#		
47		P93		MTIOC7B/GTIOC6A	CTS2#/RTS2#/SS2#		
48		P92		MTIOC6D/GTIOC4B			
49		P91		MTIOC7C/GTIOC5B			
50		P90		MTIOC7D/GTIOC6B			
51		P76	D0/[A0/D0]	MTIOC4D/GTIOC2B			
52		P75	D1/[A1/D1]	MTIOC4C/GTIOC1B			
53		P74	D2/[A2/D2]	MTIOC3D/GTIOC0B			
54		P73	D3/[A3/D3]	MTIOC4B/GTIOC2A			
55		P72	D4/[A4/D4]	MTIOC4A/GTIOC1A			
56		P71	D5/[A5/D5]	MTIOC3B/GTIOC0A			
57		P70	D6/[A6/D6]	POE0#	CTS1#/RTS1#/SS1#	IRQ5-DS	
58		P33	D7/[A7/D7]	MTIOC3A/MTCLKA	SSLA3/SSLB3		
59		P32	D8/[A8/D8]	MTIOC3C/MTCLKB	SSLA2/SSLB2		
60	VCC						
61		P31	D9/[A9/D9]	MTIOC0A/MTCLKC	SSLA1/SSLB1		
62	VSS						
63		P30	D10/[A10/ D10]	MTIOC0B/MTCLKD	SCK0/SSLA0/SSLB0		
64		P24	D11/[A11/D11]		CTS0#/RTS0#/SS0#/ RSPCKA/RSPCKB	IRQ4	
65		P23	D12/[A12/ D12]	CACREF	TXD0/SMOSI0/ SSDA0/MOSIA/ MOSIB/CTX1		
66		P22	D13/[A13/ D13]		RXD0/SMISO0/ SSCL0/MISOA/ MISOB/CRX1		ADTRG#
67		P21	D14/[A14/ D14]	MTCLKA		IRQ6-DS	ADTRG1#
68		P20	D15/[A15/ D15]	MTCLKB		IRQ7-DS	ADTRG0#
69		P65	A0/BC0#				AN5
70		P64	A1				AN4



Note 1. The address space in boot mode and user boot mode is the same as the address space in single-chip mode.
Note 2. The capacity of ROM/RAM differs depending on the products.

ROM (bytes)		RAM (bytes)		E2 DataFlash (bytes)	
Capacity	**Address**	**Capacity**	**Address**	**Capacity**	**Address**
512 K	FFF8 0000h to FFFF FFFFh	48 K	0000 0000h to 0000 BFFFh	32 K	0010 0000h to 0010 8000h
384 K	FFFA 0000h to FFFF FFFFh	32 K	0000 0000h to 0000 7FFFh		
256 K	FFFC 0000h to FFFF FFFFh	24 K	0000 0000h to 0000 5FFFh		
64 K	FFFF 0000h to FFFF FFFFh	8 K	0000 0000h to 0000 1FFFh	8 K	0010 0000h to 0010 2000h
48 K	FFFF 4000h to FFFF FFFFh				
32 K	FFFF 8000h to FFFF FFFFh				

Note:•See Table 1.3, List of Products, for the product type name.

Note 3. Reserved areas should not be accessed.
Note 4. For details on the FCU, see section 41, Flash Memory in the User's Manual: Hardware.

Figure 3.1 Memory Map in Each Operating Mode

4.1 I/O Register Addresses (Address Order)

Table 4.1 List of I/O Registers (Address Order) (1/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 0000h	SYSTEM	Mode Monitor Register	MDMONR	16	16	3 ICLK		Operating Modes	
0008 0002h	SYSTEM	Mode Status Register	MDSR	16	16	3 ICLK			Not present in versions with 64 or 48 pins.
0008 0006h	SYSTEM	System Control Register 0	SYSCR0	16	16	3 ICLK			
0008 0008h	SYSTEM	System Control Register 1	SYSCR1	16	16	3 ICLK			
0008 000Ch	SYSTEM	Standby Control Register	SBYCR	16	16	3 ICLK		Low Power Consumption	
0008 0010h	SYSTEM	Module Stop Control Register A	MSTPCRA	32	32	3 ICLK			
0008 0014h	SYSTEM	Module Stop Control Register B	MSTPCRB	32	32	3 ICLK			
0008 0018h	SYSTEM	Module Stop Control Register C	MSTPCRC	32	32	3 ICLK			
0008 0020h	SYSTEM	System Clock Control Register	SCKCR	32	32	3 ICLK		Clock Generation Circuit	
0008 0024h	SYSTEM	System Clock Control Register 2	SCKCR2	16	16	3 ICLK			Not present in versions with 64 or 48 pins.
0008 0026h	SYSTEM	System Clock Control Register 3	SCKCR3	16	16	3 ICLK			
0008 0028h	SYSTEM	PLL Control Register	PLLCR	16	16	3 ICLK			
0008 002Ah	SYSTEM	PLL Control Register 2	PLLCR2	8	8	3 ICLK			
0008 0030h	SYSTEM	External Bus Clock Control Register	BCKCR	8	8	3 ICLK			Not present in versions with 64 or 48 pins.
0008 0032h	SYSTEM	Main Clock Oscillator Control Register	MOSCCR	8	8	3 ICLK			
0008 0034h	SYSTEM	Low-Speed On-Chip Oscillator Control Register	LOCOCR	8	8	3 ICLK			
0008 0035h	SYSTEM	IWDT-Dedicated On-Chip Oscillator Control Register	ILOCOCR	8	8	3 ICLK			
0008 0040h	SYSTEM	Oscillation Stop Detection Control Register	OSTDCR	8	8	3 ICLK			
0008 0041h	SYSTEM	Oscillation Stop Detection Status Register	OSTDSR	8	8	3 ICLK			
0008 00A2h	SYSTEM	Main Clock Oscillator Wait Control Register	MOSCWTCR	8	8	3 ICLK		Low Power Consumption	
0008 00A6h	SYSTEM	PLL Wait Control Register	PLLWTCR	8	8	3 ICLK			
0008 00C0h	SYSTEM	Reset Status Register 2	RSTSR2	8	8	3 ICLK		Resets	
0008 00C2h	SYSTEM	Software Reset Register	SWRR	16	16	3 ICLK			
0008 00E0h	SYSTEM	Voltage Monitoring 1 Circuit Control Register 1	LVD1CR1	8	8	3 ICLK		LVDA	
0008 00E1h	SYSTEM	Voltage Monitoring 1 Circuit Status Register	LVD1SR	8	8	3 ICLK			
0008 00E2h	SYSTEM	Voltage Monitoring 2 Circuit Control Register 1	LVD2CR1	8	8	3 ICLK			
0008 00E3h	SYSTEM	Voltage Monitoring 2 Circuit Status Register	LVD2SR	8	8	3 ICLK			
0008 03FEh	SYSTEM	Protect Register	PRCR	16	16	3 ICLK		Register Write Protection Function	
0008 1300h	BSC	Bus Error Status Clear Register	BERCLR	8	8	2 ICLK		Buses	
0008 1304h	BSC	Bus Error Monitoring Enable Register	BEREN	8	8	2 ICLK			
0008 1308h	BSC	Bus Error Status Register 1	BERSR1	8	8	2 ICLK			
0008 130Ah	BSC	Bus Error Status Register 2	BERSR2	16	16	2 ICLK			
0008 1310h	BSC	Bus Priority Control Register	BUSPRI	16	16	2 ICLK			
0008 2000h	DMAC0	DMA Source Address Register	DMSAR	32	32	2 ICLK		DMACA	
0008 2004h	DMAC0	DMA Destination Address Register	DMDAR	32	32	2 ICLK			
0008 2008h	DMAC0	DMA Transfer Count Register	DMCRA	32	32	2 ICLK			
0008 200Ch	DMAC0	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK			
0008 2010h	DMAC0	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK			
0008 2013h	DMAC0	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK			
0008 2014h	DMAC0	DMA Address Mode Register	DMAMD	16	16	2 ICLK			
0008 2018h	DMAC0	DMA Offset Register	DMOFR	32	32	2 ICLK			
0008 201Ch	DMAC0	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK			
0008 201Dh	DMAC0	DMA Software Start Register	DMREQ	8	8	2 ICLK			
0008 201Eh	DMAC0	DMA Status Register	DMSTS	8	8	2 ICLK			

Table 4.1 List of I/O Registers (Address Order) (6/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 7098h	ICU	Interrupt Request Register 152	IR152	8	8	2 ICLK		ICUb	
0008 7099h	ICU	Interrupt Request Register 153	IR153	8	8	2 ICLK			
0008 709Ah	ICU	Interrupt Request Register 154	IR154	8	8	2 ICLK			
0008 709Bh	ICU	Interrupt Request Register 155	IR155	8	8	2 ICLK			
0008 709Ch	ICU	Interrupt Request Register 156	IR156	8	8	2 ICLK			
0008 709Dh	ICU	Interrupt Request Register 157	IR157	8	8	2 ICLK			
0008 709Eh	ICU	Interrupt Request Register 158	IR158	8	8	2 ICLK			
0008 70A1h	ICU	Interrupt Request Register 161	IR161	8	8	2 ICLK			
0008 70A2h	ICU	Interrupt Request Register 162	IR162	8	8	2 ICLK			
0008 70A3h	ICU	Interrupt Request Register 163	IR163	8	8	2 ICLK			
0008 70A4h	ICU	Interrupt Request Register 164	IR164	8	8	2 ICLK			
0008 70A5h	ICU	Interrupt Request Register 165	IR165	8	8	2 ICLK			
0008 70A6h	ICU	Interrupt Request Register 166	IR166	8	8	2 ICLK			
0008 70A7h	ICU	Interrupt Request Register 167	IR167	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70A8h	ICU	Interrupt Request Register 168	IR168	8	8	2 ICLK			
0008 70A9h	ICU	Interrupt Request Register 169	IR169	8	8	2 ICLK			
0008 70AAh	ICU	Interrupt Request Register 170	IR170	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70ABh	ICU	Interrupt Request Register 171	IR171	8	8	2 ICLK			
0008 70ACh	ICU	Interrupt Request Register 172	IR172	8	8	2 ICLK			
0008 70ADh	ICU	Interrupt Request Register 173	IR173	8	8	2 ICLK			
0008 70AEh	ICU	Interrupt Request Register 174	IR174	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70AFh	ICU	Interrupt Request Register 175	IR175	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70B0h	ICU	Interrupt Request Register 176	IR176	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70B1h	ICU	Interrupt Request Register 177	IR177	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70B2h	ICU	Interrupt Request Register 178	IR178	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70B3h	ICU	Interrupt Request Register 179	IR179	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70B4h	ICU	Interrupt Request Register 180	IR180	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70B5h	ICU	Interrupt Request Register 181	IR181	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70B6h	ICU	Interrupt Request Register 182	IR182	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70B7h	ICU	Interrupt Request Register 183	IR183	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70B8h	ICU	Interrupt Request Register 184	IR184	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70B9h	ICU	Interrupt Request Register 185	IR185	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70BAh	ICU	Interrupt Request Register 186	IR186	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70BBh	ICU	Interrupt Request Register 187	IR187	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70BCh	ICU	Interrupt Request Register 188	IR188	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70BDh	ICU	Interrupt Request Register 189	IR189	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70BEh	ICU	Interrupt Request Register 190	IR190	8	8	2 ICLK			Not present in versions with 112, 100, 64 or 48 pins.
0008 70BFh	ICU	Interrupt Request Register 191	IR191	8	8	2 ICLK			Not present in versions with 112, 100, 64 or 48 pins.

Table 4.1 List of I/O Registers (Address Order) (15/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 8308h	RIIC0	I²C Bus Status Register 1	ICSR1	8	8	2, 3 PCLKB	2 ICLK	RIIC	
0008 8309h	RIIC0	I²C Bus Status Register 2	ICSR2	8	8	2, 3 PCLKB	2 ICLK		
0008 830Ah	RIIC0	Slave Address Register L0	SARL0	8	8	2, 3 PCLKB	2 ICLK		
0008 830Ah	RIIC0	Timeout Internal Counter L	TMOCNTL	8	8	2, 3 PCLKB	2 ICLK		
0008 830Bh	RIIC0	Slave Address Register U0	SARU0	8	8	2, 3 PCLKB	2 ICLK		
0008 830Bh	RIIC0	Timeout Internal Counter U	TMOCNTU	8	8*2	2, 3 PCLKB	2 ICLK		
0008 830Ch	RIIC0	Slave Address Register L1	SARL1	8	8	2, 3 PCLKB	2 ICLK		
0008 830Dh	RIIC0	Slave Address Register U1	SARU1	8	8	2, 3 PCLKB	2 ICLK		
0008 830Eh	RIIC0	Slave Address Register L2	SARL2	8	8	2, 3 PCLKB	2 ICLK		
0008 830Fh	RIIC0	Slave Address Register U2	SARU2	8	8	2, 3 PCLKB	2 ICLK		
0008 8310h	RIIC0	I²C Bus Bit Rate Low-Level Register	ICBRL	8	8	2, 3 PCLKB	2 ICLK		
0008 8311h	RIIC0	I²C Bus Bit Rate High-Level Register	ICBRH	8	8	2, 3 PCLKB	2 ICLK		
0008 8312h	RIIC0	I²C Bus Transmit Data Register	ICDRT	8	8	2, 3 PCLKB	2 ICLK		
0008 8313h	RIIC0	I²C Bus Receive Data Register	ICDRR	8	8	2, 3 PCLKB	2 ICLK		
0008 8320h	RIIC1	I²C Bus Control Register 1	ICCR1	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
0008 8321h	RIIC1	I²C Bus Control Register 2	ICCR2	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
0008 8322h	RIIC1	I²C Bus Mode Register 1	ICMR1	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
0008 8323h	RIIC1	I²C Bus Mode Register 2	ICMR2	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
0008 8324h	RIIC1	I²C Bus Mode Register 3	ICMR3	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
0008 8325h	RIIC1	I²C Bus Function Enable Register	ICFER	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
0008 8326h	RIIC1	I²C Bus Status Enable Register	ICSER	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
0008 8327h	RIIC1	I²C Bus Interrupt Enable Register	ICIER	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
0008 8328h	RIIC1	I²C Bus Status Register 1	ICSR1	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
0008 8329h	RIIC1	I²C Bus Status Register 2	ICSR2	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
0008 832Ah	RIIC1	Slave Address Register L0	SARL0	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
0008 832Ah	RIIC1	Timeout Internal Counter L	TMOCNTL	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
0008 832Bh	RIIC1	Slave Address Register U0	SARU0	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
0008 832Bh	RIIC1	Timeout Internal Counter U	TMOCNTU	8	8*2	2, 3 PCLKB	2 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
0008 832Ch	RIIC1	Slave Address Register L1	SARL1	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
0008 832Dh	RIIC1	Slave Address Register U1	SARU1	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
0008 832Eh	RIIC1	Slave Address Register L2	SARL2	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
0008 832Fh	RIIC1	Slave Address Register U2	SARU2	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 112, 100, 64, or 48 pins.

Table 4.1 List of I/O Registers (Address Order) (17/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 83B2h	RSPI1	RSPI Command Register 1	SPCMD1	16	16	2, 3 PCLKB	2 ICLK	RSPI	Not present in versions with 64 or 48 pins.
0008 83B4h	RSPI1	RSPI Command Register 2	SPCMD2	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 83B6h	RSPI1	RSPI Command Register 3	SPCMD3	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 83B8h	RSPI1	RSPI Command Register 4	SPCMD4	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 83BAh	RSPI1	RSPI Command Register 5	SPCMD5	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 83BCh	RSPI1	RSPI Command Register 6	SPCMD6	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 83BEh	RSPI1	RSPI Command Register 7	SPCMD7	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9000h	S12AD	A/D Control Register	ADCSR	16	16	2, 3 PCLKB	2 ICLK	S12ADB	
0008 9004h	S12AD	A/D Channel Select Register A	ADANSA	16	16	2, 3 PCLKB	2 ICLK		
0008 9008h	S12AD	A/D-Converted Value Addition Mode Select Register	ADADS	16	16	2, 3 PCLKB	2 ICLK		
0008 900Ch	S12AD	A/D-Converted Value Addition Count Select Register	ADADC	8	8	2, 3 PCLKB	2 ICLK		
0008 900Eh	S12AD	A/D Control Extended Register	ADCER	16	16	2, 3 PCLKB	2 ICLK		
0008 9010h	S12AD	A/D Start Trigger Select Register	ADSTRGR	16	16	2, 3 PCLKB	2 ICLK		
0008 9014h	S12AD	A/D Channel Select Register B	ADANSB	16	16	2, 3 PCLKB	2 ICLK		
0008 9018h	S12AD	A/D Data-Doubling Register	ADDBLDR	16	16	2, 3 PCLKB	2 ICLK		
0008 901Eh	S12AD	A/D Self-Diagnosis Data Register	ADRD	16	16	2, 3 PCLKB	2 ICLK		
0008 9020h	S12AD	A/D Data Register 0	ADDR0	16	16	2, 3 PCLKB	2 ICLK		
0008 9022h	S12AD	A/D Data Register 1	ADDR1	16	16	2, 3 PCLKB	2 ICLK		
0008 9024h	S12AD	A/D Data Register 2	ADDR2	16	16	2, 3 PCLKB	2 ICLK		
0008 9026h	S12AD	A/D Data Register 3	ADDR3	16	16	2, 3 PCLKB	2 ICLK		
0008 9028h	S12AD	A/D Data Register 4	ADDR4	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 144, 120, 112, or 100 pins.
0008 902Ah	S12AD	A/D Data Register 5	ADDR5	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 144, 120, 112, or 100 pins.
0008 902Ch	S12AD	A/D Data Register 6	ADDR6	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 144, 120, 112, or 100 pins.
0008 902Eh	S12AD	A/D Data Register 7	ADDR7	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 144, 120, 112, or 100 pins.
0008 9060h	S12AD	A/D Sampling State Register 0	ADSSTR0	8	8	2, 3 PCLKB	2 ICLK		
0008 9066h	S12AD	A/D Sample and Hold Circuit Control Register	ADSHCR	16	16	2, 3 PCLKB	2 ICLK		
0008 9073h	S12AD	A/D Sampling State Register 1	ADSSTR1	8	8	2, 3 PCLKB	2 ICLK		
0008 9074h	S12AD	A/D Sampling State Register 2	ADSSTR2	8	8	2, 3 PCLKB	2 ICLK		
0008 9075h	S12AD	A/D Sampling State Register 3	ADSSTR3	8	8	2, 3 PCLKB	2 ICLK		
0008 9076h	S12AD	A/D Sampling State Register 4	ADSSTR4	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 144, 120, 112, or 100 pins.
0008 9077h	S12AD	A/D Sampling State Register 5	ADSSTR5	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 144, 120, 112, or 100 pins.
0008 9078h	S12AD	A/D Sampling State Register 6	ADSSTR6	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 144, 120, 112, or 100 pins.
0008 9079h	S12AD	A/D Sampling State Register 7	ADSSTR7	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 144, 120, 112, or 100 pins.
0008 9080h	S12AD	A/D Group Scan Priority Control Register	ADGSPCR	16	16	2, 3 PCLKB	2 ICLK		
0008 9084h	S12AD	A/D Data-Doubling Register A	ADDBLDRA	16	16	2, 3 PCLKB	2 ICLK		
0008 9086h	S12AD	A/D Data-Doubling Register B	ADDBLDRB	16	16	2, 3 PCLKB	2 ICLK		
0008 908Ah	S12AD	A/D Programmable Gain Amplifier Register	ADPG	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.

Table 4.1 List of I/O Registers (Address Order) (29/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0009 1840h	CAN1	Control Register	CTLR	16	8, 16	2, 3 PCLKB	2 ICLK	CAN	Not present in versions with 64 or 48 pins.
0009 1842h	CAN1	Status Register	STR	16	8, 16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0009 1844h	CAN1	Bit Configuration Register	BCR	32	8, 16, 32	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0009 1848h	CAN1	Receive FIFO Control Register	RFCR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0009 1849h	CAN1	Receive FIFO Pointer Control Register	RFPCR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0009 184Ah	CAN1	Transmit FIFO Control Register	TFCR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0009 184Bh	CAN1	Transmit FIFO Pointer Control Register	TFPCR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0009 184Ch	CAN1	Error Interrupt Enable Register	EIER	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0009 184Dh	CAN1	Error Interrupt Factor Judge Register	EIFR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0009 184Eh	CAN1	Receive Error Count Register	RECR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0009 184Fh	CAN1	Transmit Error Count Register	TECR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0009 1850h	CAN1	Error Code Store Register	ECSR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0009 1851h	CAN1	Channel Search Support Register	CSSR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0009 1852h	CAN1	Mailbox Search Status Register	MSSR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0009 1853h	CAN1	Mailbox Search Mode Register	MSMR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0009 1854h	CAN1	Time Stamp Register	TSR	16	8, 16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0009 1856h	CAN1	Acceptance Filter Support Register	AFSR	16	8, 16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0009 1858h	CAN1	Test Control Register	TCR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
000A 0000h	USB0	System Configuration Control Register	SYSCFG	16	16	3, 4 PCLKB	2, 3 ICLK	USBa	Not present in versions with 112, 100, 64, or 48 pins.
000A 0004h	USB0	System Configuration Status Register 0	SYSSTS0	16	16	9 PCLKB or more			Not present in versions with 112, 100, 64, or 48 pins.
000A 0008h	USB0	Device State Control Register 0	DVSTCTR0	16	16	9 PCLKB or more			Not present in versions with 112, 100, 64, or 48 pins.
000A 0014h	USB0	CFIFO Port Register	CFIFO	16	8, 16	3, 4 PCLKB	2, 3 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
000A 0018h	USB0	D0FIFO Port Registe	D0FIFO	16	8, 16	3, 4 PCLKB	2, 3 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
000A 001Ch	USB0	D1FIFO Port Register	D1FIFO	16	8, 16	3, 4 PCLKB	2, 3 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
000A 0020h	USB0	CFIFO Port Select Register	CFIFOSEL	16	16	3, 4 PCLKB	2, 3 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
000A 0022h	USB0	CFIFO Port Control Register	CFIFOCTR	16	16	3, 4 PCLKB	2, 3 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
000A 0028h	USB0	D0FIFO Port Select Register	D0FIFOSEL	16	16	3, 4 PCLKB	2, 3 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
000A 002Ah	USB0	D0FIFO Port Control Register	D0FIFOCTR	16	16	3, 4 PCLKB	2, 3 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
000A 002Ch	USB0	D1FIFO Port Select Register	D1FIFOSEL	16	16	3, 4 PCLKB	2, 3 ICLK		Not present in versions with 112, 100, 64, or 48 pins.

Table 4.1 List of I/O Registers (Address Order) (30/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
000A 002Eh	USB0	D1FIFO Port Control Register	D1FIFOCTR	16	16	3, 4 PCLKB	2, 3 ICLK	USBa	Not present in versions with 112, 100, 64, or 48 pins.
000A 0030h	USB0	Interrupt Enable Register 0	INTENB0	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 0032h	USB0	Interrupt Enable Register 1	INTENB1	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 0036h	USB0	BRDY Interrupt Enable Register	BRDYENB	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 0038h	USB0	NRDY Interrupt Enable Register	NRDYENB	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 003Ah	USB0	BEMP Interrupt Enable Register	BEMPENB	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 003Ch	USB0	SOF Output Configuration Register	SOFCFG	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 0040h	USB0	Interrupt Status Register 0	INTSTS0	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 0042h	USB0	Interrupt Status Register 1	INTSTS1	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 0046h	USB0	BRDY Interrupt Status Register	BRDYSTS	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 0048h	USB0	NRDY Interrupt Status Register	NRDYSTS	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 004Ah	USB0	BEMP Interrupt Status Register	BEMPSTS	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.

Table 4.1 List of I/O Registers (Address Order) (46/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
000C 2AA8h	GPT7	A/D Converter Start Request Timing Double-Buffer Register A	GTADTDBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK	GPT	Not present in versions with 64 or 48 pins.
000C 2AACh	GPT7	A/D Converter Start Request Timing Register B	GTADTRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2AAEh	GPT7	A/D Converter Start Request Timing Buffer Register B	GTADTBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2AB0h	GPT7	A/D Converter Start Request Timing Double-Buffer Register B	GTADTDBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2AB4h	GPT7	General PWM Timer Output Negate Control Register	GTONCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2AB6h	GPT7	General PWM Timer Dead Time Control Register	GTDTCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2AB8h	GPT7	General PWM Timer Dead Time Value Register U	GTDVU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2ABAh	GPT7	General PWM Timer Dead Time Value Register D	GTDVD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2ABCh	GPT7	General PWM Timer Dead Time Buffer Register U	GTDBU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2ABEh	GPT7	General PWM Timer Dead Time Buffer Register D	GTDBD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2AC0h	GPT7	General PWM Timer Output Protection Function Status Register	GTSOS	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2AC2h	GPT7	General PWM Timer Output Protection Function Temporary Release Register	GTSOTR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3002h	DPC	Software Start Setting Register 0	SOFTSTART 0	16	16	3 to 5 PCLKA	2, 3 ICLK	DPC	Not present in versions with 64 or 48 pins.
000C3006h	DPC	Software Start Setting Register 1	SOFTSTART 1	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C300Ah	DPC	Software Start Setting Register 2	SOFTSTART 2	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C300Eh	DPC	Software Start Setting Register 3	SOFTSTART 3	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3012h	DPC	Reference Value Setting Register 0	VOTARGET 0	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3016h	DPC	Reference Value Setting Register 1	VOTARGET 1	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C301Ah	DPC	Reference Value Setting Register 2	VOTARGET 2	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C301Eh	DPC	Reference Value Setting Register 3	VOTARGET 3	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3022h	DPC	Reference Value Select Register	REFSEL	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3026h	DPC	PWM Channel Setting Register	CHLSEL	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C302Ah	DPC	Control Enable Setting Register	ENABLE	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C302Eh	DPC	Control Calculation Parameter Setting Register KP0	PARAMKP0	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3032h	DPC	Control Calculation Parameter Setting Register KI0	PARAMKI0	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3036h	DPC	Control Calculation Parameter Setting Register KQ0	PARAMKQ0	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C303Ah	DPC	Control Calculation Parameter Setting Register KF0	PARAMKF0	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C303Eh	DPC	Control Calculation Parameter Setting Register KP1	PARAMKP1	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3042h	DPC	Control Calculation Parameter Setting Register KI1	PARAMKI1	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3046h	DPC	Control Calculation Parameter Setting Register KQ1	PARAMKQ1	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C304Ah	DPC	Control Calculation Parameter Setting Register KF1	PARAMKF1	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C304Eh	DPC	Control Calculation Parameter Setting Register KP2	PARAMKP2	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3052h	DPC	Control Calculation Parameter Setting Register KI2	PARAMKI2	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.

Table 5.15 Bus Timing (Multiplexed Bus) (4)

Condition: VCC = PLLVCC = AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V
VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V, VREFH0 = 4.0 V to AVCC0
$T_a = T_{opr}$
Output load conditions: V_{OH} = VCC x 0.5, V_{OL} = VCC x 0.5, I_{OH} = –1.0 mA, I_{OL} = 1.0 mA, C = 30 pF

Item	Symbol	Min.	Max.	Unit	Test Conditions
Address delay time	t_{AD}	—	15	ns	Figure 5.18, Figure 5.19
Byte control delay time	t_{BCD}	—	15	ns	
CS# delay time	t_{CSD}	—	15	ns	
RD# delay time	t_{RSD}	—	15	ns	
ALE delay time	t_{ALED}	—	15	ns	
Read data setup time	t_{RDS}	15	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	—	15	ns	
Write data delay time	t_{WDD}	—	15	ns	
Write data hold time	t_{WDH}	0	—	ns	
WAIT# setup time	t_{WTS}	15	—	ns	Figure 5.17
WAIT# hold time	t_{WTH}	0.0	—	ns	

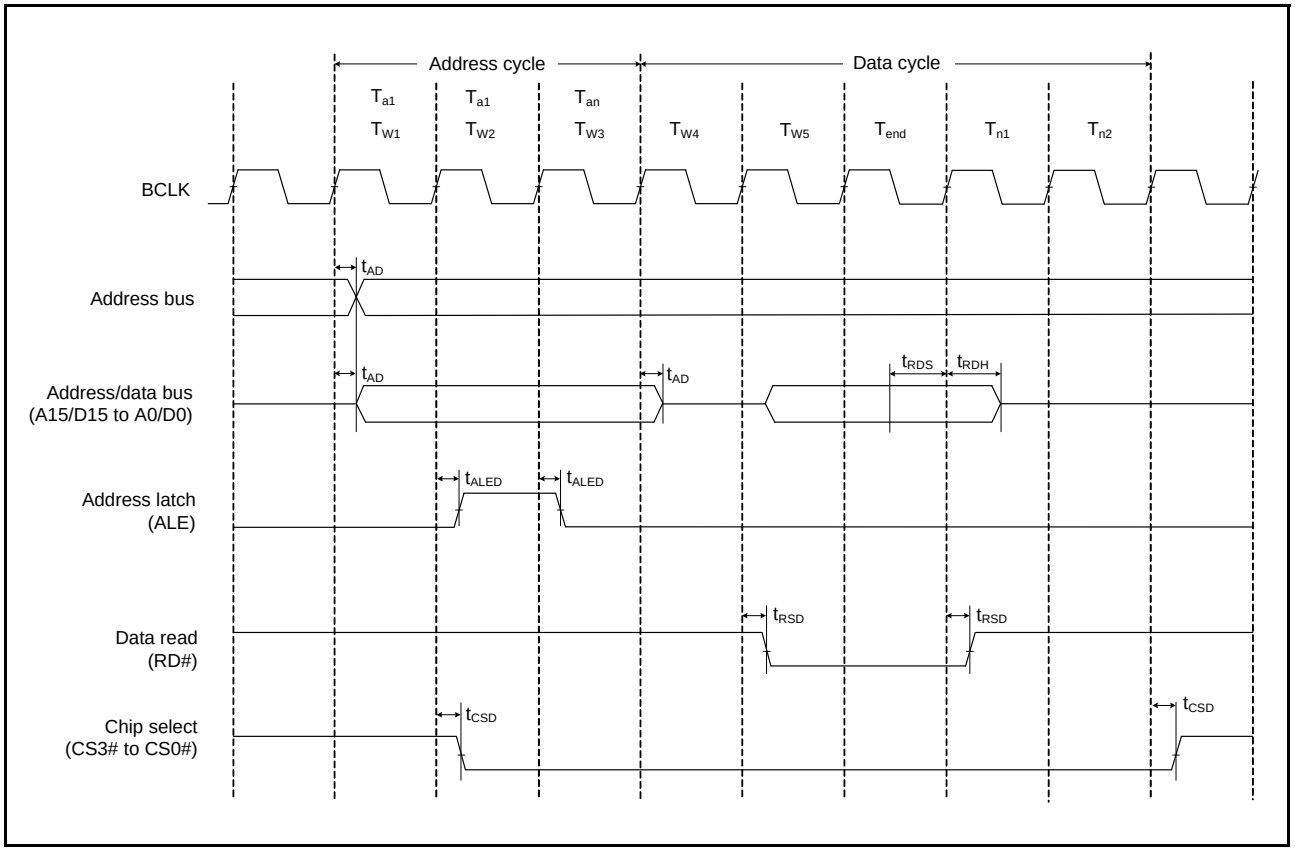


Figure 5.18 Example of External Bus Timing/Read Access Operation (Multiplexed)

Table 5.23 Characteristics of the Programmable Gain Amplifier

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Analog input capacitance		C_{in}	—	—	8	pF	
Input offset voltage		V_{off}	—	—	8	mV	
Input voltage range (V_{in})	Gain × 2.000	V_{in}	0.050 × AVcc	—	0.450 × AVcc	V	
	Gain × 2.500		0.047 × AVcc		0.360 × AVcc		
	Gain × 3.077		0.045 × AVcc		0.292 × AVcc		
	Gain × 3.636		0.042 × AVcc		0.247 × AVcc		
	Gain × 4.000		0.040 × AVcc		0.212 × AVcc		
	Gain × 4.444		0.036 × AVcc		0.191 × AVcc		
	Gain × 5.000		0.033 × AVcc		0.170 × AVcc		
	Gain × 5.714		0.031 × AVcc		0.148 × AVcc		
	Gain × 6.667		0.029 × AVcc		0.127 × AVcc		
	Gain × 10.000		0.025 × AVcc		0.08 × AVcc		
	Gain × 13.333		0.023 × AVcc	—	0.06 × AVcc		
Slew rate		SR	10	—	—	V/µs	
Gain error	Gain × 2.000	—	—	—	1	%	
	Gain × 2.500		—	—	1		
	Gain × 3.077		—	—	1		
	Gain × 3.636		—	—	1.5		
	Gain × 4.000		—	—	1.5		
	Gain × 4.444		—	—	2		
	Gain × 5.000		—	—	2		
	Gain × 5.714		—	—	2		
	Gain × 6.667		—	—	3		
	Gain × 10.000		—	—	4		
	Gain × 13.333		—	—	4		

Table 5.24 Comparator Characteristics

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Analog input capacitance	C_{in}	—	—	8	pF	
REFH pin offset voltage	V_{off}	—	—	5	mV	
REFL pin offset voltage		—	—	5	mV	
REFH input voltage range	V_{in}	1.7	—	AVcc – 0.3	V	
REFL input voltage range		0.3	—	AVcc – 1.7	V	
REFH reply time	t_{CR}	—	—	500	ns	VI = VREF±25mV
REFL reply time	t_{CF}	—	—	500	ns	

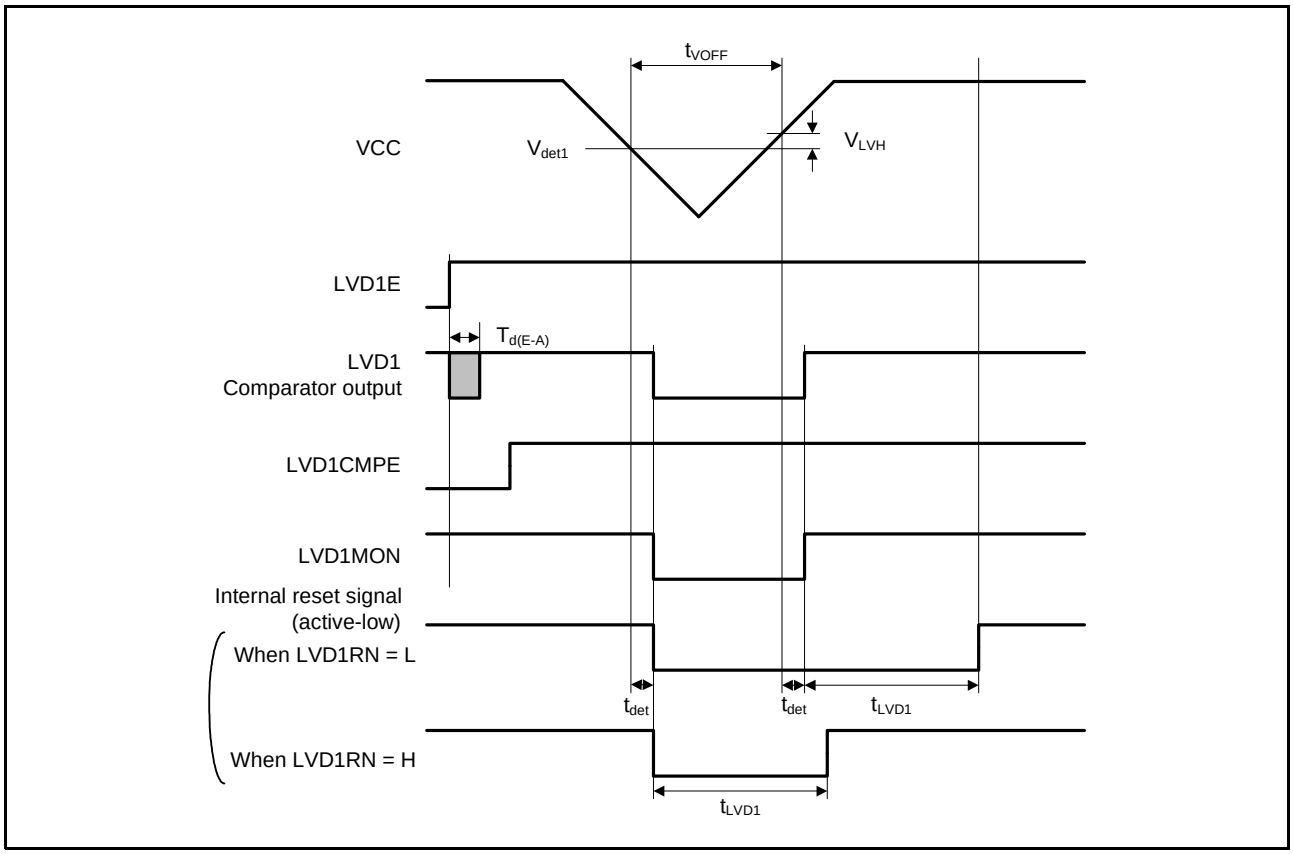


Figure 6.28 Voltage Detection Circuit Timing (V_{det1})

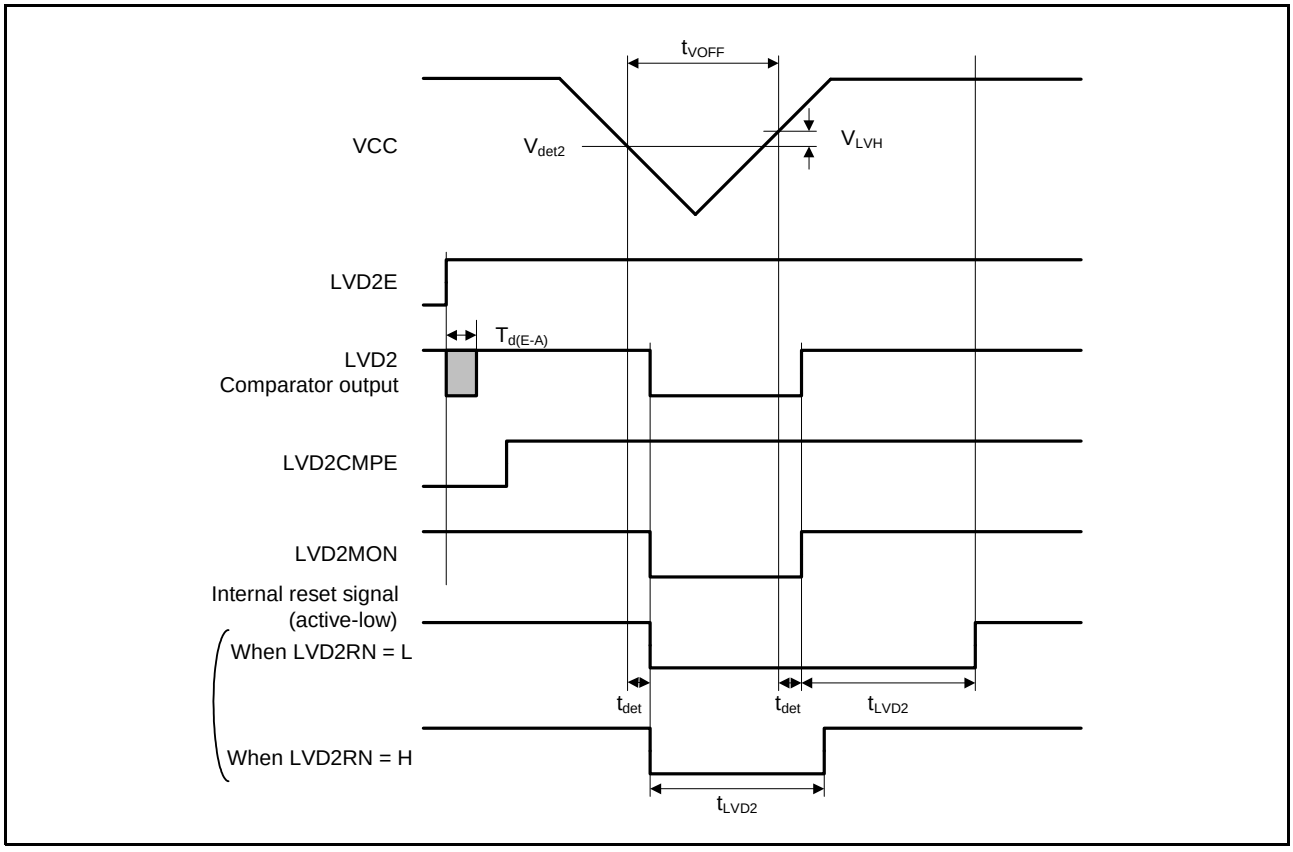
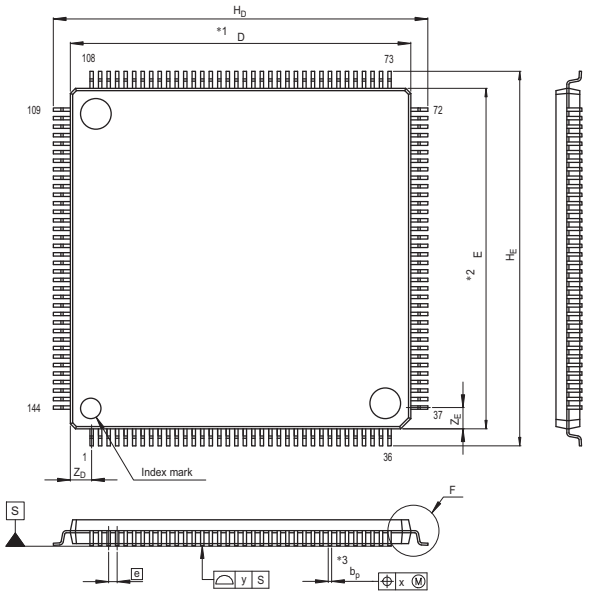


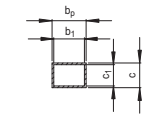
Figure 6.29 Voltage Detection Circuit Timing (V_{det2})

Appendix 1. Package Dimensions

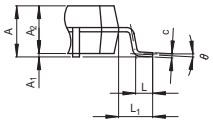
Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP144-20x20-0.50	PLQP0144KA-A	144P6Q-A / FP-144L / FP-144LV	1.2g





Terminal cross section



Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	19.9	20.0	20.1
E	19.9	20.0	20.1
A_2	—	1.4	—
H_D	21.8	22.0	22.2
H_E	21.8	22.0	22.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.17	0.22	0.27
b_1	—	0.20	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure A 144-Pin LQFP (PLQP0144KA-A)

Rev.	Date	Description	
		Page	Summary
2.10	Sep 26, 2013	36 to 39	Table 1.7 List of Pins and Pin Functions (112-Pin LQFP), changed
		40 to 42	Table 1.8 List of Pins and Pin Functions (100-Pin LQFP), changed
		43 to 45	Table 1.9 List of Pins and Pin Functions (64-Pin LQFP), changed
		46 to 47	Table 1.10 List of Pins and Pin Functions (48-Pin LQFP), changed
		4. I/O Registers	
		56 to 103	Table 4.1 List of I/O Registers (Address Order), changed
		5. Electrical Characteristics [144-, 120-, 112- and 100-Pin Versions]	
		104	Table 5.1 Absolute Maximum Ratings, changed
		107	Table 5.4 DC Characteristics (3), Note 7, deleted
		108	Table 5.6 Permissible Power Consumption, added
		128	5.3.7 Timing of PWM Delay Generation Circuit, added
		128	Table 42.21 Timing of the PWM Delay Generation Circuit, added
		132	Figure 5.32 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKB Division Ratio Set to a Value Other Than 1/2) and Simple SPI Timing (Master, CKPH = 1), changed
		133	Figure 5.34 RSPI Timing (Slave, CPHA = 0) and Simple SPI Timing (Slave, CKPH = 0), changed
		134	Figure 5.35 RSPI Timing (Slave, CPHA = 1) and Simple SPI Timing (Slave, CKPH = 1), changed
		6. Electrical Characteristics [64- and 48-Pin Versions]	
		149	Table 6.1 Absolute Maximum Ratings, changed
		151	Table 6.3 DC Characteristics (2), Note 3, changed
		152	Table 6.5 Permissible Power Consumption, added