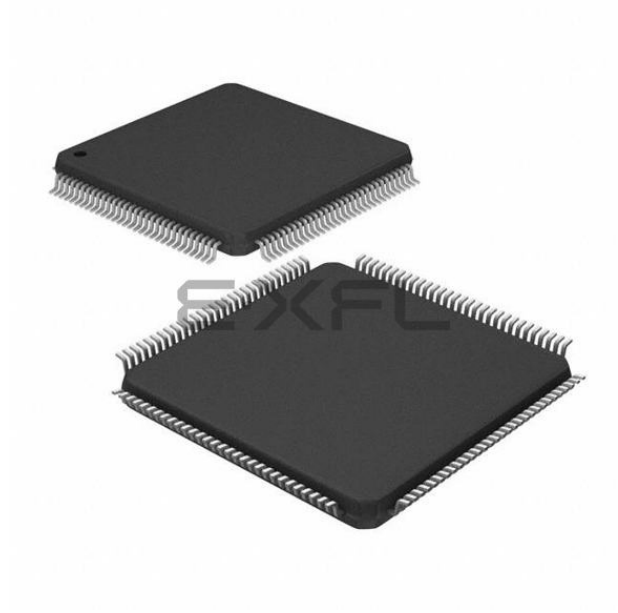
Renesas Electronics America Inc - R5F563TBADFA#V0 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	72
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x10b, 8x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	120-LQFP
Supplier Device Package	120-LQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f563tbadfa-v0

Table 1.3 List of Products (2/4)

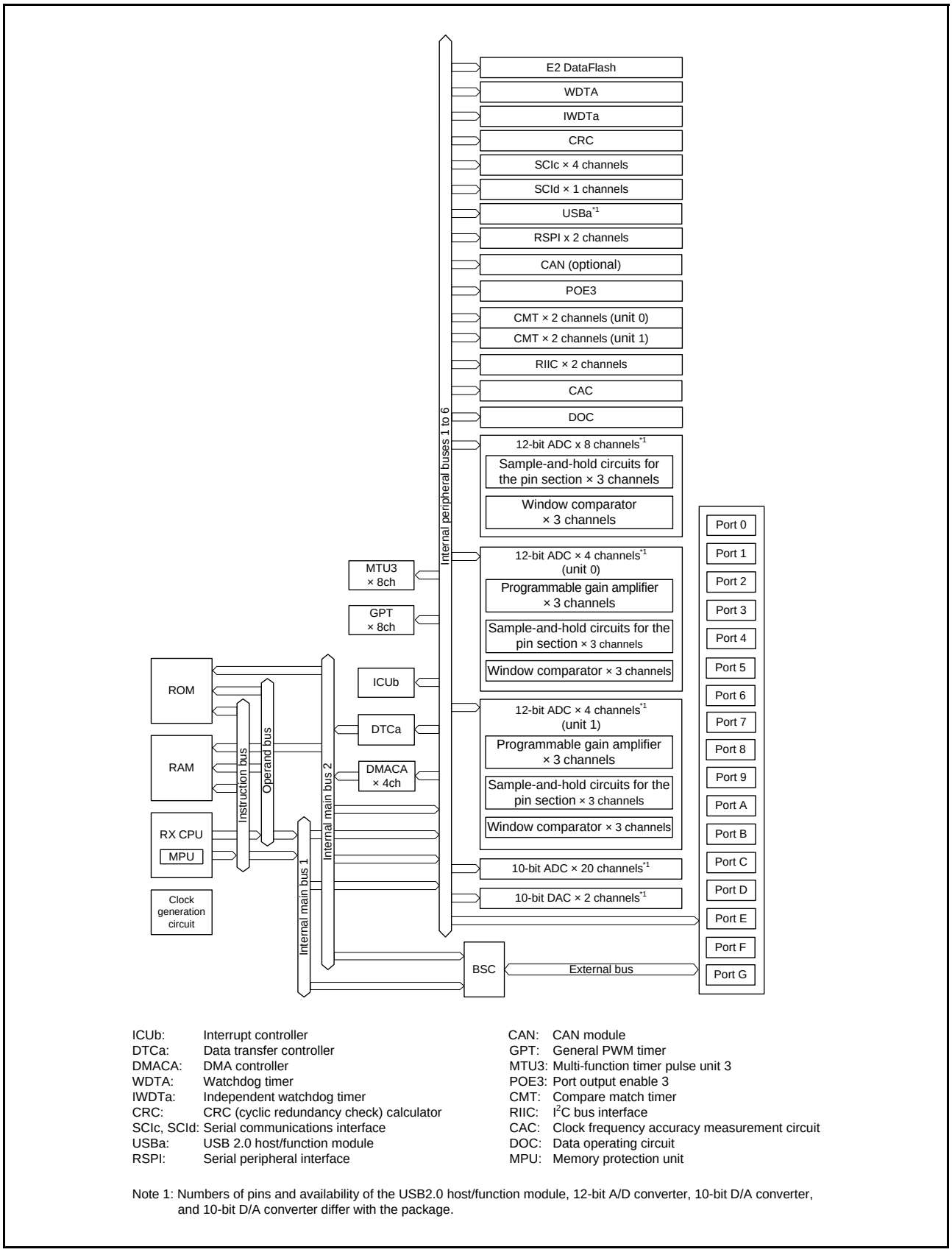
Group	Part No.	Order Part No.	Package	On-chip ROM Capacity	On-chip RAM Capacity	Option	Operating Voltage	Operating Temperature
RX63T	R5F563TCDDFB	R5F563TCDDFB#V0	PLQP0144KA-A	384 Kbytes	32 Kbytes	CAN module not included	VCC/ PLLVCC 4.0 to 5.5V VCC_USB 3.0 to 3.6V AVCC/ AVCC0 4.0 to 5.5V	-40 to +85°C (D Version)
	R5F563TCDDFA	R5F563TCDDFA#V0	PLQP0120KA-A	384 Kbytes	32 Kbytes	CAN module not included		
	R5F563TCDDFH	R5F563TCDDFH#V0	PLQP0112JA-A	384 Kbytes	32 Kbytes	CAN module not included		
	R5F563TCDDFP	R5F563TCDDFP#V0	PLQP0100KB-A	384 Kbytes	32 Kbytes	CAN module not included		
	R5F563TBDDFB	R5F563TBDDFB#V0	PLQP0144KA-A	256 Kbytes	24 Kbytes	CAN module not included		
	R5F563TBDDFA	R5F563TBDDFA#V0	PLQP0120KA-A	256 Kbytes	24 Kbytes	CAN module not included		
	R5F563TBDDFH	R5F563TBDDFH#V0	PLQP0112JA-A	256 Kbytes	24 Kbytes	CAN module not included		
	R5F563TBDDFP	R5F563TBDDFP#V0	PLQP0100KB-A	256 Kbytes	24 Kbytes	CAN module not included		
	R5F563TEBDFB	R5F563TEBDFB#V0	PLQP0144KA-A	512 Kbytes	48 Kbytes	CAN module included	VCC/ PLLVCC/ VCC_USB 2.7 to 3.6V AVCC/ AVCC0 3.0 to 3.6V or 4.0 to 5.5V	
	R5F563TEBDFB	R5F563TEBDFB#V1	PLQP0144KA-A	512 Kbytes	48 Kbytes	CAN module included		
	R5F563TEBDFA	R5F563TEBDFA#V0	PLQP0120KA-A	512 Kbytes	48 Kbytes	CAN module included		
	R5F563TEBDFA	R5F563TEBDFA#V1	PLQP0120KA-A	512 Kbytes	48 Kbytes	CAN module included		
	R5F563TEBDFH	R5F563TEBDFH#V0	PLQP0112JA-A	512 Kbytes	48 Kbytes	CAN module included		
	R5F563TEBDFH	R5F563TEBDFH#V1	PLQP0112JA-A	512 Kbytes	48 Kbytes	CAN module included		
	R5F563TEBDFP	R5F563TEBDFP#V0	PLQP0100KB-A	512 Kbytes	48 Kbytes	CAN module included		
	R5F563TEBDFP	R5F563TEBDFP#V1	PLQP0100KB-A	512 Kbytes	48 Kbytes	CAN module included		
	R5F563TCBDFB	R5F563TCBDFB#V0	PLQP0144KA-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TCBDFB	R5F563TCBDFB#V1	PLQP0144KA-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TCBDFA	R5F563TCBDFA#V0	PLQP0120KA-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TCBDFA	R5F563TCBDFA#V1	PLQP0120KA-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TCBDFH	R5F563TCBDFH#V0	PLQP0112JA-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TCBDFH	R5F563TCBDFH#V1	PLQP0112JA-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TCBDFP	R5F563TCBDFP#V0	PLQP0100KB-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TCBDFP	R5F563TCBDFP#V1	PLQP0100KB-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TBBDFB	R5F563TBBDFB#V0	PLQP0144KA-A	256 Kbytes	24 Kbytes	CAN module included		
	R5F563TBBDFB	R5F563TBBDFB#V1	PLQP0144KA-A	256 Kbytes	24 Kbytes	CAN module included		
	R5F563TBBDFA	R5F563TBBDFA#V0	PLQP0120KA-A	256 Kbytes	24 Kbytes	CAN module included		
	R5F563TBBDFA	R5F563TBBDFA#V1	PLQP0120KA-A	256 Kbytes	24 Kbytes	CAN module included		
	R5F563TBBDFH	R5F563TBBDFH#V0	PLQP0112JA-A	256 Kbytes	24 Kbytes	CAN module included		
	R5F563TBBDFH	R5F563TBBDFH#V1	PLQP0112JA-A	256 Kbytes	24 Kbytes	CAN module included		

Table 1.3 List of Products (3/4)

Group	Part No.	Order Part No.	Package	On-chip ROM Capacity	On-chip RAM Capacity	Option	Operating Voltage	Operating Temperature
RX63T	R5F563TBBDFP	R5F563TBBDFP#V0	PLQP0100KB-A	256 Kbytes	24 Kbytes	CAN module included	VCC/ PLLVCC/ VCC_USB 2.7 to 3.6V AVCC/ AVCC0 3.0 to 3.6V or 4.0 to 5.5V	-40 to +85°C (D Version)
	R5F563TBBDFP	R5F563TBBDFP#V1	PLQP0100KB-A	256 Kbytes	24 Kbytes	CAN module included		
	R5F563TEEDFB	R5F563TEEDFB#V0	PLQP0144KA-A	512 Kbytes	48 Kbytes	CAN module not included		
	R5F563TEEDFA	R5F563TEEDFA#V0	PLQP0120KA-A	512 Kbytes	48 Kbytes	CAN module not included		
	R5F563TEEDFH	R5F563TEEDFH#V0	PLQP0112JA-A	512 Kbytes	48 Kbytes	CAN module not included		
	R5F563TEEDFP	R5F563TEEDFP#V0	PLQP0100KB-A	512 Kbytes	48 Kbytes	CAN module not included		
	R5F563TCEDFB	R5F563TCEDFB#V0	PLQP0144KA-A	384 Kbytes	32 Kbytes	CAN module not included		
	R5F563TCEDFA	R5F563TCEDFA#V0	PLQP0120KA-A	384 Kbytes	32 Kbytes	CAN module not included		
	R5F563TCEDFH	R5F563TCEDFH#V0	PLQP0112JA-A	384 Kbytes	32 Kbytes	CAN module not included		
	R5F563TCEDFP	R5F563TCEDFP#V0	PLQP0100KB-A	384 Kbytes	32 Kbytes	CAN module not included		
	R5F563TBEDFB	R5F563TBEDFB#V0	PLQP0144KA-A	256 Kbytes	24 Kbytes	CAN module not included		
	R5F563TBEDFA	R5F563TBEDFA#V0	PLQP0120KA-A	256 Kbytes	24 Kbytes	CAN module not included		
	R5F563TBEDFH	R5F563TBEDFH#V0	PLQP0112JA-A	256 Kbytes	24 Kbytes	CAN module not included		
	R5F563TBEDFP	R5F563TBEDFP#V0	PLQP0100KB-A	256 Kbytes	24 Kbytes	CAN module not included		
	R5F563T6EDFM	R5F563T6EDFM#V0	PLQP0064KB-A	64 Kbytes	8 Kbytes	CAN module not included	VCC/ PLLVCC 2.7 to 3.6V AVCC0 3.0 to 3.6V	
	R5F563T5EDFM	R5F563T5EDFM#V0	PLQP0064KB-A	48 Kbytes	8 Kbytes	CAN module not included		
	R5F563T4EDFM	R5F563T4EDFM#V0	PLQP0064KB-A	32 Kbytes	8 Kbytes	CAN module not included		
	R5F563T6EDFL	R5F563T6EDFL#V0	PLQP0048KB-A	64 Kbytes	8 Kbytes	CAN module not included		
	R5F563T5EDFL	R5F563T5EDFL#V0	PLQP0048KB-A	48 Kbytes	8 Kbytes	CAN module not included		
	R5F563T4EDFL	R5F563T4EDFL#V0	PLQP0048KB-A	32 Kbytes	8 Kbytes	CAN module not included		
	R5F563TEAGFB	R5F563TEAGFB#V1	PLQP0144KA-A	512 Kbytes	48 Kbytes	CAN module included	VCC/ PLLVCC 4.0 to 5.5V VCC_USB 3.0 to 3.6V AVCC/ AVCC0 4.0 to 5.5V	-40 to +105°C (G Version)*1
	R5F563TEAGFA	R5F563TEAGFA#V1	PLQP0120KA-A	512 Kbytes	48 Kbytes	CAN module included		
	R5F563TEAGFH	R5F563TEAGFH#V1	PLQP0112JA-A	512 Kbytes	48 Kbytes	CAN module included		
	R5F563TEAGFP	R5F563TEAGFP#V1	PLQP0100KB-A	512 Kbytes	48 Kbytes	CAN module included		
	R5F563TCAGFB	R5F563TCAGFB#V1	PLQP0144KA-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TCAGFA	R5F563TCAGFA#V1	PLQP0120KA-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TCAGFH	R5F563TCAGFH#V1	PLQP0112JA-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TCAGFP	R5F563TCAGFP#V1	PLQP0100KB-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TBAGFB	R5F563TBAGFB#V1	PLQP0144KA-A	256 Kbytes	24 Kbytes	CAN module included		

1.3 Block Diagram

Figure 1.2 shows a block diagram.



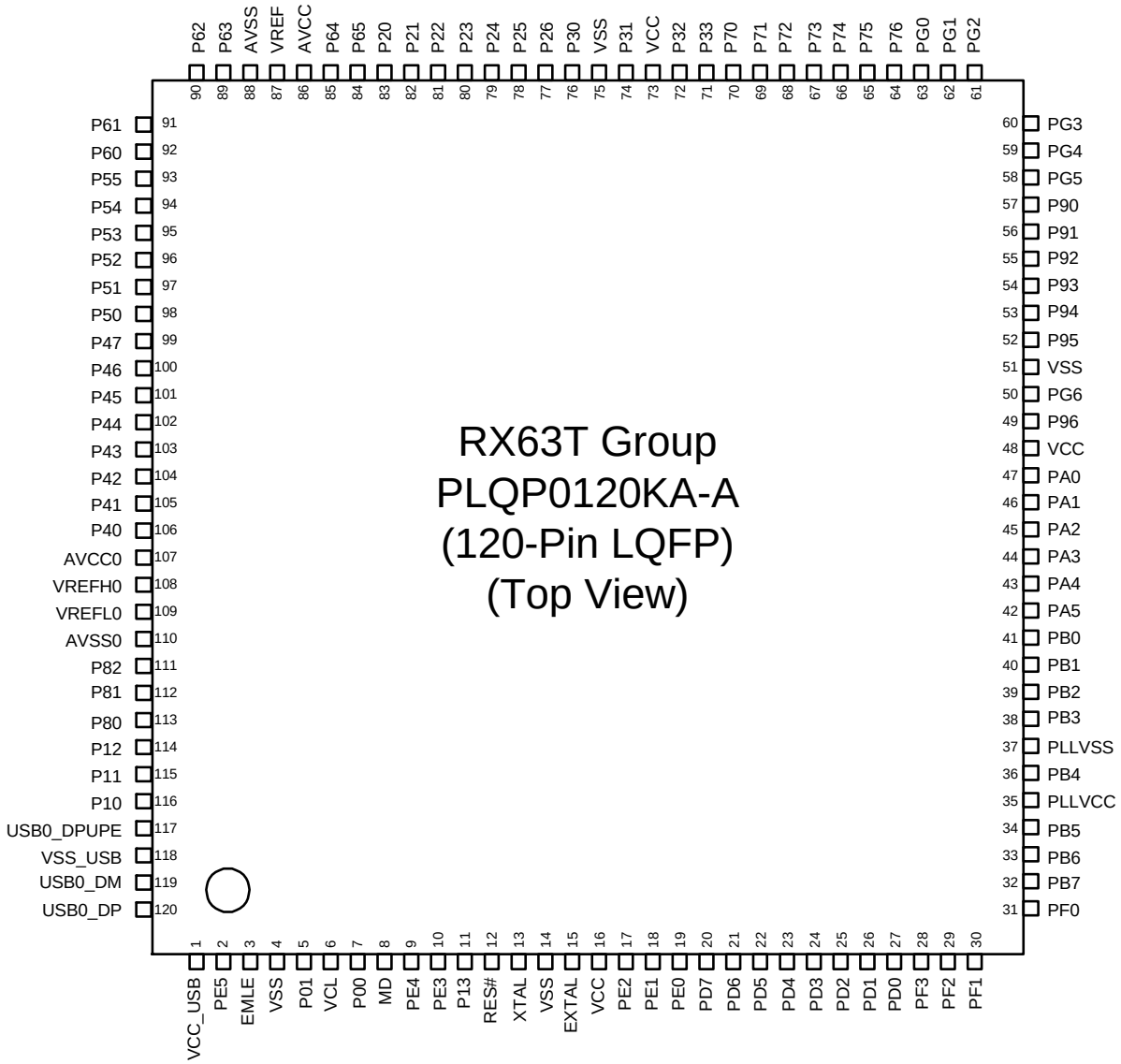
ICUb: Interrupt controller
DTCa: Data transfer controller
DMACA: DMA controller
WDTA: Watchdog timer
IWDTa: Independent watchdog timer
CRC: CRC (cyclic redundancy check) calculator
SCIc, SCId: Serial communications interface
USBa: USB 2.0 host/function module
RSPI: Serial peripheral interface
CAN: CAN module
GPT: General PWM timer
MTU3: Multi-function timer pulse unit 3
POE3: Port output enable 3
CMT: Compare match timer
RIIC: I^2C bus interface
CAC: Clock frequency accuracy measurement circuit
DOC: Data operating circuit
MPU: Memory protection unit

Note 1: Numbers of pins and availability of the USB2.0 host/function module, 12-bit A/D converter, 10-bit D/A converter, and 10-bit D/A converter differ with the package.

Figure 1.2 Block Diagram

Table 1.4 Pin Functions (3/5)

Classifications	Pin Name	I/O	Description
Serial communications interface (SCIc)	Asynchronous mode/clock synchronous mode		
	SCK0, SCK1, SCK2, SCK3	I/O	Input/output pins for clock signals.
	RXD0, RXD1, RXD2, RXD3	Input	Input pins for data reception.
	TXD0, TXD1, TXD2, TXD3	Output	Output pins for data transmission.
	CTS0#, CTS1#, CTS2#, CTS3#	Input	Transmit/receive start control input pins
	RTS0#, RTS1#, RTS2#, RTS3#	Output	Transmit/receive start control output pins
	Simple I^2C mode		
	SSCL0, SSCL1, SSCL2, SSCL3	I/O	Input/output pins for the I^2C clock
	SSDA0, SSDA1, SSDA2, SSDA3	I/O	Input/output pins for the I^2C data
	Simple SPI mode		
	SCK0, SCK1, SCK2, SCK3	I/O	Input/output pins for the clock
	SMISO0, SMISO1, SMISO2, SMISO3	I/O	Input/output pins for slave transmit data.
	SMOSI0, SMOSI1, SMOSI2, SMOSI3	I/O	Input/output pins for master transmit data.
	SS0#, SS1#, SS2#, SS3#	Input	Input pins for chip select signals
Serial communications interface (SCId)	Asynchronous mode/clock synchronous mode		
	SCK12	I/O	Input/output pin for clock signals.
	RXD12	Input	Input pin for data reception.
	TXD12	Output	Output pin for data transmission.
	CTS12#	Input	Transmit/receive start control input pins
	RTS12#	Output	Transmit/receive start control output pins
	Simple I^2C mode		
	SSCL12	I/O	Input/output pins for the I^2C clock
	SSDA12	I/O	Input/output pins for the I^2C data
	Simple SPI mode		
	SCK12	I/O	Input/output pins for the clock
	SMISO12	I/O	Input/output pins for slave transmit data.
	SMOSI12	I/O	Input/output pins for master transmit data.
	SS12#	Input	Input pins for chip select signals
	Extended serial mode		
	RXDX12	Input	Input pin for receive data
	TXDX12	Output	Output pin for transmit data
	SIOX12	I/O	Input/output pin for transfer data
I^2C bus interface	SCL, SCL0, SCL1	I/O	Clock input/output pin. N-channel open drain can directly drive buses.
	SDA, SDA0, SDA1	I/O	Data input/output pin. N-channel open drain can directly drive buses.



Note: • This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.6, List of Pins and Pin Functions (120-Pin LQFP).

Figure 1.4 Pin Assignment (120-Pin LQFP)

Table 1.5 List of Pins and Pin Functions (144-Pin LQFP) (2/4)

Pin Number 144-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3, GPT, POE3, CAC)	Communications (SCIc, SCId, RSPI, RIIC, CAN, USB)	Interrupt	S12ADB, AD, DA
39		PB6	A18		RXD12/SMISO12/ SSCL12/RXDX12/ CRX1	IRQ2	
40		PB5	A17		TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/ CTX1		
41	PLLVCC						
42		PB4	A16	POE8#/ GTETRG0		IRQ3-DS	
43	PLLVSS						
44	TDI				RXD1*1		
45	TCK/FINEC						
46	TDO				TXD1*1		
47		PB3	A15	MTIOC0A/CACREF	SCK0		
48		PB2		MTIOC0B	TXD0/SMOSI0/ SSDA0/SDA0		
49		PB1		MTIOC0C	RXD0/SMISO0/ SSCL0/SCL0	IRQ4	
50		PB0	A14	MTIOC0D	MOSIA/MOSIB		
51	TRDATA1	PA6	CS3#		CTS3#/RTS3#/SS3#		
52		PA5		MTIOC1A	RXD0/SMISO0/ SSCL0/ MISOA/MISOB		ADTRG1#
53		PA4		MTIOC1B	TXD0/SMOSI0/ SSDA0/SMOSI0/ RSPCKA/RSPCKB		ADTRG0#
54		PA3		MTIOC2A	SCK0/SSLA0/SSLB0		
55		PA2		MTIOC2B	RXD2/SMISO2/ SSCL2/ SSLA1/SSLB1		
56		PA1		MTIOC6A	TXD2/SMOSI2/ SSDA2/SMOSI2/ SSLA2/SSLB2		
57		PA0		MTIOC6C	SCK2/SSLA3/SSLB3		
58	TRDATA0	P35			TXD3/SMOSI3/SSDA3		
59	TRCLK	P34		GTETRG1	RXD3/SMISO3/SSCL3	IRQ3	
60	VCC						
61		P96	A13	POE4#	RXD1/SMISO1/SSCL1	IRQ4-DS	
62		PG6	CS2#		SCK1		
63	VSS						
64		P95		MTIOC6B/GTIOC4A	TXD1/SMOSI1/SSDA1		
65		P94		MTIOC7A/GTIOC5A	CTS1#/RTS1#/SS1#		
66		P93		MTIOC7B/GTIOC6A	CTS2#/RTS2#/SS2#		
67		P92		MTIOC6D/GTIOC4B			
68		P91		MTIOC7C/GTIOC5B			
69		P90		MTIOC7D/GTIOC6B			
70		PG5		POE12#	SCK3		ADTRG#
71		PG4		GTIOC6B	RXD3/SMISO3/SSCL3	IRQ6	

Table 1.6 List of Pins and Pin Functions (120-Pin LQFP) (1/4)

Pin Number 120-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3, GPT, POE3, CAC)	Communications (SCIc, SCId, RSPI, RIIC, CAN, USB)	Interrupt	S12ADB, AD, DA
1	VCC_USB						
2		PE5	BCLK		USB0_VBUS	IRQ0	
3	EMLE						
4	VSS						
5		P01	RD#		CTS0#/RTS0#/SS0#/ USB0_DRPD		
6	VCL						
7		P00	CS1#	CACREF			
8	MD/FINED						
9		PE4	A10	POE10#/MTCLKC		IRQ1	
10		PE3	A11	POE11#/MTCLKD		IRQ2-DS	
11		P13			CTS2#/RTS2#/SS2#/ USB0_VBUSEN		
12	RES#						
13	XTAL						
14	VSS						
15	EXTAL						
16	VCC						
17		PE2		POE10#		NMI	
18		PE1	WR0#/WR#		CTS12#/RTS12#/ SS12#/SSLA3/SSLB3/ USB0_OVRCURA		
19		PE0	WR1#/BC1#/ WAIT#		SSLA2/SSLB2/CRX1/ USB0_OVRCURB	IRQ7	
20	TRST#	PD7		GTIOC0A	CTS0#/RTS0#/SS0#/ SSLA1/SSLB1/CTX1		
21	TMS	PD6		GTIOC0B	SSLA0/SSLB0		
22	TDI	PD5		GTIOC1A	RXD1/SMISO1/SSCL1	IRQ6	
23	TCK/FINEC	PD4		GTIOC1B	SCK1		
24	TDO	PD3		GTIOC2A	TXD1/SMOSI1/SSDA1		
25		PD2	CS2#	GTIOC2B	MOSIA/MOSIB/ USB0_ID		
26		PD1	CS0#	GTIOC3A	MISOA/MISOB/ USB0_EXICEN		
27		PD0	A12	GTIOC3B	RSPCKA/RSPCKB		
28		PF3			TXD1/SMOSI1/SSDA1		
29		PF2	CS1#		RXD1/SMISO1/SSCL1	IRQ5	
30		PF1					
31		PF0					
32		PB7	A19		SCK12		
33		PB6	A18		RXD12/SMISO12/ SSCL12/RXDX12/ CRX1	IRQ2	
34		PB5	A17		TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/CTX1		
35	PLLVCC						
36		PB4	A16	POE8#/GTETRG0		IRQ3-DS	

2. CPU

The RX CPU has sixteen general-purpose registers, nine control registers, and one accumulator used for DSP instructions.

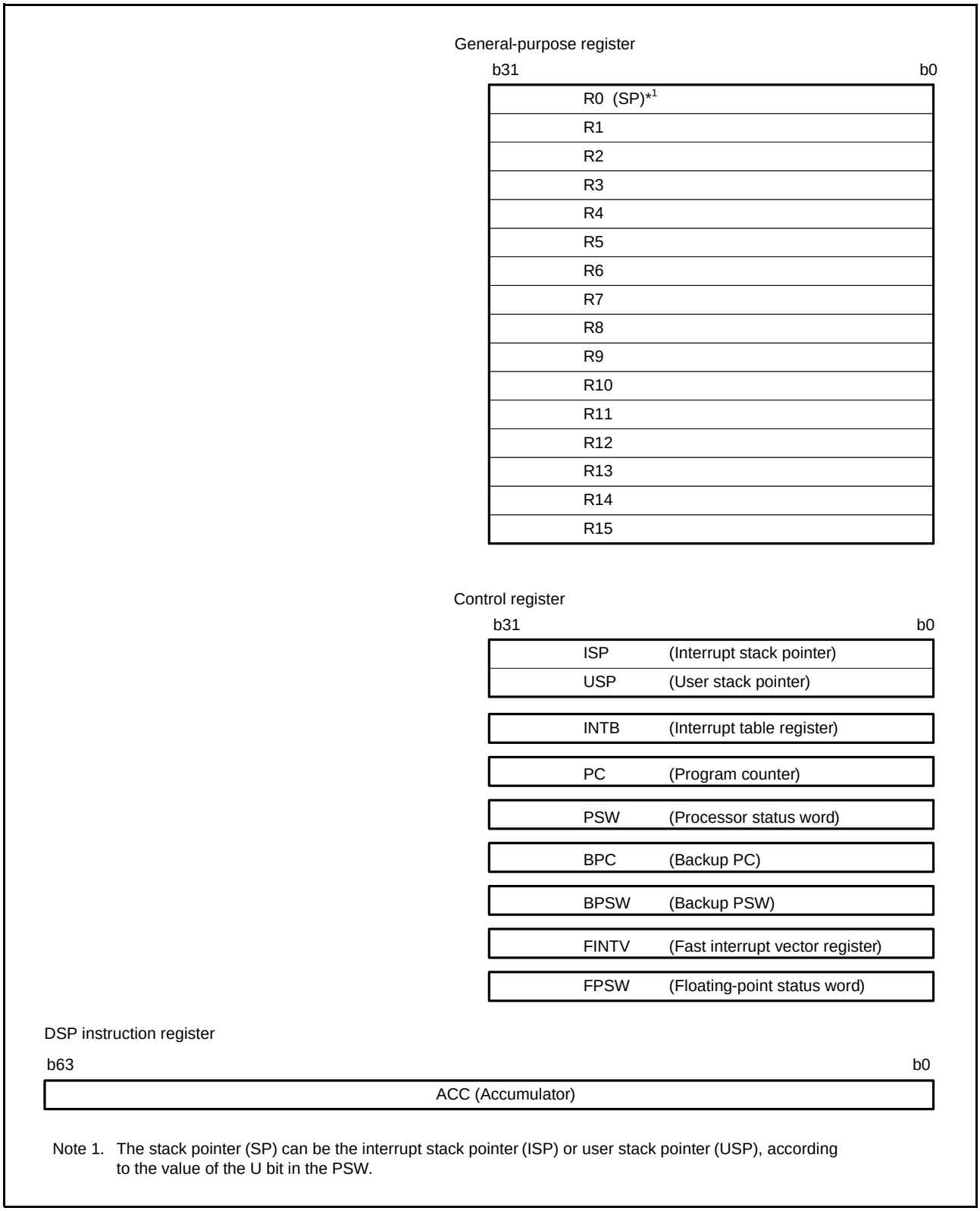


Figure 2.1 Register Set of the CPU

- Longword-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.L  #SFR_DATA, [R1]
CMP    [R1].L, R1
;; Next process
```

If multiple registers are written to and a subsequent instruction should be executed after the write operations are entirely completed, only read the I/O register that was last written to and execute the operation using the value; it is not necessary to read or execute operation for all the registers that were written to.

(3) Number of Access Cycles to I/O Registers

For the number of I/O register access cycles, refer to Table 4.1, List of I/O Registers (Address Order).
The number of access cycles to I/O registers is obtained by following equation.*1

Number of access cycles to I/O registers = Number of bus cycles for internal main bus 1 +
Number of divided clock synchronization cycles +
Number of bus cycles for internal peripheral bus 1 to 6

The number of bus cycles of internal peripheral bus 1 to 6 differs according to the register to be accessed.
When peripheral functions connected to internal peripheral bus 2 to 6 are accessed, the number of divided clock synchronization cycles is added.
The number of divided clock synchronization cycles differs depending on the frequency ratio between ICLK and PCLK (or FCLK, BCLK) or bus access timing.
In the peripheral function unit, when the frequency ratio of ICLK is equal to or greater than that of PCLK (or FCLK), the sum of the number of bus cycles for internal main bus 1 and the number of the divided clock synchronization cycles will be one cycle of PCLK (or FCLK) at a maximum. Therefore, one PCLK (or FCLK) has been added to the number of access states shown in Table 4.1.
When the frequency ratio of ICLK is lower than that of PCLK (or FCLK), the subsequent bus access is started from the ICLK cycle following the completion of the access to the peripheral functions. Therefore, the access cycles are described on an ICLK basis.
In the external bus control unit, the sum of the number of bus cycles for internal main bus 1 and the number of divided clock synchronization cycles will be one cycle of BCLK at a maximum. Therefore, one BCLK is added to the number of access cycles shown in Table 4.1.

Note 1. This applies to the number of cycles when the access from the CPU does not conflict with the instruction fetching to the external memory or bus access from the different bus master (DMAC or DTC).

(4) Note on Sleep Mode and Mode Transition

During sleep mode or a mode transition, do not write to the system control related registers (indicated by 'SYSTEM' in the Module Symbol column in Table 4.1, List of I/O Registers (Address Order)).

Table 4.1 List of I/O Registers (Address Order) (3/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 3024h	BSC	CS2 Wait Control Register 1	CS2WCR1	32	32	1, 2 BCLK		Buses	Not present in versions with 64 or 48 pins.
0008 3028h	BSC	CS2 Wait Control Register 2	CS2WCR2	32	32	1, 2 BCLK			Not present in versions with 64 or 48 pins.
0008 3032h	BSC	CS3 Mode Register	CS3MOD	16	16	1, 2 BCLK			Not present in versions with 64 or 48 pins.
0008 3034h	BSC	CS3 Wait Control Register 1	CS3WCR1	32	32	1, 2 BCLK			Not present in versions with 64 or 48 pins.
0008 3038h	BSC	CS3 Wait Control Register 2	CS3WCR2	32	32	1, 2 BCLK			Not present in versions with 64 or 48 pins.
0008 3802h	BSC	CS0 Control Register	CS0CR	16	16	1, 2 BCLK			Not present in versions with 64 or 48 pins.
0008 380Ah	BSC	CS0 Recovery Cycle Register	CS0REC	16	16	1, 2 BCLK			Not present in versions with 64 or 48 pins.
0008 3812h	BSC	CS1 Control Register	CS1CR	16	16	1, 2 BCLK			Not present in versions with 64 or 48 pins.
0008 381Ah	BSC	CS1 Recovery Cycle Register	CS1REC	16	16	1, 2 BCLK			Not present in versions with 64 or 48 pins.
0008 3822h	BSC	CS2 Control Register	CS2CR	16	16	1, 2 BCLK			Not present in versions with 64 or 48 pins.
0008 382Ah	BSC	CS2 Recovery Cycle Register	CS2REC	16	16	1, 2 BCLK			Not present in versions with 64 or 48 pins.
0008 3832h	BSC	CS3 Control Register	CS3CR	16	16	1, 2 BCLK			Not present in versions with 64 or 48 pins.
0008 383Ah	BSC	CS3 Recovery Cycle Register	CS3REC	16	16	1, 2 BCLK			Not present in versions with 64 or 48 pins.
0008 3880h	BSC	CS Recovery Cycle Insertion Enable Register	CSRECEN	16	16	1, 2 BCLK			Not present in versions with 64 or 48 pins.
0008 6400h	MPU	Region-0 Start Page Number Register	RSPAGE0	32	32	1 ICLK		MPU	
0008 6404h	MPU	Region-0 End Page Number Register	REPAGE0	32	32	1 ICLK			
0008 6408h	MPU	Region-1 Start Page Number Register	RSPAGE1	32	32	1 ICLK			
0008 640Ch	MPU	Region-1 End Page Number Register	REPAGE1	32	32	1 ICLK			
0008 6410h	MPU	Region-2 Start Page Number Register	RSPAGE2	32	32	1 ICLK			
0008 6414h	MPU	Region-2 End Page Number Register	REPAGE2	32	32	1 ICLK			
0008 6418h	MPU	Region-3 Start Page Number Register	RSPAGE3	32	32	1 ICLK			
0008 641Ch	MPU	Region-3 End Page Number Register	REPAGE3	32	32	1 ICLK			
0008 6420h	MPU	Region-4 Start Page Number Register	RSPAGE4	32	32	1 ICLK			
0008 6424h	MPU	Region-4 End Page Number Register	REPAGE4	32	32	1 ICLK			
0008 6428h	MPU	Region-5 Start Page Number Register	RSPAGE5	32	32	1 ICLK			
0008 642Ch	MPU	Region-5 End Page Number Register	REPAGE5	32	32	1 ICLK			
0008 6430h	MPU	Region-6 Start Page Number Register	RSPAGE6	32	32	1 ICLK			
0008 6434h	MPU	Region-6 End Page Number Register	REPAGE6	32	32	1 ICLK			
0008 6438h	MPU	Region-7 Start Page Number Register	RSPAGE7	32	32	1 ICLK			
0008 643Ch	MPU	Region-7 End Page Number Register	REPAGE7	32	32	1 ICLK			
0008 6500h	MPU	Memory-Protection Enable Register	MPEN	32	32	1 ICLK			
0008 6504h	MPU	Background Access Control Register	MPBAC	32	32	1 ICLK			
0008 6508h	MPU	Memory-Protection Error Status-Clearing Register	MPECLR	32	32	1 ICLK			
0008 650Ch	MPU	Memory-Protection Error Status Register	MPESTS	32	32	1 ICLK			
0008 6514h	MPU	Data Memory-Protection Error Address Register	MPDEA	32	32	1 ICLK			
0008 6520h	MPU	Region Search Address Register	MPSA	32	32	1 ICLK			
0008 6524h	MPU	Region Search Operation Register	MPOPS	16	16	1 ICLK			
0008 6526h	MPU	Region Invalidation Operation Register	MPOPI	16	16	1 ICLK			
0008 6528h	MPU	Instruction-Hit Region Register	MHITI	32	32	1 ICLK			
0008 652Ch	MPU	Data-Hit Region Register	MHITD	32	32	1 ICLK			

Table 4.1 List of I/O Registers (Address Order) (14/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 7507h	ICU	IRQ Control Register 7	IRQCR7	8	8	2 ICLK		ICUb	Not present in versions with 64 or 48 pins.
0008 7510h	ICU	IRQ Pin Digital Filter Enable Register 0	IRQFLTE0	8	8	2 ICLK			
0008 7514h	ICU	IRQ Pin Digital Filter Setting Register 0	IRQFLTC0	16	16	2 ICLK			
0008 7580h	ICU	Non-Maskable Interrupt Status Register	NMISR	8	8	2 ICLK			
0008 7581h	ICU	Non-Maskable Interrupt Enable Register	NMIER	8	8	2 ICLK			
0008 7582h	ICU	Non-Maskable Interrupt Status Clear Register	NMICLR	8	8	2 ICLK			
0008 7583h	ICU	NMI Pin Interrupt Control Register	NMICR	8	8	2 ICLK			
0008 7590h	ICU	NMI Pin Digital Filter Enable Register	NMIFLTE	8	8	2 ICLK			
0008 7594h	ICU	NMI Pin Digital Filter Setting Register	NMIFLTC	8	8	2 ICLK			
0008 8000h	CMT	Compare Match Timer Start Register 0	CMSTR0	16	16	2, 3 PCLKB	2 ICLK	CMT	
0008 8002h	CMT0	Compare Match Timer Control Register	CMCR	16	16	2, 3 PCLKB	2 ICLK		
0008 8004h	CMT0	Compare Match Timer Counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK		
0008 8006h	CMT0	Compare Match Timer Constant Register	CMCOR	16	16	2, 3 PCLKB	2 ICLK		
0008 8008h	CMT1	Compare Match Timer Control Register	CMCR	16	16	2, 3 PCLKB	2 ICLK		
0008 800Ah	CMT1	Compare Match Timer Counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK		
0008 800Ch	CMT1	Compare Match Timer Constant Register	CMCOR	16	16	2, 3 PCLKB	2 ICLK		
0008 8010h	CMT	Compare Match Timer Start Register 1	CMSTR1	16	16	2, 3 PCLKB	2 ICLK		
0008 8012h	CMT2	Compare Match Timer Control Register	CMCR	16	16	2, 3 PCLKB	2 ICLK		
0008 8014h	CMT2	Compare Match Timer Counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK		
0008 8016h	CMT2	Compare Match Timer Constant Register	CMCOR	16	16	2, 3 PCLKB	2 ICLK		
0008 8018h	CMT3	Compare Match Timer Control Register	CMCR	16	16	2, 3 PCLKB	2 ICLK		
0008 801Ah	CMT3	Compare Match Timer Counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK		
0008 801Ch	CMT3	Compare Match Timer Constant Register	CMCOR	16	16	2, 3 PCLKB	2 ICLK		
0008 8020h	WDT	WDT Refresh Register	WDTRR	8	8	2, 3 PCLKB	2 ICLK	WDTA	
0008 8022h	WDT	WDT Control Register	WDTCR	16	16	2, 3 PCLKB	2 ICLK		
0008 8024h	WDT	WDT Status Register	WDTSR	16	16	2, 3 PCLKB	2 ICLK		
0008 8026h	WDT	WDT Reset Control Register	WDTRCR	8	8	2, 3 PCLKB	2 ICLK		
0008 8030h	IWDT	IWDT Refresh Register	IWDTRR	8	8	2, 3 PCLKB	2 ICLK	IWDTa	
0008 8032h	IWDT	IWDT Control Register	IWDTCR	16	16	2, 3 PCLKB	2 ICLK		
0008 8034h	IWDT	IWDT Status Register	IWDTSR	16	16	2, 3 PCLKB	2 ICLK		
0008 8036h	IWDT	IWDT Reset Control Register	IWDTRCR	8	8	2, 3 PCLKB	2 ICLK		
0008 8038h	IWDT	IWDT Count Stop Control Register	IWDTCSTPR	8	8	2, 3 PCLKB	2 ICLK		
0008 80C0h	DA	D/A Data Register 0	DADR0	16	16	2, 3 PCLKB	2 ICLK	DAa	Not present in versions with 64 or 48 pins.
0008 80C2h	DA	D/A Data Register 1	DADR1	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 80C4h	DA	D/A Control Register	DACR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 80C5h	DA	DADRm Format Select Register	DADPR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 80C6h	DA	D/A A/D Synchronous Start Control Register	DAADSCR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 8280h	CRC	CRC Control Register	CRCCR	8	8	2, 3 PCLKB	2 ICLK	CRC	
0008 8281h	CRC	CRC Data Input Register	CRCDIR	8	8	2, 3 PCLKB	2 ICLK		
0008 8282h	CRC	CRC Data Output Register	CRCDOR	16	16	2, 3 PCLKB	2 ICLK		
0008 8300h	RIIC0	I^2C Bus Control Register 1	ICCR1	8	8	2, 3 PCLKB	2 ICLK	RIIC	
0008 8301h	RIIC0	I^2C Bus Control Register 2	ICCR2	8	8	2, 3 PCLKB	2 ICLK		
0008 8302h	RIIC0	I^2C Bus Mode Register 1	ICMR1	8	8	2, 3 PCLKB	2 ICLK		
0008 8303h	RIIC0	I^2C Bus Mode Register 2	ICMR2	8	8	2, 3 PCLKB	2 ICLK		
0008 8304h	RIIC0	I^2C Bus Mode Register 3	ICMR3	8	8	2, 3 PCLKB	2 ICLK		
0008 8305h	RIIC0	I^2C Bus Function Enable Register	ICFER	8	8	2, 3 PCLKB	2 ICLK		
0008 8306h	RIIC0	I^2C Bus Status Enable Register	ICSER	8	8	2, 3 PCLKB	2 ICLK		
0008 8307h	RIIC0	I^2C Bus Interrupt Enable Register	ICIER	8	8	2, 3 PCLKB	2 ICLK		

Table 4.1 List of I/O Registers (Address Order) (37/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
000C 2006h	GPT	General PWM Timer Hardware Source Clear Control Register	GTHCCR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK	GPT	
000C 2008h	GPT	General PWM Timer Hardware Start Source Select Register	GTHSSR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 200Ah	GPT	General PWM Timer Hardware Stop/Clear Source Select Register	GTHPSR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 200Ch	GPT	General PWM Timer Write-Protection Register	GTWP	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 200Eh	GPT	General PWM Timer Sync Register	GTSYNC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2010h	GPT	General PWM Timer External Trigger Input Interrupt Register	GTETINT	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2014h	GPT	General PWM Timer Buffer Operation Disable Register	GTBDR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2018h	GPT	General PWM Timer Start Write-Protection Register	GTSWP	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2080h	GPT	LOCO Count Control Register	LCCR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2082h	GPT	LOCO Count Status Register	LCST	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2084h	GPT	LOCO Count Value Register	LCNT	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2086h	GPT	LOCO Count Result Average Register	LCNTA	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2088h	GPT	LOCO Count Result Register 0	LCNT00	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 208Ah	GPT	LOCO Count Result Register 1	LCNT01	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 208Ch	GPT	LOCO Count Result Register 2	LCNT02	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 208Eh	GPT	LOCO Count Result Register 3	LCNT03	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2090h	GPT	LOCO Count Result Register 4	LCNT04	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2092h	GPT	LOCO Count Result Register 5	LCNT05	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2094h	GPT	LOCO Count Result Register 6	LCNT06	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2096h	GPT	LOCO Count Result Register 7	LCNT07	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2098h	GPT	LOCO Count Result Register 8	LCNT08	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 209Ah	GPT	LOCO Count Result Register 9	LCNT09	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 209Ch	GPT	LOCO Count Result Register 10	LCNT10	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 209Eh	GPT	LOCO Count Result Register 11	LCNT11	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 20A0h	GPT	LOCO Count Result Register 12	LCNT12	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 20A2h	GPT	LOCO Count Result Register 13	LCNT13	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 20A4h	GPT	LOCO Count Result Register 14	LCNT14	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 20A6h	GPT	LOCO Count Result Register 15	LCNT15	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 20A8h	GPT	LOCO Count Upper Permissible Deviation Register	LCNTDU	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 20AAh	GPT	LOCO Count Lower Permissible Deviation Register	LCNTDL	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2100h	GPT0	General PWM Timer I/O Control Register	GTIOR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2102h	GPT0	General PWM Timer Interrupt Output Setting Register	GTINTAD	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2104h	GPT0	General PWM Timer Control Register	GTCR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2106h	GPT0	General PWM Timer Buffer Enable Register	GTBER	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2108h	GPT0	General PWM Timer Count Direction Register	GTUDC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 210Ah	GPT0	General PWM Timer Interrupt, A/D Converter Start Request Skipping Setting Register	GTITC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 210Ch	GPT0	General PWM Timer Status Register	GTST	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 210Eh	GPT0	General PWM Timer Counter	GTCNT	16	16	2 to 5 PCLKA	2, 3 ICLK		
000C 2110h	GPT0	General PWM Timer Compare Capture Register A	GTCCRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2112h	GPT0	General PWM Timer Compare Capture Register B	GTCCRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2114h	GPT0	General PWM Timer Compare Capture Register C	GTCCRC	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2116h	GPT0	General PWM Timer Compare Capture Register D	GTCCRD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2118h	GPT0	General PWM Timer Compare Capture Register E	GTCCRE	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		

Table 4.1 List of I/O Registers (Address Order) (48/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
007F FFB0h	FLASH	Flash Status Register 0	FSTATR0	8	8	2, 3 FCLK	2, 3 ICLK	ROM	
007F FFB1h	FLASH	Flash Status Register 1	FSTATR1	8	8	2, 3 FCLK	2, 3 ICLK		
007F FFB2h	FLASH	Flash P/E Mode Entry Register	FENTRYR	16	16	2, 3 FCLK	2, 3 ICLK	ROM/ E2 DataFlash Memory	
007F FFB4h	FLASH	Flash Protection Register	FPROTR	16	16	2, 3 FCLK	2, 3 ICLK	ROM	
007F FFB6h	FLASH	Flash Reset Register	FRESETR	16	16	2, 3 FCLK	2, 3 ICLK		
007F FFBAh	FLASH	FCU Command Register	FCMDR	16	16	2, 3 FCLK	2, 3 ICLK		
007F FFC8h	FLASH	FCU Processing Switching Register	FCPSR	16	16	2, 3 FCLK	2, 3 ICLK		
007F FFCAh	FLASH	E2 DataFlash Blank Check Control Register	DFLBCCNT	16	16	2, 3 FCLK	2, 3 ICLK	E2 DataFlash Memory	
007F FFCCh	FLASH	Flash P/E Status Register	FPESTAT	16	16	2, 3 FCLK	2, 3 ICLK	ROM	
007F FFCEh	FLASH	E2 DataFlash Blank Check Status Register	DFLBCSTAT	16	16	2, 3 FCLK	2, 3 ICLK	E2 DataFlash Memory	
007F FFE8h	FLASH	Peripheral Clock Notification Register	PCKAR	16	16	2, 3 FCLK	2, 3 ICLK	ROM	

Note: • This table shows the maximum specifications of I/O registers. The I/O registers of individual products correspond to the list of functions given as Table 1.2. For details, refer to Table 1.2, Comparison of Functions for Different Packages.
Note 1. When the register is accessed while the USB is operating, a delay may be generated in accessing.
Note 2. Odd addresses are not accessible in 16-bit units. Obtain 16-bit access to the two registers by access to the address of TMOCNTL.
Note 3. Pins USB0 and RIIC1 are not present in 112-pin products.
Note 4. Pins USB0, RIIC1, and SCI3 are not present in 100-pin products.
Note 5. Pins GPT4 to GPT7, USB0, RSPI1, RIIC1, SCI2, SCI3, CAN1, AD, and S12AD1 are not present in 64- and 48-pin products.

Table 5.5 Permissible Output Currents

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

The following relation applies when the USB is in use under condition 1 or condition 2: Vcc = PLLVcc = Vcc_USB = 3.0 to 3.6 V.

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item		Symbol	Min.	Typ.	Max.	Unit
Permissible output low current (average value per pin)	All output pins (except for P71 to P76, P90 to P95, and RIIC pins)*1	I_{OL}	—	—	2.0	mA
	RIIC pins	I_{OL}	—	—	6.0	mA
	P71 to P76, and P90 to P95*2	I_{OL}	—	—	15.0	mA
Permissible output low current (max. value per pin)	All output pins (except for P71 to P76, P90 to P95, and RIIC pins)*1	I_{OL}	—	—	4.0	mA
	RIIC pins	I_{OL}	—	—	6.0	mA
	P71 to P76, and P90 to P95*2	I_{OL}	—	—	15.0	mA
Permissible output low current (total)	Total of output pins	ΣI_{OL}	—	—	110	mA
Permissible output high current (average value per pin)	All output pins (except for P71 to P76, P90 to P95, and USB0_DPUPE pin)*1	$-I_{OH}$	—	—	2.0	mA
	USB0_DPUPE pin	$-I_{OH}$	—	—	3.0	mA
	P71 to P76, and P90 to P95*2	$-I_{OH}$	—	—	5.0	mA
Permissible output high current (max. value per pin)	All output pins (except for P71 to P76, P90 to P95)*1	$-I_{OH}$	—	—	4.0	mA
	P71 to P76, and P90 to P95*2	$-I_{OH}$	—	—	5.0	mA
Permissible output high current (total)		$\Sigma-I_{OH}$	—	—	35	mA

Note 1. USB0_DP and USB0_DM are not included.

Note 2. For pins P71 to P76 and P90 to P95, I_{OL} = 15 mA (max.) and $-I_{OH}$ = 5 mA (max.). However, if several of the pins are to supply I_{OL} and $-I_{OH}$ of more than 2.0 mA at the same time, the number of pins should be six or less.

Caution: To protect the MCU’s reliability, the output current values should not exceed the values in this table.

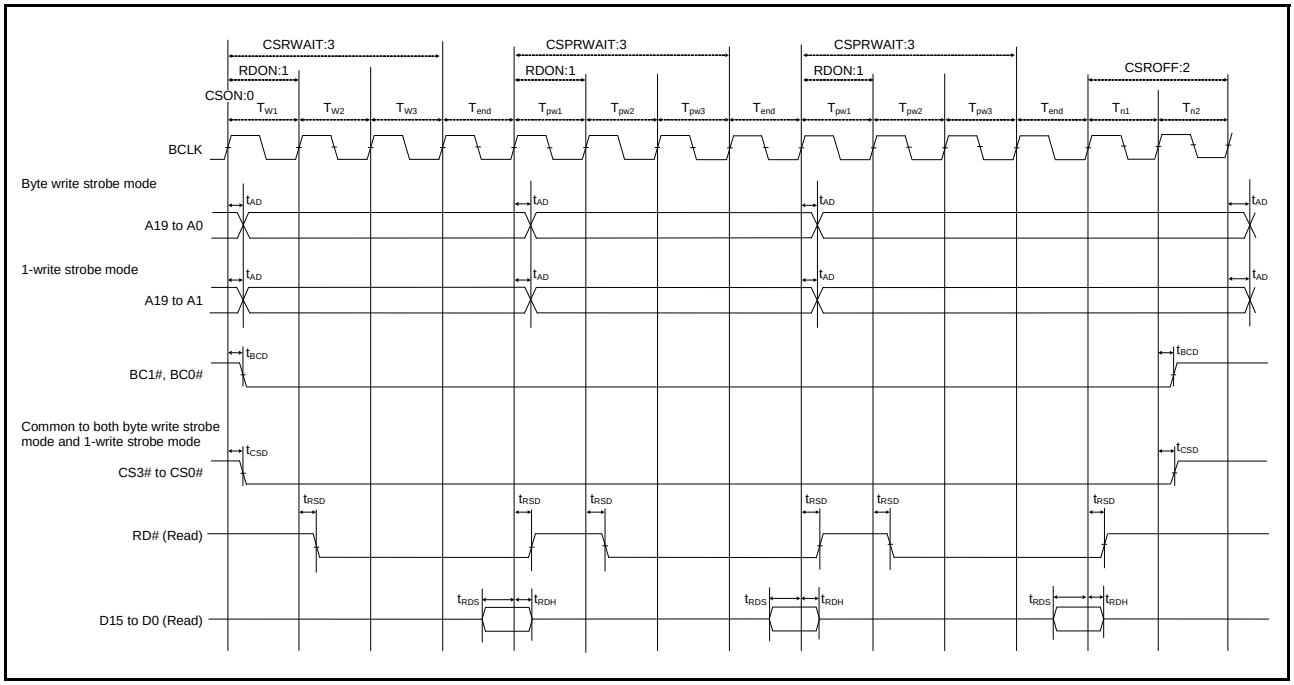
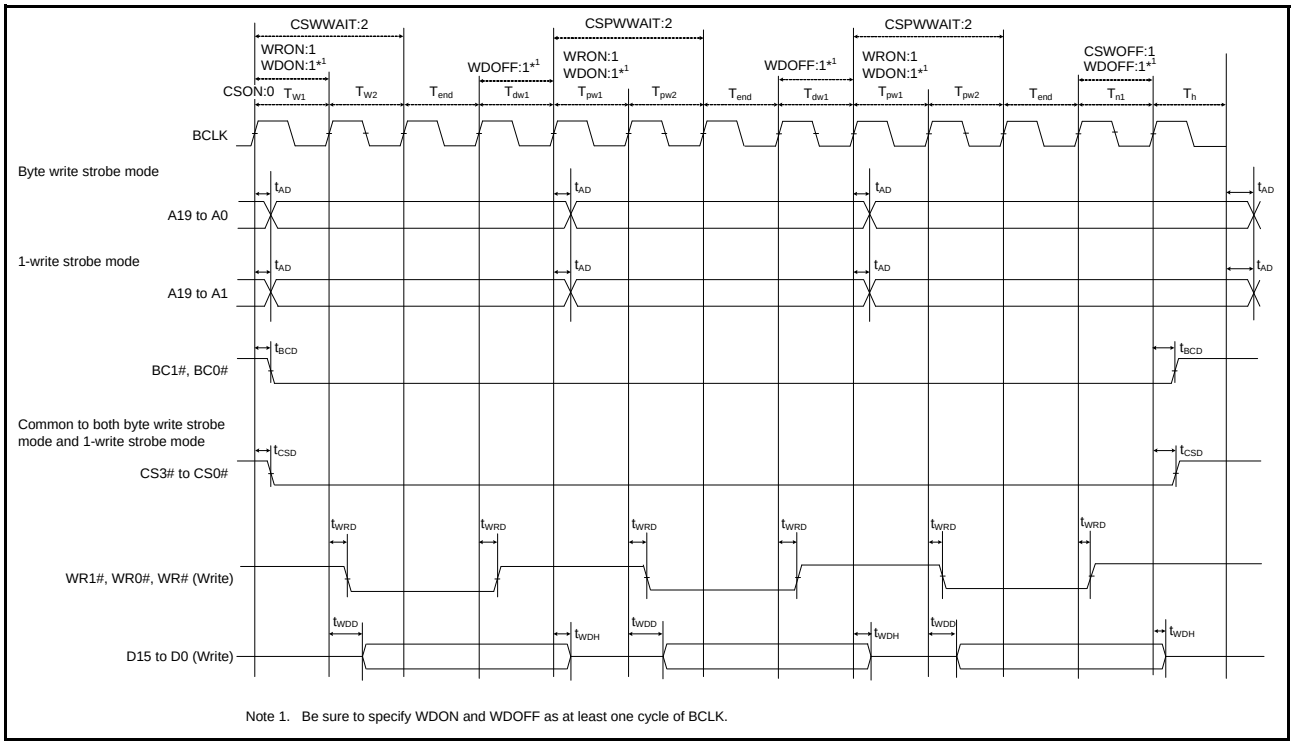


Figure 5.15 External Bus Timing/Page Read Cycle (Bus Clock Synchronized)



Note 1. Be sure to specify WDON and WDOFF as at least one cycle of BCLK.

Figure 5.16 External Bus Timing/Page Write Cycle (Bus Clock Synchronized)

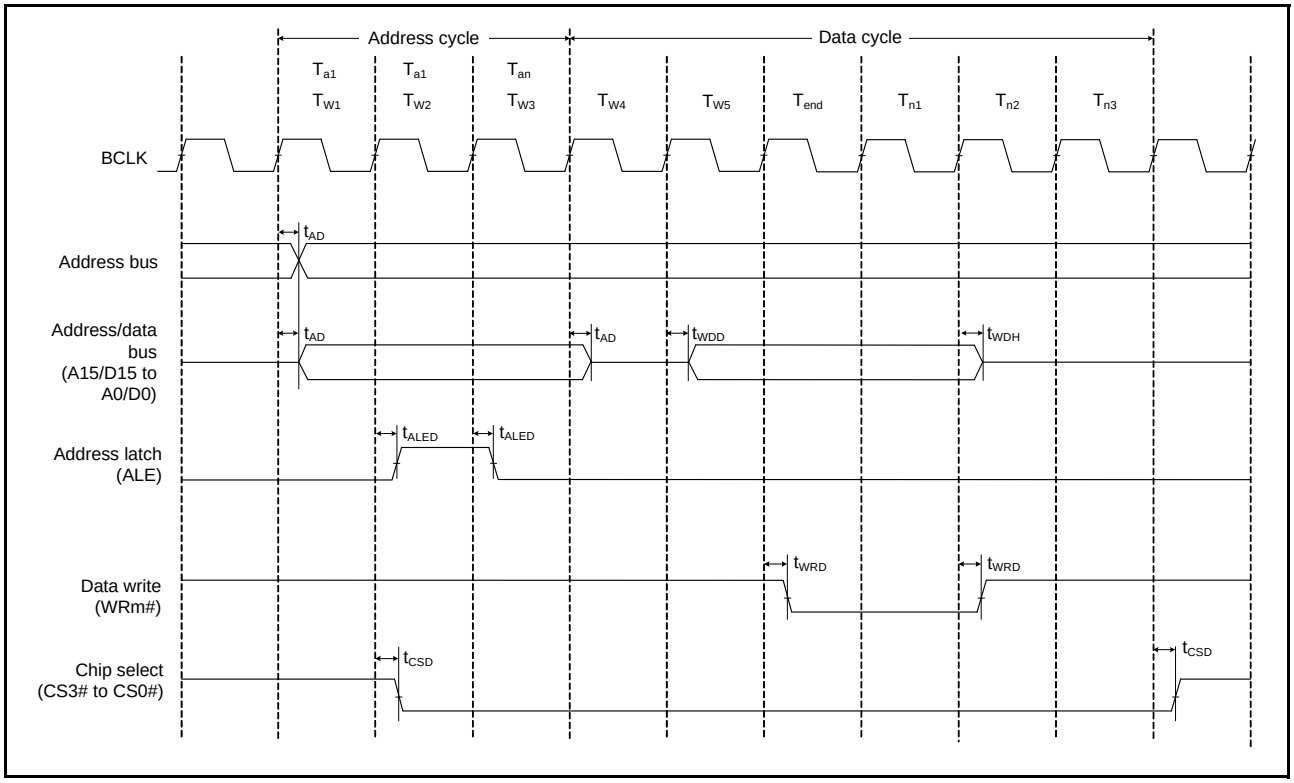


Figure 5.19 Example of External Bus Timing/Write Access Operation (Multiplexed)

Table 5.27 Power-on Reset Circuit and Voltage Detection Circuit Characteristics (2)

Condition: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0
$T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	V_{POR}	3.6	3.8	4.0	V	Figure 5.41
	Voltage detection circuit (LVD0)	V_{DET0}	4.0	4.2	4.4		Figure 5.42
	Voltage detection circuit (LVD1)*1	V_{DET1_8}	4.59	4.77	4.95		Figure 5.43
		V_{DET1_9}	4.05	4.23	4.41		
		V_{DET1_A}	4.32	4.50	4.68		
	Voltage detection circuit (LVD2)*2	V_{DET2_8}	4.59	4.77	4.95		Figure 5.44
		V_{DET2_9}	4.05	4.23	4.41		
		V_{DET2_A}	4.32	4.50	4.68		
Internal reset time	Power-on reset (POR)	t_{POR}		9.7		ms	Figure 5.41
	Voltage detection circuit (LVD0)	t_{LVD0}		9.7			Figure 5.42
	Voltage detection circuit (LVD1)	t_{LVD1}		0.9			Figure 5.43
	Voltage detection circuit (LVD2)	t_{LVD2}		0.9			Figure 5.44
Minimum VCC down time*3		t_{VOFF}	200	—	—	µs	Figure 5.41 to Figure 5.44
Response delay time		t_{DET}			200	µs	
LVD operation stabilization time (after LVD is enabled)		$Td_{(E-A)}$			3	µs	Figure 5.41 to Figure 5.44
Hysteresis width (LVD1 and LVD2)		V_{LVH}		80		mV	

Note 1. # in symbol $V_{DET1\_\#}$ indicates the value of the LVDLVLR.LVD1LVL[3:0] bits.
Note 2. # in symbol $V_{DET2\_\#}$ indicates the value of the LVDLVLR.LVD2LVL[3:0] bits.
Note 3. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{DET1}, and V_{DET2} for the POR/ LVD.

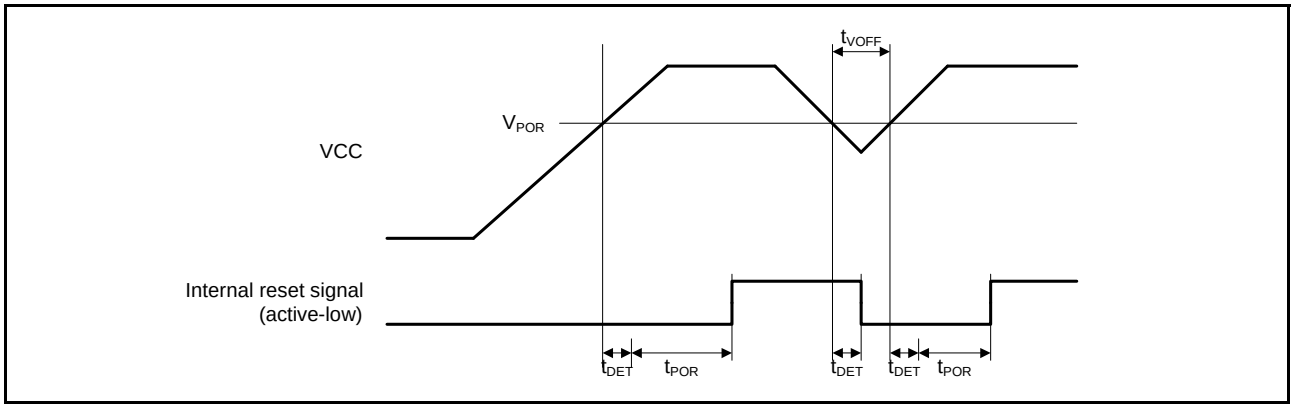


Figure 5.39 Power-on Reset Timing

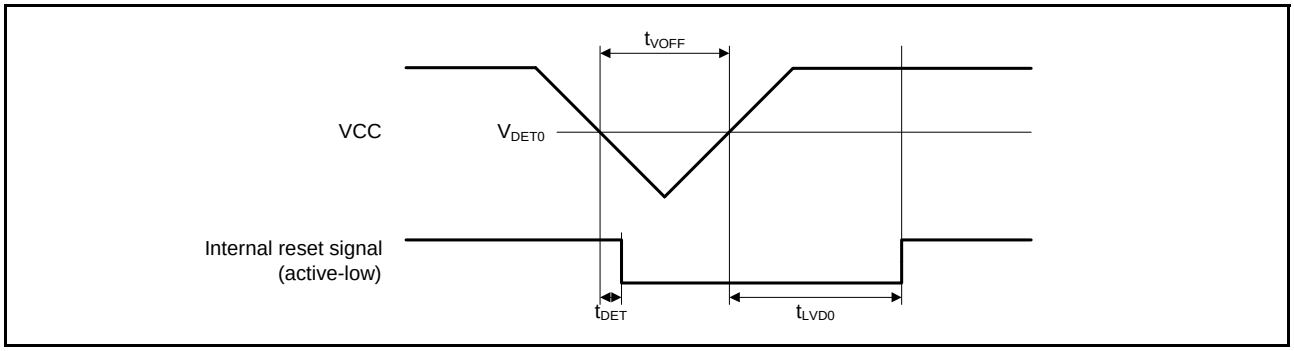


Figure 5.40 Voltage Detection Circuit Timing (V_{DET0})

6.2 DC Characteristics

Table 6.2 DC Characteristics (1)

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	IRQ input pin MTU3 input pin POE3 input pin SCI input pin A/D trigger input pin GPT input pin RES#, NMI	V_{IH}	VCC × 0.8	—	VCC + 0.3	V	
		V_{IL}	–0.3	—	VCC × 0.2		
		ΔV_T	VCC × 0.06	—	—		
	RIIC input pin (IICBus operating)	V_{IH}	VCC × 0.7	—	5.8		
		V_{IL}	–0.3	—	VCC × 0.3		
		ΔV_T	VCC × 0.05	—	—		
	Port 4 (also used as an analog port)	V_{IH}	AVCC0 × 0.8	—	AVCC0 + 0.3		
		V_{IL}	–0.3	—	AVCC0×0.2		
	Ports for 5 V tolerant*1	V_{IH}	VCC × 0.8	—	5.8		
		V_{IL}	–0.3	—	VCC × 0.2		
Input high voltage (except for Schmitt trigger input pin)	MD pin, EMLE	V_{IH}	VCC × 0.9	—	VCC + 0.3		
	EXTAL, TCK, RSPI input pin		VCC × 0.8	—	VCC + 0.3		
	RIIC input pin (SMBus operating)		2.1	—	VCC + 0.3		
Input low voltage (except for Schmitt trigger input pin)	MD pin, EMLE	V_{IL}	–0.3	—	VCC × 0.1		
	EXTAL, TCK, RSPI input pin		–0.3	—	VCC × 0.2		
	RIIC input pin (SMBus operating)		–0.3	—	0.8		
Output high voltage	All output pins	V_{OH}	VCC – 0.5	—	—	V	I_{OH} = –1 mA
Output low voltage	All output pins (except for RIIC pins)	V_{OL}	—	—	0.5	V	I_{OL} = 1.0 mA
	RIIC pins		—	—	0.4		I_{OL} = 3 mA
			—	—	0.6		I_{OL} = 6 mA
Input leakage current	RES#, MD pin, EMLE, Ports 4 and PE2	$\lvert I_{in} \rvert$	—	—	1.0	µA	V_{in} = 0V, V_{in} = VCC
Three-state leakage current (off state)	Ports for 5V tolerant	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	V_{in} = 0V, V_{in} = 5.5 V
			—	—	5.0		
Input capacitance	All input pins (except for ports PB1 and PB2)	C_{in}	—	—	15	pF	V_{in} = 0V, f = 1 MHz, T_a = 25ºC
	Ports PB1 and PB2		—	—	30		

Note 1. Ports 0, 1, 2, 3, 7, 9, A, B, and D are 5 V tolerant.

6.7 ROM (Flash Memory for Code Storage) Characteristics

Table 6.20 ROM (Flash Memory for Code Storage) Characteristics (1)

Condition: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Temperature range for the programming/erasure operation: $T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Reprogram/erase cycle*1	N_{pec}	1000	—	—	Times	
Data hold time	t_{DRP}	30*2	—	—	Year	Ta = +85°C

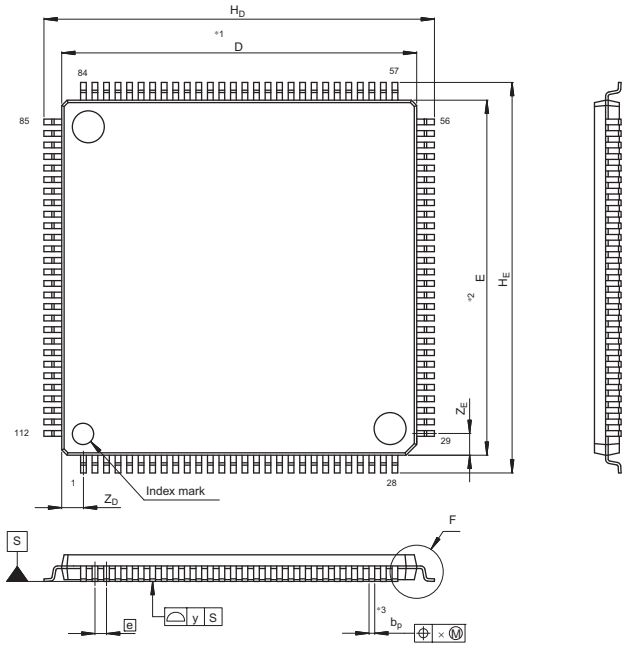
Note 1. Definition of reprogram/erase cycle:
The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 128-byte programming is performed 16 times for different addresses in 2-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).
Note 2. The value is obtained from the reliability test.

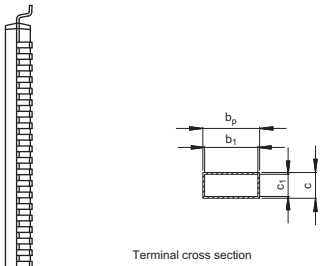
Table 6.21 ROM (Flash Memory for Code Storage) Characteristics (2)

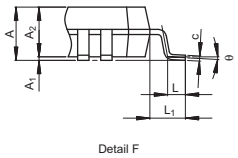
Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Temperature range for the programming/erasure operation: $T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item		Symbol	min	typ	max	Unit	Test Conditions
Programming time	128 bytes	t_{P128}	—	1	10	ms	FCLK = 50MHz $N_{PEC} \leq 100$
	4 Kbytes	t_{P4K}	—	23	50	ms	
	16 Kbytes	t_{P16K}	—	90	200	ms	
	128 bytes	t_{P128}	—	1.2	12	ms	FCLK=50MHz $N_{PEC} > 100$
	4 Kbytes	t_{P4K}	—	27.6	60	ms	
	16 Kbytes	t_{P16K}	—	108	240	ms	
Erasure time	4 Kbytes	t_{E4K}	—	25	60	ms	FCLK=50MHz $N_{PEC} \leq 100$
	16 Kbytes	t_{E16K}	—	100	240	ms	
	4 Kbytes	t_{E4K}	—	30	72	ms	FCLK=50MHz $N_{PEC} > 100$
	16 Kbytes	t_{E16K}	—	120	288	ms	
Suspend delay time during programming		t_{SPD}	—	—	120	µs	Figure 6.31 FCLK = 50MHz
First suspend delay time during erasing (in suspend priority mode)		t_{SESD1}	—	—	120	µs	
Second suspend delay time during erasing (in suspend priority mode)		t_{SESD2}	—	—	1.7	ms	
Suspend delay time during erasing (in erasure priority mode)		t_{SEED}	—	—	1.7	ms	
FCU reset time		t_{FCUR}	35	—	—	µs	

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP112-20x20-0.65	PLQP0112JA-A	FP-112E/FP-112EV	1.2g







NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	19.9	20.0	20.1
E	19.9	20.0	20.1
A_2	—	1.4	—
H_D	21.8	22.0	22.2
H_E	21.8	22.0	22.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.27	0.32	0.37
b_1	—	0.30	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z_D	—	1.225	—
Z_E	—	1.225	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure C 112-Pin LQFP (PLQP0112JA-A)