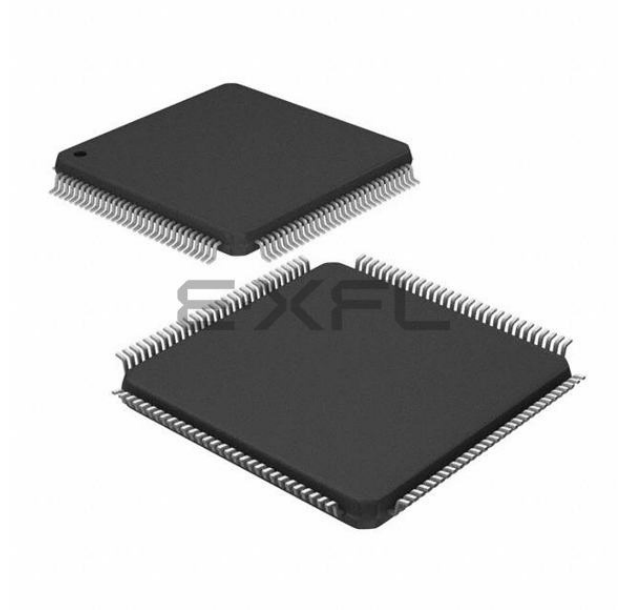
Renesas Electronics America Inc - R5F563TBADFA#V1 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	72
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x10b, 8x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	120-LQFP
Supplier Device Package	120-LQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f563tbadfa-v1

Table 1.1 Outline of Specifications (2/7)

Classification	Module/Function	Description
Clock	Clock generation circuit	• Main clock oscillator, low-speed on-chip oscillator, PLL frequency synthesizer, and dedicated on-chip oscillator for the IWDT • Main-clock oscillation stop detection • Separate frequency-division and multiplication settings for the system clock (ICLK), peripheral module clock (PCLKA), peripheral module clock (PCLKB), AD clock (PCLKC), FlashIF clock (FCLK) and S12AD clock (PCLKD). The CPU and other bus masters run in synchronization with the system clock (ICLK): Up to 100 MHz Multi-function timer pulse unit 3 and general PWM timer run in synchronization with PCLKA: Up to 100 MHz Peripheral modules run in synchronization with the peripheral module clock (PCLKB): Up to 50 MHz Flash IF run in synchronization with the FlashIF clock (FCLK): Up to 50 MHz Devices connected to the external bus run in synchronization with the external bus clock (BCLK): Up to 50 MHz 10-bit A/D converter runs in synchronization with the AD clock (PCLKC): Up to 100 MHz 12-bit A/D converter runs in synchronization with the S12AD clock (PCLKD): Up to 50 MHz
Clock	Clock frequency accuracy measurement circuit (CAC)	The frequency of the following clocks can be measured; the main clock oscillator, PLL circuit, and IWDT-dedicated on-chip oscillator.
Reset		RES# pin reset, power-on reset, voltage-monitoring reset, independent watchdog timer reset, watchdog timer reset, deep software standby reset, and software reset
Voltage detection circuit		When the voltage on VCC passes the voltage detection level (Vdet), an internal reset or internal interrupt is generated.
Low power consumption	Low power consumption facilities	• Module stop function • Four low power consumption modes Sleep mode, all-module clock stop mode, software standby mode, and deep software standby mode
Interrupt	Interrupt controller (ICUb)	• Peripheral function interrupts: Up to 169 sources • External interrupts: Up to 8 (pins IRQ0 to IRQ7) • Software interrupts: One source • Non-maskable interrupts: 6 sources • Sixteen levels specifiable for the order of priority
External bus extension		• The external address space can be divided into four areas (CS0 to CS3), each with independent control of access settings. Capacity of each area: 1 Mbyte (CS0 to CS3) A chip-select signal (CS0# to CS3#) can be output for each area. Each area is specifiable as an 8- or 16-bit bus space The data arrangement in each area is selectable as little or big endian (only for data). • Bus format: Separate bus, multiplex bus • Wait control • Write buffer facility
DMA	DMA controller (DMACA)	• 4 channels • Three transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Software trigger, external interrupts, and interrupt requests from peripheral functions
	Data transfer controller (DTCa)	• Three transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Software interrupt activation register settings, external interrupts, and interrupt requests from peripheral functions

Table 1.1 Outline of Specifications (5/7)

Classification	Module/Function	Description
Communication function	I^2C bus interfaces (RIIC)	• 2 channels Communication formats I^2C bus format/SMBus format Supports the multi-master Max. transfer rate: 400 kbps
	CAN module (CAN)	• 1 channels • Compliance with the ISO11898-1 specification (standard frame and extended frame) • 32 mailboxes per channel
	Serial peripheral interfaces (RSPI)	• 2 channels • RSPI transfer facility Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPCK (RSPI clock) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) Capable of handling serial transfer as a master or slave • Data formats Switching between MSB first and LSB first The number of bits in each transfer can be changed to any number of bits from 8 to 16, or to 20, 24, or 32 bits. 128-bit buffers for transmission and reception Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) • Buffered structure Double buffers for both transmission and reception • Max. transfer rate In master mode: [144-, 120-, 112- and 100-pin versions] 25 Mbps [64- and 48-pin versions] 12.5 Mbps In slave mode: 6.25 Mbps
12-bit A/D converter (S12ADB) [144-, 120-, 112- and 100-pin versions]		• 12 bits (4 channels x 2 unit) • 12-bit resolution • Conversion time 1.0 μs per channel (clock for S12ADB, PCLKD (A/D conversion clock ADCLK) = 50 MHz, AVCC0 = 4.0 to 5.5 V) 2.0 μs per channel (clock for S12ADB, PCLKD (A/D conversion clock ADCLK) = 25 MHz, AVCC0 = 3.0 to 3.6 V) • Operating modes Scan mode (single-cycle scan mode/continuous scan mode/group scan mode) Group A priority control (only for the group scan mode) • Sample-and-hold function A common sample-and-hold circuit for units is included. Additionally, sample-and-hold circuit for each unit is included. (three channels per unit) • Self-diagnostic function The self-diagnostic function internally generates three analog input voltages (VREFL0, VREFH0 x 1/2, VREFH0). • Double trigger mode (duplication of A/D converted data) • Input signal amplification function using programmable gain amplifier (three channels per unit) Amplification factors: 2.0 times, 2.5 times, 3.077 times, 3.636 times, 4.0 times, 4.444 times, 5.0 times, 5.714 times, 6.667 times, 10.0 times, 13.333 times (total of 11 steps) • Three ways to start A/D conversion Conversion can be started by software, a conversion start trigger from a timer (MTU3 or GPT), or an external trigger signal. • Window comparators (three channels per unit)

Table 1.7 List of Pins and Pin Functions (112-Pin LQFP) (1/4)

Pin Number 112-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3, GPT, POE3, CAC)	Communications (SCIc, SCId, RSPI, RIIC, CAN)	Interrupt	S12ADB, AD, DA
1		PE5	BCLK			IRQ0	
2	EMLE						
3	VSS						
4		P01	RD#		CTS0#/RTS0#/SS0#		
5	VCL						
6		P00	CS1#	CACREF			
7	MD/FINED						
8		PE4	A10	POE10#/MTCLKC		IRQ1	
9		PE3	A11	POE11#/MTCLKD		IRQ2-DS	
10	RES#						
11	XTAL						
12	VSS						
13	EXTAL						
14	VCC						
15		PE2		POE10#		NMI	
16		PE1	WR0#/WR#		CTS12#/RTS12#/ SS12#/SSLA3/SSLB3		
17		PE0	WR1#/BC1#/ WAIT#		SSLA2/SSLB2/CRX1	IRQ7	
18		PD7		GTIOC0A	CTS0#/RTS0#/SS0#/ SSLA1/SSLB1/CTX1		
19		PD6		GTIOC0B	SSLA0/SSLB0		
20		PD5		GTIOC1A	RXD1/SMISO1/SSCL1	IRQ6	
21		PD4		GTIOC1B	SCK1		
22		PD3		GTIOC2A	TXD1/SMOSI1/SSDA1		
23		PD2	CS2#	GTIOC2B	MOSIA/MOSIB		
24		PD1	CS0#	GTIOC3A	MISOA/MISOB		
25		PD0	A12	GTIOC3B	RSPCKA/RSPCKB		
26	TDI	PF4	CS3#		RXD1*1		
27	TCK/FINEC	PF3			TXD1/SMOSI1/SSDA1		
28	TDO	PF2	CS1#		RXD1/SMISO1/ SSCL1/TXD1*1	IRQ5	
29		PB7	A19		SCK12		
30		PB6	A18		RXD12/SMISO12/ SSCL12/RXDX12/ CRX1	IRQ2	
31		PB5	A17		TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/CTX1		
32	PLLVCC						
33		PB4	A16	POE8#/GTETRG0		IRQ3-DS	
34	PLLVSS						
35		PB3	A15	MTIOC0A/CACREF	SCK0		
36		PB2		MTIOC0B	TXD0/SMOSI0/ SSDA0/SDA0		
37		PB1		MTIOC0C	RXD0/SMISO0/ SSCL0/SCL0	IRQ4	

Table 1.8 List of Pins and Pin Functions (100-Pin LQFP) (1/3)

Pin Number 100-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3, GPT, POE3, CAC)	Communications (SCIc, SCId, RSPI, RIIC, CAN)	Interrupt	S12ADB, AD, DA
1		PE5	BCLK			IRQ0	
2	EMLE						
3	VSS						
4		P01	RD#		CTS0#/RTS0#/SS0#		
5	VCL						
6		P00	CS1#	CACREF			
7	MD/FINED						
8		PE4	A10	POE10#/MTCLKC		IRQ1	
9		PE3	A11	POE11#/MTCLKD		IRQ2-DS	
10	RES#						
11	XTAL						
12	VSS						
13	EXTAL						
14	VCC						
15		PE2		POE10#		NMI	
16		PE1	WR0#/WR#		CTS12#/RTS12#/ SS12#/SSLA3/SSLB3		
17		PE0	WR1#/BC1#/ WAIT#		SSLA2/SSLB2/CRX1	IRQ7	
18	TRST#	PD7		GTIOC0A	CTS0#/RTS0#/SS0#/ SSLA1/SSLB1/CTX1		
19	TMS	PD6		GTIOC0B	SSLA0/SSLB0		
20	TDI	PD5		GTIOC1A	RXD1/SMISO1/SSCL1	IRQ6	
21	TCK/FINEC	PD4		GTIOC1B	SCK1		
22	TDO	PD3		GTIOC2A	TXD1/SMOSI1/SSDA1		
23		PD2	CS2#	GTIOC2B	MOSIA/MOSIB		
24		PD1	CS0#	GTIOC3A	MISOA/MISOB		
25		PD0	A12	GTIOC3B	RSPCKA/RSPCKB		
26		PB7	A19		SCK12		
27		PB6	A18		RXD12/SMISO12/ SSCL12/RXDX12/ CRX1	IRQ2	
28		PB5	A17		TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/CTX1		
29	PLLVCC						
30		PB4	A16	POE8#/GTETRG0		IRQ3-DS	
31	PLLVSS						
32		PB3	A15	MTIOC0A/CACREF	SCK0		
33		PB2		MTIOC0B	TXD0/SMOSI0/ SSDA0/SDA0		
34		PB1		MTIOC0C	RXD0/SMISO0/ SSCL0/SCL0	IRQ4	
35		PB0	A14	MTIOC0D	MOSIA/MOSIB		
36		PA5		MTIOC1A	RXD0/SMISO0/ SSCL0/ MISOA/MISOB		ADTRG1#

2. CPU

The RX CPU has sixteen general-purpose registers, nine control registers, and one accumulator used for DSP instructions.

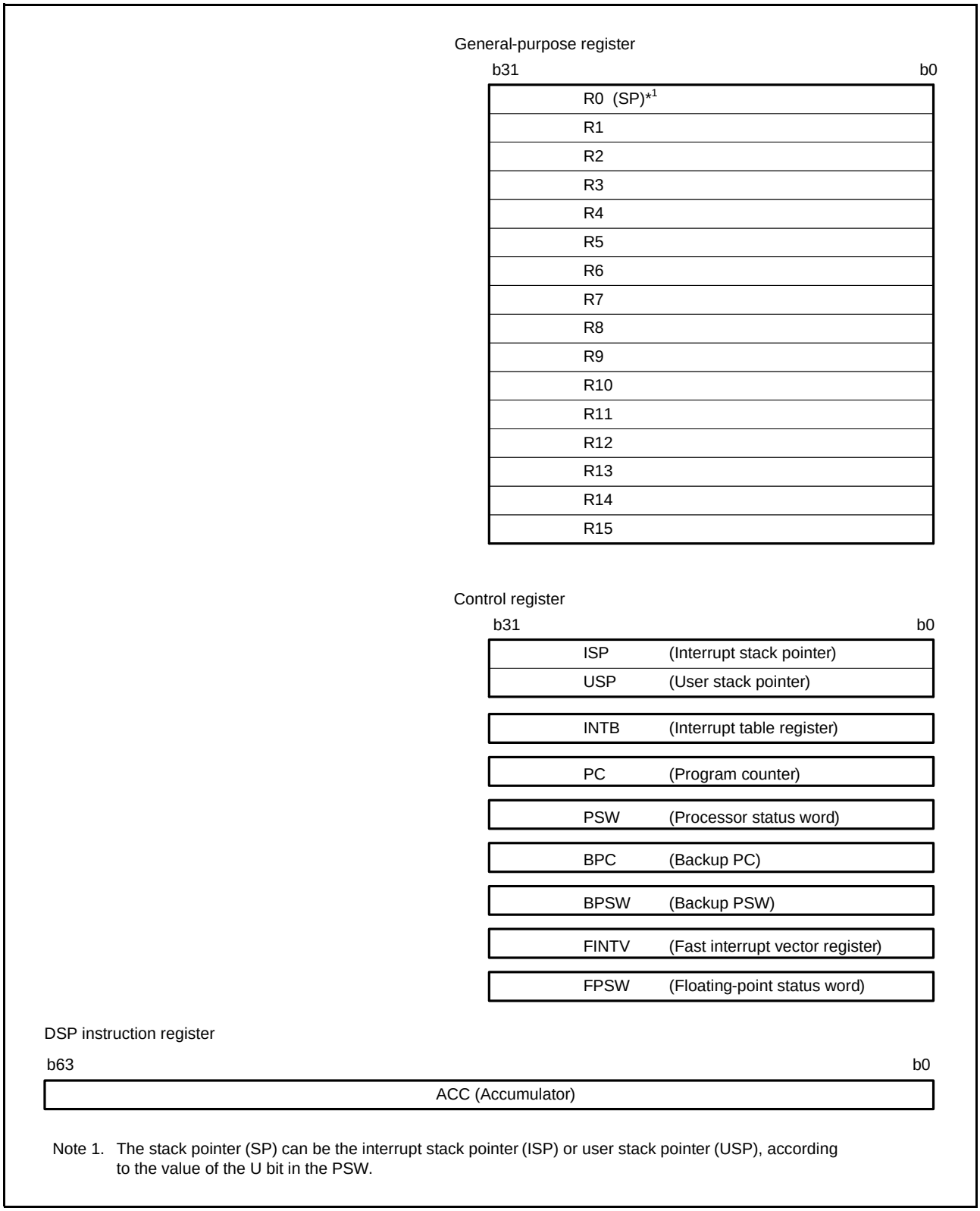


Figure 2.1 Register Set of the CPU

4.1 I/O Register Addresses (Address Order)

Table 4.1 List of I/O Registers (Address Order) (1/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 0000h	SYSTEM	Mode Monitor Register	MDMONR	16	16	3 ICLK		Operating Modes	
0008 0002h	SYSTEM	Mode Status Register	MDSR	16	16	3 ICLK			Not present in versions with 64 or 48 pins.
0008 0006h	SYSTEM	System Control Register 0	SYSCR0	16	16	3 ICLK			
0008 0008h	SYSTEM	System Control Register 1	SYSCR1	16	16	3 ICLK			
0008 000Ch	SYSTEM	Standby Control Register	SBYCR	16	16	3 ICLK		Low Power Consumption	
0008 0010h	SYSTEM	Module Stop Control Register A	MSTPCRA	32	32	3 ICLK			
0008 0014h	SYSTEM	Module Stop Control Register B	MSTPCRB	32	32	3 ICLK			
0008 0018h	SYSTEM	Module Stop Control Register C	MSTPCRC	32	32	3 ICLK			
0008 0020h	SYSTEM	System Clock Control Register	SCKCR	32	32	3 ICLK		Clock Generation Circuit	
0008 0024h	SYSTEM	System Clock Control Register 2	SCKCR2	16	16	3 ICLK			Not present in versions with 64 or 48 pins.
0008 0026h	SYSTEM	System Clock Control Register 3	SCKCR3	16	16	3 ICLK			
0008 0028h	SYSTEM	PLL Control Register	PLLCR	16	16	3 ICLK			
0008 002Ah	SYSTEM	PLL Control Register 2	PLLCR2	8	8	3 ICLK			
0008 0030h	SYSTEM	External Bus Clock Control Register	BCKCR	8	8	3 ICLK			Not present in versions with 64 or 48 pins.
0008 0032h	SYSTEM	Main Clock Oscillator Control Register	MOSCCR	8	8	3 ICLK			
0008 0034h	SYSTEM	Low-Speed On-Chip Oscillator Control Register	LOCOCR	8	8	3 ICLK			
0008 0035h	SYSTEM	IWDT-Dedicated On-Chip Oscillator Control Register	ILOCOCR	8	8	3 ICLK			
0008 0040h	SYSTEM	Oscillation Stop Detection Control Register	OSTDCR	8	8	3 ICLK			
0008 0041h	SYSTEM	Oscillation Stop Detection Status Register	OSTDSR	8	8	3 ICLK			
0008 00A2h	SYSTEM	Main Clock Oscillator Wait Control Register	MOSCWTCR	8	8	3 ICLK		Low Power Consumption	
0008 00A6h	SYSTEM	PLL Wait Control Register	PLLWTCR	8	8	3 ICLK			
0008 00C0h	SYSTEM	Reset Status Register 2	RSTSR2	8	8	3 ICLK		Resets	
0008 00C2h	SYSTEM	Software Reset Register	SWRR	16	16	3 ICLK			
0008 00E0h	SYSTEM	Voltage Monitoring 1 Circuit Control Register 1	LVD1CR1	8	8	3 ICLK		LVDA	
0008 00E1h	SYSTEM	Voltage Monitoring 1 Circuit Status Register	LVD1SR	8	8	3 ICLK			
0008 00E2h	SYSTEM	Voltage Monitoring 2 Circuit Control Register 1	LVD2CR1	8	8	3 ICLK			
0008 00E3h	SYSTEM	Voltage Monitoring 2 Circuit Status Register	LVD2SR	8	8	3 ICLK			
0008 03FEh	SYSTEM	Protect Register	PRCR	16	16	3 ICLK		Register Write Protection Function	
0008 1300h	BSC	Bus Error Status Clear Register	BERCLR	8	8	2 ICLK		Buses	
0008 1304h	BSC	Bus Error Monitoring Enable Register	BEREN	8	8	2 ICLK			
0008 1308h	BSC	Bus Error Status Register 1	BERSR1	8	8	2 ICLK			
0008 130Ah	BSC	Bus Error Status Register 2	BERSR2	16	16	2 ICLK			
0008 1310h	BSC	Bus Priority Control Register	BUSPRI	16	16	2 ICLK			
0008 2000h	DMAC0	DMA Source Address Register	DMSAR	32	32	2 ICLK		DMACA	
0008 2004h	DMAC0	DMA Destination Address Register	DMDAR	32	32	2 ICLK			
0008 2008h	DMAC0	DMA Transfer Count Register	DMCRA	32	32	2 ICLK			
0008 200Ch	DMAC0	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK			
0008 2010h	DMAC0	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK			
0008 2013h	DMAC0	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK			
0008 2014h	DMAC0	DMA Address Mode Register	DMAMD	16	16	2 ICLK			
0008 2018h	DMAC0	DMA Offset Register	DMOFR	32	32	2 ICLK			
0008 201Ch	DMAC0	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK			
0008 201Dh	DMAC0	DMA Software Start Register	DMREQ	8	8	2 ICLK			
0008 201Eh	DMAC0	DMA Status Register	DMSTS	8	8	2 ICLK			

Table 4.1 List of I/O Registers (Address Order) (3/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 3024h	BSC	CS2 Wait Control Register 1	CS2WCR1	32	32	1, 2 BCLK		Buses	Not present in versions with 64 or 48 pins.
0008 3028h	BSC	CS2 Wait Control Register 2	CS2WCR2	32	32	1, 2 BCLK			Not present in versions with 64 or 48 pins.
0008 3032h	BSC	CS3 Mode Register	CS3MOD	16	16	1, 2 BCLK			Not present in versions with 64 or 48 pins.
0008 3034h	BSC	CS3 Wait Control Register 1	CS3WCR1	32	32	1, 2 BCLK			Not present in versions with 64 or 48 pins.
0008 3038h	BSC	CS3 Wait Control Register 2	CS3WCR2	32	32	1, 2 BCLK			Not present in versions with 64 or 48 pins.
0008 3802h	BSC	CS0 Control Register	CS0CR	16	16	1, 2 BCLK			Not present in versions with 64 or 48 pins.
0008 380Ah	BSC	CS0 Recovery Cycle Register	CS0REC	16	16	1, 2 BCLK			Not present in versions with 64 or 48 pins.
0008 3812h	BSC	CS1 Control Register	CS1CR	16	16	1, 2 BCLK			Not present in versions with 64 or 48 pins.
0008 381Ah	BSC	CS1 Recovery Cycle Register	CS1REC	16	16	1, 2 BCLK			Not present in versions with 64 or 48 pins.
0008 3822h	BSC	CS2 Control Register	CS2CR	16	16	1, 2 BCLK			Not present in versions with 64 or 48 pins.
0008 382Ah	BSC	CS2 Recovery Cycle Register	CS2REC	16	16	1, 2 BCLK			Not present in versions with 64 or 48 pins.
0008 3832h	BSC	CS3 Control Register	CS3CR	16	16	1, 2 BCLK			Not present in versions with 64 or 48 pins.
0008 383Ah	BSC	CS3 Recovery Cycle Register	CS3REC	16	16	1, 2 BCLK			Not present in versions with 64 or 48 pins.
0008 3880h	BSC	CS Recovery Cycle Insertion Enable Register	CSRECEN	16	16	1, 2 BCLK			Not present in versions with 64 or 48 pins.
0008 6400h	MPU	Region-0 Start Page Number Register	RSPAGE0	32	32	1 ICLK		MPU	
0008 6404h	MPU	Region-0 End Page Number Register	REPAGE0	32	32	1 ICLK			
0008 6408h	MPU	Region-1 Start Page Number Register	RSPAGE1	32	32	1 ICLK			
0008 640Ch	MPU	Region-1 End Page Number Register	REPAGE1	32	32	1 ICLK			
0008 6410h	MPU	Region-2 Start Page Number Register	RSPAGE2	32	32	1 ICLK			
0008 6414h	MPU	Region-2 End Page Number Register	REPAGE2	32	32	1 ICLK			
0008 6418h	MPU	Region-3 Start Page Number Register	RSPAGE3	32	32	1 ICLK			
0008 641Ch	MPU	Region-3 End Page Number Register	REPAGE3	32	32	1 ICLK			
0008 6420h	MPU	Region-4 Start Page Number Register	RSPAGE4	32	32	1 ICLK			
0008 6424h	MPU	Region-4 End Page Number Register	REPAGE4	32	32	1 ICLK			
0008 6428h	MPU	Region-5 Start Page Number Register	RSPAGE5	32	32	1 ICLK			
0008 642Ch	MPU	Region-5 End Page Number Register	REPAGE5	32	32	1 ICLK			
0008 6430h	MPU	Region-6 Start Page Number Register	RSPAGE6	32	32	1 ICLK			
0008 6434h	MPU	Region-6 End Page Number Register	REPAGE6	32	32	1 ICLK			
0008 6438h	MPU	Region-7 Start Page Number Register	RSPAGE7	32	32	1 ICLK			
0008 643Ch	MPU	Region-7 End Page Number Register	REPAGE7	32	32	1 ICLK			
0008 6500h	MPU	Memory-Protection Enable Register	MPEN	32	32	1 ICLK			
0008 6504h	MPU	Background Access Control Register	MPBAC	32	32	1 ICLK			
0008 6508h	MPU	Memory-Protection Error Status-Clearing Register	MPECLR	32	32	1 ICLK			
0008 650Ch	MPU	Memory-Protection Error Status Register	MPESTS	32	32	1 ICLK			
0008 6514h	MPU	Data Memory-Protection Error Address Register	MPDEA	32	32	1 ICLK			
0008 6520h	MPU	Region Search Address Register	MPSA	32	32	1 ICLK			
0008 6524h	MPU	Region Search Operation Register	MPOPS	16	16	1 ICLK			
0008 6526h	MPU	Region Invalidation Operation Register	MPOPI	16	16	1 ICLK			
0008 6528h	MPU	Instruction-Hit Region Register	MHITI	32	32	1 ICLK			
0008 652Ch	MPU	Data-Hit Region Register	MHITD	32	32	1 ICLK			

Table 4.1 List of I/O Registers (Address Order) (37/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
000C 2006h	GPT	General PWM Timer Hardware Source Clear Control Register	GTHCCR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK	GPT	
000C 2008h	GPT	General PWM Timer Hardware Start Source Select Register	GTHSSR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 200Ah	GPT	General PWM Timer Hardware Stop/Clear Source Select Register	GTHPSR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 200Ch	GPT	General PWM Timer Write-Protection Register	GTWP	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 200Eh	GPT	General PWM Timer Sync Register	GTSYNC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2010h	GPT	General PWM Timer External Trigger Input Interrupt Register	GTETINT	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2014h	GPT	General PWM Timer Buffer Operation Disable Register	GTBDR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2018h	GPT	General PWM Timer Start Write-Protection Register	GTSWP	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2080h	GPT	LOCO Count Control Register	LCCR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2082h	GPT	LOCO Count Status Register	LCST	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2084h	GPT	LOCO Count Value Register	LCNT	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2086h	GPT	LOCO Count Result Average Register	LCNTA	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2088h	GPT	LOCO Count Result Register 0	LCNT00	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 208Ah	GPT	LOCO Count Result Register 1	LCNT01	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 208Ch	GPT	LOCO Count Result Register 2	LCNT02	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 208Eh	GPT	LOCO Count Result Register 3	LCNT03	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2090h	GPT	LOCO Count Result Register 4	LCNT04	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2092h	GPT	LOCO Count Result Register 5	LCNT05	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2094h	GPT	LOCO Count Result Register 6	LCNT06	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2096h	GPT	LOCO Count Result Register 7	LCNT07	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2098h	GPT	LOCO Count Result Register 8	LCNT08	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 209Ah	GPT	LOCO Count Result Register 9	LCNT09	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 209Ch	GPT	LOCO Count Result Register 10	LCNT10	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 209Eh	GPT	LOCO Count Result Register 11	LCNT11	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 20A0h	GPT	LOCO Count Result Register 12	LCNT12	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 20A2h	GPT	LOCO Count Result Register 13	LCNT13	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 20A4h	GPT	LOCO Count Result Register 14	LCNT14	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 20A6h	GPT	LOCO Count Result Register 15	LCNT15	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 20A8h	GPT	LOCO Count Upper Permissible Deviation Register	LCNTDU	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 20AAh	GPT	LOCO Count Lower Permissible Deviation Register	LCNTDL	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2100h	GPT0	General PWM Timer I/O Control Register	GTIOR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2102h	GPT0	General PWM Timer Interrupt Output Setting Register	GTINTAD	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2104h	GPT0	General PWM Timer Control Register	GTCR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2106h	GPT0	General PWM Timer Buffer Enable Register	GTBER	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2108h	GPT0	General PWM Timer Count Direction Register	GTUDC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 210Ah	GPT0	General PWM Timer Interrupt, A/D Converter Start Request Skipping Setting Register	GTITC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 210Ch	GPT0	General PWM Timer Status Register	GTST	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 210Eh	GPT0	General PWM Timer Counter	GTCNT	16	16	2 to 5 PCLKA	2, 3 ICLK		
000C 2110h	GPT0	General PWM Timer Compare Capture Register A	GTCCRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2112h	GPT0	General PWM Timer Compare Capture Register B	GTCCRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2114h	GPT0	General PWM Timer Compare Capture Register C	GTCCRC	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2116h	GPT0	General PWM Timer Compare Capture Register D	GTCCRD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2118h	GPT0	General PWM Timer Compare Capture Register E	GTCCRE	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		

Table 4.1 List of I/O Registers (Address Order) (45/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
000C 2A24h	GPT6	A/D Converter Start Request Timing Register A	GTADTRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK	GPT	Not present in versions with 64 or 48 pins.
000C 2A26h	GPT6	A/D Converter Start Request Timing Buffer Register A	GTADTBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A28h	GPT6	A/D Converter Start Request Timing Double-Buffer Register A	GTADTDBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A2Ch	GPT6	A/D Converter Start Request Timing Register B	GTADTRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A2Eh	GPT6	A/D Converter Start Request Timing Buffer Register B	GTADTBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A30h	GPT6	A/D Converter Start Request Timing Double-Buffer Register B	GTADTDBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A34h	GPT6	General PWM Timer Output Negate Control Register	GTONCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A36h	GPT6	General PWM Timer Dead Time Control Register	GTDTCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A38h	GPT6	General PWM Timer Dead Time Value Register U	GTDVU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A3Ah	GPT6	General PWM Timer Dead Time Value Register D	GTDVD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A3Ch	GPT6	General PWM Timer Dead Time Buffer Register U	GTDBU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A3Eh	GPT6	General PWM Timer Dead Time Buffer Register D	GTDBD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A40h	GPT6	General PWM Timer Output Protection Function Status Register	GTSOS	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A42h	GPT6	General PWM Timer Output Protection Function Temporary Release Register	GTSOTR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A80h	GPT7	General PWM Timer I/O Control Register	GTIOR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A82h	GPT7	General PWM Timer Interrupt Output Setting Register	GTINTAD	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A84h	GPT7	General PWM Timer Control Register	GTCR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A86h	GPT7	General PWM Timer Buffer Enable Register	GTBER	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A88h	GPT7	General PWM Timer Count Direction Register	GTUDC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A8Ah	GPT7	General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register	GTITC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A8Ch	GPT7	General PWM Timer Status Register	GTST	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A8Eh	GPT7	General PWM Timer Counter	GTCNT	16	16	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A90h	GPT7	General PWM Timer Compare Capture Register A	GTCCRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A92h	GPT7	General PWM Timer Compare Capture Register B	GTCCRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A94h	GPT7	General PWM Timer Compare Capture Register C	GTCCRC	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A96h	GPT7	General PWM Timer Compare Capture Register D	GTCCRD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A98h	GPT7	General PWM Timer Compare Capture Register E	GTCCRE	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A9Ah	GPT7	General PWM Timer Compare Capture Register F	GTCCRF	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A9Ch	GPT7	General PWM Timer Cycle Setting Register	GTPR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A9Eh	GPT7	General PWM Timer Cycle Setting Buffer Register	GTPBR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2AA0h	GPT7	General PWM Timer Cycle Setting Double-Buffer Register	GTPDBR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2AA4h	GPT7	A/D Converter Start Request Timing Register A	GTADTRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2AA6h	GPT7	A/D Converter Start Request Timing Buffer Register A	GTADTBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.

Table 5.6 Permissible Power Consumption (G version product only)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0V
AVCC0 = AVCC = 4.0 to 5.5V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Ta = -40 to +105°C. Ta is common to conditions 1 to 3.

Item	Symbol	Typ.	Max.	Unit	Test Conditions
Total permissible power consumption*1	Pd	—	345	mW	85°C < Ta ≤ 105°C

Note: • Please contact Renesas Electronics sales office for derating of operation under Ta = +85°C to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.

Note 1. The total power consumption of the whole chip including output current.

5.3 AC Characteristics

Table 5.7 Operation Frequency Value

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS =PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item		Symbol	Min.	Typ.	Max.	Unit
Operation frequency	System clock (ICLK)	f	—	—	100	MHz
	Peripheral module clock (PCLK) *1		—	—	50	
	Timer module clock (PCLKA)		—	—	100	
	AD clock (PCLKC)		—	—	100	
	S12AD clock (PCLKD)		—	—	50	
	FlashIF clock (FCLK)		—	—	50	
	External bus clock (BCLK)		—	—	50	
	BCLK pin output		—	—	25	
	USB clock (UCLK)		—	—	48	

Note 1. The PCLK must run at a frequency of at least 24 MHz when the USB is in use.

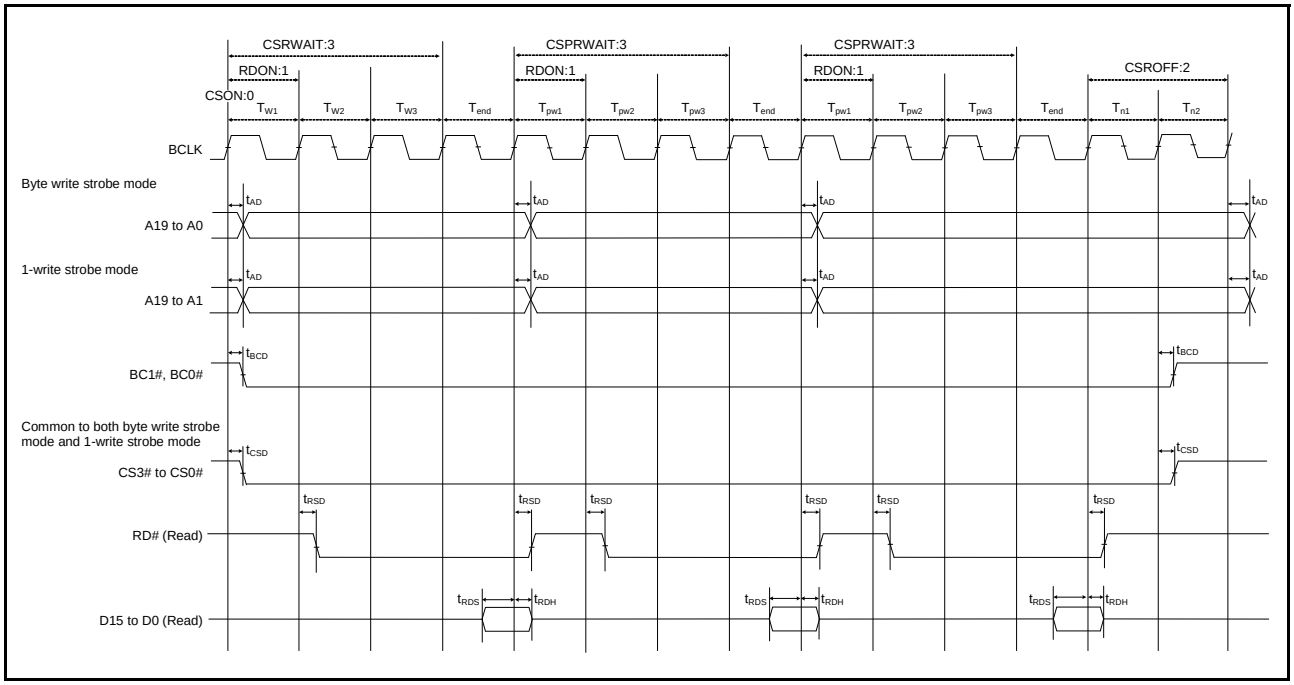
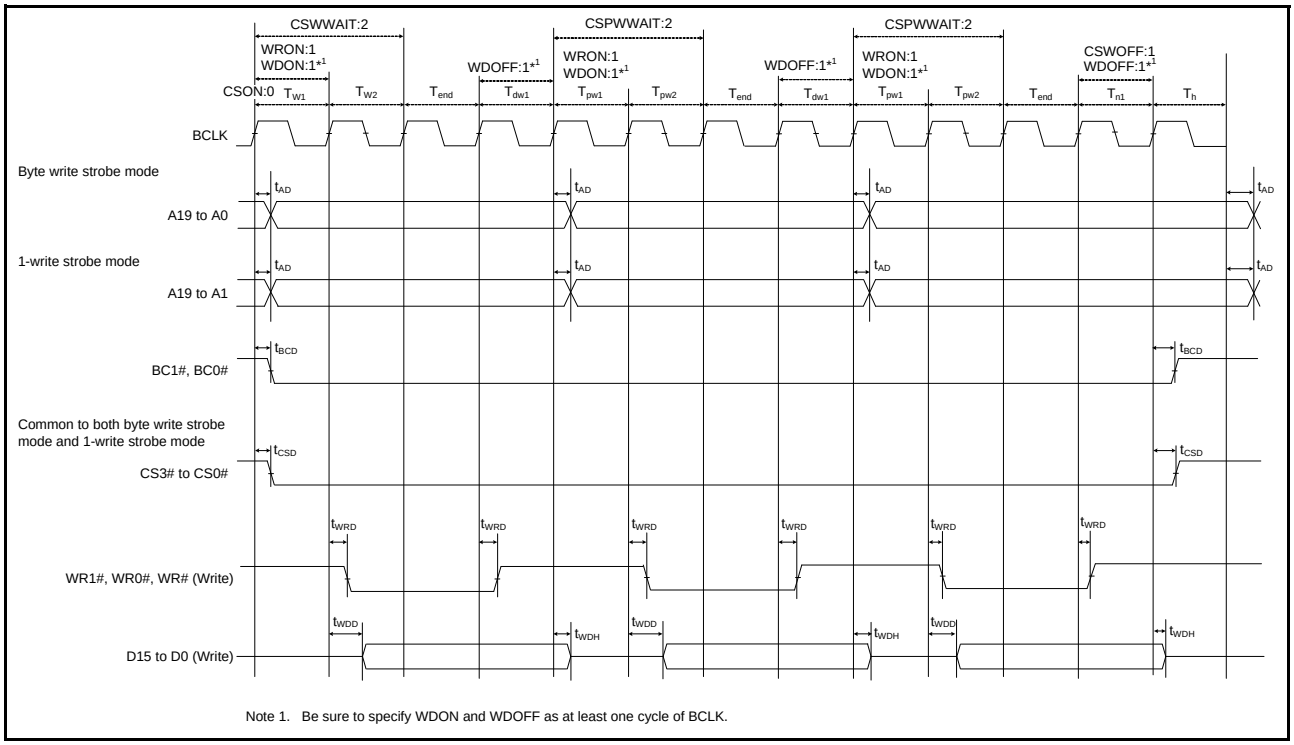


Figure 5.15 External Bus Timing/Page Read Cycle (Bus Clock Synchronized)



Note 1. Be sure to specify WDON and WDOFF as at least one cycle of BCLK.

Figure 5.16 External Bus Timing/Page Write Cycle (Bus Clock Synchronized)

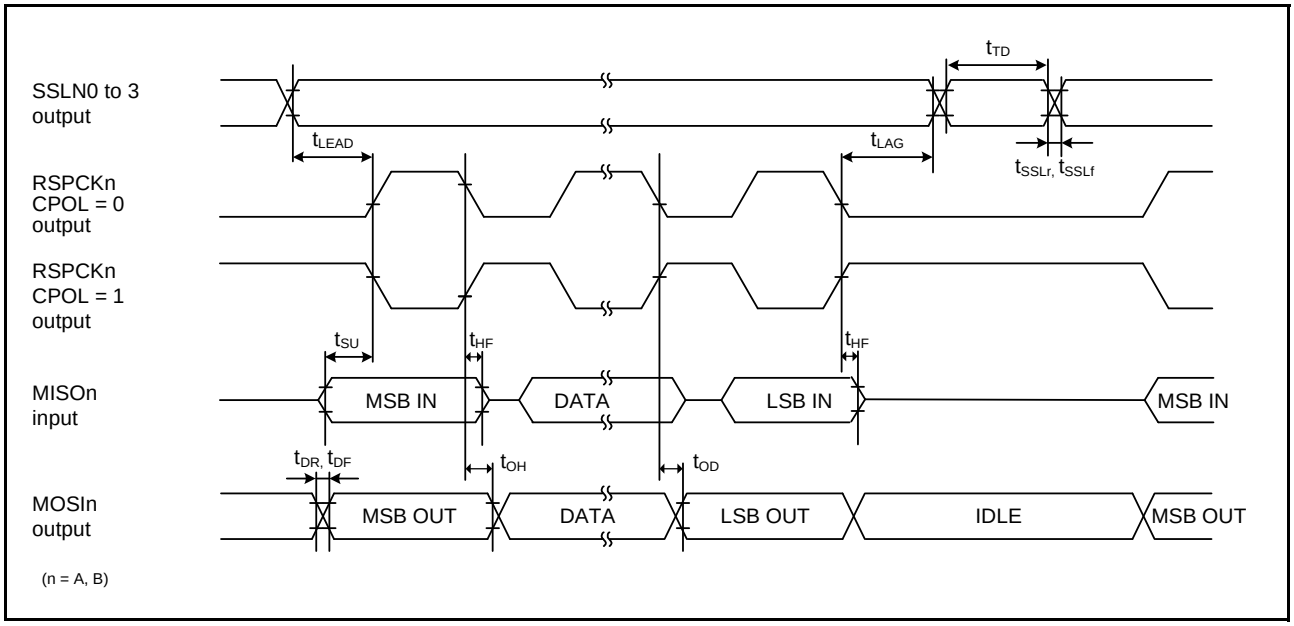


Figure 5.31 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKB Division Ratio Set to 1/2)

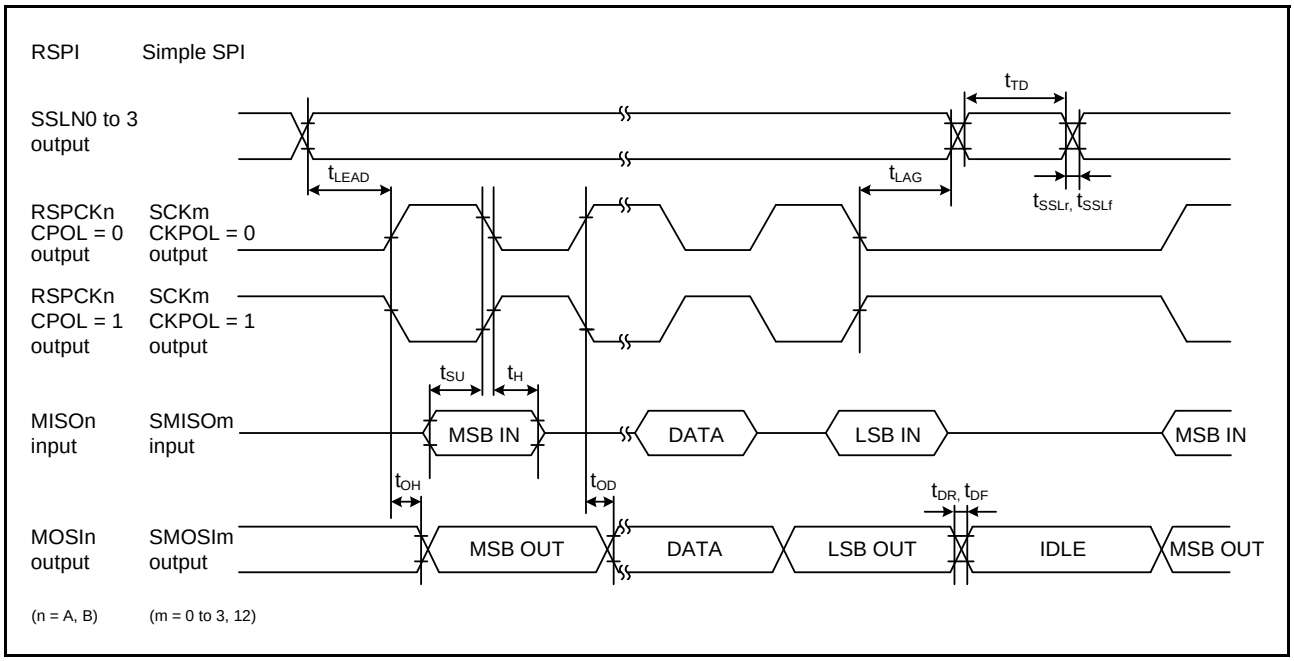


Figure 5.32 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKB Division Ratio Set to a Value Other Than 1/2) and Simple SPI Timing (Master, CKPH = 0)

5.7 Power-on Reset Circuit and Voltage Detection Circuit Characteristics

Table 5.26 Power-on Reset Circuit and Voltage Detection Circuit Characteristics (1)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” and “Condition 2” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. T_a is common to conditions 1 and 2.

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	V_{POR}	2.46	2.58	2.7	V	Figure 5.41
	Voltage detection circuit (LVD0)	V_{DET0}	2.7	2.82	2.94		Figure 5.42
	Voltage detection circuit (LVD1)*1	V_{DET1_8}	2.75	2.90	3.05		Figure 5.43
		V_{DET1_9}	2.70	2.85	3.00		
		V_{DET1_A}	2.73	2.88	3.03		
	Voltage detection circuit (LVD2)*2	V_{DET2_8}	2.75	2.9	3.05		Figure 5.44
		V_{DET2_9}	2.70	2.85	3.00		
		V_{DET2_A}	2.73	2.88	3.03		
Internal reset time	Power-on reset (POR)	t_{POR}		9.7		ms	Figure 5.41
	Voltage detection circuit (LVD0)	t_{LVD0}		9.7			Figure 5.42
	Voltage detection circuit (LVD1)	t_{LVD1}		0.9			Figure 5.43
	Voltage detection circuit (LVD2)	t_{LVD2}		0.9			Figure 5.44
Minimum VCC down time*3		t_{VOFF}	200	—	—	µs	Figure 5.41 and Figure 5.42
Response delay time		t_{DET}			200	µs	
LVD operation stabilization time (after LVD is enabled)		$Td_{(E-A)}$			3	µs	Figure 5.41 to Figure 5.44
Hysteresis width (LVD1 and LVD2)		V_{LVH}		80		mV	

Note 1. # in symbol $V_{DET1\_\#}$ indicates the value of the LVDLVLR.LVD1LVL[3:0] bits.
Note 2. # in symbol $V_{DET2\_\#}$ indicates the value of the LVDLVLR.LVD2LVL[3:0] bits.
Note 3. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{DET1}, and V_{DET2} for the POR/ LVD.

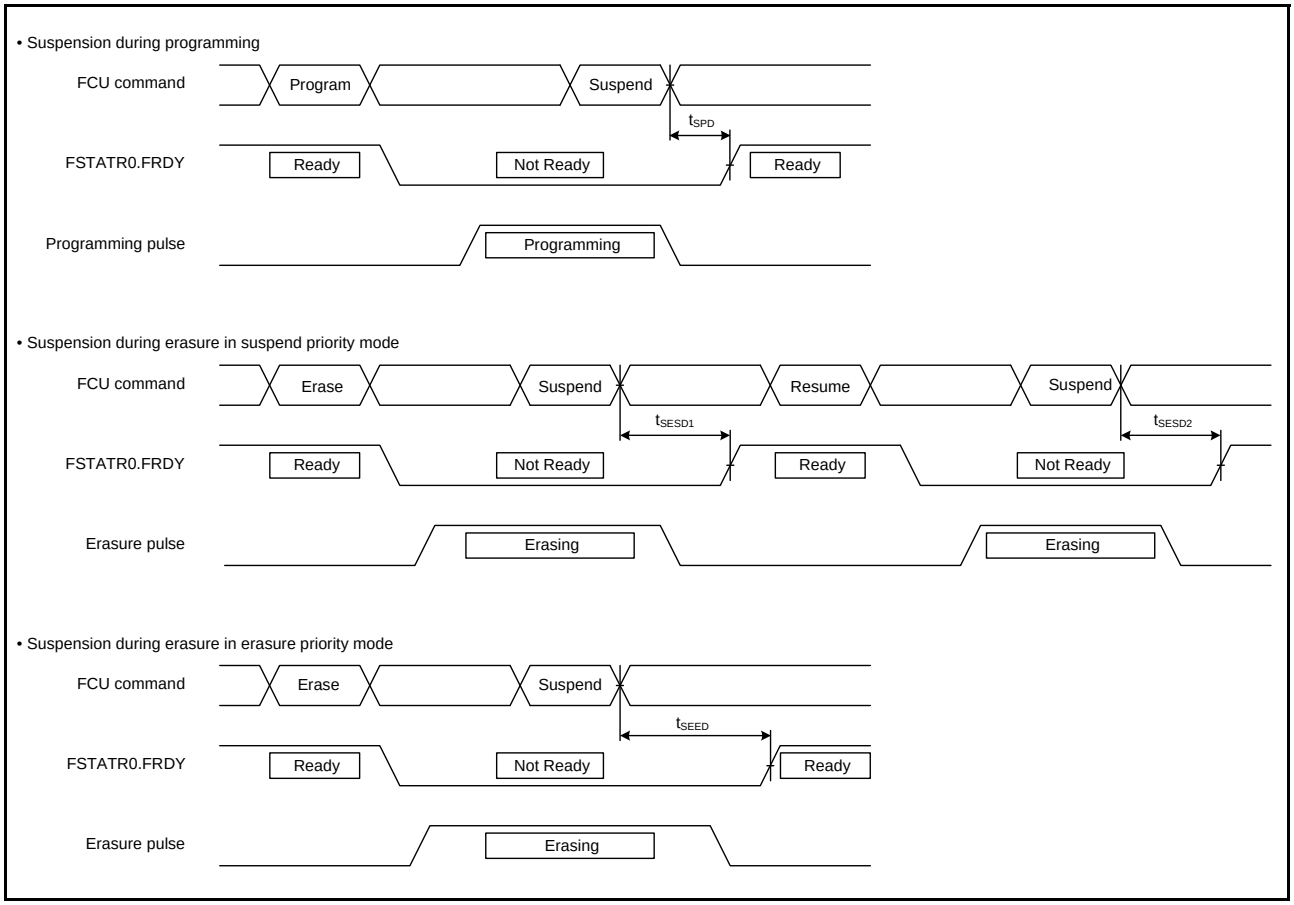


Figure 5.44 Flash Memory Program/Erase Suspend Timing

Note 4. This is calculated from the formula below, where n is the number of cycles set by the PLLWTCR.PSTS[4:0] bits.

$$t_{PLLWT1} = t_{PLL1} + \frac{n + 131072}{f_{PLL}}$$

$$t_{PLLWT2} = t_{PLL2} + \frac{n + 131072}{f_{PLL}} = t_{MAINOSC} + t_{PLL1} + \frac{n + 131072}{f_{PLL}}$$

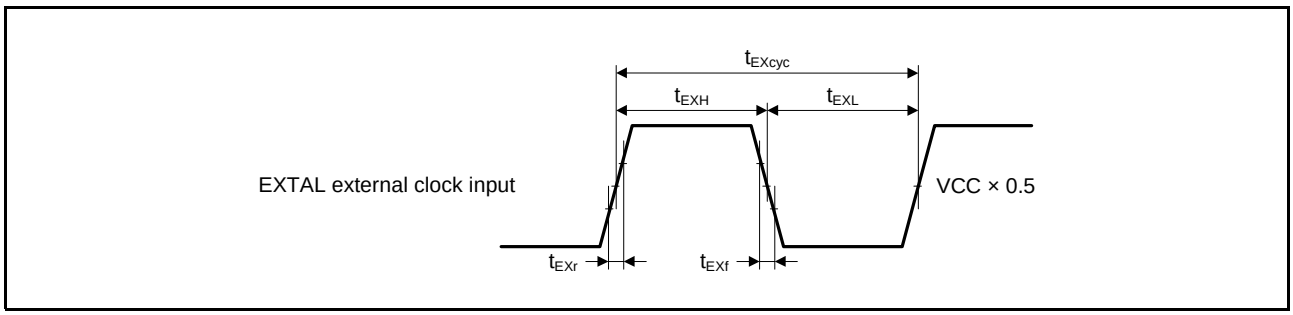


Figure 6.1 EXTAL External Clock Input Timing

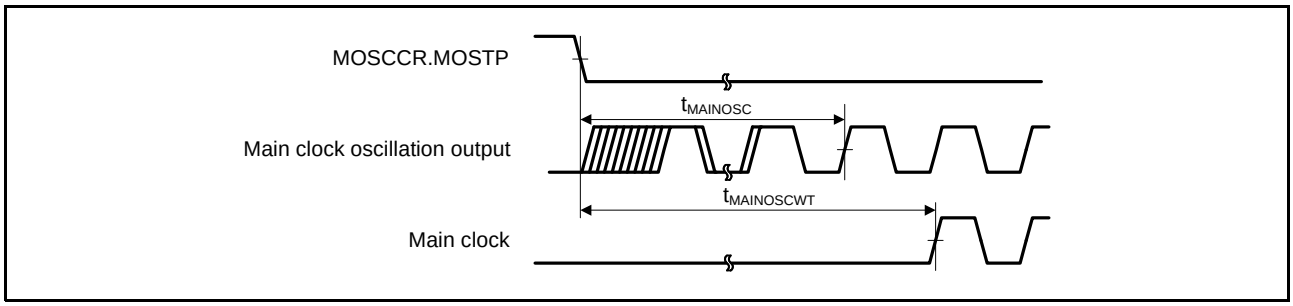


Figure 6.2 Main Clock Oscillation Start Timing

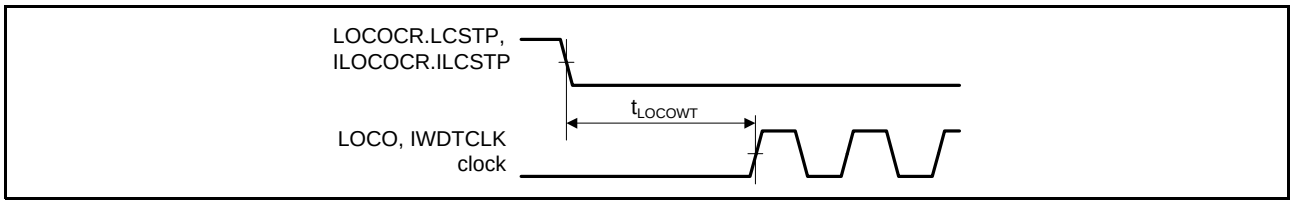


Figure 6.3 LOCO, IWDTCLK Clock Oscillation Start Timing

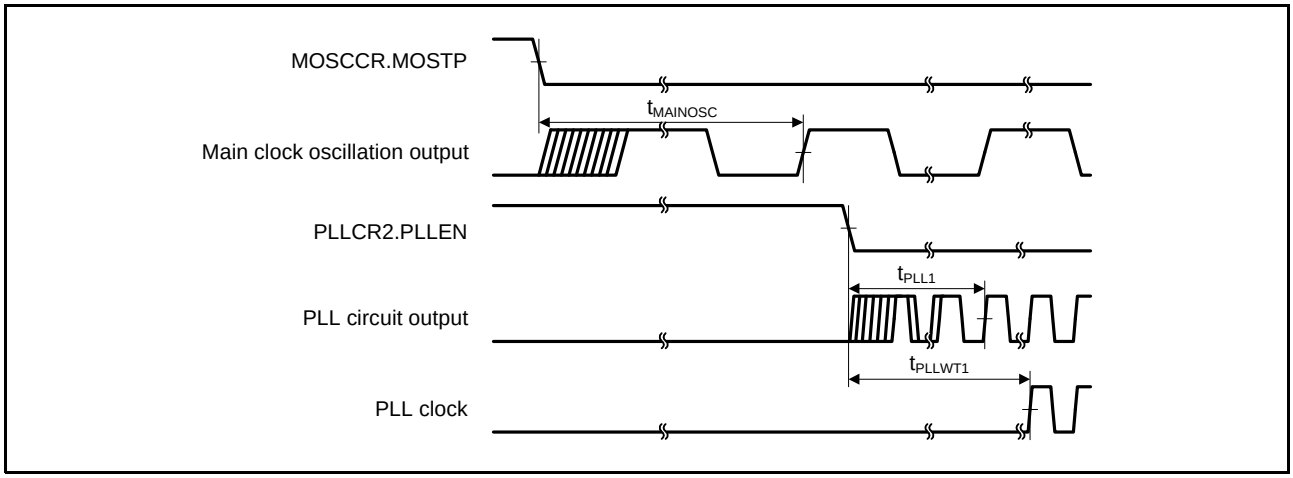


Figure 6.4 PLL Clock Oscillation Start Timing (PLL is Operated after Main Clock Oscillation Has Settled)

6.3.2 Reset Timing

Table 6.8 Reset Timing

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item		Symbol	Min	Typ	Max.	Unit	Test Conditions
RES# pulse width	Power-on	t_{RESWP}	2	—	—	ms	Figure 6.6
	Deep software standby mode	t_{RESWD}	1	—	—	ms	Figure 6.7
	Software standby mode	t_{RESWS}	1	—	—	ms	
	Other than above (except for programming or erasure of the ROM or E2 DataFlash memory or blank checking of the E2 DataFlash memory)	t_{RESW}	200	—	—	µs	
Wait time after RES# cancellation		t_{RESWT}	59	—	60	t_{cyc}	
Internal reset time (independent watchdog timer reset, watchdog timer reset, software reset)		t_{RESW2}	112	—	120	t_{cyc}	

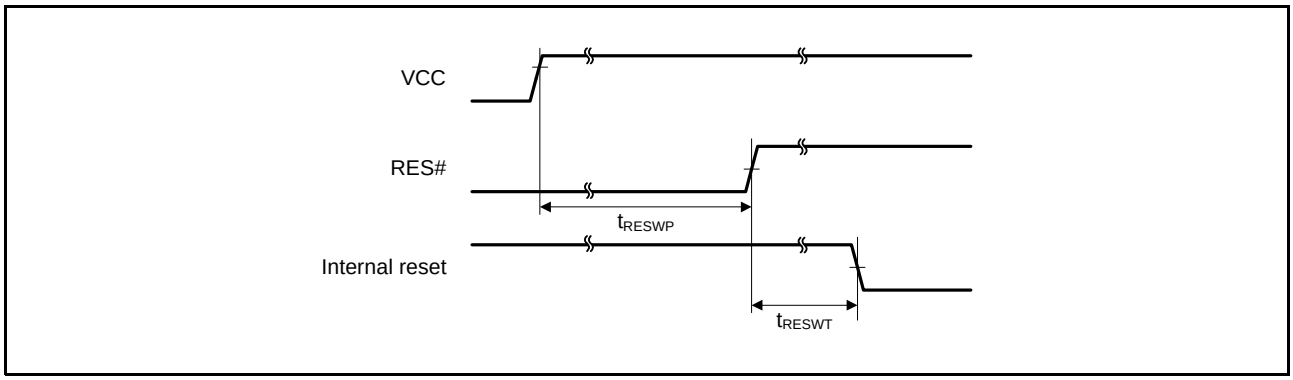


Figure 6.6 Reset Input Timing at Power-On

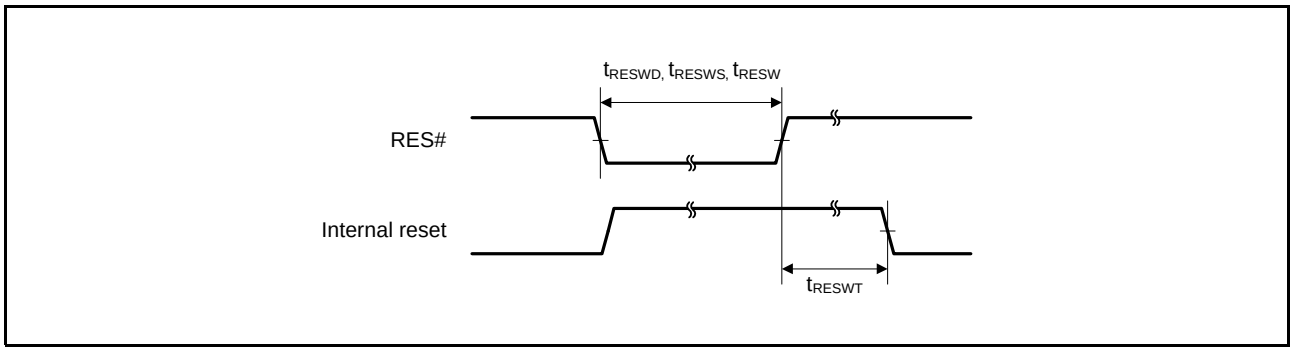


Figure 6.7 Reset Input Timing

6.5 Power-on Reset Circuit and Voltage Detection Circuit Characteristics

Table 6.18 Power-on Reset Circuit and Voltage Detection Circuit Characteristics

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	V_{POR}	2.5	2.6	2.7	V	Figure 6.26
	Voltage detection circuit (LVD0)	V_{DET0}	2.7	2.8	2.9		Figure 6.27
	Voltage detection circuit (LVD1)	V_{DET1}	2.80	2.95	3.10		
	Voltage detection circuit (LVD2)	V_{DET2}	2.80	2.95	3.10		
Internal reset time	Power-on reset (POR)	t_{POR}	—	4.6		ms	Figure 6.26
	Voltage detection circuit (LVD0)	t_{LVD0}	—	4.6			Figure 6.27
	Voltage detection circuit (LVD1)	t_{LVD1}	—	0.9			Figure 6.28
	Voltage detection circuit (LVD2)	t_{LVD2}	—	0.9			Figure 6.29
Minimum VCC down time*1		t_{VOFF}	200	—	—	µs	Figure 6.26, Figure 6.27
Response delay time		t_{det}			200	µs	Figure 6.26 to Figure 6.29
LVD operation stabilization time (after LVD is enabled)		$Td_{(E-A)}$			3	µs	Figure 6.28 Figure 6.29
Hysteresis width (LVD1 and LVD2)		V_{LVH}		80		mV	

Note 1. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{DET1}, and V_{DET2} for the POR/ LVD.

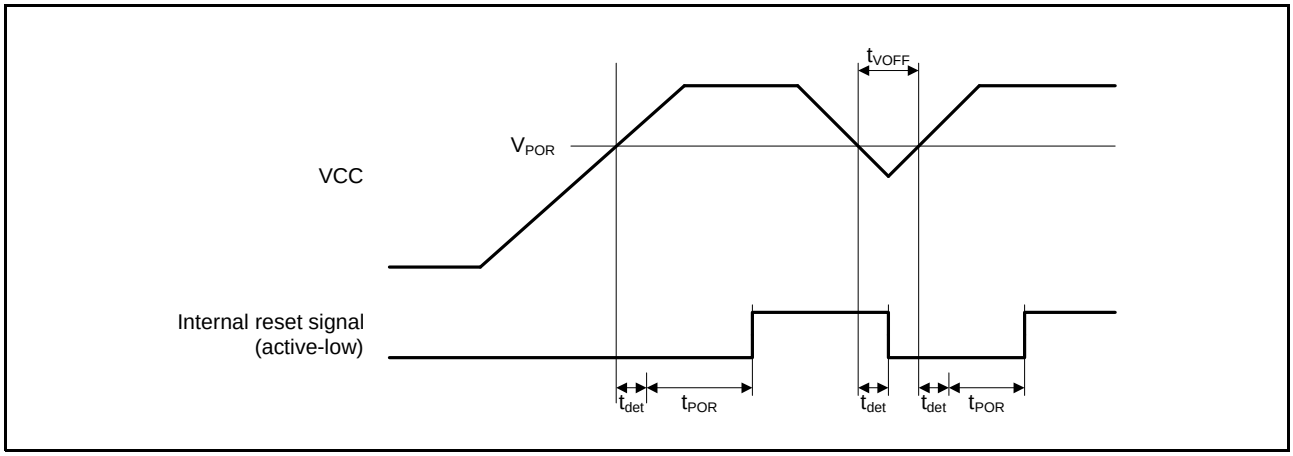


Figure 6.26 Power-on Reset Timing

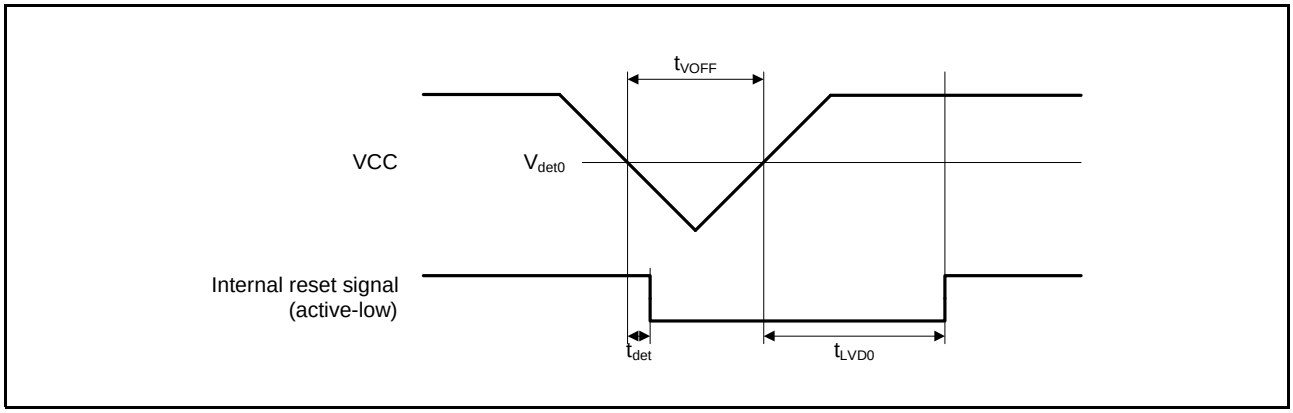


Figure 6.27 Voltage Detection Circuit Timing (V_{det0})

6.6 Oscillation Stop Detection Circuit Characteristics

Table 6.19 Oscillation Stop Detection Circuit Characteristics

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V, AVCC0 = 3.0 to 3.6 V,
VREFH0 = 3.0 V to AVCC0, Ta = T_{opr}

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection time	t_{dr}	—	—	1.0	ms	Figure 6.30

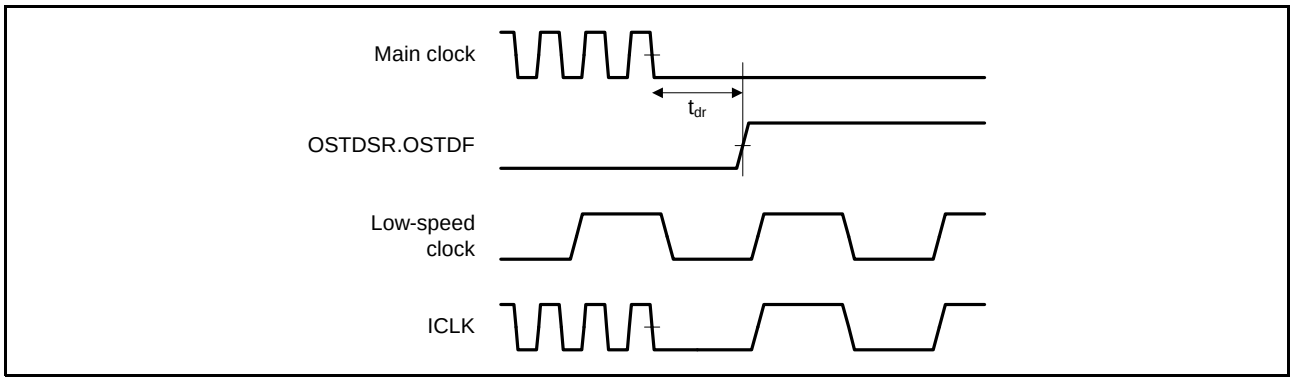


Figure 6.30 Oscillation Stop Detection Timing

6.8 E^2 DataFlash Characteristic

Table 6.22 E^2 DataFlash (Flash Memory for Data Storage) Characteristics (1)

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0
Temperature range for the programming/erasure operation: $T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Reprogram/erase cycle*1	N_{DPEC}	100000	—	—	Times	
Data hold time	t_{DDRP}	30*2	—	—	Year	Ta = +85°C

Note 1. Definition of reprogram/erase cycle:
The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 128-byte programming is performed 16 times for different addresses in 2-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).
Note 2. The value is obtained from the reliability test.

Table 6.23 E^2 DataFlash (Flash Memory for Data Storage) Characteristics (2)

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item		Symbol	min	typ	max	Unit	Test Condition
Programming time	2 bytes	t_{DP2}	—	0.25	2	ms	FCLK = 50 MHz
Erasure time	32 bytes	t_{DE32}	—	2	20	ms	FCLK = 50 MHz $N_{DPEC} \leq 100$
	32 bytes	t_{DE32}	—	4	20	ms	FCLK = 50 MHz $N_{DPEC} > 100$
Blank check time	2 bytes	t_{DBC2}	—	—	30	µs	FCLK = 50 MHz
Suspend delay time during programming		t_{DSPD}	—	—	120	µs	Figure 6.31 PCLKB = 50 MHz
First suspend delay time during erasing (in suspend priority mode)		t_{DSESD1}	—	—	120	µs	
Second suspend delay time during erasing (in suspend priority mode)		t_{DSESD2}	—	—	300	µs	
Suspend delay time during erasing (in erasure priority mode)		t_{DSEED}	—	—	300	µs	