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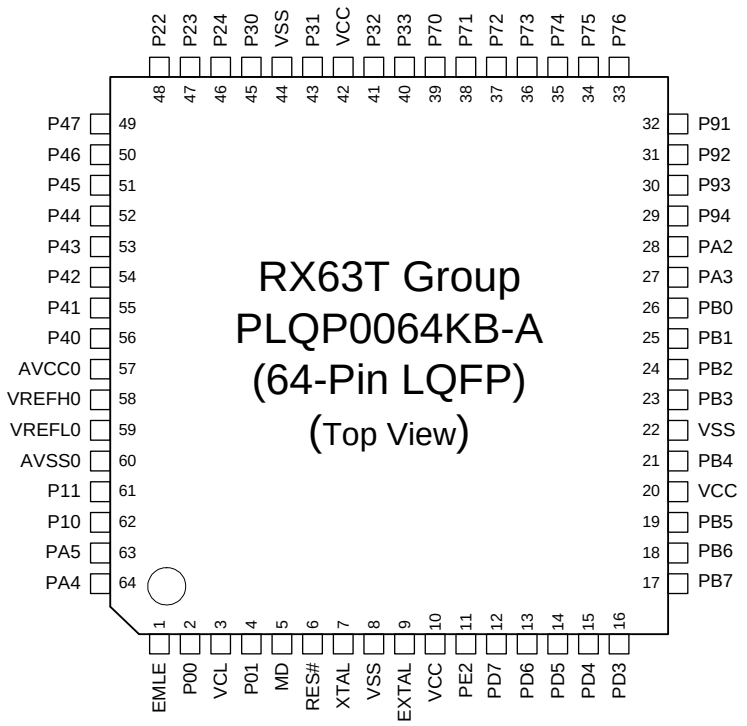
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	81
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 20x10b, 8x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f563tbadfb-v1

Table 1.3 List of Products (2/4)

Group	Part No.	Order Part No.	Package	On-chip ROM Capacity	On-chip RAM Capacity	Option	Operating Voltage	Operating Temperature
RX63T	R5F563TCDDFB	R5F563TCDDFB#V0	PLQP0144KA-A	384 Kbytes	32 Kbytes	CAN module not included	VCC/ PLLVCC 4.0 to 5.5V VCC_USB 3.0 to 3.6V AVCC/ AVCC0 4.0 to 5.5V	-40 to +85°C (D Version)
	R5F563TCDDFA	R5F563TCDDFA#V0	PLQP0120KA-A	384 Kbytes	32 Kbytes	CAN module not included		
	R5F563TCDDFH	R5F563TCDDFH#V0	PLQP0112JA-A	384 Kbytes	32 Kbytes	CAN module not included		
	R5F563TCDDFP	R5F563TCDDFP#V0	PLQP0100KB-A	384 Kbytes	32 Kbytes	CAN module not included		
	R5F563TBDDFB	R5F563TBDDFB#V0	PLQP0144KA-A	256 Kbytes	24 Kbytes	CAN module not included		
	R5F563TBDDFA	R5F563TBDDFA#V0	PLQP0120KA-A	256 Kbytes	24 Kbytes	CAN module not included		
	R5F563TBDDFH	R5F563TBDDFH#V0	PLQP0112JA-A	256 Kbytes	24 Kbytes	CAN module not included		
	R5F563TBDDFP	R5F563TBDDFP#V0	PLQP0100KB-A	256 Kbytes	24 Kbytes	CAN module not included		
	R5F563TEBDFB	R5F563TEBDFB#V0	PLQP0144KA-A	512 Kbytes	48 Kbytes	CAN module included	VCC/ PLLVCC/ VCC_USB 2.7 to 3.6V AVCC/ AVCC0 3.0 to 3.6V or 4.0 to 5.5V	
	R5F563TEBDFB	R5F563TEBDFB#V1	PLQP0144KA-A	512 Kbytes	48 Kbytes	CAN module included		
	R5F563TEBDFA	R5F563TEBDFA#V0	PLQP0120KA-A	512 Kbytes	48 Kbytes	CAN module included		
	R5F563TEBDFA	R5F563TEBDFA#V1	PLQP0120KA-A	512 Kbytes	48 Kbytes	CAN module included		
	R5F563TEBDFH	R5F563TEBDFH#V0	PLQP0112JA-A	512 Kbytes	48 Kbytes	CAN module included		
	R5F563TEBDFH	R5F563TEBDFH#V1	PLQP0112JA-A	512 Kbytes	48 Kbytes	CAN module included		
	R5F563TEBDFP	R5F563TEBDFP#V0	PLQP0100KB-A	512 Kbytes	48 Kbytes	CAN module included		
	R5F563TEBDFP	R5F563TEBDFP#V1	PLQP0100KB-A	512 Kbytes	48 Kbytes	CAN module included		
	R5F563TCBDFB	R5F563TCBDFB#V0	PLQP0144KA-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TCBDFB	R5F563TCBDFB#V1	PLQP0144KA-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TCBDFA	R5F563TCBDFA#V0	PLQP0120KA-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TCBDFA	R5F563TCBDFA#V1	PLQP0120KA-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TCBDFH	R5F563TCBDFH#V0	PLQP0112JA-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TCBDFH	R5F563TCBDFH#V1	PLQP0112JA-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TCBDFP	R5F563TCBDFP#V0	PLQP0100KB-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TCBDFP	R5F563TCBDFP#V1	PLQP0100KB-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TBBDFB	R5F563TBBDFB#V0	PLQP0144KA-A	256 Kbytes	24 Kbytes	CAN module included		
	R5F563TBBDFB	R5F563TBBDFB#V1	PLQP0144KA-A	256 Kbytes	24 Kbytes	CAN module included		
	R5F563TBBDFA	R5F563TBBDFA#V0	PLQP0120KA-A	256 Kbytes	24 Kbytes	CAN module included		
	R5F563TBBDFA	R5F563TBBDFA#V1	PLQP0120KA-A	256 Kbytes	24 Kbytes	CAN module included		
	R5F563TBBDFH	R5F563TBBDFH#V0	PLQP0112JA-A	256 Kbytes	24 Kbytes	CAN module included		
	R5F563TBBDFH	R5F563TBBDFH#V1	PLQP0112JA-A	256 Kbytes	24 Kbytes	CAN module included		



Note: • This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.9, List of Pins and Pin Functions (64-Pin LQFP).

Figure 1.7 Pin Assignment (64-Pin LQFP)

Table 1.8 List of Pins and Pin Functions (100-Pin LQFP) (1/3)

Pin Number 100-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3, GPT, POE3, CAC)	Communications (SCIc, SCId, RSPI, RIIC, CAN)	Interrupt	S12ADB, AD, DA
1		PE5	BCLK			IRQ0	
2	EMLE						
3	VSS						
4		P01	RD#		CTS0#/RTS0#/SS0#		
5	VCL						
6		P00	CS1#	CACREF			
7	MD/FINED						
8		PE4	A10	POE10#/MTCLKC		IRQ1	
9		PE3	A11	POE11#/MTCLKD		IRQ2-DS	
10	RES#						
11	XTAL						
12	VSS						
13	EXTAL						
14	VCC						
15		PE2		POE10#		NMI	
16		PE1	WR0#/WR#		CTS12#/RTS12#/ SS12#/SSLA3/SSLB3		
17		PE0	WR1#/BC1#/ WAIT#		SSLA2/SSLB2/CRX1	IRQ7	
18	TRST#	PD7		GTIOC0A	CTS0#/RTS0#/SS0#/ SSLA1/SSLB1/CTX1		
19	TMS	PD6		GTIOC0B	SSLA0/SSLB0		
20	TDI	PD5		GTIOC1A	RXD1/SMISO1/SSCL1	IRQ6	
21	TCK/FINEC	PD4		GTIOC1B	SCK1		
22	TDO	PD3		GTIOC2A	TXD1/SMOSI1/SSDA1		
23		PD2	CS2#	GTIOC2B	MOSIA/MOSIB		
24		PD1	CS0#	GTIOC3A	MISOA/MISOB		
25		PD0	A12	GTIOC3B	RSPCKA/RSPCKB		
26		PB7	A19		SCK12		
27		PB6	A18		RXD12/SMISO12/ SSCL12/RXDX12/ CRX1	IRQ2	
28		PB5	A17		TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/CTX1		
29	PLLVCC						
30		PB4	A16	POE8#/GTETRG0		IRQ3-DS	
31	PLLVSS						
32		PB3	A15	MTIOC0A/CACREF	SCK0		
33		PB2		MTIOC0B	TXD0/SMOSI0/ SSDA0/SDA0		
34		PB1		MTIOC0C	RXD0/SMISO0/ SSCL0/SCL0	IRQ4	
35		PB0	A14	MTIOC0D	MOSIA/MOSIB		
36		PA5		MTIOC1A	RXD0/SMISO0/ SSCL0/ MISOA/MISOB		ADTRG1#

3. Address Space

3.1 Address Space

This MCU has a 4-Gbyte address space, consisting of the range of addresses from 0000 0000h to FFFF FFFFh. That is, linear access to an address space of up to 4 Gbytes is possible, and this contains both program and data areas.
Figure 3.1 shows the memory maps in the respective operating modes. Accessible areas will differ according to the operating mode and states of control bits.

Table 4.1 List of I/O Registers (Address Order) (10/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 71BBh	ICU	DTC Activation Enable Register 187	DTCER187	8	8	2 ICLK		ICUb	Not present in versions with 64 or 48 pins.
0008 71BCh	ICU	DTC Activation Enable Register 188	DTCER188	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 71BDh	ICU	DTC Activation Enable Register 189	DTCER189	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 71BFh	ICU	DTC Activation Enable Register 191	DTCER191	8	8	2 ICLK			Not present in versions with 112, 100, 64 or 48 pins.
0008 71C0h	ICU	DTC Activation Enable Register 192	DTCER192	8	8	2 ICLK			Not present in versions with 112, 100, 64 or 48 pins.
0008 71C3h	ICU	DTC Activation Enable Register 195	DTCER195	8	8	2 ICLK			
0008 71C4h	ICU	DTC Activation Enable Register 196	DTCER196	8	8	2 ICLK			
0008 71C6h	ICU	DTC Activation Enable Register 198	DTCER198	8	8	2 ICLK			
0008 71C7h	ICU	DTC Activation Enable Register 199	DTCER199	8	8	2 ICLK			
0008 71C8h	ICU	DTC Activation Enable Register 200	DTCER200	8	8	2 ICLK			
0008 71C9h	ICU	DTC Activation Enable Register 201	DTCER201	8	8	2 ICLK			
0008 71D6h	ICU	DTC Activation Enable Register 214	DTCER214	8	8	2 ICLK			
0008 71D7h	ICU	DTC Activation Enable Register 215	DTCER215	8	8	2 ICLK			
0008 71D9h	ICU	DTC Activation Enable Register 217	DTCER217	8	8	2 ICLK			
0008 71DAh	ICU	DTC Activation Enable Register 218	DTCER218	8	8	2 ICLK			
0008 71DCh	ICU	DTC Activation Enable Register 220	DTCER220	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 71DDh	ICU	DTC Activation Enable Register 221	DTCER221	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 71DFh	ICU	DTC Activation Enable Register 223	DTCER223	8	8	2 ICLK			Not present in versions with 100, 64 or 48 pins.
0008 71E0h	ICU	DTC Activation Enable Register 224	DTCER224	8	8	2 ICLK			Not present in versions with 100, 64 or 48 pins.
0008 71E2h	ICU	DTC Activation Enable Register 226	DTCER226	8	8	2 ICLK			
0008 71E3h	ICU	DTC Activation Enable Register 227	DTCER227	8	8	2 ICLK			
0008 71E4h	ICU	DTC Activation Enable Register 228	DTCER228	8	8	2 ICLK			
0008 71E5h	ICU	DTC Activation Enable Register 229	DTCER229	8	8	2 ICLK			
0008 71E6h	ICU	DTC Activation Enable Register 230	DTCER230	8	8	2 ICLK			
0008 71E7h	ICU	DTC Activation Enable Register 231	DTCER231	8	8	2 ICLK			
0008 71E8h	ICU	DTC Activation Enable Register 232	DTCER232	8	8	2 ICLK			
0008 71E9h	ICU	DTC Activation Enable Register 233	DTCER233	8	8	2 ICLK			
0008 71EAh	ICU	DTC Activation Enable Register 234	DTCER234	8	8	2 ICLK			
0008 71EBh	ICU	DTC Activation Enable Register 235	DTCER235	8	8	2 ICLK			
0008 71ECh	ICU	DTC Activation Enable Register 236	DTCER236	8	8	2 ICLK			
0008 71EEh	ICU	DTC Activation Enable Register 238	DTCER238	8	8	2 ICLK			
0008 71EFh	ICU	DTC Activation Enable Register 239	DTCER239	8	8	2 ICLK			
0008 71F0h	ICU	DTC Activation Enable Register 240	DTCER240	8	8	2 ICLK			
0008 71F1h	ICU	DTC Activation Enable Register 241	DTCER241	8	8	2 ICLK			
0008 71F2h	ICU	DTC Activation Enable Register 242	DTCER242	8	8	2 ICLK			
0008 71F4h	ICU	DTC Activation Enable Register 244	DTCER244	8	8	2 ICLK			
0008 71F5h	ICU	DTC Activation Enable Register 245	DTCER245	8	8	2 ICLK			
0008 71F6h	ICU	DTC Activation Enable Register 246	DTCER246	8	8	2 ICLK			
0008 71F7h	ICU	DTC Activation Enable Register 247	DTCER247	8	8	2 ICLK			
0008 71F8h	ICU	DTC Activation Enable Register 248	DTCER248	8	8	2 ICLK			
0008 71FAh	ICU	DTC Activation Enable Register 250	DTCER250	8	8	2 ICLK			
0008 71FBh	ICU	DTC Activation Enable Register 251	DTCER251	8	8	2 ICLK			
0008 7202h	ICU	Interrupt Request Enable Register 02	IER02	8	8	2 ICLK			
0008 7203h	ICU	Interrupt Request Enable Register 03	IER03	8	8	2 ICLK			
0008 7204h	ICU	Interrupt Request Enable Register 04	IER04	8	8	2 ICLK			
0008 7205h	ICU	Interrupt Request Enable Register 05	IER05	8	8	2 ICLK			

Table 4.1 List of I/O Registers (Address Order) (33/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
000A 0092h	USB0	PIPE1 Transaction Counter Register	PIPE1TRN	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1	USBa	Not present in versions with 112, 100, 64, or 48 pins.
000A 0094h	USB0	PIPE2 Transaction Counter Enable Register	PIPE2TRE	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 0096h	USB0	PIPE2 Transaction Counter Register	PIPE2TRN	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 0098h	USB0	PIPE3 Transaction Counter Enable Register	PIPE3TRE	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 009Ah	USB0	PIPE3 Transaction Counter Register	PIPE3TRN	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 009Ch	USB0	PIPE4 Transaction Counter Enable Register	PIPE4TRE	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 009Eh	USB0	PIPE4 Transaction Counter Register	PIPE4TRN	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 00A0h	USB0	PIPE5 Transaction Counter Enable Register	PIPE5TRE	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 00A2h	USB0	PIPE5 Transaction Counter Register	PIPE5TRN	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000C 1200h	MTU3	Timer Control Register	TCR	8	8, 16, 32	4, 5 PCLKA	2, 3 ICLK	MTU3	
000C 1201h	MTU4	Timer Control Register	TCR	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1202h	MTU3	Timer Mode Register 1	TMDR1	8	8, 16	4, 5 PCLKA	2, 3 ICLK		
000C 1203h	MTU4	Timer Mode Register 1	TMDR1	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1204h	MTU3	Timer I/O Control Register H	TIORH	8	8, 16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1205h	MTU3	Timer I/O Control Register L	TIORL	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1206h	MTU4	Timer I/O Control Register H	TIORH	8	8, 16	4, 5 PCLKA	2, 3 ICLK		
000C 1207h	MTU4	Timer I/O Control Register L	TIORL	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1208h	MTU3	Timer Interrupt Enable Register	TIER	8	8, 16	4, 5 PCLKA	2, 3 ICLK		
000C 1209h	MTU4	Timer Interrupt Enable Register	TIER	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 120Ah	MTU	Timer Output Master Enable Register A	TOERA	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 120Dh	MTU	Timer Gate Control Register A	TGCRA	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 120Eh	MTU	Timer Output Control Register 1A	TOCR1A	8	8, 16	4, 5 PCLKA	2, 3 ICLK		

Table 4.1 List of I/O Registers (Address Order) (34/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
000C 120Fh	MTU	Timer Output Control Register 2A	TOCR2A	8	8	4, 5 PCLKA	2, 3 ICLK	MTU3	
000C 1210h	MTU3	Timer Counter	TCNT	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1212h	MTU4	Timer Counter	TCNT	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1214h	MTU	Timer Cycle Data Register A	TCDRA	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1216h	MTU	Timer Dead Time Data Register A	TDDRA	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1218h	MTU3	Timer General Register A	TGRA	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 121Ah	MTU3	Timer General Register B	TGRB	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 121Ch	MTU4	Timer General Register A	TGRA	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 121Eh	MTU4	Timer General Register B	TGRB	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1220h	MTU	Timer Subcounter A	TCNTSA	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1222h	MTU	Timer Cycle Buffer Register A	TCBRA	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1224h	MTU3	Timer General Register C	TGRC	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1226h	MTU3	Timer General Register D	TGRD	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1228h	MTU4	Timer General Register C	TGRC	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 122Ah	MTU4	Timer General Register D	TGRD	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 122Ch	MTU3	Timer Status Register	TSR	8	8, 16	4, 5 PCLKA	2, 3 ICLK		
000C 122Dh	MTU4	Timer Status Register	TSR	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1230h	MTU	Timer Interrupt Skipping Set Register 1A	TITCR1A	8	8, 16	4, 5 PCLKA	2, 3 ICLK		
000C 1231h	MTU	Timer Interrupt Skipping Counters 1A	TITCNT1A	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1232h	MTU	Timer Buffer Transfer Set Register A	TBTERA	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1234h	MTU	Timer dead time enable register A	TDERA	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1236h	MTU	Timer output level buffer register A	TOLBRA	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1238h	MTU3	Timer Buffer Operation Transfer Mode Register	TBTM	8	8, 16	4, 5 PCLKA	2, 3 ICLK		
000C 1239h	MTU4	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 123Ah	MTU	Timer Interrupt Skipping Mode Register A	TITMRA	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 123Bh	MTU	Timer Interrupt Skipping Set Register 2A	TITCR2A	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 123Ch	MTU	Timer Interrupt Skipping Counters 2A	TITCNT2A	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1240h	MTU4	Timer A/D Converter Start Request Control Register	TADCR	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1244h	MTU4	Timer A/D Converter Start Request Cycle Set Register A	TADCORA	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1246h	MTU4	Timer A/D Converter Start Request Cycle Set Register B	TADCORB	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1248h	MTU4	Timer A/D Converter Start Request Cycle Set Buffer Register A	TADCOBRA	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 124Ah	MTU4	Timer A/D Converter Start Request Cycle Set Buffer Register B	TADCOBRB	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1260h	MTU	Timer Waveform Control Register A	TWCRA	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1270h	MTU	Timer Mode Register 2A	TMDR2A	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1272h	MTU3	Timer General Register E	TGRE	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1274h	MTU4	Timer General Register E	TGRE	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1276h	MTU4	Timer General Register F	TGRF	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1280h	MTU	Timer Start Register A	TSTRA	8	8, 16	4, 5 PCLKA	2, 3 ICLK		
000C 1281h	MTU	Timer Synchronous Register A	TSYRA	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1282h	MTU	Timer Counter Synchronous Start Register	TCSYSTR	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1284h	MTU	Timer Read/Write Enable Register A	TRWERA	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1300h	MTU0	Timer Control Register	TCR	8	8, 16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1301h	MTU0	Timer Mode Register 1	TMDR1	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1302h	MTU0	Timer I/O Control Register H	TIORH	8	8, 16	4, 5 PCLKA	2, 3 ICLK		
000C 1303h	MTU0	Timer I/O Control Register L	TIORL	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1304h	MTU0	Timer Interrupt Enable Register	TIER	8	8, 16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1305h	MTU0	Timer Status Register	TSR	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1306h	MTU0	Timer Counter	TCNT	16	16	4, 5 PCLKA	2, 3 ICLK		

Table 4.1 List of I/O Registers (Address Order) (41/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
000C 22BAh	GPT3	General PWM Timer Dead Time Value Register D	GTDVD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK	GPT	
000C 22BCh	GPT3	General PWM Timer Dead Time Buffer Register U	GTDBU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 22BEh	GPT3	General PWM Timer Dead Time Buffer Register D	GTDBD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 22C0h	GPT3	General PWM Timer Output Protection Function Status Register	GTSOS	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 22C2h	GPT3	General PWM Timer Output Protection Function Temporary Release Register	GTSOTR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2318h	GPT0	GTIOCA Rising Output Delay Register	GTDLYRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64, or 48 pins.
000C 231Ah	GPT0	GTIOCB Rising Output Delay Register	GTDLYRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64, or 48 pins.
000C 231Ch	GPT1	GTIOCA Rising Output Delay Register	GTDLYRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64, or 48 pins.
000C 231Eh	GPT1	GTIOCB Rising Output Delay Register	GTDLYRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64, or 48 pins.
000C 2320h	GPT2	GTIOCA Rising Output Delay Register	GTDLYRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64, or 48 pins.
000C 2322h	GPT2	GTIOCB Rising Output Delay Register	GTDLYRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64, or 48 pins.
000C 2324h	GPT3	GTIOCA Rising Output Delay Register	GTDLYRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64, or 48 pins.
000C 2326h	GPT3	GTIOCB Rising Output Delay Register	GTDLYRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64, or 48 pins.
000C 2328h	GPT0	GTIOCA Falling Output Delay Register	GTDLYFA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64, or 48 pins.
000C 232Ah	GPT0	GTIOCB Falling Output Delay Register	GTDLYFB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64, or 48 pins.
000C 232Ch	GPT1	GTIOCA Falling Output Delay Register	GTDLYFA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64, or 48 pins.
000C 232Eh	GPT1	GTIOCB Falling Output Delay Register	GTDLYFB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64, or 48 pins.
000C 2330h	GPT2	GTIOCA Falling Output Delay Register	GTDLYFA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64, or 48 pins.
000C 2332h	GPT2	GTIOCB Falling Output Delay Register	GTDLYFB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64, or 48 pins.
000C 2334h	GPT3	GTIOCA Falling Output Delay Register	GTDLYFA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64, or 48 pins.
000C 2336h	GPT3	GTIOCB Falling Output Delay Register	GTDLYFB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64, or 48 pins.
000C 2800h	GPTB	General PWM Timer Software Start Register	GTSTR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64, or 48 pins.
000C 2804h	GPTB	General PWM Timer Hardware Source Start Control Register	GTHSCR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64, or 48 pins.
000C 2806h	GPTB	General PWM Timer Hardware Source Clear Control Register	GTHCCR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64, or 48 pins.
000C 2808h	GPTB	General PWM Timer Hardware Start Source Select Register	GTHSSR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64, or 48 pins.
000C 280Ah	GPTB	General PWM Timer Hardware Stop/Clear Source Select Register	GTHPSR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64, or 48 pins.
000C 280Ch	GPTB	General PWM Timer Write-Protection Register	GTWP	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64, or 48 pins.
000C 280Eh	GPTB	General PWM Timer Sync Register	GTSYNC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64, or 48 pins.
000C 2810h	GPTB	General PWM Timer External Trigger Input Interrupt Register	GTETINT	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64, or 48 pins.
000C 2814h	GPTB	General PWM Timer Buffer Operation Disable Register	GTBDR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64, or 48 pins.
000C 2818h	GPTB	General PWM Timer Start Write-Protection Register	GTSWP	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64, or 48 pins.
000C 2880h	GPTB	LOCO Count Control Register	LCCR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64, or 48 pins.
000C 2882h	GPTB	LOCO Count Status Register	LCST	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64, or 48 pins.

Table 4.1 List of I/O Registers (Address Order) (42/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
000C 2884h	GPTB	LOCO Count Value Register	LCNT	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK	GPT	Not present in versions with 64, or 48 pins.
000C 2886h	GPTB	LOCO Count Result Average Register	LCNTA	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64, or 48 pins.
000C 2888h	GPTB	LOCO Count Result Register 0	LCNT00	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64, or 48 pins.
000C 288Ah	GPTB	LOCO Count Result Register 1	LCNT01	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64, or 48 pins.
000C 288Ch	GPTB	LOCO Count Result Register 2	LCNT02	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 288Eh	GPTB	LOCO Count Result Register 3	LCNT03	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2890h	GPTB	LOCO Count Result Register 4	LCNT04	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2892h	GPTB	LOCO Count Result Register 5	LCNT05	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2894h	GPTB	LOCO Count Result Register 6	LCNT06	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2896h	GPTB	LOCO Count Result Register 7	LCNT07	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2898h	GPTB	LOCO Count Result Register 8	LCNT08	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 289Ah	GPTB	LOCO Count Result Register 9	LCNT09	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 289Ch	GPTB	LOCO Count Result Register 10	LCNT10	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 289Eh	GPTB	LOCO Count Result Register 11	LCNT11	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 28A0h	GPTB	LOCO Count Result Register 12	LCNT12	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 28A2h	GPTB	LOCO Count Result Register 13	LCNT13	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 28A4h	GPTB	LOCO Count Result Register 14	LCNT14	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 28A6h	GPTB	LOCO Count Result Register 15	LCNT15	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 28A8h	GPTB	LOCO Count Upper Permissible Deviation Register	LCNTDU	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 28AAh	GPTB	LOCO Count Lower Permissible Deviation Register	LCNTDL	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2900h	GPT4	General PWM Timer I/O Control Register	GTIOR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2902h	GPT4	General PWM Timer Interrupt Output Setting Register	GTINTAD	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2904h	GPT4	General PWM Timer Control Register	GTCR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2906h	GPT4	General PWM Timer Buffer Enable Register	GTBER	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2908h	GPT4	General PWM Timer Count Direction Register	GTUDC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 290Ah	GPT4	General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register	GTITC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 290Ch	GPT4	General PWM Timer Status Register	GTST	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 290Eh	GPT4	General PWM Timer Counter	GTCNT	16	16	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2910h	GPT4	General PWM Timer Compare Capture Register A	GTCCRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2912h	GPT4	General PWM Timer Compare Capture Register B	GTCCRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2914h	GPT4	General PWM Timer Compare Capture Register C	GTCCRC	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2916h	GPT4	General PWM Timer Compare Capture Register D	GTCCRD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2918h	GPT4	General PWM Timer Compare Capture Register E	GTCCRE	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.

5.3 AC Characteristics

Table 5.7 Operation Frequency Value

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS =PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item		Symbol	Min.	Typ.	Max.	Unit
Operation frequency	System clock (ICLK)	f	—	—	100	MHz
	Peripheral module clock (PCLK) *1		—	—	50	
	Timer module clock (PCLKA)		—	—	100	
	AD clock (PCLKC)		—	—	100	
	S12AD clock (PCLKD)		—	—	50	
	FlashIF clock (FCLK)		—	—	50	
	External bus clock (BCLK)		—	—	50	
	BCLK pin output		—	—	25	
	USB clock (UCLK)		—	—	48	

Note 1. The PCLK must run at a frequency of at least 24 MHz when the USB is in use.

5.3.2 Clock Timing

Table 5.9 Clock Timing

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BCLK pin output cycle time	Only condition 3	t_{Bcyc}	20	—	—	ns	Figure 5.3
	Other than condition 3	t_{Bcyc}	40	—	—	ns	
BCLK pin output high pulse width		t_{CH}	5	—	—	ns	
BCLK pin output low pulse width		t_{CL}	5	—	—	ns	
BCLK pin output rising time		t_{Cr}	—	—	5	ns	
BCLK pin output falling time		t_{Cf}	—	—	5	ns	
EXTAL external clock input cycle time		t_{EXcyc}	70	—	—	ns	Figure 5.4
EXTAL external clock input high pulse width		t_{EXH}	35	—	—	ns	
EXTAL external clock input low pulse width		t_{EXL}	35	—	—	ns	
EXTAL external clock rising time		t_{EXr}	—	—	5	ns	
EXTAL external clock falling time		t_{EXf}	—	—	5	ns	
EXTAL external clock input wait time*1		t_{EXWT}	1	—	—	ms	
Main clock oscillator oscillation frequency		f_{MAIN}	8	—	12.5	MHz	
Main clock oscillation stabilization time (crystal)		$t_{MAINOSC}$	—	—	*2	ms	Figure 5.5
Main clock oscillation stabilization wait time (crystal)		$t_{MAINOSCWT}$	—	—	*3	ms	
LOCO, IWDTCLK clock cycle time		$t_{LOCOCYC}$	6.96	8	9.4	μs	
LOCO, IWDTCLK clock oscillation frequency		f_{LOCO}	106.25	125	143.75	kHz	
LOCO, IWDTCLK clock oscillation stabilization wait time		t_{LOCOWT}	—	—	20	μs	Figure 5.6
PLL clock frequency		f_{PLL}	104	—	200	MHz	
PLL clock oscillation stabilization time	PLL operation started after main clock oscillation has settled	t_{PLL1}	—	—	500	μs	Figure 5.7
PLL clock oscillation stabilization wait time		t_{PLLWT1}	—	—	*4	ms	
PLL clock oscillation stabilization time	PLL operation started before main clock oscillation has settled	t_{PLL2}	—	—	$t_{MAINOSC} + t_{PLL1}$	ms	Figure 5.8
PLL clock oscillation stabilization wait time		t_{PLLWT2}	—	—	*4	ms	

Note 1. This is the time until the clock is used after clearing the main clock oscillator stop bit (MOSCCR.MOSTP) to 0 (selecting operation).

Note 2. When using a main clock, ask the manufacturer of the oscillator to evaluate its oscillation. Refer to the results of evaluation provided by the manufacturer for the oscillation stabilization time.

Note 3. This is calculated from the formula below, where n is the number of cycles set by the MOSCWTCR.MSTS[4:0] bits.

$$t_{MAINOSCWT} = t_{MAINOSC} + \frac{n + 16384}{f_{MAIN}}$$

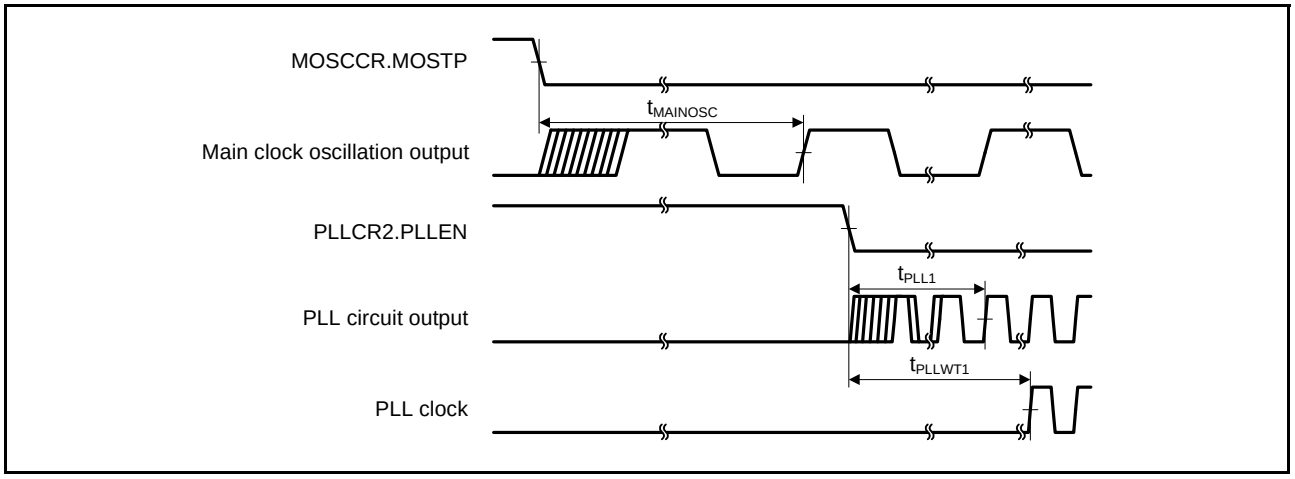


Figure 5.7 PLL Clock Oscillation Start Timing (PLL is Operated after Main Clock Oscillation Has Settled)

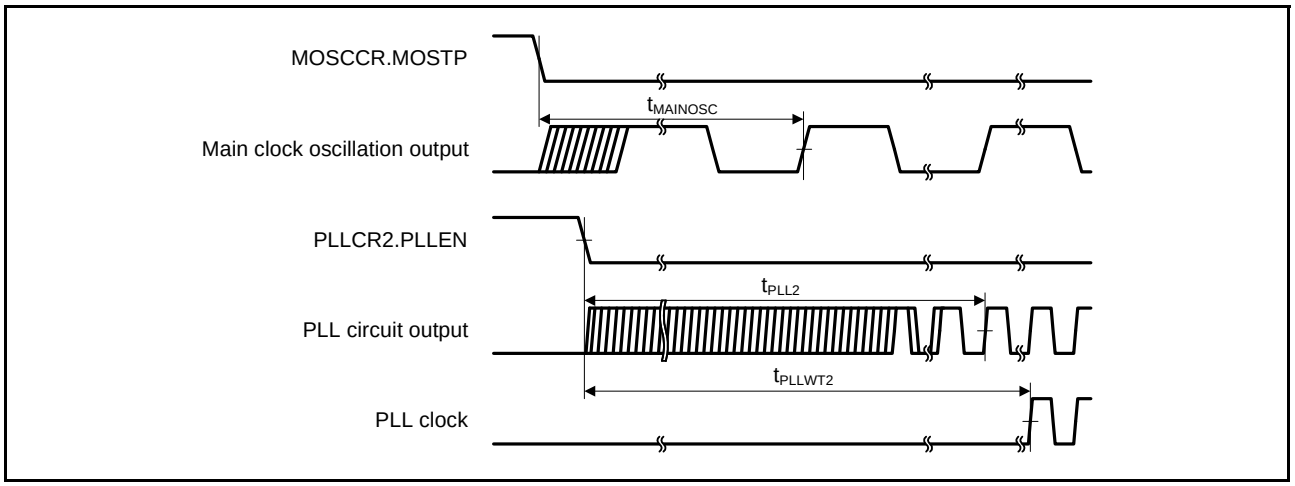
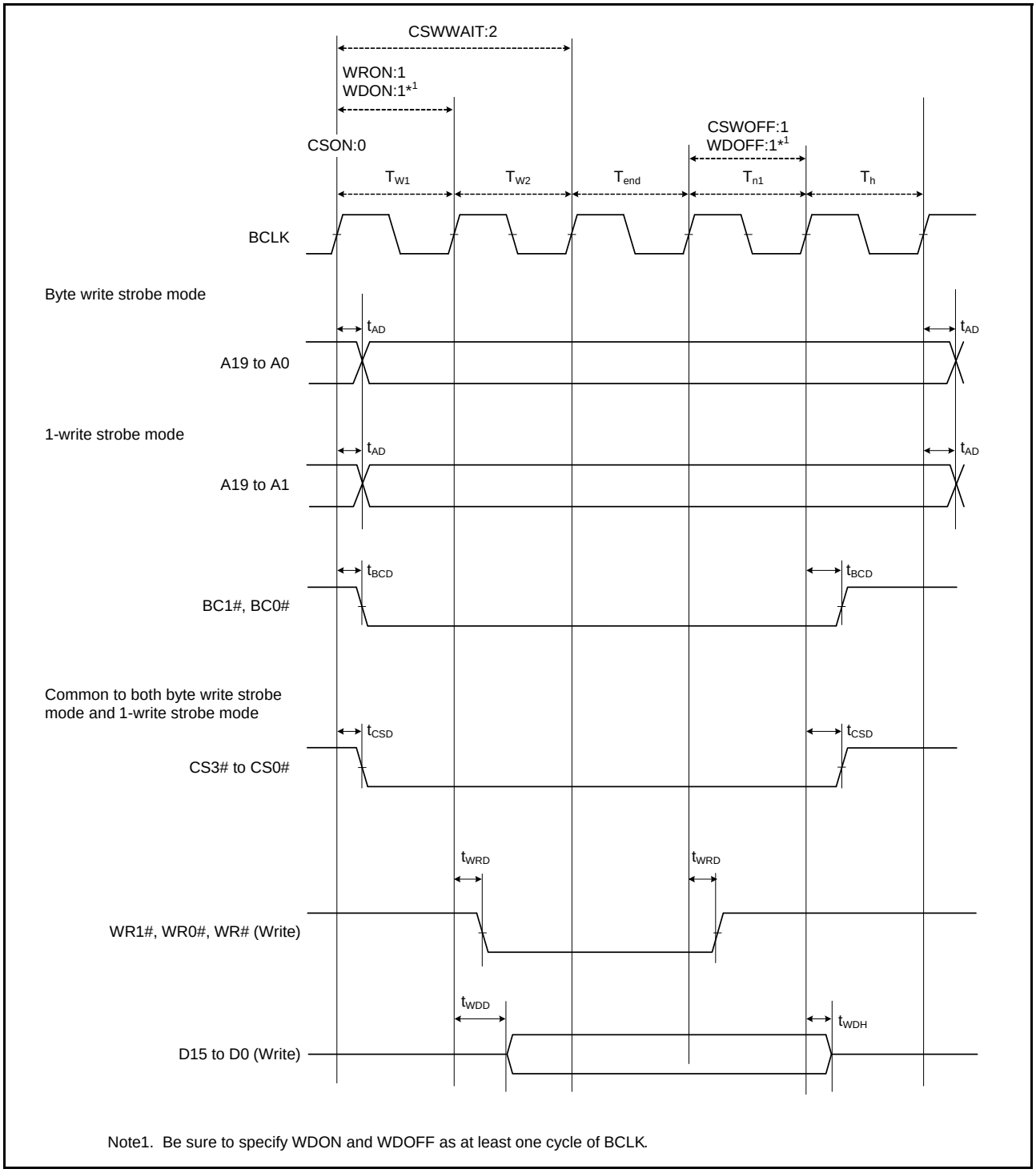


Figure 5.8 PLL Clock Oscillation Start Timing (PLL is Operated before Main Clock Oscillation Has Settled)



Note1. Be sure to specify WDON and WDOFF as at least one cycle of BCLK.

Figure 5.14 External Bus Timing/Normal Write Cycle (Bus Clock Synchronized)

Table 5.16 Timing of On-Chip Peripheral Modules (3)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS =PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

High drive output is selected by the drive capacity control register.

Item				Symbol	Min.	Max.	Unit*1	Test Conditions
RSPI	RSPCK clock cycle	Master		t_{SPcyc}	2	4096	t_{Pcyc}	C = 30 pF, Figure 5.32
		Slave			8	4096		
	RSPCK clock high pulse width	Master		t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2 - 3$	—	ns	
		Slave			$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2$	—		
	RSPCK clock low pulse width	Master		t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2 - 3$	—	ns	
		Slave			$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2$	—		
	RSPCK clock rise/fall time	Output		t_{SPCKR}, t_{SPCKF}	—	5	ns	
		Input			—	1	μs	
	RSPCK clock fall time	Input		t_{SPCKF}	—	0.1	μs/V	
	Data input setup time	Master		t_{SU}	4	—	ns	C = 30 pF, Figure 5.33 to Figure 5.40
		Slave			20 – t_{Pcyc}	—		
	Data input hold time	Master	PCLKB division ratio set to a value other than 1/2	t_H	t_{Pcyc}	—	ns	
			PCLKB division ratio set to 1/2	t_{HF}	0	—		
		Slave		t_H	20 + 2 × t_{Pcyc}	—		
	SSL setup time	Master		t_{LEAD}	1	8	t_{SPcyc}	
		Slave			4	—	t_{Pcyc}	
	SSL hold time	Master		t_{LAG}	1	8	t_{SPcyc}	
		Slave			4	—	t_{Pcyc}	
	Data output delay time	Master		t_{OD}	—	10	ns	
		Slave			—	3 × t_{Pcyc} + 40		
	Data output hold time	Master		t_{OH}	0	—	ns	
		Slave			0	—		
	Successive transmission delay time	Master		t_{TD}	t_{SPcyc} + 2 × t_{Pcyc}	8 × t_{SPcyc}+ 2 × t_{Pcyc}	ns	
		Slave			4 × t_{Pcyc}	—		
	MOSI and MISO rise/fall time	Output		t_{DR}, t_{DF}	—	5	ns	
		Input			—	1	μs	
	SSL rise/fall time	Output		t_{SSLr}, t_{SSLf}	—	15	ns	
		Input			—	1	μs	
	Slave access time			t_{SA}	—	4	t_{Pcyc}	Figure 5.39 and Figure 5.40
	Slave output release time			t_{REL}	—	3	t_{Pcyc}	

Note 1. t_{Pcyc}: PCLK cycle

Table 5.20 10-Bit A/D Conversion Characteristics (2)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$ is common to conditions 1 to 3.

Item			Min.	Typ.	Max.	Unit	Test Conditions
Resolution			10	10	10	Bit	
Conversion time*1 (Operation at ADCLK = 50 MHz)	Without 0.1-μF external capacitor Permissible signal source impedance (max.) = 1 kΩ	AN0 to AN7	0.8	—	—	μs	Sampling in 15 states
		Other channels	1.0	—	—	μs	Sampling in 25 states
Analog input capacitance			—	—	6	pF	
Integral nonlinearity error			—	—	±2.0	LSB	
Offset error			—	—	±2.0	LSB	
Full-scale error			—	—	±3.0	LSB	
Quantization error			—	±0.5	—	LSB	
Absolute accuracy			—	—	±4.0	LSB	

Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

5.9 ROM (Flash Memory for Code Storage) Characteristics

Table 5.29 ROM (Flash Memory for Code Storage) Characteristics (1)

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Temperature range for the programming/erasure operation: $T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Reprogram/erase cycle*1	N_{pec}	1000	—	—	Times	
Data hold time	t_{DRP}	30*2	—	—	Year	Ta = +85°C

Note 1. Definition of reprogram/erase cycle:
The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 128-byte programming is performed 16 times for different addresses in 2-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. The value is obtained from the reliability test.

Table 5.30 ROM (Flash Memory for Code Storage) Characteristics (2)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Temperature range for the programming/erasure operation: $T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time N_{PEC} ≤ 100 times	128 bytes	t_{P128}	—	2.8	28	—	1	10	ms
	4 Kbytes	t_{P4K}	—	63	140	—	23	50	ms
	16 Kbytes	t_{P16K}	—	252	560	—	90	200	ms
Programming time N_{PEC} > 100 times	128 bytes	t_{P128}	—	3.4	33.6	—	1.2	12	ms
	4 Kbytes	t_{P4K}	—	75.6	168	—	27.6	60	ms
	16 Kbytes	t_{P16K}	—	302.4	672	—	108	240	ms
Erasure time N_{PEC} ≤ 100 times	4 Kbytes	t_{E4K}	—	50	120	—	25	60	ms
	16 Kbytes	t_{E16K}	—	200	480	—	100	240	ms
Erasure time N_{PEC} > 100 times	4 Kbytes	t_{E4K}	—	60	144	—	30	72	ms
	16 Kbytes	t_{E16K}	—	240	576	—	120	288	ms
Suspend delay time during programming		t_{SPD}	—	—	400	—	—	120	μs
First suspend delay time during erasing (in suspend priority mode)		t_{SESD1}	—	—	300	—	—	120	μs
Second suspend delay time during erasing (in suspend priority mode)		t_{SESD2}	—	—	1.7	—	—	1.7	ms
Suspend delay time during erasing (in erasure priority mode)		t_{SEED}	—	—	1.7	—	—	1.7	ms
FCU reset time		t_{FCUR}	35	—	—	35	—	—	μs

6.3.2 Reset Timing

Table 6.8 Reset Timing

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item		Symbol	Min	Typ	Max.	Unit	Test Conditions
RES# pulse width	Power-on	t_{RESWP}	2	—	—	ms	Figure 6.6
	Deep software standby mode	t_{RESWD}	1	—	—	ms	Figure 6.7
	Software standby mode	t_{RESWS}	1	—	—	ms	
	Other than above (except for programming or erasure of the ROM or E2 DataFlash memory or blank checking of the E2 DataFlash memory)	t_{RESW}	200	—	—	μs	
Wait time after RES# cancellation		t_{RESWT}	59	—	60	t_{cyc}	
Internal reset time (independent watchdog timer reset, watchdog timer reset, software reset)		t_{RESW2}	112	—	120	t_{cyc}	

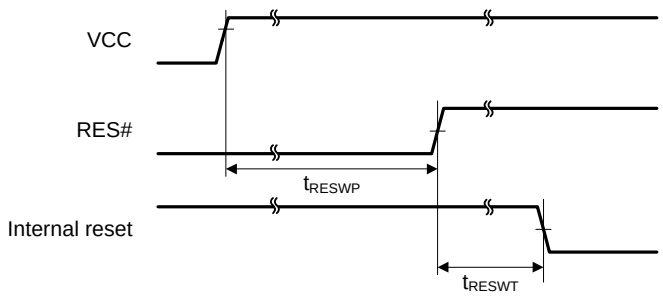


Figure 6.6 Reset Input Timing at Power-On

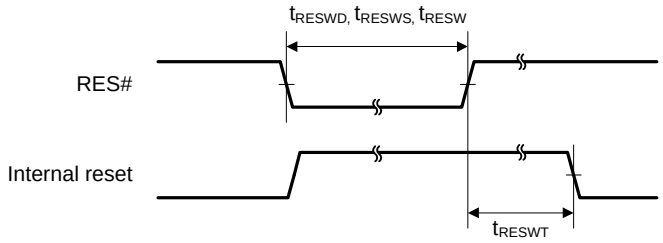


Figure 6.7 Reset Input Timing

6.8 E^2 DataFlash Characteristic

Table 6.22 E^2 DataFlash (Flash Memory for Data Storage) Characteristics (1)

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0
Temperature range for the programming/erasure operation: $T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Reprogram/erase cycle*1	N_{DPEC}	100000	—	—	Times	
Data hold time	t_{DDRP}	30*2	—	—	Year	Ta = +85°C

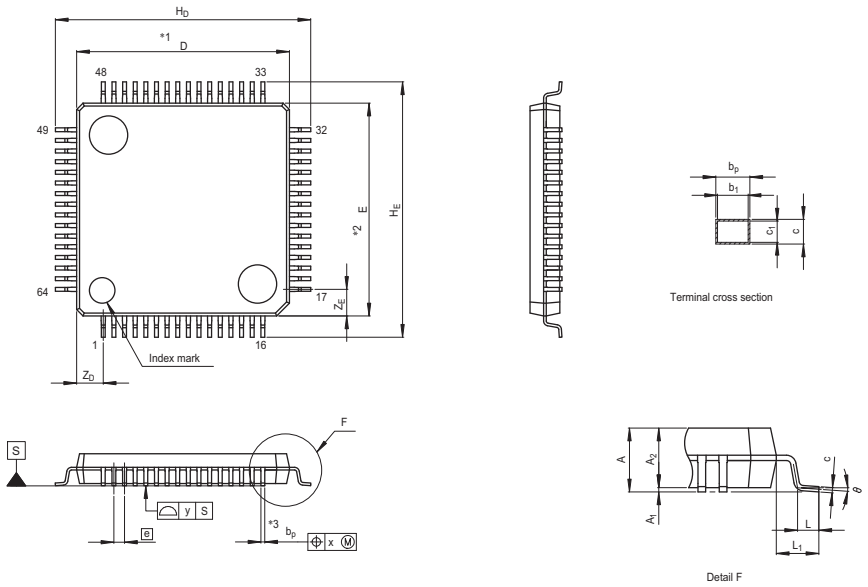
Note 1. Definition of reprogram/erase cycle:
The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 128-byte programming is performed 16 times for different addresses in 2-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).
Note 2. The value is obtained from the reliability test.

Table 6.23 E^2 DataFlash (Flash Memory for Data Storage) Characteristics (2)

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
$Ta = T_{opr}$

Item		Symbol	min	typ	max	Unit	Test Condition
Programming time	2 bytes	t_{DP2}	—	0.25	2	ms	FCLK = 50 MHz
Erasure time	32 bytes	t_{DE32}	—	2	20	ms	FCLK = 50 MHz $N_{DPEC} \leq 100$
	32 bytes	t_{DE32}	—	4	20	ms	FCLK = 50 MHz $N_{DPEC} > 100$
Blank check time	2 bytes	t_{DBC2}	—	—	30	μs	FCLK = 50 MHz
Suspend delay time during programming		t_{DSPD}	—	—	120	μs	Figure 6.31 PCLKB = 50 MHz
First suspend delay time during erasing (in suspend priority mode)		t_{DSESD1}	—	—	120	μs	
Second suspend delay time during erasing (in suspend priority mode)		t_{DSESD2}	—	—	300	μs	
Suspend delay time during erasing (in erasure priority mode)		t_{DSEED}	—	—	300	μs	

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP64-10x10-0.50	PLQP0064KB-A	64P6Q-A / FP-64K / FP-64KV	0.3g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure E 64-Pin LQFP (PLQP0064KB-A)

REVISION HISTORY	RX63T Group Datasheet

Rev.	Date	Description	
		Page	Summary
1.00	Aug 28, 2012	—	First Edition issued
2.00	Mar 11, 2013	Features	
		1	Changed
		1. Overview	
		2	1.1 Outline of Specifications, description changed
		2 to 8	Table 1.1 Outline of Specifications, changed
		9	Table 1.2 Comparison of Functions for Different Packages, changed
		10 to 12	Table 1.3 List of Products, changed
		12	Figure 1.1 How to Read the Product Part Number, changed
		13	Figure 1.2 Block Diagram, changed
		14 to 18	Table 1.4 Pin Functions, changed
		19	Figure 1.3 Pin Assignment (144-Pin LQFP), added
		20	Figure 1.4 Pin Assignment (120-Pin LQFP), added
		21	Figure 1.5 Pin Assignment (112-Pin LQFP), added
		22	Figure 1.6 Pin Assignment (100-Pin LQFP), added
		23	Figure 1.7 Pin Assignment (64-Pin LQFP), notes changed
		24	Figure 1.8 Pin Assignment (48-Pin LQFP), notes changed
		25 to 28	Table 1.5 List of Pins and Pin Functions (144-Pin LQFP), added
		29 to 32	Table 1.6 List of Pins and Pin Functions (120-Pin LQFP), added
		33 to 36	Table 1.7 List of Pins and Pin Functions (112-Pin LQFP), added
		37 to 39	Table 1.8 List of Pins and Pin Functions (100-Pin LQFP), added
		3. Address Space	
		49	Figure 3.1 Memory Map in Each Operating Mode, changed
		50	3.2 External Address Space, added
		4. I/O Registers	
		52	(3) Number of Access Cycles to I/O Registers, description changed
		53 to 103	Table 4.1 List of I/O Registers (Address Order), changed
		5. Electrical Characteristics [144-, 120-, 112- and 100-Pin Versions]	
		104 to 148	Added
		6. Electrical Characteristics [64- and 48-Pin Versions]	
		149	Title changed
		152	Table 6.6 Clock Timing, changed
		158	Table 6.10 Timing of On-Chip Peripheral Modules (1), changed
		160	Table 6.12 Timing of On-Chip Peripheral Modules (3), changed
		170	6.6 Oscillation Stop Detection Circuit Characteristics, title changed
		170	Table 6.18 Oscillation Stop Detection Circuit Characteristics, title changed
		171	Table 6.19 ROM (Flash Memory for Code Storage) Characteristics (1), added
		171	Table 6.20 ROM (Flash Memory for Code Storage) Characteristics (2), title and description changed
		172	Table 6.21 DataFlash (Flash Memory for Data Storage) Characteristics (1), added
		172	Table 6.22 DataFlash (Flash Memory for Data Storage) Characteristics (2), title and description changed
		Appendix 1. Package Dimensions	
		174 to 177	Figure A 144-Pin LQFP (PLQP0144KA-A) to Figure D 100-Pin LQFP (PLQP0100KB-A), added
2.10	Sep 26, 2013	The RX63T Group and RX63T changed to this MCU	
		Features	
		1	Changed
		1. Overview	
		2 to 8	Table 1.1 Outline of Specifications, changed, Note 1, added.
		9	Table 1.2 Comparison of Functions for Different Packages, changed, Note 2, added.
		10 to 14	Table 1.3 List of Products, changed, Note 1, added
		15	Figure 1.1 How to Read the Product Part Number, changed
		28 to 31	Table 1.5 List of Pins and Pin Functions (144-Pin LQFP), changed
		32 to 35	Table 1.6 List of Pins and Pin Functions (120-Pin LQFP), changed