# Renesas Electronics America Inc - R5F563TBBDFB#V1 Datasheet

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Not For New Designs |
| Core Processor | RX |
| Core Size | 32-Bit Single-Core |
| Speed | 100MHz |
| Connectivity | CANbus, EBI/EMI, I²C, LINbus, SCI, SPI, USB |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 81 |
| Program Memory Size | 256KB (256K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 32K x 8 |
| RAM Size | 24K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 3.6V |
| Data Converters | A/D 20x10b, 8x12b; D/A 2x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 144-LQFP |
| Supplier Device Package | 144-LFQFP (20x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f563tbbdfb-v1 |

**Table 1.2 Comparison of Functions for Different Packages**

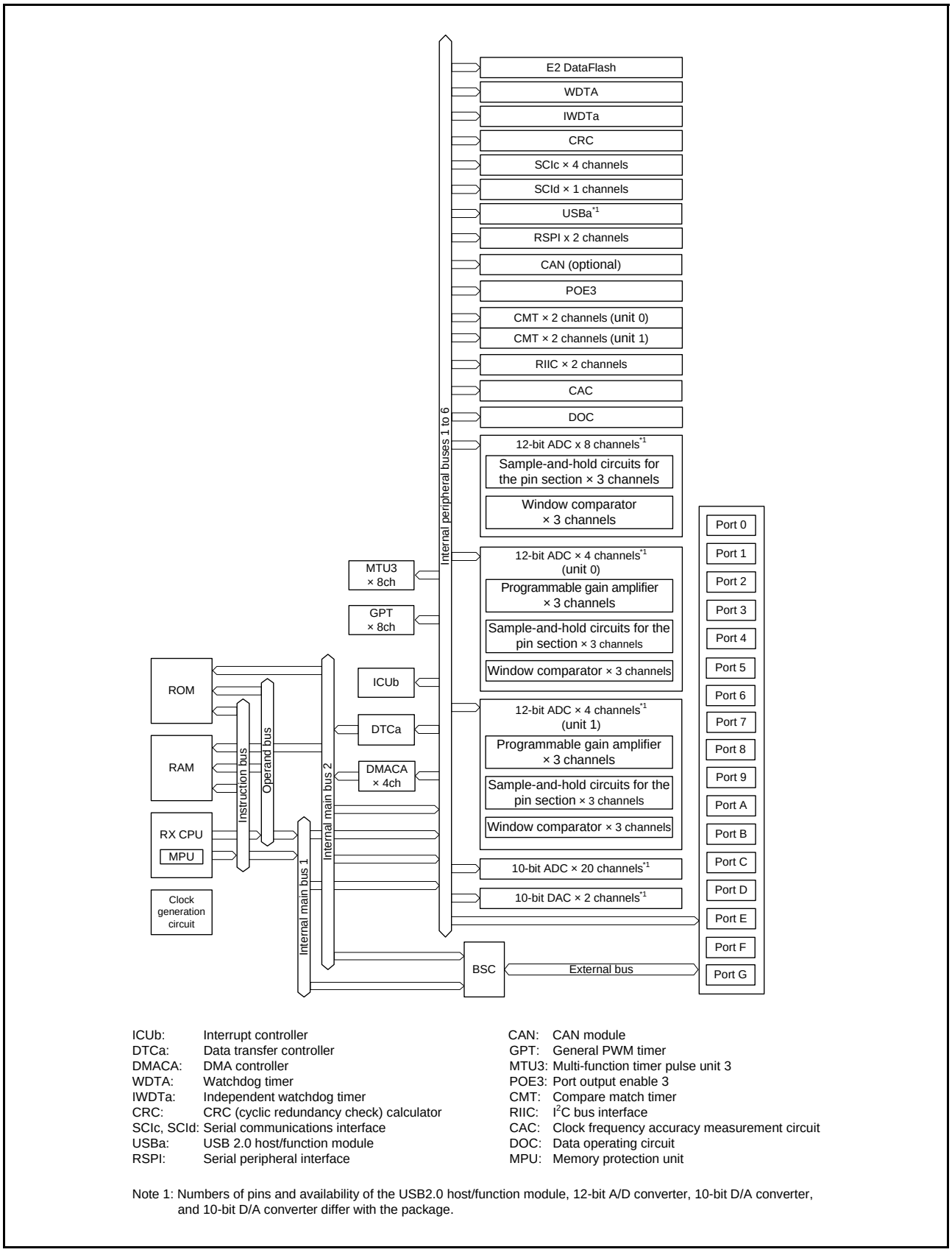
| Functions | | | RX63T Group | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Package** | | | **144 Pins** | **120 Pins** | **112 Pins** | **100 Pins** | **64 Pins** | **48 Pins** |
| External bus | | | 16 bits | | | | — | |
| External address space | | | 1 Mbyte × 4 areas | | | | — | |
| DMA | DMA controller (DMACA) | | Ch. 0 to 3 | | | | | |
| | Data transfer controller (DTCa) | | Supported | | | | | |
| Interrupt controller (ICUb) | NMI pin | | Supported | | | | | |
| | IRQ pin | | Supported (x 8) | | | | Supported (x 6) | |
| Timers | Multi-function timer pulse unit 3 (MTU3)*1 | | Ch. 0 to 7 | | | | | |
| | General PWM timer (GPT)*1 | Generation of delays in PWM, not supported | Ch. 0 to 7 | | | | Ch. 0 to 3 | |
| | | Generation of delays in PWM, supported | Ch. 0 to 3 | | | | — | |
| | Port output enable 3 (POE3) | | Supported (POE pins × 6) | | | Supported (POE pins × 5) | Supported (POE pins × 4) | |
| | Compare match timer (CMT) | | Ch. 0 to 3 | | | | | |
| | Watchdog timer (WDTA) | | Supported | | | | | |
| | Independent watchdog timer (IWDTa) | | Supported | | | | | |
| Communication function | USB2.0 host/function module (USBa) | | Ch. 0 | | — | | | |
| | Serial communications interfaces (SCIc) | | Ch. 0 to 3 | | | Ch. 0 to 2 | Ch. 0, 1 | |
| | Serial communications interfaces (SCId) | | Ch. 12 | | | | | |
| | $I^2C$ bus interfaces (RIIC) | | Ch. 0, 1 | | Ch. 0 | | | |
| | Serial peripheral interfaces (RSPI) | | Ch. 0, 1 | | | | Ch. 0 | |
| | CAN module (CAN) (as an optional function)*1 | | Ch. 0 | | | | — | |
| 12-bit A/D converter (S12ADB) | | | 4 channels × 2 units | | | | 8 channels × 1 unit (AN000 to 007) | 8 channels × 1 unit (AN000 to 004, 007) |
| | Three-channel simultaneous sampling function | | 2 units | | | | 1 unit | |
| | Programmable gain amplifier | | 3 channels × 2 units | | | | — | |
| | Window comparator | | 3 channels × 2 units | | | | 3 channels × 1 unit | |
| 10-bit A/D converter (ADA) | | | 20 channels | 12 channels | | | — | |
| D/A converter (DAa) | | | Ch. 0, 1 | | | | — | |
| Clock Frequency Accuracy Measurement Circuit | | | Supported | | | | | |
| Digital power supply controller (DPC)*2 | | | Supported | | | | Not supported | |

Note 1. For the MTU3 and GPT, the number of pins will differ with the package. See the list of pins and pin functions for details. In addition, the CAN module is an optional function. For details, see Table 1.3.

Note 2. Not provided for the product ID code O.

## 1.3 Block Diagram

Figure 1.2 shows a block diagram.



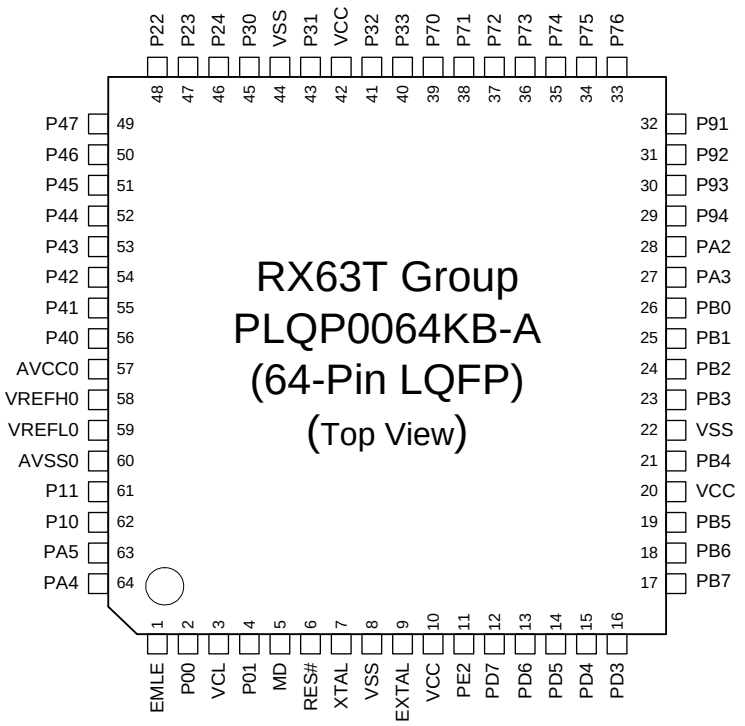

ICUb: Interrupt controller
DTCa: Data transfer controller
DMACA: DMA controller
WDTA: Watchdog timer
IWDTa: Independent watchdog timer
CRC: CRC (cyclic redundancy check) calculator
SCIc, SCId: Serial communications interface
USBa: USB 2.0 host/function module
RSPI: Serial peripheral interface
CAN: CAN module
GPT: General PWM timer
MTU3: Multi-function timer pulse unit 3
POE3: Port output enable 3
CMT: Compare match timer
RIIC: $I^2C$ bus interface
CAC: Clock frequency accuracy measurement circuit
DOC: Data operating circuit
MPU: Memory protection unit

Note 1: Numbers of pins and availability of the USB2.0 host/function module, 12-bit A/D converter, 10-bit D/A converter, and 10-bit D/A converter differ with the package.

**Figure 1.2 Block Diagram**

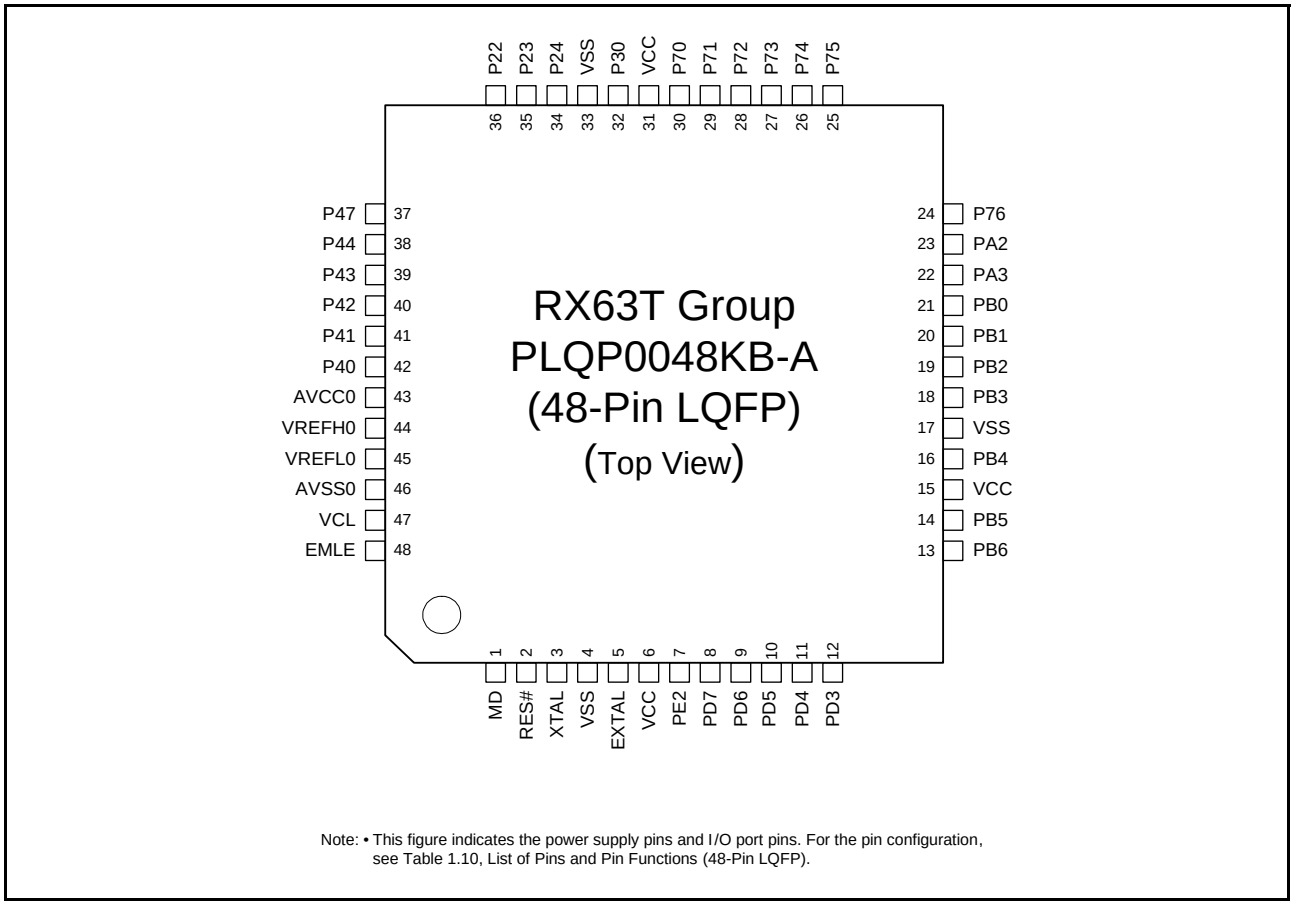
**Table 1.4 Pin Functions (2/5)**

| Classifications | Pin Name | I/O | Description |
|---|---|---|---|
| Interrupt | NMI | Input | Non-maskable interrupt request pin |
| | IRQ0 to IRQ7 | Input | Maskable interrupt request pin |
| Multi-function timer pulse unit 3 | MTIOC0A, MTIOC0B MTIOC0C, MTIOC0D | I/O | The TGRA0 to TGRD0 input capture input/output compare output/ PWM output pins |
| | MTIOC1A, MTIOC1B | I/O | The TGRA1 and TGRB1 input capture input/output compare output/ PWM output pins |
| | MTIOC2A, MTIOC2B | I/O | The TGRA2 and TGRB2 input capture input/output compare output/ PWM output pins |
| | MTIOC3A, MTIOC3B MTIOC3C, MTIOC3D | I/O | The TGRA3 to TGRD3 input capture input/output compare output/ PWM output pins |
| | MTIOC4A, MTIOC4B MTIOC4C, MTIOC4D | I/O | The TGRA4 to TGRD4 input capture input/output compare output/ PWM output pins |
| | MTIC5U, MTIC5V MTIC5W | Input | The TGRU5, TGRV5, and TGRW5 input capture input/dead time compensation input pins |
| | MTIOC6A, MTIOC6B MTIOC6C, MTIOC6D | I/O | The TGRA6 to TGRD6 input capture input/output compare output/ PWM output pins |
| | MTIOC7A, MTIOC7B MTIOC7C, MTIOC7D | I/O | The TGRA7 to TGRD7 input capture input/output compare output/ PWM output pins |
| | MTCLKA, MTCLKB MTCLKC, MTCLKD | Input | Input pins for external clock |
| Port output enable 3 | POE0#, POE4# POE8#, POE10# POE11#, POE12# | Input | Input pins for request signals to place the MTU/GPT large-current pins in the high impedance state |
| General PWM timer | GTIOC0A, GTIOC0B | I/O | The GPT0.GTGRA and GPT0.GTGRB input capture input/output compare output/PWM output pins. |
| | GTIOC1A, GTIOC1B | I/O | The GPT1.GTGRA and GPT1.GTGRB input capture input/output compare output/PWM output pins. |
| | GTIOC2A, GTIOC2B | I/O | The GPT2.GTGRA and GPT2.GTGRB input capture input/output compare output/PWM output pins. |
| | GTIOC3A, GTIOC3B | I/O | The GPT3.GTGRA and GPT3.GTGRB input capture input/output compare output/PWM output pins. |
| | GTETRG0 | Input | External trigger input pin for the GPT0 to GPT3 |
| | GTIOC4A, GTIOC4B | I/O | The GPT4.GTGRA and GPT4.GTGRB input capture input/output compare output/PWM output pins. |
| | GTIOC5A, GTIOC5B | I/O | The GPT5.GTGRA and GPT5.GTGRB input capture input/output compare output/PWM output pins. |
| | GTIOC6A, GTIOC6B | I/O | The GPT6.GTGRA and GPT6.GTGRB input capture input/output compare output/PWM output pins. |
| | GTIOC7A, GTIOC7B | I/O | The GPT7.GTGRA and GPT7.GTGRB input capture input/output compare output/PWM output pins. |
| | GTETRG1 | Input | External trigger input pin for the GPT4 to GPT7 |




Note: • This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.9, List of Pins and Pin Functions (64-Pin LQFP).

**Figure 1.7 Pin Assignment (64-Pin LQFP)**




Note: • This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.10, List of Pins and Pin Functions (48-Pin LQFP).

**Figure 1.8 Pin Assignment (48-Pin LQFP)**

**Table 1.6 List of Pins and Pin Functions (120-Pin LQFP) (3/4)**

| Pin Number 120-Pin LQFP | Power Supply Clock System Control | I/O Port | Bus | Timer (MTU3, GPT, POE3, CAC) | Communications (SCIc, SCId, RSPI, RIIC, CAN, USB) | Interrupt | S12ADB, AD, DA |
|---|---|---|---|---|---|---|---|
| 75 | VSS | | | | | | |
| 76 | | P30 | D10/[A10/D10] | MTIOC0B/MTCLKD | SCK0/SSLA0/SSLB0 | | |
| 77 | | P26 | CS0# | | TXD1/SMOSI1/SSDA1/SDA1 | | |
| 78 | | P25 | CS1# | | SCK1/SCL1 | | |
| 79 | | P24 | D11/[A11/D11] | | CTS0#/RTS0#/SS0#/RSPCKA/RSPCKB | IRQ4 | |
| 80 | | P23 | D12/[A12/D12] | CACREF | TXD0/SMOSI0/SSDA0/MOSIA/MOSIB/CTX1 | | |
| 81 | | P22 | D13/[A13/D13] | | RXD0/SMISO0/SSCL0/MISOA/MISOB/CRX1 | | ADTRG# |
| 82 | | P21 | D14/[A14/D14] | MTCLKA | | IRQ6-DS | ADTRG1# |
| 83 | | P20 | D15/[A15/D15] | MTCLKB | | IRQ7-DS | ADTRG0# |
| 84 | | P65 | A0/BC0# | | | | AN5 |
| 85 | | P64 | A1 | | | | AN4 |
| 86 | AVCC | | | | | | |
| 87 | VREF | | | | | | |
| 88 | AVSS | | | | | | |
| 89 | | P63 | A2 | | | | AN3 |
| 90 | | P62 | A3 | | | | AN2 |
| 91 | | P61 | A4 | | | | AN1 |
| 92 | | P60 | A5 | | | | AN0 |
| 93 | | P55 | | | | | AN11/DA1 |
| 94 | | P54 | | | | | AN10/DA0 |
| 95 | | P53 | A6 | | | | AN9 |
| 96 | | P52 | A7 | | | | AN8 |
| 97 | | P51 | | | | | AN7 |
| 98 | | P50 | | | | | AN6 |
| 99 | | P47 | | | | | AN103/CVREFH |
| 100 | | P46 | | | | | AN102 |
| 101 | | P45 | | | | | AN101 |
| 102 | | P44 | | | | | AN100 |
| 103 | | P43 | | | | | AN003/CVREFL |
| 104 | | P42 | | | | | AN002 |
| 105 | | P41 | | | | | AN001 |
| 106 | | P40 | | | | | AN000 |
| 107 | AVCC0 | | | | | | |
| 108 | VREFH0 | | | | | | |
| 109 | VREFL0 | | | | | | |
| 110 | AVSS0 | | | | | | |

**Table 1.8 List of Pins and Pin Functions (100-Pin LQFP) (1/3)**

| Pin Number 100-Pin LQFP | Power Supply Clock System Control | I/O Port | Bus | Timer (MTU3, GPT, POE3, CAC) | Communications (SCIc, SCId, RSPI, RIIC, CAN) | Interrupt | S12ADB, AD, DA |
|---|---|---|---|---|---|---|---|
| 1 | | PE5 | BCLK | | | IRQ0 | |
| 2 | EMLE | | | | | | |
| 3 | VSS | | | | | | |
| 4 | | P01 | RD# | | CTS0#/RTS0#/SS0# | | |
| 5 | VCL | | | | | | |
| 6 | | P00 | CS1# | CACREF | | | |
| 7 | MD/FINED | | | | | | |
| 8 | | PE4 | A10 | POE10#/MTCLKC | | IRQ1 | |
| 9 | | PE3 | A11 | POE11#/MTCLKD | | IRQ2-DS | |
| 10 | RES# | | | | | | |
| 11 | XTAL | | | | | | |
| 12 | VSS | | | | | | |
| 13 | EXTAL | | | | | | |
| 14 | VCC | | | | | | |
| 15 | | PE2 | | POE10# | | NMI | |
| 16 | | PE1 | WR0#/WR# | | CTS12#/RTS12#/ SS12#/SSLA3/SSLB3 | | |
| 17 | | PE0 | WR1#/BC1#/ WAIT# | | SSLA2/SSLB2/CRX1 | IRQ7 | |
| 18 | TRST# | PD7 | | GTIOC0A | CTS0#/RTS0#/SS0#/ SSLA1/SSLB1/CTX1 | | |
| 19 | TMS | PD6 | | GTIOC0B | SSLA0/SSLB0 | | |
| 20 | TDI | PD5 | | GTIOC1A | RXD1/SMISO1/SSCL1 | IRQ6 | |
| 21 | TCK/FINEC | PD4 | | GTIOC1B | SCK1 | | |
| 22 | TDO | PD3 | | GTIOC2A | TXD1/SMOSI1/SSDA1 | | |
| 23 | | PD2 | CS2# | GTIOC2B | MOSIA/MOSIB | | |
| 24 | | PD1 | CS0# | GTIOC3A | MISOA/MISOB | | |
| 25 | | PD0 | A12 | GTIOC3B | RSPCKA/RSPCKB | | |
| 26 | | PB7 | A19 | | SCK12 | | |
| 27 | | PB6 | A18 | | RXD12/SMISO12/ SSCL12/RXDX12/ CRX1 | IRQ2 | |
| 28 | | PB5 | A17 | | TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/CTX1 | | |
| 29 | PLLVCC | | | | | | |
| 30 | | PB4 | A16 | POE8#/GTETRG0 | | IRQ3-DS | |
| 31 | PLLVSS | | | | | | |
| 32 | | PB3 | A15 | MTIOC0A/CACREF | SCK0 | | |
| 33 | | PB2 | | MTIOC0B | TXD0/SMOSI0/ SSDA0/SDA0 | | |
| 34 | | PB1 | | MTIOC0C | RXD0/SMISO0/ SSCL0/SCL0 | IRQ4 | |
| 35 | | PB0 | A14 | MTIOC0D | MOSIA/MOSIB | | |
| 36 | | PA5 | | MTIOC1A | RXD0/SMISO0/ SSCL0/ MISOA/MISOB | | ADTRG1# |

- Longword-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.L  #SFR_DATA, [R1]
CMP    [R1].L, R1
;; Next process
```

If multiple registers are written to and a subsequent instruction should be executed after the write operations are entirely completed, only read the I/O register that was last written to and execute the operation using the value; it is not necessary to read or execute operation for all the registers that were written to.

### (3) Number of Access Cycles to I/O Registers

For the number of I/O register access cycles, refer to Table 4.1, List of I/O Registers (Address Order).
The number of access cycles to I/O registers is obtained by following equation.*1

Number of access cycles to I/O registers = Number of bus cycles for internal main bus 1 +
Number of divided clock synchronization cycles +
Number of bus cycles for internal peripheral bus 1 to 6

The number of bus cycles of internal peripheral bus 1 to 6 differs according to the register to be accessed.
When peripheral functions connected to internal peripheral bus 2 to 6 are accessed, the number of divided clock synchronization cycles is added.
The number of divided clock synchronization cycles differs depending on the frequency ratio between ICLK and PCLK (or FCLK, BCLK) or bus access timing.
In the peripheral function unit, when the frequency ratio of ICLK is equal to or greater than that of PCLK (or FCLK), the sum of the number of bus cycles for internal main bus 1 and the number of the divided clock synchronization cycles will be one cycle of PCLK (or FCLK) at a maximum. Therefore, one PCLK (or FCLK) has been added to the number of access states shown in Table 4.1.
When the frequency ratio of ICLK is lower than that of PCLK (or FCLK), the subsequent bus access is started from the ICLK cycle following the completion of the access to the peripheral functions. Therefore, the access cycles are described on an ICLK basis.
In the external bus control unit, the sum of the number of bus cycles for internal main bus 1 and the number of divided clock synchronization cycles will be one cycle of BCLK at a maximum. Therefore, one BCLK is added to the number of access cycles shown in Table 4.1.

Note 1. This applies to the number of cycles when the access from the CPU does not conflict with the instruction fetching to the external memory or bus access from the different bus master (DMAC or DTC).

### (4) Note on Sleep Mode and Mode Transition

During sleep mode or a mode transition, do not write to the system control related registers (indicated by 'SYSTEM' in the Module Symbol column in Table 4.1, List of I/O Registers (Address Order)).

**Table 4.1 List of I/O Registers (Address Order) (17/48)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Module Name | Remarks |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | | |
| 0008 83B2h | RSPI1 | RSPI Command Register 1 | SPCMD1 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | RSPI | Not present in versions with 64 or 48 pins. |
| 0008 83B4h | RSPI1 | RSPI Command Register 2 | SPCMD2 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 64 or 48 pins. |
| 0008 83B6h | RSPI1 | RSPI Command Register 3 | SPCMD3 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 64 or 48 pins. |
| 0008 83B8h | RSPI1 | RSPI Command Register 4 | SPCMD4 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 64 or 48 pins. |
| 0008 83BAh | RSPI1 | RSPI Command Register 5 | SPCMD5 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 64 or 48 pins. |
| 0008 83BCh | RSPI1 | RSPI Command Register 6 | SPCMD6 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 64 or 48 pins. |
| 0008 83BEh | RSPI1 | RSPI Command Register 7 | SPCMD7 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 64 or 48 pins. |
| 0008 9000h | S12AD | A/D Control Register | ADCSR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADB | |
| 0008 9004h | S12AD | A/D Channel Select Register A | ADANSA | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 9008h | S12AD | A/D-Converted Value Addition Mode Select Register | ADADS | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 900Ch | S12AD | A/D-Converted Value Addition Count Select Register | ADADC | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 900Eh | S12AD | A/D Control Extended Register | ADCER | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 9010h | S12AD | A/D Start Trigger Select Register | ADSTRGR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 9014h | S12AD | A/D Channel Select Register B | ADANSB | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 9018h | S12AD | A/D Data-Doubling Register | ADDBLDR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 901Eh | S12AD | A/D Self-Diagnosis Data Register | ADRD | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 9020h | S12AD | A/D Data Register 0 | ADDR0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 9022h | S12AD | A/D Data Register 1 | ADDR1 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 9024h | S12AD | A/D Data Register 2 | ADDR2 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 9026h | S12AD | A/D Data Register 3 | ADDR3 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 9028h | S12AD | A/D Data Register 4 | ADDR4 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 144, 120, 112, or 100 pins. |
| 0008 902Ah | S12AD | A/D Data Register 5 | ADDR5 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 144, 120, 112, or 100 pins. |
| 0008 902Ch | S12AD | A/D Data Register 6 | ADDR6 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 144, 120, 112, or 100 pins. |
| 0008 902Eh | S12AD | A/D Data Register 7 | ADDR7 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 144, 120, 112, or 100 pins. |
| 0008 9060h | S12AD | A/D Sampling State Register 0 | ADSSTR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 9066h | S12AD | A/D Sample and Hold Circuit Control Register | ADSHCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 9073h | S12AD | A/D Sampling State Register 1 | ADSSTR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 9074h | S12AD | A/D Sampling State Register 2 | ADSSTR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 9075h | S12AD | A/D Sampling State Register 3 | ADSSTR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 9076h | S12AD | A/D Sampling State Register 4 | ADSSTR4 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 144, 120, 112, or 100 pins. |
| 0008 9077h | S12AD | A/D Sampling State Register 5 | ADSSTR5 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 144, 120, 112, or 100 pins. |
| 0008 9078h | S12AD | A/D Sampling State Register 6 | ADSSTR6 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 144, 120, 112, or 100 pins. |
| 0008 9079h | S12AD | A/D Sampling State Register 7 | ADSSTR7 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 144, 120, 112, or 100 pins. |
| 0008 9080h | S12AD | A/D Group Scan Priority Control Register | ADGSPCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 9084h | S12AD | A/D Data-Doubling Register A | ADDBLDRA | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 9086h | S12AD | A/D Data-Doubling Register B | ADDBLDRB | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 908Ah | S12AD | A/D Programmable Gain Amplifier Register | ADPG | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 64 or 48 pins. |

**Table 4.1 List of I/O Registers (Address Order) (25/48)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Module Name | Remarks |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | | |
| 0008 C14Ch | MPC | P14 Pin Function Control Register | P14PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC | Not present in versions with 120, 112, 100, 64, or 48 pins. |
| 0008 C150h | MPC | P20 Pin Function Control Register | P20PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 64 or 48 pins. |
| 0008 C151h | MPC | P21 Pin Function Control Register | P21PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 64 or 48 pins. |
| 0008 C152h | MPC | P22 Pin Function Control Register | P22PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 C153h | MPC | P23 Pin Function Control Register | P23PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 C154h | MPC | P24 Pin Function Control Register | P24PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 C155h | MPC | P25 Pin Function Control Register | P25PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 112, 100, 64, or 48 pins. |
| 0008 C156h | MPC | P26 Pin Function Control Register | P26PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 112, 100, 64, or 48 pins. |
| 0008 C158h | MPC | P30 Pin Function Control Register | P30PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 C159h | MPC | P31 Pin Function Control Register | P31PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 48 pins. |
| 0008 C15Ah | MPC | P32 Pin Function Control Register | P32PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 48 pins. |
| 0008 C15Bh | MPC | P33 Pin Function Control Register | P33PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 48 pins. |
| 0008 C15Ch | MPC | P34 Pin Function Control Register | P34PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 120, 112, 100, 64, or 48 pins. |
| 0008 C15Dh | MPC | P35 Pin Function Control Register | P35PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 120, 112, 100, 64, or 48 pins. |
| 0008 C160h | MPC | P40 Pin Function Control Register | P40PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 C161h | MPC | P41 Pin Function Control Register | P41PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 C162h | MPC | P42 Pin Function Control Register | P42PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 C163h | MPC | P43 Pin Function Control Register | P43PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 C164h | MPC | P44 Pin Function Control Register | P44PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 C165h | MPC | P45 Pin Function Control Register | P45PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 48 pins. |
| 0008 C166h | MPC | P46 Pin Function Control Register | P46PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 48 pins. |
| 0008 C167h | MPC | P47 Pin Function Control Register | P47PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 C168h | MPC | P50 Pin Function Control Register | P50PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 64 or 48 pins. |
| 0008 C169h | MPC | P51 Pin Function Control Register | P51PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 64 or 48 pins. |
| 0008 C16Ah | MPC | P52 Pin Function Control Register | P52PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 64 or 48 pins. |
| 0008 C16Bh | MPC | P53 Pin Function Control Register | P53PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 64 or 48 pins. |
| 0008 C16Ch | MPC | P54 Pin Function Control Register | P54PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 64 or 48 pins. |
| 0008 C16Dh | MPC | P55 Pin Function Control Register | P55PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 64 or 48 pins. |
| 0008 C16Eh | MPC | P56 Pin Function Control Register | P56PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 120, 112, 100, 64, or 48 pins. |
| 0008 C16Fh | MPC | P57 Pin Function Control Register | P57PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 120, 112, 100, 64, or 48 pins. |
| 0008 C170h | MPC | P60 Pin Function Control Register | P60PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 64 or 48 pins. |
| 0008 C171h | MPC | P61 Pin Function Control Register | P61PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 64 or 48 pins. |
| 0008 C172h | MPC | P62 Pin Function Control Register | P62PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 64 or 48 pins. |
| 0008 C173h | MPC | P63 Pin Function Control Register | P63PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 64 or 48 pins. |

**Table 4.1 List of I/O Registers (Address Order) (42/48)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Module Name | Remarks |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | | |
| 000C 2884h | GPTB | LOCO Count Value Register | LCNT | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | GPT | Not present in versions with 64, or 48 pins. |
| 000C 2886h | GPTB | LOCO Count Result Average Register | LCNTA | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64, or 48 pins. |
| 000C 2888h | GPTB | LOCO Count Result Register 0 | LCNT00 | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64, or 48 pins. |
| 000C 288Ah | GPTB | LOCO Count Result Register 1 | LCNT01 | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64, or 48 pins. |
| 000C 288Ch | GPTB | LOCO Count Result Register 2 | LCNT02 | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 288Eh | GPTB | LOCO Count Result Register 3 | LCNT03 | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 2890h | GPTB | LOCO Count Result Register 4 | LCNT04 | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 2892h | GPTB | LOCO Count Result Register 5 | LCNT05 | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 2894h | GPTB | LOCO Count Result Register 6 | LCNT06 | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 2896h | GPTB | LOCO Count Result Register 7 | LCNT07 | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 2898h | GPTB | LOCO Count Result Register 8 | LCNT08 | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 289Ah | GPTB | LOCO Count Result Register 9 | LCNT09 | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 289Ch | GPTB | LOCO Count Result Register 10 | LCNT10 | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 289Eh | GPTB | LOCO Count Result Register 11 | LCNT11 | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 28A0h | GPTB | LOCO Count Result Register 12 | LCNT12 | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 28A2h | GPTB | LOCO Count Result Register 13 | LCNT13 | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 28A4h | GPTB | LOCO Count Result Register 14 | LCNT14 | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 28A6h | GPTB | LOCO Count Result Register 15 | LCNT15 | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 28A8h | GPTB | LOCO Count Upper Permissible Deviation Register | LCNTDU | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 28AAh | GPTB | LOCO Count Lower Permissible Deviation Register | LCNTDL | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 2900h | GPT4 | General PWM Timer I/O Control Register | GTIOR | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 2902h | GPT4 | General PWM Timer Interrupt Output Setting Register | GTINTAD | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 2904h | GPT4 | General PWM Timer Control Register | GTCR | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 2906h | GPT4 | General PWM Timer Buffer Enable Register | GTBER | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 2908h | GPT4 | General PWM Timer Count Direction Register | GTUDC | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 290Ah | GPT4 | General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register | GTITC | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 290Ch | GPT4 | General PWM Timer Status Register | GTST | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 290Eh | GPT4 | General PWM Timer Counter | GTCNT | 16 | 16 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 2910h | GPT4 | General PWM Timer Compare Capture Register A | GTCCRA | 16 | 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 2912h | GPT4 | General PWM Timer Compare Capture Register B | GTCCRB | 16 | 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 2914h | GPT4 | General PWM Timer Compare Capture Register C | GTCCRC | 16 | 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 2916h | GPT4 | General PWM Timer Compare Capture Register D | GTCCRD | 16 | 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 2918h | GPT4 | General PWM Timer Compare Capture Register E | GTCCRE | 16 | 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |

## 5.3.1 Reset Timing

**Table 5.8 Reset Timing**

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. $T_a$ is common to conditions 1 to 3.

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| RES# pulse width | Power-on | $t_{RESWP}$ | 2 | — | — | ms | Figure 5.1 |
| | Deep software standby mode | $t_{RESWD}$ | 1 | — | — | ms | Figure 5.2 |
| | Software standby mode | $t_{RESWS}$ | 1 | — | — | ms | |
| | Programming or erasure of the ROM or E2 DataFlash memory or blank checking of the E2 DataFlash memory | $t_{RESWF}$ | 200 | — | — | µs | |
| | Other than above | $t_{RESW}$ | 200 | — | — | µs | |
| Wait time after RES# cancellation | | $t_{RESWT}$ | 59 | — | 60 | $t_{cyc}$ | |
| Internal reset time (independent watchdog timer reset, watchdog timer reset, software reset) | | $t_{RESW2}$ | 112 | — | 120 | $t_{cyc}$ | |

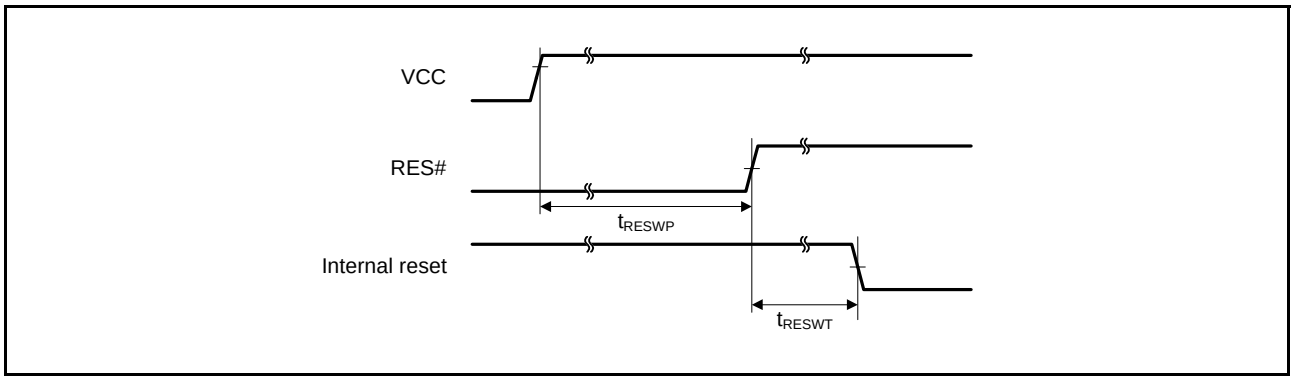



**Figure 5.1 Reset Input Timing at Power-On**

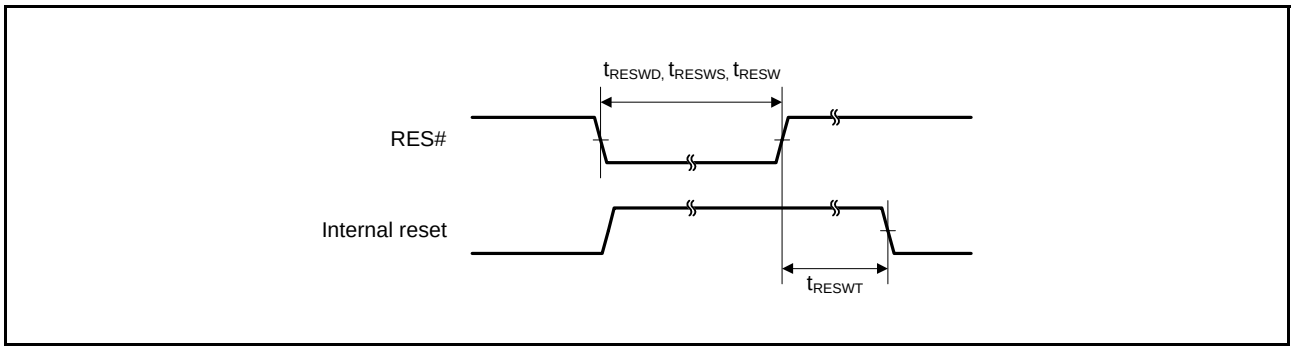
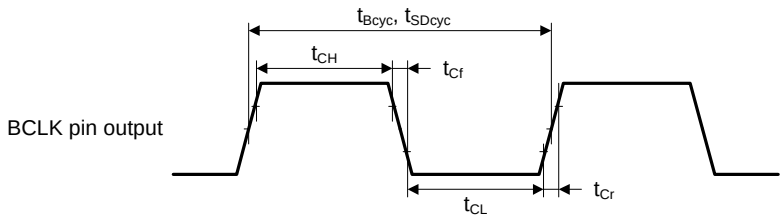



**Figure 5.2 Reset Input Timing**

Note 4. This is calculated from the formula below, where n is the number of cycles set by the PLLWTCR.PSTS[4:0] bits.

$$t_{PLLWT1} = t_{PLL1} + \frac{n + 131072}{f_{PLL}}$$

$$t_{PLLWT2} = t_{PLL2} + \frac{n + 131072}{f_{PLL}} = t_{MAINOSC} + t_{PLL1} + \frac{n + 131072}{f_{PLL}}$$




Test conditions: VOH = VCC × 0.7, VOL = VCC × 0.3, IOH = –1.0 mA, IOL = 1.0 mA, C = 30 pF

**Figure 5.3 BCLK Pin Output Timing**

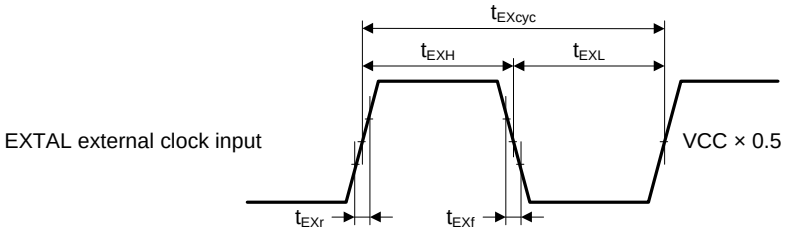



**Figure 5.4 EXTAL External Clock Input Timing**

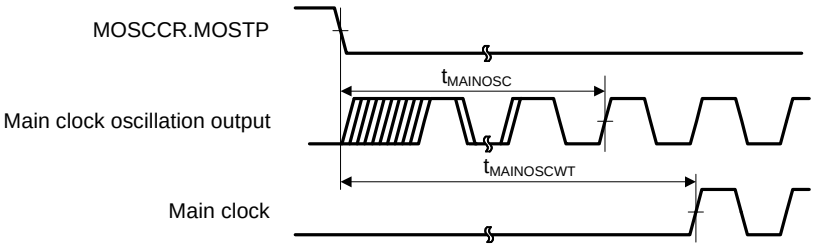



**Figure 5.5 Main Clock Oscillation Start Timing**

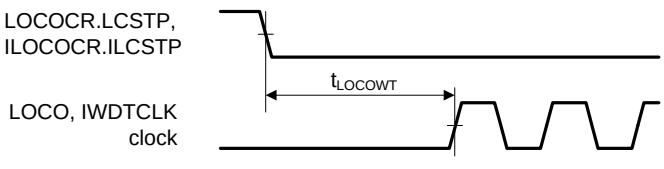



**Figure 5.6 LOCO, IWDTCLK Clock Oscillation Start Timing**

## 5.3.6 Timing of On-Chip Peripheral Modules

**Table 5.16 Timing of On-Chip Peripheral Modules (1)**

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. $T_a$ is common to conditions 1 to 3.

| Item | | | Symbol | Min. | Max. | Unit*1 | Test Conditions |
|---|---|---|---|---|---|---|---|
| I/O ports | Input data pulse width | | $t_{PRW}$ | 1.5 | — | $t_{Pcyc}$ | Figure 5.22 |
| MTU3 | Input capture input pulse width | Single-edge setting | $t_{TICW}$ | 3 | — | $t_{PAcyc}$ | Figure 5.23 |
| | | Both-edge setting | | 5 | — | | |
| | Input capture input fall time | | $t_{TICTF}$ | — | 0.1 | µs/V | When Input capture at rising edge, or Input capture at both edges is selected. |
| | Timer clock pulse width | Single-edge setting | $t_{TCKWH}$, $t_{TCKWL}$ | 3 | — | $t_{PAcyc}$ | Figure 5.25 |
| | | Both-edge setting | | 5 | — | | |
| | | Phase counting mode | | 5 | — | | |
| | Timer clock input fall time | | $t_{TCKTF}$ | — | 0.1 | µs/V | |
| POE3 | POE# input pulse width | | $t_{POEW}$ | 1.5 | — | $t_{Pcyc}$ | Figure 5.28 |
| GPT | Input capture input pulse width | Single-edge setting | $t_{GTICW}$ | 3 | — | $t_{PAcyc}$ | Figure 5.26 |
| | | Both-edge setting | | 5 | — | | |
| | Input capture input fall time | | $t_{GTICTF}$ | — | 0.1 | µs/V | When Input capture at rising edge, or Input capture at both edges is selected. When Count operation is started at rising edge, or Count operation is started at both edges is selected. When Count operation is stopped at rising edge, or Count operation is stopped at both edges is selected. When Counter is cleared at rising edge, or Counter is cleared at both edges is selected. |
| | External trigger input pulse width | Single-edge setting | $t_{OTETW}$ | 3 | — | $t_{PAcyc}$ | Figure 5.27 |
| | | Both-edge setting | | 5 | — | | |
| | External trigger input fall time | | $t_{GTETRGTF}$ | — | 0.1 | µs/V | When Count operation is started at rising edge, or Count operation is started at both edges is selected. When Count operation is stopped at rising edge, or Count operation is stopped at both edges is selected. When Counter is cleared at rising edge, or Counter is cleared at both edges is selected. |

### Table 5.16 Timing of On-Chip Peripheral Modules (2)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. $T_a$ is common to conditions 1 to 3.

| Item | | | Symbol | Min. | Max. | Unit*1 | Test Conditions |
|---|---|---|---|---|---|---|---|
| SCI | Input clock cycle | Asynchronous | $t_{Scyc}$ | 4 | — | $t_{Pcyc}$ | C = 30 pF<br>Figure 5.29 |
| | | Clock synchronous | | 6 | — | | |
| | Input clock pulse width | | $t_{SCKW}$ | 0.4 | 0.6 | $t_{Scyc}$ | |
| | Input clock rise time | | $t_{SCKr}$ | — | 20 | ns | |
| | Input clock fall time | | $t_{SCKf}$ | — | 20 | ns | |
| | Output clock cycle | Asynchronous | $t_{Scyc}$ | 16 | — | $t_{Pcyc}$ | |
| | | Clock synchronous | | 4 | — | | |
| | Output clock pulse width | | $t_{SCKW}$ | 0.4 | 0.6 | $t_{Scyc}$ | |
| | Output clock rise time | | $t_{SCKr}$ | — | 20 | ns | |
| | Output clock fall time | | $t_{SCKf}$ | — | 20 | ns | |
| | Transmit data delay time | Clock synchronous | $t_{TXD}$ | — | 40 | ns | Figure 5.30 |
| | Receive data setup time | Clock synchronous | $t_{RXS}$ | 40 | — | ns | |
| | Receive data hold time | Clock synchronous | $t_{RXH}$ | 40 | — | ns | |
| | Receive data fall time | | $t_{TICTF}$ | — | 0.1 | µs/V | When Noise Cancellation Function is not used. |
| A/D converter | 10-bit A/D converter trigger input pulse width | | $t_{TRGW}$ | 1.5 | — | $t_{Pcyc}$ | Figure 5.31 |
| | 12-bit A/D converter trigger input pulse width | | | 1.5 | — | | |
| CAC | CACREF input pulse width | $t_{Pcyc} \leq t_{cac}$*2 | $t_{CACREF}$ | 4.5 $t_{cac}$ + 3 $t_{Pcyc}$ | — | ns | |
| | | $t_{Pcyc} > t_{cac}$*2 | | 5 $t_{cac}$ + 6.5 $t_{Pcyc}$ | — | ns | |
| | CACREF input fall time | | $t_{CACREFTF}$ | — | 0.1 | µs/V | |

Note 1. $t_{Pcyc}$: PCLK cycle, $t_{PAcye}$: PCLKA cycle
Note 2. $t_{cac}$: CAC count clock source cycle.

### Table 5.16 Timing of On-Chip Peripheral Modules (3)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS =PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. $T_a$ is common to conditions 1 to 3.

High drive output is selected by the drive capacity control register.

| Item | | | | Symbol | Min. | Max. | Unit*1 | Test Conditions |
|---|---|---|---|---|---|---|---|---|
| RSPI | RSPCK clock cycle | Master | | $t_{SPcyc}$ | 2 | 4096 | $t_{Pcyc}$ | C = 30 pF, Figure 5.32 |
| | | Slave | | | 8 | 4096 | | |
| | RSPCK clock high pulse width | Master | | $t_{SPCKWH}$ | $(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2 - 3$ | — | ns | |
| | | Slave | | | $(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2$ | — | | |
| | RSPCK clock low pulse width | Master | | $t_{SPCKWL}$ | $(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2 - 3$ | — | ns | |
| | | Slave | | | $(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2$ | — | | |
| | RSPCK clock rise/fall time | Output | | $t_{SPCKR}$, $t_{SPCKF}$ | — | 5 | ns | |
| | | Input | | | — | 1 | µs | |
| | RSPCK clock fall time | Input | | $t_{SPCKF}$ | — | 0.1 | µs/V | |
| | Data input setup time | Master | | $t_{SU}$ | 4 | — | ns | C = 30 pF, Figure 5.33 to Figure 5.40 |
| | | Slave | | | $20 - t_{Pcyc}$ | — | | |
| | Data input hold time | Master | PCLKB division ratio set to a value other than 1/2 | $t_H$ | $t_{Pcyc}$ | — | ns | |
| | | | PCLKB division ratio set to 1/2 | $t_{HF}$ | 0 | — | | |
| | | Slave | | $t_H$ | $20 + 2 \times t_{Pcyc}$ | — | | |
| | SSL setup time | Master | | $t_{LEAD}$ | 1 | 8 | $t_{SPcyc}$ | |
| | | Slave | | | 4 | — | $t_{Pcyc}$ | |
| | SSL hold time | Master | | $t_{LAG}$ | 1 | 8 | $t_{SPcyc}$ | |
| | | Slave | | | 4 | — | $t_{Pcyc}$ | |
| | Data output delay time | Master | | $t_{OD}$ | — | 10 | ns | |
| | | Slave | | | — | $3 \times t_{Pcyc} + 40$ | | |
| | Data output hold time | Master | | $t_{OH}$ | 0 | — | ns | |
| | | Slave | | | 0 | — | | |
| | Successive transmission delay time | Master | | $t_{TD}$ | $t_{SPcyc} + 2 \times t_{Pcyc}$ | $8 \times t_{SPcyc} + 2 \times t_{Pcyc}$ | ns | |
| | | Slave | | | $4 \times t_{Pcyc}$ | — | | |
| | MOSI and MISO rise/fall time | Output | | $t_{DR}$, $t_{DF}$ | — | 5 | ns | |
| | | Input | | | — | 1 | µs | |
| | SSL rise/fall time | Output | | $t_{SSLr}$, $t_{SSLf}$ | — | 15 | ns | |
| | | Input | | | — | 1 | µs | |
| | Slave access time | | | $t_{SA}$ | — | 4 | $t_{Pcyc}$ | Figure 5.39 and Figure 5.40 |
| | Slave output release time | | | $t_{REL}$ | — | 3 | $t_{Pcyc}$ | |

Note 1. $t_{Pcyc}$: PCLK cycle

### Table 5.16 Timing of On-Chip Peripheral Modules (5)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. $T_a$ is common to conditions 1 to 3.

| Item | | Symbol | Min.*1,*2 | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| RIIC (Standard-mode) | SCL input cycle time | $t_{SCL}$ | $6(12) \times t_{IICcyc} + 1300$ | — | ns | Figure 5.36 |
| | SCL input high pulse width | $t_{SCLH}$ | $3(6) \times t_{IICcyc} + 300$ | — | ns | |
| | SCL input low pulse width | $t_{SCLL}$ | $3(6) \times t_{IICcyc} + 300$ | — | ns | |
| | SCL, SDA input rise time | $t_{Sr}$ | — | 1000 | ns | |
| | SCL, SDA input fall time | $t_{Sf}$ | — | 300 | ns | |
| | SCL, SDA input spike pulse removal time | $t_{SP}$ | 0 | $1(4) \times t_{IICcyc}$ | ns | |
| | SDA input bus free time | $t_{BUF}$ | $3(6) \times t_{IICcyc} + 300$ | — | ns | |
| | Start condition input hold time | $t_{STAH}$ | $t_{IICcyc} + 300$ | — | ns | |
| | Restart condition input setup time | $t_{STAS}$ | 1000 | — | ns | |
| | Stop condition input setup time | $t_{STOS}$ | 1000 | — | ns | |
| | Data input setup time | $t_{SDAS}$ | $t_{IICcyc} + 50$ | — | ns | |
| | Data input hold time | $t_{SDAH}$ | 0 | — | ns | |
| | SCL, SDA capacitive load | $C_b$ | — | 400 | pF | |
| RIIC (Fast-mode) | SCL input cycle time | $t_{SCL}$ | $6(12) \times t_{IICcyc} + 600$ | — | ns | |
| | SCL input high pulse width | $t_{SCLH}$ | $3(6) \times t_{IICcyc} + 300$ | — | ns | |
| | SCL input low pulse width | $t_{SCLL}$ | $3(6) \times t_{IICcyc} + 300$ | — | ns | |
| | SCL, SDA input rise time | $t_{Sr}$ | $20 + 0.1C_b$ | 300 | ns | |
| | SCL, SDA input fall time | $t_{Sf}$ | $20 + 0.1C_b$ | 300 | ns | |
| | SCL, SDA input spike pulse removal time | $t_{SP}$ | 0 | $1(4) \times t_{IICcyc}$ | ns | |
| | SDA input bus free time | $t_{BUF}$ | $3(6) \times t_{IICcyc} + 300$ | — | ns | |
| | Start condition input hold time | $t_{STAH}$ | $t_{IICcyc} + 300$ | — | ns | |
| | Restart condition input setup time | $t_{STAS}$ | 300 | — | ns | |
| | Stop condition input setup time | $t_{STOS}$ | 300 | — | ns | |
| | Data input setup time | $t_{SDAS}$ | $t_{IICcyc} + 50$ | — | ns | |
| | Data input hold time | $t_{SDAH}$ | 0 | — | ns | |
| | SCL, SDA capacitive load | $C_b$ | — | 400 | pF | |

Note: • $t_{IICcyc}$: RIIC internal reference clock (IICϕ) cycle

Note 1. The value within parentheses is applicable when the value of the ICMR3.NF[1:0] bits is 11b while the digital filter is enabled by the setting ICFER.NFE = 1.

Note 2. Cb is the total capacitance of the bus lines.

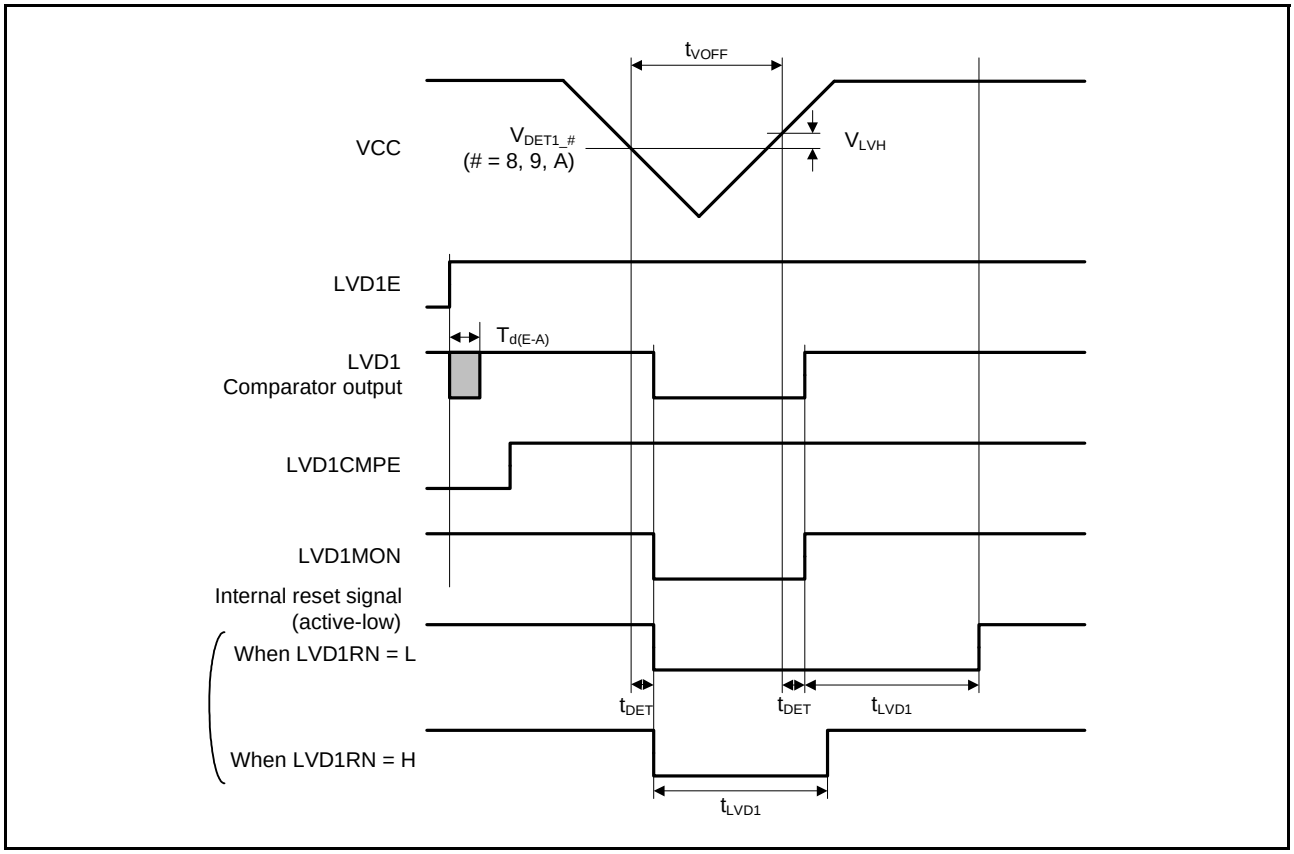



**Figure 5.41 Voltage Detection Circuit Timing ($V_{DET1}$)**

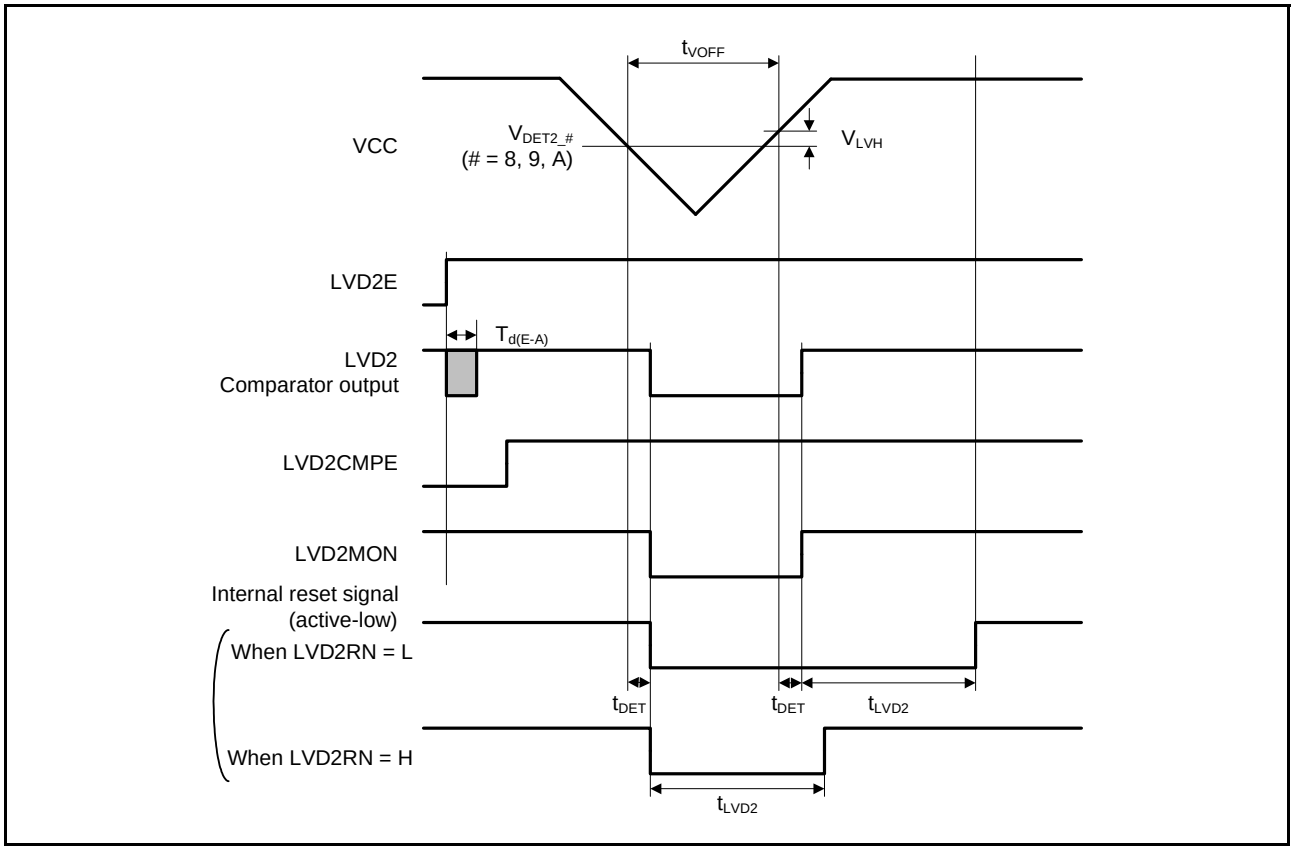



**Figure 5.42 Voltage Detection Circuit Timing ($V_{DET2}$)**

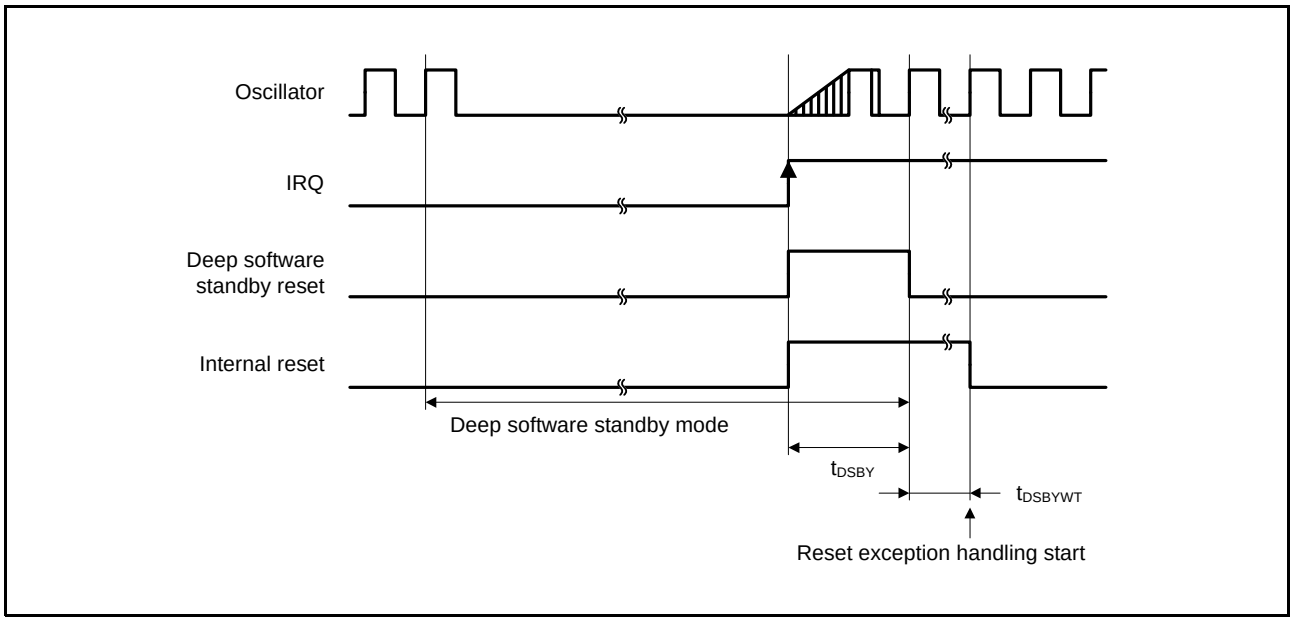



**Figure 6.9 Deep Software Standby Mode Cancellation Timing**

## 6.3.4 Control Signal Timing

**Table 6.10 Control Signal Timing**

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = $T_{opr}$

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| NMI pulse width | $t_{NMIW}$ | 200 | — | — | ns | $t_{Pcyc}$ × 2 ≤ 200ns, Figure 6.10 |
| | | 2 | | | $t_{Pcyc}$ | $t_{Pcyc}$ × 2 > 200ns, Figure 6.10 |
| IRQ pulse width | $t_{IRQW}$ | 200 | — | — | ns | $t_{Pcyc}$ × 2 ≤ 200ns, Figure 6.11 |
| | | 2 | | | $t_{Pcyc}$ | $t_{Pcyc}$ × 2 > 200ns, Figure 6.11 |

Note 1. $t_{Pcyc}$: PCLK cycle

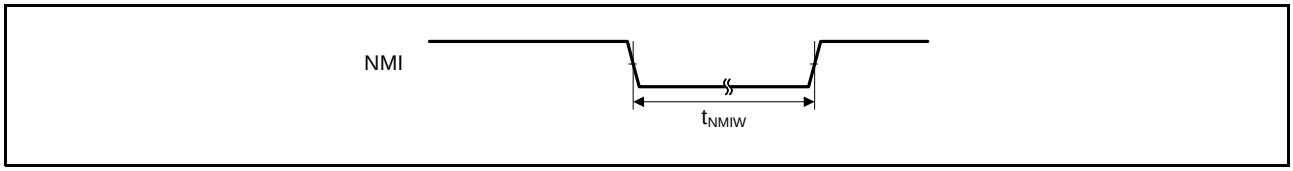



**Figure 6.10 NMI Interrupt Input Timing**

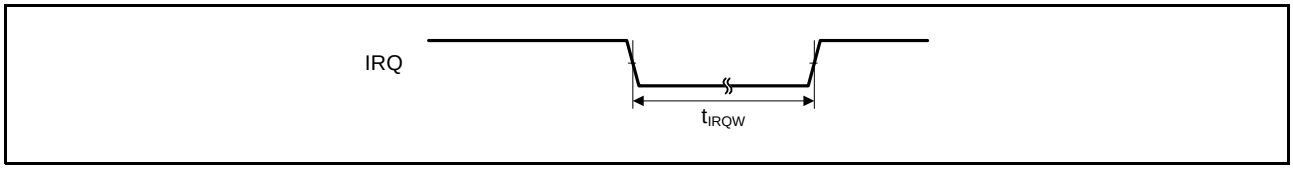



**Figure 6.11 IRQ Interrupt Input Timing**

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 2.10 | Sep 26, 2013 | 36 to 39 | Table 1.7 List of Pins and Pin Functions (112-Pin LQFP), changed |
| | | 40 to 42 | Table 1.8 List of Pins and Pin Functions (100-Pin LQFP), changed |
| | | 43 to 45 | Table 1.9 List of Pins and Pin Functions (64-Pin LQFP), changed |
| | | 46 to 47 | Table 1.10 List of Pins and Pin Functions (48-Pin LQFP), changed |
| | | 4. I/O Registers | |
| | | 56 to 103 | Table 4.1 List of I/O Registers (Address Order), changed |
| | | 5. Electrical Characteristics [144-, 120-, 112- and 100-Pin Versions] | |
| | | 104 | Table 5.1 Absolute Maximum Ratings, changed |
| | | 107 | Table 5.4 DC Characteristics (3), Note 7, deleted |
| | | 108 | Table 5.6 Permissible Power Consumption, added |
| | | 128 | 5.3.7 Timing of PWM Delay Generation Circuit, added |
| | | 128 | Table 42.21 Timing of the PWM Delay Generation Circuit, added |
| | | 132 | Figure 5.32 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKB Division Ratio Set to a Value Other Than 1/2) and Simple SPI Timing (Master, CKPH = 1), changed |
| | | 133 | Figure 5.34 RSPI Timing (Slave, CPHA = 0) and Simple SPI Timing (Slave, CKPH = 0), changed |
| | | 134 | Figure 5.35 RSPI Timing (Slave, CPHA = 1) and Simple SPI Timing (Slave, CKPH = 1), changed |
| | | 6. Electrical Characteristics [64- and 48-Pin Versions] | |
| | | 149 | Table 6.1 Absolute Maximum Ratings, changed |
| | | 151 | Table 6.3 DC Characteristics (2), Note 3, changed |
| | | 152 | Table 6.5 Permissible Power Consumption, added |