Renesas Electronics America Inc - R5F563TBBDFH#V1 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	69
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 12x10b, 8x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f563tbbdfh-v1

1. Overview

1.1 Outline of Specifications

Table 1.1 lists the specifications in outline, and Table 1.2 lists the functions of products.
Table 1.1 shows an outline of the maximum specifications, and the available peripheral modules and number of channels differ according to the number of pins on the package and the ROM capacity. For details, see Table 1.2, Comparison of Functions for Different Packages.

Table 1.1 Outline of Specifications (1/7)

Classification	Module/Function	Description
CPU	CPU	• Maximum operating frequency: 100 MHz • 32-bit RX CPU • Minimum instruction execution time: One instruction per state (cycle of the system clock) • Address space: 4-Gbyte linear • Register set of the CPU General purpose: Sixteen 32-bit registers Control: Nine 32-bit registers Accumulator: One 64-bit register • Basic instructions: 73 • Floating-point operation instructions: 8 • DSP instructions: 9 • Addressing modes: 10 • Data arrangement Instructions: Little endian Data: Selectable as little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits • Memory protection unit (MPU)
	FPU	• Single precision floating point (32 bits) • Data types and floating-point exceptions in conformance with the IEEE754 standard
Memory	ROM	• Capacity: 512 Kbytes, 384 Kbytes, 256 Kbytes, 64 Kbytes, 48 Kbytes, 32 Kbytes • 100 MHz, no-wait access • On-board programming: Programs can be modified through SCI or USB while the MCU is mounted on the board. • Off-board programming: Programs can be modified using parallel programmer. (only in 144-, 120-, 112- and 100-pin versions)
	RAM	• Capacity: 48 Kbytes, 32 Kbytes, 24 Kbytes, 8 Kbytes • 100 MHz, no-wait access
	E^2 data flash	• Capacity: 32 Kbytes, 8 Kbytes • Programming/erasing: 100,000 times • On-board programming: Programs can be modified through SCI or USB while the MCU is mounted on the board. Programming from the user program is possible.
MCU operating modes		[144-, 120-, 112- and 100-pin versions] Single-chip mode, on-chip ROM enabled extended mode, on-chip ROM disabled extended mode (switchable by software) [64- and 48-pin versions] Single-chip mode

Table 1.1 Outline of Specifications (3/7)

Classification	Module/Function	Description
I/O ports	General I/O ports	• 144-pin LQFP I/O pins: 81 Input pins: 29 Open-drain outputs: 27 • 120-pin LQFP I/O pins: 72 Input pin: 21 Open-drain outputs: 26 • 112-pin LQFP I/O pins: 69 Input pins: 21 Open-drain outputs: 20 • 100-pin LQFP I/O pins: 57 Input pins: 21 Open-drain outputs: 16 • 64-pin LQFP I/O pins: 39 Input pins: 9 Open-drain outputs: 10 5-V tolerance: 39 • 48-pin LQFP I/O pins: 25 Input pins: 7 Open-drain outputs: 8 5-V tolerance: 25
Timers	Multi-function timer pulse unit 3 (MTU3)	• (16 bits × 8 channels) • Maximum of 16 pulse-input/output and 3 pulse-input possible • Select eight clocks from among ten count clocks (PCLKA/1, PCLKA/4, PCLKA/16, PCLKA/64, PCLKA/256, PCLKA/1024, MTCLKA, MTCLKB, MTCLKC, and MTCLKD) for each channel (seven clocks for channel 1, four clocks for channel 5, and six clocks for channel 6 or 7) • 24 output compare/input capture registers • Counter-clearing operation (simultaneous clearing on compare match or input capture) • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous input and output to registers in synchronization with counter operations • Buffer operation specifiable • Capable of cascade-connected operation • Interrupts: 38 sources • Automatic transfer of register data • Pulse output modes Topple, PWM, complementary PWM, and reset-synchronous PWM modes • Complementary PWM output mode Outputs non-overlapping waveforms for controlling 3-phase inverters Automatic specification of dead times PWM duty cycle: Selectable as any value from 0% to 100% Delay can be applied to requests for A/D conversion. Non-generation of interrupt requests at peak or trough values of counters can be selected. Double buffering • Reset-synchronous PWM mode Three PWM waveforms and corresponding inverse waveforms are output with the desired duty cycles. • Phase-counting mode • Counter functionality for dead-time compensation • Generation of triggers for A/D converters • Differential timing for initiation of A/D conversion
	Port output enable 3 (POE3)	• Control of the high-impedance state of the MTU3 and GPT's waveform output pins • Six pins for input from signal sources: POE0, POE4, POE8, POE10, POE11, and POE12 • Initiation on detection of short-circuited outputs (detection of PWM outputs having simultaneously become an active level.) • Initiation by comparator-detection, oscillation-stoppage detection, or software • Software control of the states of pins for output control can also be added.

Table 1.1 Outline of Specifications (5/7)

Classification	Module/Function	Description
Communication function	I^2C bus interfaces (RIIC)	• 2 channels Communication formats I^2C bus format/SMBus format Supports the multi-master Max. transfer rate: 400 kbps
	CAN module (CAN)	• 1 channels • Compliance with the ISO11898-1 specification (standard frame and extended frame) • 32 mailboxes per channel
	Serial peripheral interfaces (RSPI)	• 2 channels • RSPI transfer facility Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPCK (RSPI clock) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) Capable of handling serial transfer as a master or slave • Data formats Switching between MSB first and LSB first The number of bits in each transfer can be changed to any number of bits from 8 to 16, or to 20, 24, or 32 bits. 128-bit buffers for transmission and reception Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) • Buffered structure Double buffers for both transmission and reception • Max. transfer rate In master mode: [144-, 120-, 112- and 100-pin versions] 25 Mbps [64- and 48-pin versions] 12.5 Mbps In slave mode: 6.25 Mbps
12-bit A/D converter (S12ADB) [144-, 120-, 112- and 100-pin versions]		• 12 bits (4 channels x 2 unit) • 12-bit resolution • Conversion time 1.0 μs per channel (clock for S12ADB, PCLKD (A/D conversion clock ADCLK) = 50 MHz, AVCC0 = 4.0 to 5.5 V) 2.0 μs per channel (clock for S12ADB, PCLKD (A/D conversion clock ADCLK) = 25 MHz, AVCC0 = 3.0 to 3.6 V) • Operating modes Scan mode (single-cycle scan mode/continuous scan mode/group scan mode) Group A priority control (only for the group scan mode) • Sample-and-hold function A common sample-and-hold circuit for units is included. Additionally, sample-and-hold circuit for each unit is included. (three channels per unit) • Self-diagnostic function The self-diagnostic function internally generates three analog input voltages (VREFL0, VREFH0 x 1/2, VREFH0). • Double trigger mode (duplication of A/D converted data) • Input signal amplification function using programmable gain amplifier (three channels per unit) Amplification factors: 2.0 times, 2.5 times, 3.077 times, 3.636 times, 4.0 times, 4.444 times, 5.0 times, 5.714 times, 6.667 times, 10.0 times, 13.333 times (total of 11 steps) • Three ways to start A/D conversion Conversion can be started by software, a conversion start trigger from a timer (MTU3 or GPT), or an external trigger signal. • Window comparators (three channels per unit)

1.2 List of Products

Table 1.3 is a list of products, and Figure 1.1 shows how to read the product part number.

Table 1.3 List of Products (1/4)

Group	Part No.	Order Part No.	Package	On-chip ROM Capacity	On-chip RAM Capacity	Option	Operating Voltage	Operating Temperature
RX63T	R5F563TEADFB	R5F563TEADFB#V0	PLQP0144KA-A	512 Kbytes	48 Kbytes	CAN module included	VCC/ PLLVCC 4.0 to 5.5V VCC_USB 3.0 to 3.6V AVCC/ AVCC0 4.0 to 5.5V	-40 to +85°C (D Version)
	R5F563TEADFB	R5F563TEADFB#V1	PLQP0144KA-A	512 Kbytes	48 Kbytes	CAN module included		
	R5F563TEADFA	R5F563TEADFA#V0	PLQP0120KA-A	512 Kbytes	48 Kbytes	CAN module included		
	R5F563TEADFA	R5F563TEADFA#V1	PLQP0120KA-A	512 Kbytes	48 Kbytes	CAN module included		
	R5F563TEADFH	R5F563TEADFH#V0	PLQP0112JA-A	512 Kbytes	48 Kbytes	CAN module included		
	R5F563TEADFH	R5F563TEADFH#V1	PLQP0112JA-A	512 Kbytes	48 Kbytes	CAN module included		
	R5F563TEADFP	R5F563TEADFP#V0	PLQP0100KB-A	512 Kbytes	48 Kbytes	CAN module included		
	R5F563TEADFP	R5F563TEADFP#V1	PLQP0100KB-A	512 Kbytes	48 Kbytes	CAN module included		
	R5F563TCADFB	R5F563TCADFB#V0	PLQP0144KA-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TCADFB	R5F563TCADFB#V1	PLQP0144KA-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TCADFA	R5F563TCADFA#V0	PLQP0120KA-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TCADFA	R5F563TCADFA#V1	PLQP0120KA-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TCADFH	R5F563TCADFH#V0	PLQP0112JA-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TCADFH	R5F563TCADFH#V1	PLQP0112JA-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TCADFP	R5F563TCADFP#V0	PLQP0100KB-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TCADFP	R5F563TCADFP#V1	PLQP0100KB-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TBADFB	R5F563TBADFB#V0	PLQP0144KA-A	256 Kbytes	24 Kbytes	CAN module included		
	R5F563TBADFB	R5F563TBADFB#V1	PLQP0144KA-A	256 Kbytes	24 Kbytes	CAN module included		
	R5F563TBADFA	R5F563TBADFA#V0	PLQP0120KA-A	256 Kbytes	24 Kbytes	CAN module included		
	R5F563TBADFA	R5F563TBADFA#V1	PLQP0120KA-A	256 Kbytes	24 Kbytes	CAN module included		
	R5F563TBADFH	R5F563TBADFH#V0	PLQP0112JA-A	256 Kbytes	24 Kbytes	CAN module included		
	R5F563TBADFH	R5F563TBADFH#V1	PLQP0112JA-A	256 Kbytes	24 Kbytes	CAN module included		
	R5F563TBADFP	R5F563TBADFP#V0	PLQP0100KB-A	256 Kbytes	24 Kbytes	CAN module included		
	R5F563TBADFP	R5F563TBADFP#V1	PLQP0100KB-A	256 Kbytes	24 Kbytes	CAN module included		
	R5F563TEDDFB	R5F563TEDDFB#V0	PLQP0144KA-A	512 Kbytes	48 Kbytes	CAN module not included		
	R5F563TEDDFA	R5F563TEDDFA#V0	PLQP0120KA-A	512 Kbytes	48 Kbytes	CAN module not included		
	R5F563TEDDFH	R5F563TEDDFH#V0	PLQP0112JA-A	512 Kbytes	48 Kbytes	CAN module not included		
	R5F563TEDDFP	R5F563TEDDFP#V0	PLQP0100KB-A	512 Kbytes	48 Kbytes	CAN module not included		

Table 1.5 List of Pins and Pin Functions (144-Pin LQFP) (2/4)

Pin Number 144-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3, GPT, POE3, CAC)	Communications (SCIc, SCId, RSPI, RIIC, CAN, USB)	Interrupt	S12ADB, AD, DA
39		PB6	A18		RXD12/SMISO12/ SSCL12/RXDX12/ CRX1	IRQ2	
40		PB5	A17		TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/ CTX1		
41	PLLVCC						
42		PB4	A16	POE8#/ GTETRG0		IRQ3-DS	
43	PLLVSS						
44	TDI				RXD1*1		
45	TCK/FINEC						
46	TDO				TXD1*1		
47		PB3	A15	MTIOC0A/CACREF	SCK0		
48		PB2		MTIOC0B	TXD0/SMOSI0/ SSDA0/SDA0		
49		PB1		MTIOC0C	RXD0/SMISO0/ SSCL0/SCL0	IRQ4	
50		PB0	A14	MTIOC0D	MOSIA/MOSIB		
51	TRDATA1	PA6	CS3#		CTS3#/RTS3#/SS3#		
52		PA5		MTIOC1A	RXD0/SMISO0/ SSCL0/ MISOA/MISOB		ADTRG1#
53		PA4		MTIOC1B	TXD0/SMOSI0/ SSDA0/SMOSI0/ RSPCKA/RSPCKB		ADTRG0#
54		PA3		MTIOC2A	SCK0/SSLA0/SSLB0		
55		PA2		MTIOC2B	RXD2/SMISO2/ SSCL2/ SSLA1/SSLB1		
56		PA1		MTIOC6A	TXD2/SMOSI2/ SSDA2/SMOSI2/ SSLA2/SSLB2		
57		PA0		MTIOC6C	SCK2/SSLA3/SSLB3		
58	TRDATA0	P35			TXD3/SMOSI3/SSDA3		
59	TRCLK	P34		GTETRG1	RXD3/SMISO3/SSCL3	IRQ3	
60	VCC						
61		P96	A13	POE4#	RXD1/SMISO1/SSCL1	IRQ4-DS	
62		PG6	CS2#		SCK1		
63	VSS						
64		P95		MTIOC6B/GTIOC4A	TXD1/SMOSI1/SSDA1		
65		P94		MTIOC7A/GTIOC5A	CTS1#/RTS1#/SS1#		
66		P93		MTIOC7B/GTIOC6A	CTS2#/RTS2#/SS2#		
67		P92		MTIOC6D/GTIOC4B			
68		P91		MTIOC7C/GTIOC5B			
69		P90		MTIOC7D/GTIOC6B			
70		PG5		POE12#	SCK3		ADTRG#
71		PG4		GTIOC6B	RXD3/SMISO3/SSCL3	IRQ6	

Table 4.1 List of I/O Registers (Address Order) (2/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 201Fh	DMAC0	DMA Activation Source Flag Control Register	DMCSL	8	8	2 ICLK		DMACA	
0008 2040h	DMAC1	DMA Source Address Register	DMSAR	32	32	2 ICLK			
0008 2044h	DMAC1	DMA Destination Address Register	DMDAR	32	32	2 ICLK			
0008 2048h	DMAC1	DMA Transfer Count Register	DMCRA	32	32	2 ICLK			
0008 204Ch	DMAC1	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK			
0008 2050h	DMAC1	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK			
0008 2053h	DMAC1	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK			
0008 2054h	DMAC1	DMA Address Mode Register	DMAMD	16	16	2 ICLK			
0008 205Ch	DMAC1	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK			
0008 205Dh	DMAC1	DMA Software Start Register	DMREQ	8	8	2 ICLK			
0008 205Eh	DMAC1	DMA Status Register	DMSTS	8	8	2 ICLK			
0008 205Fh	DMAC1	DMA Activation Source Flag Control Register	DMCSL	8	8	2 ICLK			
0008 2080h	DMAC2	DMA Source Address Register	DMSAR	32	32	2 ICLK			
0008 2084h	DMAC2	DMA Destination Address Register	DMDAR	32	32	2 ICLK			
0008 2088h	DMAC2	DMA Transfer Count Register	DMCRA	32	32	2 ICLK			
0008 208Ch	DMAC2	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK			
0008 2090h	DMAC2	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK			
0008 2093h	DMAC2	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK			
0008 2094h	DMAC2	DMA Address Mode Register	DMAMD	16	16	2 ICLK			
0008 209Ch	DMAC2	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK			
0008 209Dh	DMAC2	DMA Software Start Register	DMREQ	8	8	2 ICLK			
0008 209Eh	DMAC2	DMA Status Register	DMSTS	8	8	2 ICLK			
0008 209Fh	DMAC2	DMA Activation Source Flag Control Register	DMCSL	8	8	2 ICLK			
0008 20C0h	DMAC3	DMA Source Address Register	DMSAR	32	32	2 ICLK			
0008 20C4h	DMAC3	DMA Destination Address Register	DMDAR	32	32	2 ICLK			
0008 20C8h	DMAC3	DMA Transfer Count Register	DMCRA	32	32	2 ICLK			
0008 20CCh	DMAC3	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK			
0008 20D0h	DMAC3	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK			
0008 20D3h	DMAC3	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK			
0008 20D4h	DMAC3	DMA Address Mode Register	DMAMD	16	16	2 ICLK			
0008 20DCh	DMAC3	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK			
0008 20DDh	DMAC3	DMA Software Start Register	DMREQ	8	8	2 ICLK			
0008 20DEh	DMAC3	DMA Status Register	DMSTS	8	8	2 ICLK			
0008 20DFh	DMAC3	DMA Activation Source Flag Control Register	DMCSL	8	8	2 ICLK			
0008 2200h	DMAC	DMACA Module Activation Register	DMAST	8	8	2 ICLK			
0008 2400h	DTC	DTC Control Register	DTCCR	8	8	2ICLK		DTCa	
0008 2404h	DTC	DTC Vector Base Register	DTCVBR	32	32	2ICLK			
0008 2408h	DTC	DTC Address Mode Register	DTCADMOD	8	8	2ICLK			
0008 240Ch	DTC	DTC Module Start Register	DTCST	8	8	2ICLK			
0008 240Eh	DTC	DTC Status Register	DTCSTS	16	16	2ICLK			
0008 3002h	BSC	CS0 Mode Register	CS0MOD	16	16	1, 2 BCLK		Buses	Not present in versions with 64 or 48 pins.
0008 3004h	BSC	CS0 Wait Control Register 1	CS0WCR1	32	32	1, 2 BCLK			Not present in versions with 64 or 48 pins.
0008 3008h	BSC	CS0 Wait Control Register 2	CS0WCR2	32	32	1, 2 BCLK			Not present in versions with 64 or 48 pins.
0008 3012h	BSC	CS1 Mode Register	CS1MOD	16	16	1, 2 BCLK			Not present in versions with 64 or 48 pins.
0008 3014h	BSC	CS1 Wait Control Register 1	CS1WCR1	32	32	1, 2 BCLK			Not present in versions with 64 or 48 pins.
0008 3018h	BSC	CS1 Wait Control Register 2	CS1WCR2	32	32	1, 2 BCLK			Not present in versions with 64 or 48 pins.
0008 3022h	BSC	CS2 Mode Register	CS2MOD	16	16	1, 2 BCLK			Not present in versions with 64 or 48 pins.

Table 4.1 List of I/O Registers (Address Order) (17/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 83B2h	RSPI1	RSPI Command Register 1	SPCMD1	16	16	2, 3 PCLKB	2 ICLK	RSPI	Not present in versions with 64 or 48 pins.
0008 83B4h	RSPI1	RSPI Command Register 2	SPCMD2	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 83B6h	RSPI1	RSPI Command Register 3	SPCMD3	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 83B8h	RSPI1	RSPI Command Register 4	SPCMD4	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 83BAh	RSPI1	RSPI Command Register 5	SPCMD5	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 83BCh	RSPI1	RSPI Command Register 6	SPCMD6	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 83BEh	RSPI1	RSPI Command Register 7	SPCMD7	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9000h	S12AD	A/D Control Register	ADCSR	16	16	2, 3 PCLKB	2 ICLK	S12ADB	
0008 9004h	S12AD	A/D Channel Select Register A	ADANSA	16	16	2, 3 PCLKB	2 ICLK		
0008 9008h	S12AD	A/D-Converted Value Addition Mode Select Register	ADADS	16	16	2, 3 PCLKB	2 ICLK		
0008 900Ch	S12AD	A/D-Converted Value Addition Count Select Register	ADADC	8	8	2, 3 PCLKB	2 ICLK		
0008 900Eh	S12AD	A/D Control Extended Register	ADCER	16	16	2, 3 PCLKB	2 ICLK		
0008 9010h	S12AD	A/D Start Trigger Select Register	ADSTRGR	16	16	2, 3 PCLKB	2 ICLK		
0008 9014h	S12AD	A/D Channel Select Register B	ADANSB	16	16	2, 3 PCLKB	2 ICLK		
0008 9018h	S12AD	A/D Data-Doubling Register	ADDBLDR	16	16	2, 3 PCLKB	2 ICLK		
0008 901Eh	S12AD	A/D Self-Diagnosis Data Register	ADRD	16	16	2, 3 PCLKB	2 ICLK		
0008 9020h	S12AD	A/D Data Register 0	ADDR0	16	16	2, 3 PCLKB	2 ICLK		
0008 9022h	S12AD	A/D Data Register 1	ADDR1	16	16	2, 3 PCLKB	2 ICLK		
0008 9024h	S12AD	A/D Data Register 2	ADDR2	16	16	2, 3 PCLKB	2 ICLK		
0008 9026h	S12AD	A/D Data Register 3	ADDR3	16	16	2, 3 PCLKB	2 ICLK		
0008 9028h	S12AD	A/D Data Register 4	ADDR4	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 144, 120, 112, or 100 pins.
0008 902Ah	S12AD	A/D Data Register 5	ADDR5	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 144, 120, 112, or 100 pins.
0008 902Ch	S12AD	A/D Data Register 6	ADDR6	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 144, 120, 112, or 100 pins.
0008 902Eh	S12AD	A/D Data Register 7	ADDR7	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 144, 120, 112, or 100 pins.
0008 9060h	S12AD	A/D Sampling State Register 0	ADSSTR0	8	8	2, 3 PCLKB	2 ICLK		
0008 9066h	S12AD	A/D Sample and Hold Circuit Control Register	ADSHCR	16	16	2, 3 PCLKB	2 ICLK		
0008 9073h	S12AD	A/D Sampling State Register 1	ADSSTR1	8	8	2, 3 PCLKB	2 ICLK		
0008 9074h	S12AD	A/D Sampling State Register 2	ADSSTR2	8	8	2, 3 PCLKB	2 ICLK		
0008 9075h	S12AD	A/D Sampling State Register 3	ADSSTR3	8	8	2, 3 PCLKB	2 ICLK		
0008 9076h	S12AD	A/D Sampling State Register 4	ADSSTR4	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 144, 120, 112, or 100 pins.
0008 9077h	S12AD	A/D Sampling State Register 5	ADSSTR5	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 144, 120, 112, or 100 pins.
0008 9078h	S12AD	A/D Sampling State Register 6	ADSSTR6	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 144, 120, 112, or 100 pins.
0008 9079h	S12AD	A/D Sampling State Register 7	ADSSTR7	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 144, 120, 112, or 100 pins.
0008 9080h	S12AD	A/D Group Scan Priority Control Register	ADGSPCR	16	16	2, 3 PCLKB	2 ICLK		
0008 9084h	S12AD	A/D Data-Doubling Register A	ADDBLDRA	16	16	2, 3 PCLKB	2 ICLK		
0008 9086h	S12AD	A/D Data-Doubling Register B	ADDBLDRB	16	16	2, 3 PCLKB	2 ICLK		
0008 908Ah	S12AD	A/D Programmable Gain Amplifier Register	ADPG	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.

Table 4.1 List of I/O Registers (Address Order) (31/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
000A 004Ch	USB0	Frame Number Register	FRMNUM	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1	USBa	Not present in versions with 112, 100, 64, or 48 pins.
000A 004Eh	USB0	Device State Change Register	DVCHGR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 0050h	USB0	USB Address Register	USBADDR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 0054h	USB0	USB Request Type Register	USBREQ	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 0056h	USB0	USB Request Value Register	USBVAL	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 0058h	USB0	USB Request Index Register	USBINDX	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 005Ah	USB0	USB Request Length Register	USBLENG	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 005Ch	USB0	DCP Configuration Register	DCPCFG	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 005Eh	USB0	DCP Maximum Packet Size Register	DCPMAXP	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 0060h	USB0	DCP Control Register	DCPCTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 0064h	USB0	Pipe Window Select Register	PIPESEL	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 0068h	USB0	Pipe Configuration Register	PIPECFG	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.

Table 4.1 List of I/O Registers (Address Order) (35/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
000C 1308h	MTU0	Timer General Register A	TGRA	16	16, 32	4, 5 PCLKA	2, 3 ICLK	MTU3	
000C 130Ah	MTU0	Timer General Register B	TGRB	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 130Ch	MTU0	Timer General Register C	TGRC	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 130Eh	MTU0	Timer General Register D	TGRD	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1320h	MTU0	Timer General Register E	TGRE	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1322h	MTU0	Timer General Register F	TGRF	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1324h	MTU0	Timer Interrupt Enable Register 2	TIER2	8	8, 16	4, 5 PCLKA	2, 3 ICLK		
000C 1325h	MTU0	Timer Status Register 2	TSR2	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1326h	MTU0	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1380h	MTU1	Timer Control Register	TCR	8	8, 16	4, 5 PCLKA	2, 3 ICLK		
000C 1381h	MTU1	Timer Mode Register 1	TMDR1	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1382h	MTU1	Timer I/O Control Register	TIOR	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1384h	MTU1	Timer Interrupt Enable Register	TIER	8	8, 16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1385h	MTU1	Timer Status Register	TSR	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1386h	MTU1	Timer Counter	TCNT	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1388h	MTU1	Timer General Register A	TGRA	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 138Ah	MTU1	Timer General Register B	TGRB	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1390h	MTU1	Timer Input Capture Control Register	TICCR	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1400h	MTU2	Timer Control Register	TCR	8	8, 16	4, 5 PCLKA	2, 3 ICLK		
000C 1401h	MTU2	Timer Mode Register 1	TMDR1	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1402h	MTU2	Timer I/O Control Register	TIOR	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1404h	MTU2	Timer Interrupt Enable Register	TIER	8	8, 16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1405h	MTU2	Timer Status Register	TSR	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1406h	MTU2	Timer Counter	TCNT	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1408h	MTU2	Timer General Register A	TGRA	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 140Ah	MTU2	Timer General Register B	TGRB	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1A00h	MTU6	Timer Control Register	TCR	8	8, 16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1A01h	MTU7	Timer Control Register	TCR	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1A02h	MTU6	Timer Mode Register 1	TMDR1	8	8, 16	4, 5 PCLKA	2, 3 ICLK		
000C 1A03h	MTU7	Timer Mode Register 1	TMDR1	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1A04h	MTU6	Timer I/O Control Register H	TIORH	8	8, 16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1A05h	MTU6	Timer I/O Control Register L	TIORL	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1A06h	MTU7	Timer I/O Control Register H	TIORH	8	8, 16	4, 5 PCLKA	2, 3 ICLK		
000C 1A07h	MTU7	Timer I/O Control Register L	TIORL	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1A08h	MTU6	Timer Interrupt Enable Register	TIER	8	8, 16	4, 5 PCLKA	2, 3 ICLK		
000C 1A09h	MTU7	Timer Interrupt Enable Register	TIER	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1A0Ah	MTU	Timer Output Master Enable Register B	TOERB	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1A0Eh	MTU	Timer Output Control Register 1B	TOCR1B	8	8, 16	4, 5 PCLKA	2, 3 ICLK		
000C 1A0Fh	MTU	Timer Output Control Register 2B	TOCR2B	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1A10h	MTU6	Timer Counter	TCNT	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1A12h	MTU7	Timer Counter	TCNT	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1A14h	MTU	Timer Cycle Data Register B	TCDRB	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1A16h	MTU	Timer Dead Time Data Register B	TDDRB	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1A18h	MTU6	Timer General Register A	TGRA	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1A1Ah	MTU6	Timer General Register B	TGRB	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1A1Ch	MTU7	Timer General Register A	TGRA	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1A1Eh	MTU7	Timer General Register B	TGRB	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1A20h	MTU	Timer Subcounter B	TCNTSB	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1A22h	MTU	Timer Cycle Buffer Register B	TCBRB	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1A24h	MTU6	Timer General Register C	TGRC	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1A26h	MTU6	Timer General Register D	TGRD	16	16	4, 5 PCLKA	2, 3 ICLK		

Table 4.1 List of I/O Registers (Address Order) (40/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
000C 2230h	GPT2	A/D Converter Start Request Timing Double-Buffer Register B	GTADTDBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK	GPT	
000C 2234h	GPT2	General PWM Timer Output Negate Control Register	GTONCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2236h	GPT2	General PWM Timer Dead Time Control Register	GTDTCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2238h	GPT2	General PWM Timer Dead Time Value Register U	GTDVU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 223Ah	GPT2	General PWM Timer Dead Time Value Register D	GTDVD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 223Ch	GPT2	General PWM Timer Dead Time Buffer Register U	GTDBU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 223Eh	GPT2	General PWM Timer Dead Time Buffer Register D	GTDBD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2240h	GPT2	General PWM Timer Output Protection Function Status Register	GTSOS	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2242h	GPT2	General PWM Timer Output Protection Function Temporary Release Register	GTSOTR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2280h	GPT3	General PWM Timer I/O Control Register	GTIOR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2282h	GPT3	General PWM Timer Interrupt Output Setting Register	GTINTAD	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2284h	GPT3	General PWM Timer Control Register	GTCR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2286h	GPT3	General PWM Timer Buffer Enable Register	GTBER	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2288h	GPT3	General PWM Timer Count Direction Register	GTUDC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 228Ah	GPT3	General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register	GTITC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 228Ch	GPT3	General PWM Timer Status Register	GTST	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 228Eh	GPT3	General PWM Timer Counter	GTCNT	16	16	2 to 5 PCLKA	2, 3 ICLK		
000C 2290h	GPT3	General PWM Timer Compare Capture Register A	GTCCRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2292h	GPT3	General PWM Timer Compare Capture Register B	GTCCRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2294h	GPT3	General PWM Timer Compare Capture Register C	GTCCRC	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2296h	GPT3	General PWM Timer Compare Capture Register D	GTCCRD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2298h	GPT3	General PWM Timer Compare Capture Register E	GTCCRE	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 229Ah	GPT3	General PWM Timer Compare Capture Register F	GTCCRF	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 229Ch	GPT3	General PWM Timer Cycle Setting Register	GTPR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 229Eh	GPT3	General PWM Timer Cycle Setting Buffer Register	GTPBR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 22A0h	GPT3	General PWM Timer Cycle Setting Double-Buffer Register	GTPDBR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 22A4h	GPT3	A/D Converter Start Request Timing Register A	GTADTRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 22A6h	GPT3	A/D Converter Start Request Timing Buffer Register A	GTADTBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 22A8h	GPT3	A/D Converter Start Request Timing Double-Buffer Register A	GTADTDBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 22ACh	GPT3	A/D Converter Start Request Timing Register B	GTADTRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 22AEh	GPT3	A/D Converter Start Request Timing Buffer Register B	GTADTBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 22B0h	GPT3	A/D Converter Start Request Timing Double-Buffer Register B	GTADTDBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 22B4h	GPT3	General PWM Timer Output Negate Control Register	GTONCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 22B6h	GPT3	General PWM Timer Dead Time Control Register	GTDTCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 22B8h	GPT3	General PWM Timer Dead Time Value Register U	GTDVU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		

Table 4.1 List of I/O Registers (Address Order) (46/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
000C 2AA8h	GPT7	A/D Converter Start Request Timing Double-Buffer Register A	GTADTDBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK	GPT	Not present in versions with 64 or 48 pins.
000C 2AACh	GPT7	A/D Converter Start Request Timing Register B	GTADTRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2AAEh	GPT7	A/D Converter Start Request Timing Buffer Register B	GTADTBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2AB0h	GPT7	A/D Converter Start Request Timing Double-Buffer Register B	GTADTDBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2AB4h	GPT7	General PWM Timer Output Negate Control Register	GTONCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2AB6h	GPT7	General PWM Timer Dead Time Control Register	GTDTCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2AB8h	GPT7	General PWM Timer Dead Time Value Register U	GTDVU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2ABAh	GPT7	General PWM Timer Dead Time Value Register D	GTDVD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2ABCh	GPT7	General PWM Timer Dead Time Buffer Register U	GTDBU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2ABEh	GPT7	General PWM Timer Dead Time Buffer Register D	GTDBD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2AC0h	GPT7	General PWM Timer Output Protection Function Status Register	GTSOS	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2AC2h	GPT7	General PWM Timer Output Protection Function Temporary Release Register	GTSOTR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3002h	DPC	Software Start Setting Register 0	SOFTSTART 0	16	16	3 to 5 PCLKA	2, 3 ICLK	DPC	Not present in versions with 64 or 48 pins.
000C3006h	DPC	Software Start Setting Register 1	SOFTSTART 1	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C300Ah	DPC	Software Start Setting Register 2	SOFTSTART 2	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C300Eh	DPC	Software Start Setting Register 3	SOFTSTART 3	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3012h	DPC	Reference Value Setting Register 0	VOTARGET 0	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3016h	DPC	Reference Value Setting Register 1	VOTARGET 1	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C301Ah	DPC	Reference Value Setting Register 2	VOTARGET 2	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C301Eh	DPC	Reference Value Setting Register 3	VOTARGET 3	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3022h	DPC	Reference Value Select Register	REFSEL	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3026h	DPC	PWM Channel Setting Register	CHLSEL	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C302Ah	DPC	Control Enable Setting Register	ENABLE	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C302Eh	DPC	Control Calculation Parameter Setting Register KP0	PARAMKP0	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3032h	DPC	Control Calculation Parameter Setting Register KI0	PARAMKI0	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3036h	DPC	Control Calculation Parameter Setting Register KQ0	PARAMKQ0	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C303Ah	DPC	Control Calculation Parameter Setting Register KF0	PARAMKF0	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C303Eh	DPC	Control Calculation Parameter Setting Register KP1	PARAMKP1	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3042h	DPC	Control Calculation Parameter Setting Register KI1	PARAMKI1	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3046h	DPC	Control Calculation Parameter Setting Register KQ1	PARAMKQ1	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C304Ah	DPC	Control Calculation Parameter Setting Register KF1	PARAMKF1	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C304Eh	DPC	Control Calculation Parameter Setting Register KP2	PARAMKP2	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3052h	DPC	Control Calculation Parameter Setting Register KI2	PARAMKI2	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.

Table 4.1 List of I/O Registers (Address Order) (47/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
000C3056h	DPC	Control Calculation Parameter Setting Register KQ2	PARAMKQ2	16	16	3 to 5 PCLKA	2, 3 ICLK	DPC	Not present in versions with 64 or 48 pins.
000C305Ah	DPC	Control Calculation Parameter Setting Register KF2	PARAMKF2	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C305Eh	DPC	Control Calculation Parameter Setting Register KP3	PARAMKP3	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3062h	DPC	Control Calculation Parameter Setting Register KI3	PARAMKI3	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3066h	DPC	Control Calculation Parameter Setting Register KQ3	PARAMKQ3	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C306Ah	DPC	Control Calculation Parameter Setting Register KF3	PARAMKF3	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C306Ch	DPC	Control Calculation Result Higher-Order Bits Store Register 0	RESULTU0	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C306Eh	DPC	Control Calculation Result Lower-Order Bits Store Register 0	RESULTL0	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3070h	DPC	Control Calculation Result Higher-Order Bits Store Register 1	RESULTU1	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3072h	DPC	Control Calculation Result Lower-Order Bits Store Register 1	RESULTL1	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3074h	DPC	Control Calculation Result Higher-Order Bits Store Register 2	RESULTU2	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3076h	DPC	Control Calculation Result Lower-Order Bits Store Register 2	RESULTL2	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3078h	DPC	Control Calculation Result Higher-Order Bits Store Register 3	RESULTU3	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C307Ah	DPC	Control Calculation Result Lower-Order Bits Store Register 3	RESULTL3	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C307Eh	DPC	Input Code Monitor Enable Register	TMONEN	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3082h	DPC	Maximum Input Code Monitor Register 0	TMONMAX0	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3086h	DPC	Minimum Input Code Monitor Register 0	TMONMIN0	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C308Ah	DPC	Maximum Input Code Monitor Register 1	TMONMAX1	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C308Eh	DPC	Minimum Input Code Monitor Register 1	TMONMIN1	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3092h	DPC	Maximum Input Code Monitor Register 2	TMONMAX2	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3096h	DPC	Minimum Input Code Monitor Register 2	TMONMIN2	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C309Ah	DPC	Maximum Input Code Monitor Register 3	TMONMAX3	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C309Eh	DPC	Minimum Input Code Monitor Register 3	TMONMIN3	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C30A2h	DPC	Overvoltage Output Error Judgment Threshold Setting Register 0	ERRVTH0	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C30A6h	DPC	Overvoltage Output Error Judgment Threshold Setting Register 1	ERRVTH1	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C30AAh	DPC	Overvoltage Output Error Judgment Threshold Setting Register 2	ERRVTH2	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C30AEh	DPC	Overvoltage Output Error Judgment Threshold Setting Register 3	ERRVTH3	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C30B2h	DPC	PWM Shut-Down at Overvoltage Output Error Setting Register	ERRDWN	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
007F C402h	FLASH	Flash Mode Register	FMODR	8	8	2, 3 FCLK	2, 3 ICLK	ROM/ E2 DataFlash Memory	
007F C410h	FLASH	Flash Access Status Register	FASTAT	8	8	2, 3 FCLK	2, 3 ICLK		
007F C411h	FLASH	Flash Access Error Interrupt Enable Register	FAEINT	8	8	2, 3 FCLK	2, 3 ICLK		
007F C412h	FLASH	Flash Ready Interrupt Enable Register	FRDYIE	8	8	2, 3 FCLK	2, 3 ICLK	ROM	
007F C440h	FLASH	E2 DataFlash Read Enable Register 0	DFLRE0	16	16	2, 3 FCLK	2, 3 ICLK	E2 DataFlash Memory	
007F C442h	FLASH	E2 DataFlash Read Enable Register 1	DFLRE1	16	16	2, 3 FCLK	2, 3 ICLK		
007F C450h	FLASH	E2 DataFlash P/E Enable Register 0	DFLWE0	16	16	2, 3 FCLK	2, 3 ICLK		
007F C452h	FLASH	E2 DataFlash P/E Enable Register 1	DFLWE1	16	16	2, 3 FCLK	2, 3 ICLK		

Table 4.1 List of I/O Registers (Address Order) (48/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
007F FFB0h	FLASH	Flash Status Register 0	FSTATR0	8	8	2, 3 FCLK	2, 3 ICLK	ROM	
007F FFB1h	FLASH	Flash Status Register 1	FSTATR1	8	8	2, 3 FCLK	2, 3 ICLK		
007F FFB2h	FLASH	Flash P/E Mode Entry Register	FENTRYR	16	16	2, 3 FCLK	2, 3 ICLK	ROM/ E2 DataFlash Memory	
007F FFB4h	FLASH	Flash Protection Register	FPROTR	16	16	2, 3 FCLK	2, 3 ICLK	ROM	
007F FFB6h	FLASH	Flash Reset Register	FRESETR	16	16	2, 3 FCLK	2, 3 ICLK		
007F FFBAh	FLASH	FCU Command Register	FCMDR	16	16	2, 3 FCLK	2, 3 ICLK		
007F FFC8h	FLASH	FCU Processing Switching Register	FCPSR	16	16	2, 3 FCLK	2, 3 ICLK		
007F FFCAh	FLASH	E2 DataFlash Blank Check Control Register	DFLBCCNT	16	16	2, 3 FCLK	2, 3 ICLK	E2 DataFlash Memory	
007F FFCCh	FLASH	Flash P/E Status Register	FPESTAT	16	16	2, 3 FCLK	2, 3 ICLK	ROM	
007F FFCEh	FLASH	E2 DataFlash Blank Check Status Register	DFLBCSTAT	16	16	2, 3 FCLK	2, 3 ICLK	E2 DataFlash Memory	
007F FFE8h	FLASH	Peripheral Clock Notification Register	PCKAR	16	16	2, 3 FCLK	2, 3 ICLK	ROM	

Note: • This table shows the maximum specifications of I/O registers. The I/O registers of individual products correspond to the list of functions given as Table 1.2. For details, refer to Table 1.2, Comparison of Functions for Different Packages.
Note 1. When the register is accessed while the USB is operating, a delay may be generated in accessing.
Note 2. Odd addresses are not accessible in 16-bit units. Obtain 16-bit access to the two registers by access to the address of TMOCNTL.
Note 3. Pins USB0 and RIIC1 are not present in 112-pin products.
Note 4. Pins USB0, RIIC1, and SCI3 are not present in 100-pin products.
Note 5. Pins GPT4 to GPT7, USB0, RSPI1, RIIC1, SCI2, SCI3, CAN1, AD, and S12AD1 are not present in 64- and 48-pin products.

5. Electrical Characteristics [144-, 120-, 112- and 100-Pin Versions]

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

Conditions: VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V

Item		Symbol	Value	Unit
Power supply voltage		VCC, PLLVCC	–0.3 to +6.5	V
USB power supply voltage		VCC_USB*1	–0.3 to +6.5	V
Analog power supply voltage		AVCC0, AVCC*2	–0.3 to +6.5	V
Reference power supply voltage		VREFH0*2	–0.3 to AVCC0 + 0.3	V
		VREF*2	–0.3 to AVCC0 + 0.3	V
Input voltage (except for ports 4 to 6, C, USB0_DP, and USB0_DM)		V_{in}	–0.3 to VCC + 0.3	V
Input voltage (USB0_DP and USB0_DM)		V_{in}	–0.3 to VCC_USB + 0.3	V
Input voltage (port 4)		V_{in}	–0.3 to AVCC0 + 0.3	V
Input voltage (ports 5, 6, and C)		V_{in}	–0.3 to AVCC + 0.3	V
Analog input voltage (port 4)		V_{AN}	–0.3 to AVCC0 + 0.3	V
Analog input voltage (ports 5, 6, and C)		V_{AN}	–0.3 to AVCC + 0.3	V
Operating temperature	D version product	T_{opr}	–40 to +85	ºC
	G version product	T_{opr}	–40 to +105	ºC
Storage temperature		T_{stg}	–55 to +125	ºC

Caution: Permanent damage to the LSI may result if absolute maximum ratings are exceeded.

Note 1. When the USB is not in use, do not leave the VCC_USB and VSS_USB pins open.
Connect the VCC_USB pin to VCC, and the VSS_USB pin to VSS, respectively.

Note 2. When the A/D converter is not in use, do not leave the AVCC0, VREFH0, VREFL0, AVSS0, AVCC, VREF, and AVSS pins open.
- When the 12-bit A/D converter is not in use
  Connect the AVCC0 pin to AVCC, the VREFH0 pin to VREF, and the AVSS0 and VREFL0 pins to AVSS, respectively.
- When the 10-bit A/D converter is not in use
  Connect the AVCC pin to AVCC0, the VREF pin to VREFH0, and the AVSS pin to AVSS0, respectively.
- When the 12-bit A/D converter and 10-bit A/D converter are not in use
  Connect the AVCC0, VREFH0, AVCC, and VREF pins to VCC, and the AVSS0, VREFL0, and AVSS pins to VSS, respectively.

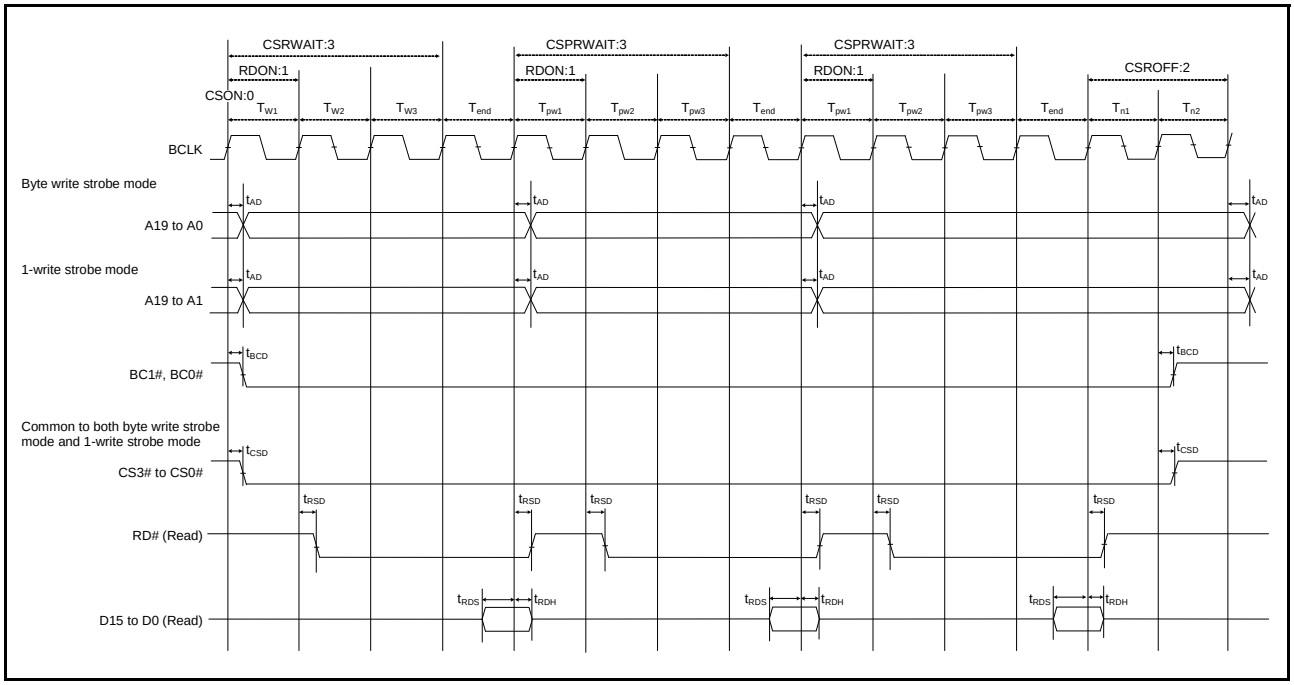
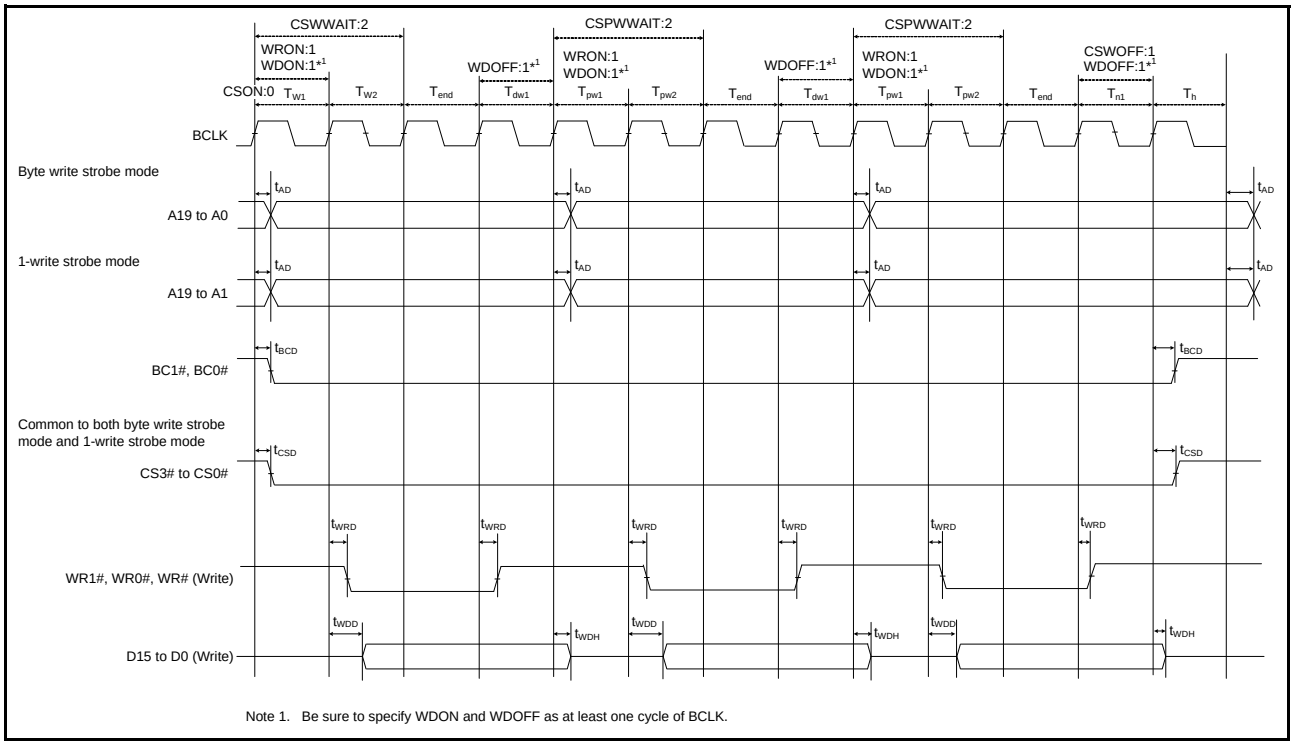


Figure 5.15 External Bus Timing/Page Read Cycle (Bus Clock Synchronized)



Note 1. Be sure to specify WDON and WDOFF as at least one cycle of BCLK.

Figure 5.16 External Bus Timing/Page Write Cycle (Bus Clock Synchronized)

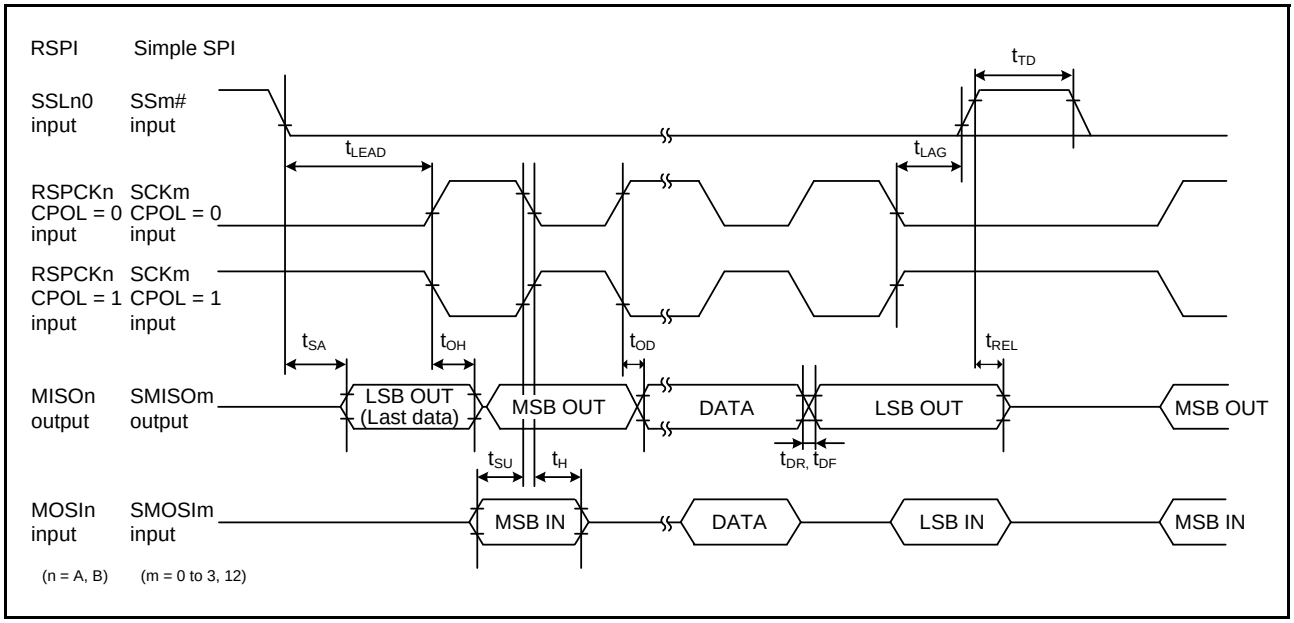
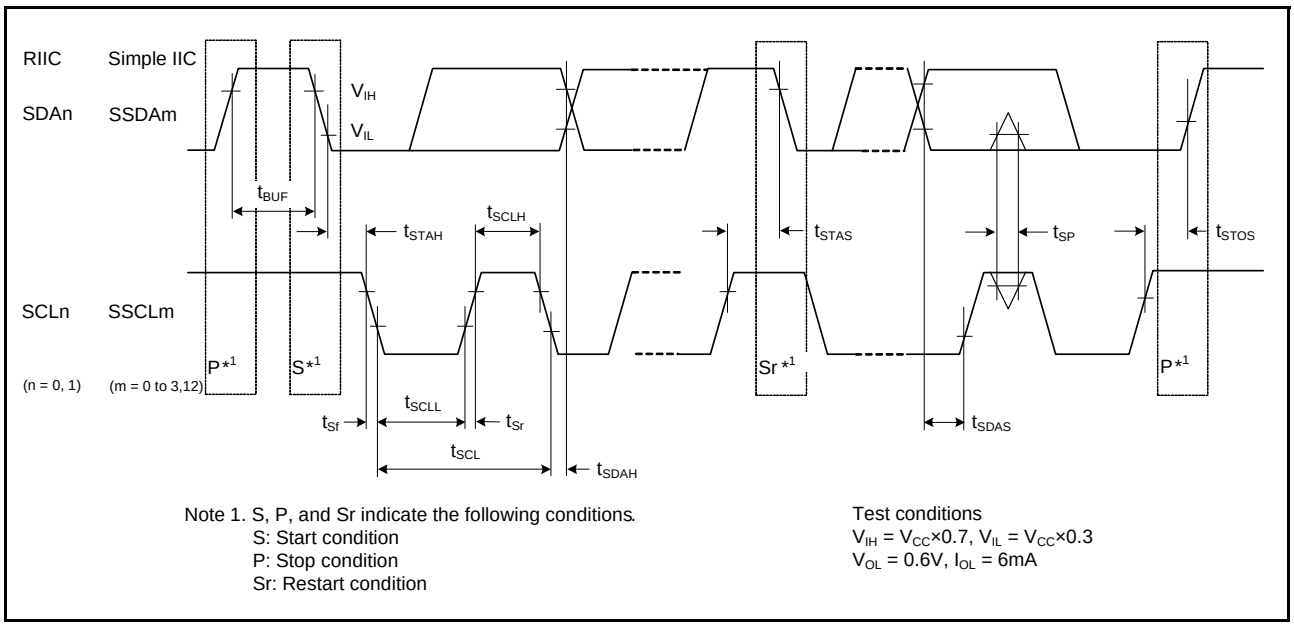


Figure 5.35 RSPI Timing (Slave, CPHA = 1) and Simple SPI Timing (Slave, CKPH = 0)



Note 1. S, P, and Sr indicate the following conditions.
S: Start condition
P: Stop condition
Sr: Restart condition

Test conditions
$V_{IH} = V_{CC} \times 0.7$, $V_{IL} = V_{CC} \times 0.3$
$V_{OL} = 0.6V$, $I_{OL} = 6mA$

Figure 5.36 RIIC Bus Interface Input/Output Timing and Simple IIC Bus Interface Input/Output Timing

Table 6.3 DC Characteristics (2)

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Supply current*1	During operation	Max. *2	I_{CC}*3	—	—	60	mA	ICLK = 100MHz PCLKA = 100MHz PCLKB = 50MHz PCLKD = 50MHz FCLK = 50MHz
		Normal *4		—	25	—		
		Increased by BGO operation*5		—	15	—		
	Sleep mode				25	35		
	All-module-clock-stop mode*6				14	25		
	During standby	Software standby mode		—	0.2	6	mA	
		Deep software standby mode		—	16	40	µA	
Analog power supply current	During 12-bit A/D conversion (sample & hold circuit in use)		AI_{CC0}	—	3	4	mA	
	During 12-bit A/D conversion (sample & hold circuit not in use)			—	2	3	mA	
	Window comparator (1-channel operation)				0.4	1	mA	
	Window comparator (3-channel operation)			—	0.5	1	mA	
	Waiting for 12-bit AD conversion			—	25	32	µA	
Reference power supply current	During 12-bit A/D conversion		AI_{REFH0}	—	0.6	0.7	mA	
	Waiting for 12-bit A/D conversion			—	0.6	0.7	mA	
VCC rising gradient			SrVcc	—	—	20000	ms/V	

Note 1. Supply current values are with all output pins unloaded.
Note 2. Measured with clocks supplied to the peripheral functions. This does not include the BGO operation.
Note 3. I_{CC} depends on f (ICLK) as follows. (ICLK: PCLK = 8:4)
ICC max = 0.45 × f + 15 (Max)
ICC typ = 0.18 × f + 7 (Normal)
ICC max = 0.22 × f + 13 (sleep mode)
Note 4. Measured with clocks not supplied to the peripheral functions. This does not include the BGO operation.
Note 5. Incremented if data is written to or erased from the on-chip ROM or on-chip data-flash memory for data storage during the program execution.
Note 6. The values are for reference.

Table 6.4 Permissible Output Currents

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item	Symbol	Min.	Typ.	Max.	Unit
Permissible output low current (average value per pin)	I_{OL}	—	—	2.0*1	mA
Permissible output low current (max. value per pin)	I_{OL}	—	—	4.0*1	mA
Permissible output low current (total)	ΣI_{OL}	—	—	32	mA
Permissible output high current (average value per pin)	$-I_{OH}$	—	—	2.0	mA
Permissible output high current (max. value per pin)	$-I_{OH}$	—	—	4.0	mA
Permissible output high current (total)	$\Sigma-I_{OH}$	—	—	32	mA

Caution: To protect the MCU's reliability, the output current values should not exceed the values in this table.
Note 1. RIIC pin: IOL = 6 mA (max.)

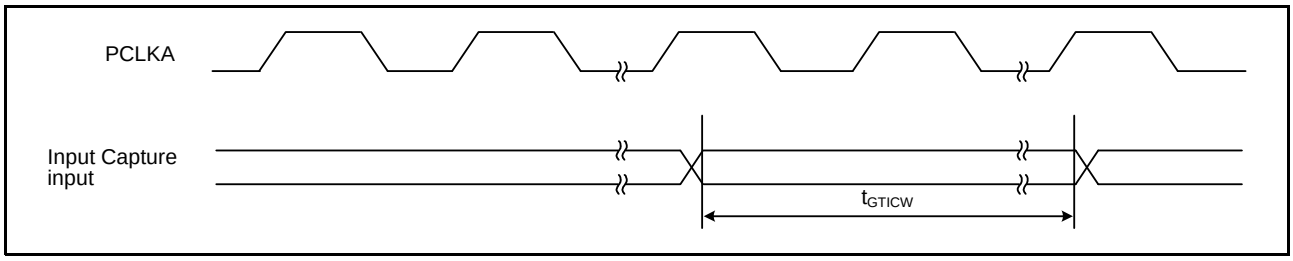


Figure 6.15 GPT Input/Output Timing

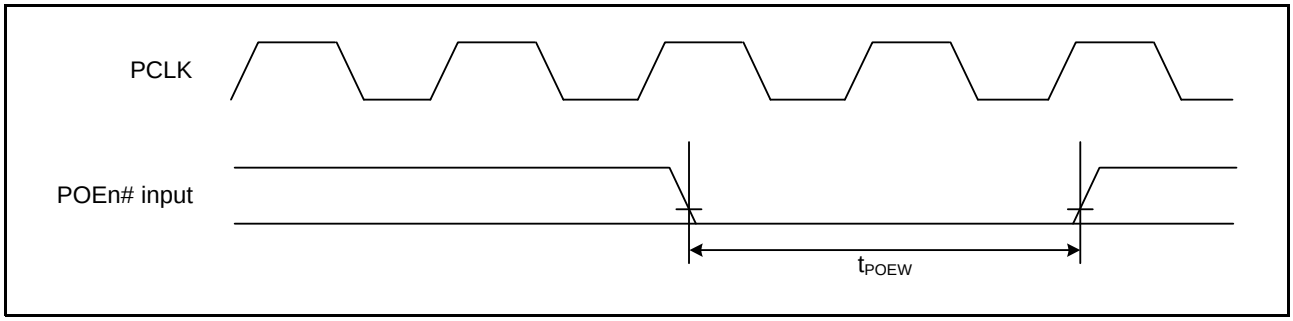


Figure 6.16 POE3# Input Timing

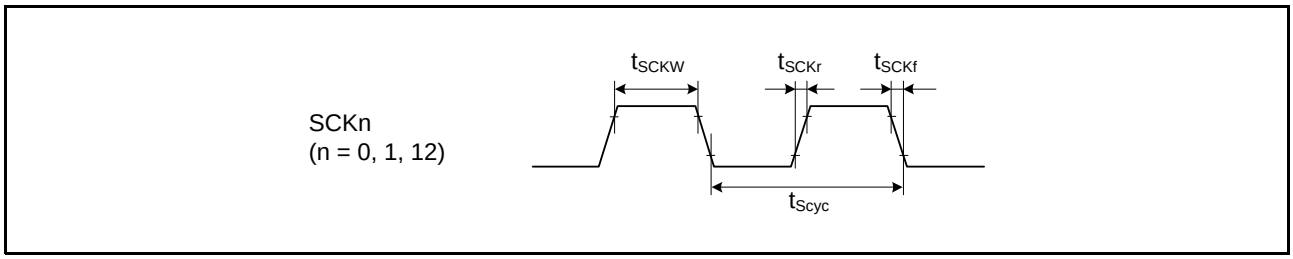


Figure 6.17 SCK Clock Input Timing

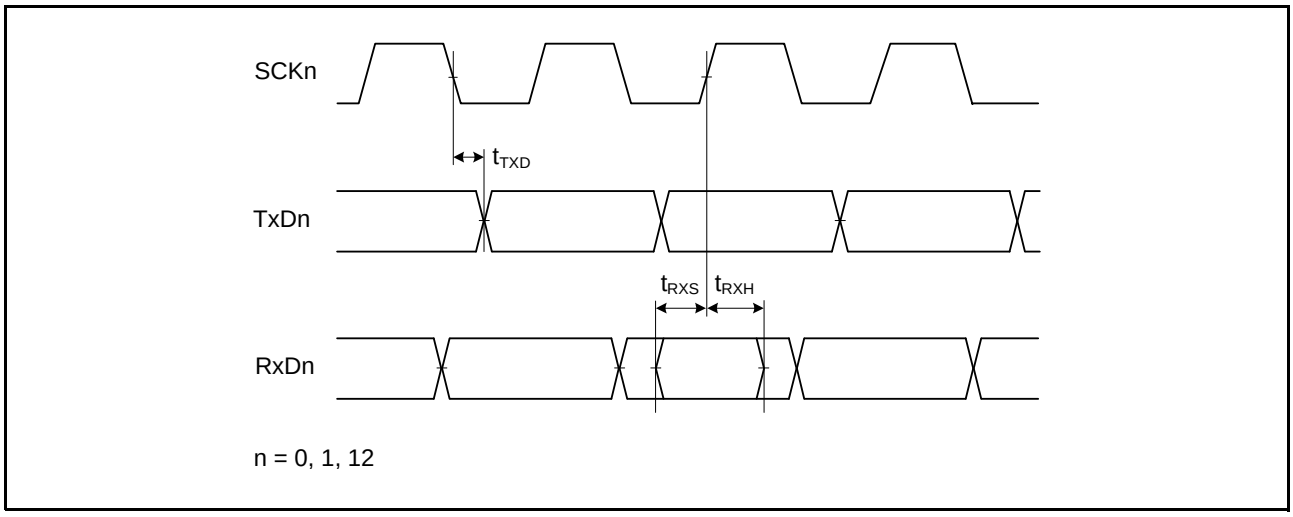


Figure 6.18 SCI Input/Output Timing: Clock Synchronous Mode

REVISION HISTORY — RX63T Group Datasheet

Rev.	Date	Description	
		Page	Summary
1.00	Aug 28, 2012	—	First Edition issued
2.00	Mar 11, 2013	Features	
		1	Changed
		1. Overview	
		2	1.1 Outline of Specifications, description changed
		2 to 8	Table 1.1 Outline of Specifications, changed
		9	Table 1.2 Comparison of Functions for Different Packages, changed
		10 to 12	Table 1.3 List of Products, changed
		12	Figure 1.1 How to Read the Product Part Number, changed
		13	Figure 1.2 Block Diagram, changed
		14 to 18	Table 1.4 Pin Functions, changed
		19	Figure 1.3 Pin Assignment (144-Pin LQFP), added
		20	Figure 1.4 Pin Assignment (120-Pin LQFP), added
		21	Figure 1.5 Pin Assignment (112-Pin LQFP), added
		22	Figure 1.6 Pin Assignment (100-Pin LQFP), added
		23	Figure 1.7 Pin Assignment (64-Pin LQFP), notes changed
		24	Figure 1.8 Pin Assignment (48-Pin LQFP), notes changed
		25 to 28	Table 1.5 List of Pins and Pin Functions (144-Pin LQFP), added
		29 to 32	Table 1.6 List of Pins and Pin Functions (120-Pin LQFP), added
		33 to 36	Table 1.7 List of Pins and Pin Functions (112-Pin LQFP), added
		37 to 39	Table 1.8 List of Pins and Pin Functions (100-Pin LQFP), added
		3. Address Space	
		49	Figure 3.1 Memory Map in Each Operating Mode, changed
		50	3.2 External Address Space, added
		4. I/O Registers	
		52	(3) Number of Access Cycles to I/O Registers, description changed
		53 to 103	Table 4.1 List of I/O Registers (Address Order), changed
		5. Electrical Characteristics [144-, 120-, 112- and 100-Pin Versions]	
		104 to 148	Added
		6. Electrical Characteristics [64- and 48-Pin Versions]	
		149	Title changed
		152	Table 6.6 Clock Timing, changed
		158	Table 6.10 Timing of On-Chip Peripheral Modules (1), changed
		160	Table 6.12 Timing of On-Chip Peripheral Modules (3), changed
		170	6.6 Oscillation Stop Detection Circuit Characteristics, title changed
		170	Table 6.18 Oscillation Stop Detection Circuit Characteristics, title changed
		171	Table 6.19 ROM (Flash Memory for Code Storage) Characteristics (1), added
		171	Table 6.20 ROM (Flash Memory for Code Storage) Characteristics (2), title and description changed
		172	Table 6.21 DataFlash (Flash Memory for Data Storage) Characteristics (1), added
		172	Table 6.22 DataFlash (Flash Memory for Data Storage) Characteristics (2), title and description changed
		Appendix 1. Package Dimensions	
		174 to 177	Figure A 144-Pin LQFP (PLQP0144KA-A) to Figure D 100-Pin LQFP (PLQP0100KB-A), added
2.10	Sep 26, 2013	The RX63T Group and RX63T changed to this MCU	
		Features	
		1	Changed
		1. Overview	
		2 to 8	Table 1.1 Outline of Specifications, changed, Note 1, added.
		9	Table 1.2 Comparison of Functions for Different Packages, changed, Note 2, added.
		10 to 14	Table 1.3 List of Products, changed, Note 1, added
		15	Figure 1.1 How to Read the Product Part Number, changed
		28 to 31	Table 1.5 List of Pins and Pin Functions (144-Pin LQFP), changed
		32 to 35	Table 1.6 List of Pins and Pin Functions (120-Pin LQFP), changed

Classifications

- Items with Technical Update document number: Changes according to the corresponding issued Technical Update
- Items without Technical Update document number: Minor changes that do not require Technical Update to be issued

Rev.	Date	Description		Classification
		Page	Summary	
2.20	Mar 31, 2016	1. Overview		
		2 to 8	Table 1.1 Outline of Specifications, Note 1 changed	TN-RX*-A086A/E
		10 to 13	Table 1.3 List of Products, changed	TN-RX*-A086A/E
		16	Table 1.4 Pin Functions, changed	
		27 to 30	Table 1.5 List of Pins and Pin Functions (144-Pin LQFP), changed	
		30	Table 1.5 List of Pins and Pin Functions (144-Pin LQFP), Note 1 added	
		31 to 34	Table 1.6 List of Pins and Pin Functions (120-Pin LQFP), changed	
		35 to 38	Table 1.7 List of Pins and Pin Functions (112-Pin LQFP), changed	
		38	Table 1.7 List of Pins and Pin Functions (112-Pin LQFP), Note 1 added	
		4. I/O Registers		
		54	(4) Notes on Sleep Mode and Mode Transition, added	TN-RX*-A140A/E
		55 to 102	Table 4.1 List of I/O Registers (Address Order), changed	TN-RX*-A086A/E, TN-RX*-A140A/E
		5. Electrical Characteristics [144-, 120-, 112- and 100-Pin Versions]		
		103	Table 5.1 Absolute Maximum Ratings, changed	TN-RX*-A086A/E
		106	Table 5.4 DC Characteristics (3), changed	
		107	Table 5.5 Permissible Output Currents, changed	
		108	Table 5.6 Permissible Power Consumption (G version product only), title changed, notes added	TN-RX*-A086A/E
		111	Table 5.9 Clock Timing, changed	TN-RX*-A097A/E
		112	Figure 5.6 LOCO, IWDTCLK Clock Oscillation Start Timing, title changed	TN-RX*-A097A/E
		112	Figure 5.6 LOCO, IWDTCLK Clock Oscillation Start Timing, changed	TN-RX*-A097A/E
		124	Table 5.16 Timing of On-Chip Peripheral Modules (1), changed	TN-RX*-A121A/E
		125	Table 5.16 Timing of On-Chip Peripheral Modules (2), changed	TN-RX*-A121A/E
		126	Table 5.16 Timing of On-Chip Peripheral Modules (3), changed	TN-RX*-A121A/E
		127	Table 5.16 Timing of On-Chip Peripheral Modules (4), changed	
		129	Table 5.17 Timing of the PWM Delay Generation Circuit	TN-RX*-A086A/E
		132	Figure 5.30 RSPI Timing (Master, CPHA = 0) (Bit Rate: PCLKB Division Ratio Set to a Value Other Than 1/2) and Simple SPI Timing (Master, CKPH = 1), title and figure changed	
		133	Figure 5.32 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKB Division Ratio Set to a Value Other Than 1/2) and Simple SPI Timing (Master, CKPH = 0), title changed	
		134	Figure 5.34 RSPI Timing (Slave, CPHA = 0) and Simple SPI Timing (Slave, CKPH = 1), title changed	
		135	Figure 5.35 RSPI Timing (Slave, CPHA = 1) and Simple SPI Timing (Slave, CKPH = 0), title changed	
		136	Table 5.18 On-Chip USB Full-Speed Characteristics (DP and DM Pin Characteristics), Condition 1, 2 changed	TN-RX*-A086A/E
		143	Table 5.26 Power-on Reset Circuit and Voltage Detection Circuit Characteristics (1), changed	
		6. Electrical Characteristics [64- and 48-Pin Versions]		
		150	Table 6.1 Absolute Maximum Ratings, changed	TN-RX*-A086A/E
		153	Table 6.5 Permissible Power Consumption (G version product only), title changed, note added	TN-RX*-A086A/E
		154	Table 6.7 Clock Timing, changed	TN-RX*-A097A/E
		155	Figure 6.3 LOCO, IWDTCLK Clock Oscillation Start Timing, title changed	TN-RX*-A097A/E
		155	Figure 6.3 LOCO, IWDTCLK Clock Oscillation Start Timing, changed	TN-RX*-A097A/E
		161	Table 6.12 Timing of On-Chip Peripheral Modules (2), changed	
		170	Table 6.18 Power-on Reset Circuit and Voltage Detection Circuit Characteristics, changed	