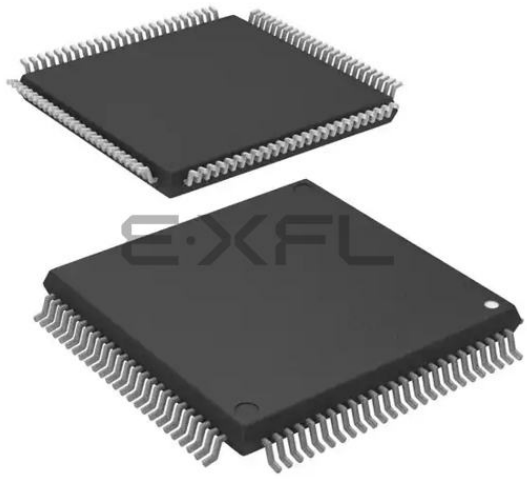
Renesas Electronics America Inc - R5F563TBBDFP#V1 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	57
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 12x10b, 8x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f563tbbdfp-v1

Table 1.1 Outline of Specifications (4/7)

Classification	Module/Function	Description
Timers	General PWM timer (GPT)	• 16 bits x 8 channels • Counting up or down (saw-wave), counting up and down (triangle-wave) selectable for all channels • Select from among four count clocks (PCLKA/1, PCLKA/4, PCLKA/8, and PCLKA/16) for each channel • 2 input/output pins per channel • 2 output compare/input capture registers per channel • For the 2 output compare/input capture registers of each channel, 4 registers are provided as buffer registers and are capable of operating as comparison registers when buffering is not in use. • In output compare operation, buffer switching can be at peaks or troughs, enabling the generation of laterally asymmetrically PWM waveforms. • Registers for setting up frame intervals on each channel (with capability for generating interrupts on overflow or underflow) • Synchronizable operation of the several counters • Modes of synchronized operation (synchronized, or displaced by desired times for phase shifting) • Generation of dead times in PWM operation • Through combination of three counters, generation of automatic three-phase PWM waveforms incorporating dead times • Starting, clearing, and stopping counters in response to external or internal triggers • Internal trigger sources: Output of the internal comparator detection, software, and compare-match • The main clock can be used as a counter clock for measuring the timing of the edges of signals produced by frequency-dividing the dedicated clock signal for the IWDT (to detect abnormal oscillation). • A PWM delay with an accuracy of up to 1/32 times the period of the system clock (ICLK) can be generated to control the timing with which signals from the two PWM output pins from each of channels 0 to 3 rise and fall.
	Compare match timer (CMT)	• (16 bits × 2 channels) × 2 units • Select from among four internal clock signals (PCLK/8, PCLK/32, PCLK/128, PCLK/512)
	Watchdog timer (WDTA)	• 14 bits × 1 channel • Select from among 6 counter-input clock signals (PCLK/4, PCLK/64, PCLK/128, PCLK/512, PCLK/2048, PCLK/8192)
	Independent watchdog timer (IWDTa)	• 14 bits × 1 channel • Counter-input clock: Dedicated on-chip oscillator • Dedicated clock/1, dedicated clock/16, dedicated clock/32, dedicated clock/64, dedicated clock/128, dedicated clock/256
Communication function	USB 2.0 host/function module (USBa)	• Includes a UDC (USB Device Controller) and transceiver for USB 2.0 • Single port • Compliance with the USB 2.0 specification • Transfer rate: Full speed (12 Mbps) • Self-power mode and bus power mode are selectable • Supports the OTG (On-The-Go) • Incorporates 2 Kbytes of RAM as a transfer buffer
	Serial communications interfaces (SCIc, SCId)	• 5 channels (SCIc: 4 channels + SCId: 1 channel) • SCIc Serial communications modes: Asynchronous, clock synchronous, and smart-card interface Multi-processor function On-chip baud rate generator allows selection of the desired bit rate Choice of LSB-first or MSB-first transfer Simple I^2C Simple SPI • SCId (The following functions are added to SCIc) Supports the serial communications protocol, which contains the start frame and information frame Supports the LIN format

Table 1.4 Pin Functions (3/5)

Classifications	Pin Name	I/O	Description
Serial communications interface (SCIc)	Asynchronous mode/clock synchronous mode		
	SCK0, SCK1, SCK2, SCK3	I/O	Input/output pins for clock signals.
	RXD0, RXD1, RXD2, RXD3	Input	Input pins for data reception.
	TXD0, TXD1, TXD2, TXD3	Output	Output pins for data transmission.
	CTS0#, CTS1#, CTS2#, CTS3#	Input	Transmit/receive start control input pins
	RTS0#, RTS1#, RTS2#, RTS3#	Output	Transmit/receive start control output pins
	Simple I^2C mode		
	SSCL0, SSCL1, SSCL2, SSCL3	I/O	Input/output pins for the I^2C clock
	SSDA0, SSDA1, SSDA2, SSDA3	I/O	Input/output pins for the I^2C data
	Simple SPI mode		
	SCK0, SCK1, SCK2, SCK3	I/O	Input/output pins for the clock
	SMISO0, SMISO1, SMISO2, SMISO3	I/O	Input/output pins for slave transmit data.
	SMOSI0, SMOSI1, SMOSI2, SMOSI3	I/O	Input/output pins for master transmit data.
	SS0#, SS1#, SS2#, SS3#	Input	Input pins for chip select signals
Serial communications interface (SCId)	Asynchronous mode/clock synchronous mode		
	SCK12	I/O	Input/output pin for clock signals.
	RXD12	Input	Input pin for data reception.
	TXD12	Output	Output pin for data transmission.
	CTS12#	Input	Transmit/receive start control input pins
	RTS12#	Output	Transmit/receive start control output pins
	Simple I^2C mode		
	SSCL12	I/O	Input/output pins for the I^2C clock
	SSDA12	I/O	Input/output pins for the I^2C data
	Simple SPI mode		
	SCK12	I/O	Input/output pins for the clock
	SMISO12	I/O	Input/output pins for slave transmit data.
	SMOSI12	I/O	Input/output pins for master transmit data.
	SS12#	Input	Input pins for chip select signals
	Extended serial mode		
	RXDX12	Input	Input pin for receive data
	TXDX12	Output	Output pin for transmit data
	SIOX12	I/O	Input/output pin for transfer data
I^2C bus interface	SCL, SCL0, SCL1	I/O	Clock input/output pin. N-channel open drain can directly drive buses.
	SDA, SDA0, SDA1	I/O	Data input/output pin. N-channel open drain can directly drive buses.

Table 1.6 List of Pins and Pin Functions (120-Pin LQFP) (2/4)

Pin Number 120-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3, GPT, POE3, CAC)	Communications (SCIc, SCId, RSPI, RIIC, CAN, USB)	Interrupt	S12ADB, AD, DA
37	PLLVSS						
38		PB3	A15	MTIOC0A/CACREF	SCK0		
39		PB2		MTIOC0B	TXD0/SMOSI0/ SSDA0/SDA0		
40		PB1		MTIOC0C	RXD0/SMISO0/ SSCL0/SCL0	IRQ4	
41		PB0	A14	MTIOC0D	MOSIA/MOSIB		
42		PA5		MTIOC1A	RXD0/SMISO0/ SSCL0/ MISOA/MISOB		ADTRG1#
43		PA4		MTIOC1B	TXD0/SMOSI0/ SSDA0/RSPCKA/ RSPCKB		ADTRG0#
44		PA3		MTIOC2A	SCK0/SSLA0/SSLB0		
45		PA2		MTIOC2B	RXD2/SMISO2/ SSCL2/ SSLA1/SSLB1		
46		PA1		MTIOC6A	TXD2/SMOSI2/ SSDA2/SSLA2/SSLB2		
47		PA0		MTIOC6C	SCK2/SSLA3/SSLB3		
48	VCC						
49		P96	A13	POE4#	RXD1/SMISO1/SSCL1	IRQ4-DS	
50		PG6	CS2#		SCK1		
51	VSS						
52		P95		MTIOC6B/GTIOC4A	TXD1/SMOSI1/SSDA1		
53		P94		MTIOC7A/GTIOC5A	CTS1#/RTS1#/SS1#		
54		P93		MTIOC7B/GTIOC6A	CTS2#/RTS2#/SS2#		
55		P92		MTIOC6D/GTIOC4B			
56		P91		MTIOC7C/GTIOC5B			
57		P90		MTIOC7D/GTIOC6B			
58	TRCLK	PG5		POE12#	SCK3		ADTRG#
59	TRDATA3	PG4		GTIOC6B	RXD3/SMISO3/SSCL3	IRQ6	
60	TRDATA2	PG3		GTIOC6A	TXD3/SMOSI3/SSDA3		
61	TRDATA1	PG2			SCK2	IRQ2	
62	TRDATA0	PG1		GTIOC7B	RXD2/SMISO2/SSCL2	IRQ1	
63	TRSYNC	PG0		GTIOC7A	TXD2/SMOSI2/SSDA2	IRQ0	
64		P76	D0/[A0/D0]	MTIOC4D/GTIOC2B			
65		P75	D1/[A1/D1]	MTIOC4C/GTIOC1B			
66		P74	D2/[A2/D2]	MTIOC3D/GTIOC0B			
67		P73	D3/[A3/D3]	MTIOC4B/GTIOC2A			
68		P72	D4/[A4/D4]	MTIOC4A/GTIOC1A			
69		P71	D5/[A5/D5]	MTIOC3B/GTIOC0A			
70		P70	D6/[A6/D6]	POE0#	CTS1#/RTS1#/SS1#	IRQ5-DS	
71		P33	D7/[A7/D7]	MTIOC3A/MTCLKA	SSLA3/SSLB3		
72		P32	D8/[A8/D8]	MTIOC3C/MTCLKB	SSLA2/SSLB2		
73	VCC						
74		P31	D9/[A9/D9]	MTIOC0A/MTCLKC	SSLA1/SSLB1		

Table 1.8 List of Pins and Pin Functions (100-Pin LQFP) (2/3)

Pin Number 100-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3, GPT, POE3, CAC)	Communications (SCIc, SCId, RSPI, RIIC, CAN)	Interrupt	S12ADB, AD, DA
37		PA4		MTIOC1B	TXD0/SMOSI0/ SSDA0/ RSPCKA/RSPCKB		ADTRG0#
38		PA3		MTIOC2A	SCK0/SSLA0/SSLB0		
39		PA2		MTIOC2B	RXD2/SMISO2/ SSCL2/ SSLA1/SSLB1		
40		PA1		MTIOC6A	TXD2/SMOSI2/ SSDA2/ SSLA2/SSLB2		
41		PA0		MTIOC6C	SCK2/SSLA3/SSLB3		
42	VCC						
43		P96	A13	POE4#	RXD1/SMISO1/SSCL1	IRQ4-DS	
44	VSS						
45		P95		MTIOC6B/GTIOC4A	TXD1/SMOSI1/SSDA1		
46		P94		MTIOC7A/GTIOC5A	CTS1#/RTS1#/SS1#		
47		P93		MTIOC7B/GTIOC6A	CTS2#/RTS2#/SS2#		
48		P92		MTIOC6D/GTIOC4B			
49		P91		MTIOC7C/GTIOC5B			
50		P90		MTIOC7D/GTIOC6B			
51		P76	D0/[A0/D0]	MTIOC4D/GTIOC2B			
52		P75	D1/[A1/D1]	MTIOC4C/GTIOC1B			
53		P74	D2/[A2/D2]	MTIOC3D/GTIOC0B			
54		P73	D3/[A3/D3]	MTIOC4B/GTIOC2A			
55		P72	D4/[A4/D4]	MTIOC4A/GTIOC1A			
56		P71	D5/[A5/D5]	MTIOC3B/GTIOC0A			
57		P70	D6/[A6/D6]	POE0#	CTS1#/RTS1#/SS1#	IRQ5-DS	
58		P33	D7/[A7/D7]	MTIOC3A/MTCLKA	SSLA3/SSLB3		
59		P32	D8/[A8/D8]	MTIOC3C/MTCLKB	SSLA2/SSLB2		
60	VCC						
61		P31	D9/[A9/D9]	MTIOC0A/MTCLKC	SSLA1/SSLB1		
62	VSS						
63		P30	D10/[A10/ D10]	MTIOC0B/MTCLKD	SCK0/SSLA0/SSLB0		
64		P24	D11/[A11/D11]		CTS0#/RTS0#/SS0#/ RSPCKA/RSPCKB	IRQ4	
65		P23	D12/[A12/ D12]	CACREF	TXD0/SMOSI0/ SSDA0/MOSIA/ MOSIB/CTX1		
66		P22	D13/[A13/ D13]		RXD0/SMISO0/ SSCL0/MISOA/ MISOB/CRX1		ADTRG#
67		P21	D14/[A14/ D14]	MTCLKA		IRQ6-DS	ADTRG1#
68		P20	D15/[A15/ D15]	MTCLKB		IRQ7-DS	ADTRG0#
69		P65	A0/BC0#				AN5
70		P64	A1				AN4

2.2.1 Register Associated with DSP Instructions

(1) Accumulator (ACC)

The accumulator (ACC) is a 64-bit register used for DSP instructions. The accumulator is also used for the multiply and multiply-and-accumulate instructions; EMUL, EMULU, FMUL, MUL, and RMPA, in which case the prior value in the accumulator is modified by execution of the instruction.
Use the MVTACHI and MVTACLO instructions for writing to the accumulator. The MVTACHI and MVTACLO instructions write data to the higher-order 32 bits (bits 63 to 32) and the lower-order 32 bits (bits 31 to 0), respectively.
Use the MVFACHI and MVFACMI instructions for reading data from the accumulator. The MVFACHI and MVFACMI instructions read data from the higher-order 32 bits (bits 63 to 32) and the middle 32 bits (bits 47 to 16), respectively.

Table 4.1 List of I/O Registers (Address Order) (3/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 3024h	BSC	CS2 Wait Control Register 1	CS2WCR1	32	32	1, 2 BCLK		Buses	Not present in versions with 64 or 48 pins.
0008 3028h	BSC	CS2 Wait Control Register 2	CS2WCR2	32	32	1, 2 BCLK			Not present in versions with 64 or 48 pins.
0008 3032h	BSC	CS3 Mode Register	CS3MOD	16	16	1, 2 BCLK			Not present in versions with 64 or 48 pins.
0008 3034h	BSC	CS3 Wait Control Register 1	CS3WCR1	32	32	1, 2 BCLK			Not present in versions with 64 or 48 pins.
0008 3038h	BSC	CS3 Wait Control Register 2	CS3WCR2	32	32	1, 2 BCLK			Not present in versions with 64 or 48 pins.
0008 3802h	BSC	CS0 Control Register	CS0CR	16	16	1, 2 BCLK			Not present in versions with 64 or 48 pins.
0008 380Ah	BSC	CS0 Recovery Cycle Register	CS0REC	16	16	1, 2 BCLK			Not present in versions with 64 or 48 pins.
0008 3812h	BSC	CS1 Control Register	CS1CR	16	16	1, 2 BCLK			Not present in versions with 64 or 48 pins.
0008 381Ah	BSC	CS1 Recovery Cycle Register	CS1REC	16	16	1, 2 BCLK			Not present in versions with 64 or 48 pins.
0008 3822h	BSC	CS2 Control Register	CS2CR	16	16	1, 2 BCLK			Not present in versions with 64 or 48 pins.
0008 382Ah	BSC	CS2 Recovery Cycle Register	CS2REC	16	16	1, 2 BCLK			Not present in versions with 64 or 48 pins.
0008 3832h	BSC	CS3 Control Register	CS3CR	16	16	1, 2 BCLK			Not present in versions with 64 or 48 pins.
0008 383Ah	BSC	CS3 Recovery Cycle Register	CS3REC	16	16	1, 2 BCLK			Not present in versions with 64 or 48 pins.
0008 3880h	BSC	CS Recovery Cycle Insertion Enable Register	CSRECEN	16	16	1, 2 BCLK			Not present in versions with 64 or 48 pins.
0008 6400h	MPU	Region-0 Start Page Number Register	RSPAGE0	32	32	1 ICLK		MPU	
0008 6404h	MPU	Region-0 End Page Number Register	REPAGE0	32	32	1 ICLK			
0008 6408h	MPU	Region-1 Start Page Number Register	RSPAGE1	32	32	1 ICLK			
0008 640Ch	MPU	Region-1 End Page Number Register	REPAGE1	32	32	1 ICLK			
0008 6410h	MPU	Region-2 Start Page Number Register	RSPAGE2	32	32	1 ICLK			
0008 6414h	MPU	Region-2 End Page Number Register	REPAGE2	32	32	1 ICLK			
0008 6418h	MPU	Region-3 Start Page Number Register	RSPAGE3	32	32	1 ICLK			
0008 641Ch	MPU	Region-3 End Page Number Register	REPAGE3	32	32	1 ICLK			
0008 6420h	MPU	Region-4 Start Page Number Register	RSPAGE4	32	32	1 ICLK			
0008 6424h	MPU	Region-4 End Page Number Register	REPAGE4	32	32	1 ICLK			
0008 6428h	MPU	Region-5 Start Page Number Register	RSPAGE5	32	32	1 ICLK			
0008 642Ch	MPU	Region-5 End Page Number Register	REPAGE5	32	32	1 ICLK			
0008 6430h	MPU	Region-6 Start Page Number Register	RSPAGE6	32	32	1 ICLK			
0008 6434h	MPU	Region-6 End Page Number Register	REPAGE6	32	32	1 ICLK			
0008 6438h	MPU	Region-7 Start Page Number Register	RSPAGE7	32	32	1 ICLK			
0008 643Ch	MPU	Region-7 End Page Number Register	REPAGE7	32	32	1 ICLK			
0008 6500h	MPU	Memory-Protection Enable Register	MPEN	32	32	1 ICLK			
0008 6504h	MPU	Background Access Control Register	MPBAC	32	32	1 ICLK			
0008 6508h	MPU	Memory-Protection Error Status-Clearing Register	MPECLR	32	32	1 ICLK			
0008 650Ch	MPU	Memory-Protection Error Status Register	MPESTS	32	32	1 ICLK			
0008 6514h	MPU	Data Memory-Protection Error Address Register	MPDEA	32	32	1 ICLK			
0008 6520h	MPU	Region Search Address Register	MPSA	32	32	1 ICLK			
0008 6524h	MPU	Region Search Operation Register	MPOPS	16	16	1 ICLK			
0008 6526h	MPU	Region Invalidation Operation Register	MPOPI	16	16	1 ICLK			
0008 6528h	MPU	Instruction-Hit Region Register	MHITI	32	32	1 ICLK			
0008 652Ch	MPU	Data-Hit Region Register	MHITD	32	32	1 ICLK			

Table 4.1 List of I/O Registers (Address Order) (11/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 7206h	ICU	Interrupt Request Enable Register 06	IER06	8	8	2 ICLK		ICUb	Not present in versions with 64 or 48 pins.
0008 7207h	ICU	Interrupt Request Enable Register 07	IER07	8	8	2 ICLK			
0008 7208h	ICU	Interrupt Request Enable Register 08	IER08	8	8	2 ICLK			
0008 720Bh	ICU	Interrupt Request Enable Register 0B	IER0B	8	8	2 ICLK			Not present in versions with 112, 100, 64 or 48 pins.
0008 720Ch	ICU	Interrupt Request Enable Register 0C	IER0C	8	8	2 ICLK			
0008 720Dh	ICU	Interrupt Request Enable Register 0D	IER0D	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 720Eh	ICU	Interrupt Request Enable Register 0E	IER0E	8	8	2 ICLK			
0008 720Fh	ICU	Interrupt Request Enable Register 0F	IER0F	8	8	2 ICLK			
0008 7210h	ICU	Interrupt Request Enable Register 10	IER10	8	8	2 ICLK			
0008 7211h	ICU	Interrupt Request Enable Register 11	IER11	8	8	2 ICLK			
0008 7212h	ICU	Interrupt Request Enable Register 12	IER12	8	8	2 ICLK			
0008 7213h	ICU	Interrupt Request Enable Register 13	IER13	8	8	2 ICLK			
0008 7214h	ICU	Interrupt Request Enable Register 14	IER14	8	8	2 ICLK			
0008 7215h	ICU	Interrupt Request Enable Register 15	IER15	8	8	2 ICLK			
0008 7216h	ICU	Interrupt Request Enable Register 16	IER16	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7217h	ICU	Interrupt Request Enable Register 17	IER17	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7218h	ICU	Interrupt Request Enable Register 18	IER18	8	8	2 ICLK			
0008 7219h	ICU	Interrupt Request Enable Register 19	IER19	8	8	2 ICLK			
0008 721Ah	ICU	Interrupt Request Enable Register 1A	IER1A	8	8	2 ICLK			
0008 721Bh	ICU	Interrupt Request Enable Register 1B	IER1B	8	8	2 ICLK			
0008 721Ch	ICU	Interrupt Request Enable Register 1C	IER1C	8	8	2 ICLK			
0008 721Dh	ICU	Interrupt Request Enable Register 1D	IER1D	8	8	2 ICLK			
0008 721Eh	ICU	Interrupt Request Enable Register 1E	IER1E	8	8	2 ICLK			
0008 721Fh	ICU	Interrupt Request Enable Register 1F	IER1F	8	8	2 ICLK			
0008 72E0h	ICU	Software Interrupt Activation Register	SWINTR	8	8	2 ICLK			
0008 72F0h	ICU	Fast Interrupt Set Register	FIR	16	16	2 ICLK			
0008 7300h	ICU	Interrupt Source Priority Register 000	IPR000	8	8	2 ICLK			
0008 7301h	ICU	Interrupt Source Priority Register 001	IPR001	8	8	2 ICLK			
0008 7302h	ICU	Interrupt Source Priority Register 002	IPR002	8	8	2 ICLK			
0008 7303h	ICU	Interrupt Source Priority Register 003	IPR003	8	8	2 ICLK			
0008 7304h	ICU	Interrupt Source Priority Register 004	IPR004	8	8	2 ICLK			
0008 7305h	ICU	Interrupt Source Priority Register 005	IPR005	8	8	2 ICLK			
0008 7306h	ICU	Interrupt Source Priority Register 006	IPR006	8	8	2 ICLK			
0008 7307h	ICU	Interrupt Source Priority Register 007	IPR007	8	8	2 ICLK			
0008 7321h	ICU	Interrupt Source Priority Register 033	IPR033	8	8	2 ICLK			Not present in versions with 112, 100, 64 or 48 pins.
0008 7322h	ICU	Interrupt Source Priority Register 034	IPR034	8	8	2 ICLK			Not present in versions with 112, 100, 64 or 48 pins.
0008 7323h	ICU	Interrupt Source Priority Register 035	IPR035	8	8	2 ICLK			Not present in versions with 112, 100, 64 or 48 pins.
0008 7324h	ICU	Interrupt Source Priority Register 036	IPR036	8	8	2 ICLK			
0008 7327h	ICU	Interrupt Source Priority Register 039	IPR039	8	8	2 ICLK			
0008 7328h	ICU	Interrupt Source Priority Register 040	IPR040	8	8	2 ICLK			
0008 7329h	ICU	Interrupt Source Priority Register 041	IPR041	8	8	2 ICLK			
0008 732Ah	ICU	Interrupt Source Priority Register 042	IPR042	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 732B	ICU	Interrupt Source Priority Register 043	IPR043	8	8	2 ICLK			Not present in versions with 64 or 48 pins.

Table 4.1 List of I/O Registers (Address Order) (14/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 7507h	ICU	IRQ Control Register 7	IRQCR7	8	8	2 ICLK		ICUb	Not present in versions with 64 or 48 pins.
0008 7510h	ICU	IRQ Pin Digital Filter Enable Register 0	IRQFLTE0	8	8	2 ICLK			
0008 7514h	ICU	IRQ Pin Digital Filter Setting Register 0	IRQFLTC0	16	16	2 ICLK			
0008 7580h	ICU	Non-Maskable Interrupt Status Register	NMISR	8	8	2 ICLK			
0008 7581h	ICU	Non-Maskable Interrupt Enable Register	NMIER	8	8	2 ICLK			
0008 7582h	ICU	Non-Maskable Interrupt Status Clear Register	NMICLR	8	8	2 ICLK			
0008 7583h	ICU	NMI Pin Interrupt Control Register	NMICR	8	8	2 ICLK			
0008 7590h	ICU	NMI Pin Digital Filter Enable Register	NMIFLTE	8	8	2 ICLK			
0008 7594h	ICU	NMI Pin Digital Filter Setting Register	NMIFLTC	8	8	2 ICLK			
0008 8000h	CMT	Compare Match Timer Start Register 0	CMSTR0	16	16	2, 3 PCLKB	2 ICLK	CMT	
0008 8002h	CMT0	Compare Match Timer Control Register	CMCR	16	16	2, 3 PCLKB	2 ICLK		
0008 8004h	CMT0	Compare Match Timer Counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK		
0008 8006h	CMT0	Compare Match Timer Constant Register	CMCOR	16	16	2, 3 PCLKB	2 ICLK		
0008 8008h	CMT1	Compare Match Timer Control Register	CMCR	16	16	2, 3 PCLKB	2 ICLK		
0008 800Ah	CMT1	Compare Match Timer Counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK		
0008 800Ch	CMT1	Compare Match Timer Constant Register	CMCOR	16	16	2, 3 PCLKB	2 ICLK		
0008 8010h	CMT	Compare Match Timer Start Register 1	CMSTR1	16	16	2, 3 PCLKB	2 ICLK		
0008 8012h	CMT2	Compare Match Timer Control Register	CMCR	16	16	2, 3 PCLKB	2 ICLK		
0008 8014h	CMT2	Compare Match Timer Counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK		
0008 8016h	CMT2	Compare Match Timer Constant Register	CMCOR	16	16	2, 3 PCLKB	2 ICLK		
0008 8018h	CMT3	Compare Match Timer Control Register	CMCR	16	16	2, 3 PCLKB	2 ICLK		
0008 801Ah	CMT3	Compare Match Timer Counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK		
0008 801Ch	CMT3	Compare Match Timer Constant Register	CMCOR	16	16	2, 3 PCLKB	2 ICLK		
0008 8020h	WDT	WDT Refresh Register	WDTRR	8	8	2, 3 PCLKB	2 ICLK	WDTA	
0008 8022h	WDT	WDT Control Register	WDTCR	16	16	2, 3 PCLKB	2 ICLK		
0008 8024h	WDT	WDT Status Register	WDTSR	16	16	2, 3 PCLKB	2 ICLK		
0008 8026h	WDT	WDT Reset Control Register	WDTRCR	8	8	2, 3 PCLKB	2 ICLK		
0008 8030h	IWDT	IWDT Refresh Register	IWDTRR	8	8	2, 3 PCLKB	2 ICLK	IWDTa	
0008 8032h	IWDT	IWDT Control Register	IWDTCR	16	16	2, 3 PCLKB	2 ICLK		
0008 8034h	IWDT	IWDT Status Register	IWDTSR	16	16	2, 3 PCLKB	2 ICLK		
0008 8036h	IWDT	IWDT Reset Control Register	IWDTRCR	8	8	2, 3 PCLKB	2 ICLK		
0008 8038h	IWDT	IWDT Count Stop Control Register	IWDTCSTPR	8	8	2, 3 PCLKB	2 ICLK		
0008 80C0h	DA	D/A Data Register 0	DADR0	16	16	2, 3 PCLKB	2 ICLK	DAa	Not present in versions with 64 or 48 pins.
0008 80C2h	DA	D/A Data Register 1	DADR1	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 80C4h	DA	D/A Control Register	DACR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 80C5h	DA	DADRm Format Select Register	DADPR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 80C6h	DA	D/A A/D Synchronous Start Control Register	DAADSCR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 8280h	CRC	CRC Control Register	CRCCR	8	8	2, 3 PCLKB	2 ICLK	CRC	
0008 8281h	CRC	CRC Data Input Register	CRCDIR	8	8	2, 3 PCLKB	2 ICLK		
0008 8282h	CRC	CRC Data Output Register	CRCDOR	16	16	2, 3 PCLKB	2 ICLK		
0008 8300h	RIIC0	I^2C Bus Control Register 1	ICCR1	8	8	2, 3 PCLKB	2 ICLK	RIIC	
0008 8301h	RIIC0	I^2C Bus Control Register 2	ICCR2	8	8	2, 3 PCLKB	2 ICLK		
0008 8302h	RIIC0	I^2C Bus Mode Register 1	ICMR1	8	8	2, 3 PCLKB	2 ICLK		
0008 8303h	RIIC0	I^2C Bus Mode Register 2	ICMR2	8	8	2, 3 PCLKB	2 ICLK		
0008 8304h	RIIC0	I^2C Bus Mode Register 3	ICMR3	8	8	2, 3 PCLKB	2 ICLK		
0008 8305h	RIIC0	I^2C Bus Function Enable Register	ICFER	8	8	2, 3 PCLKB	2 ICLK		
0008 8306h	RIIC0	I^2C Bus Status Enable Register	ICSER	8	8	2, 3 PCLKB	2 ICLK		
0008 8307h	RIIC0	I^2C Bus Interrupt Enable Register	ICIER	8	8	2, 3 PCLKB	2 ICLK		

Table 4.1 List of I/O Registers (Address Order) (30/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
000A 002Eh	USB0	D1FIFO Port Control Register	D1FIFOCTR	16	16	3, 4 PCLKB	2, 3 ICLK	USBa	Not present in versions with 112, 100, 64, or 48 pins.
000A 0030h	USB0	Interrupt Enable Register 0	INTENB0	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 0032h	USB0	Interrupt Enable Register 1	INTENB1	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 0036h	USB0	BRDY Interrupt Enable Register	BRDYENB	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 0038h	USB0	NRDY Interrupt Enable Register	NRDYENB	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 003Ah	USB0	BEMP Interrupt Enable Register	BEMPENB	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 003Ch	USB0	SOF Output Configuration Register	SOFCFG	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 0040h	USB0	Interrupt Status Register 0	INTSTS0	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 0042h	USB0	Interrupt Status Register 1	INTSTS1	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 0046h	USB0	BRDY Interrupt Status Register	BRDYSTS	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 0048h	USB0	NRDY Interrupt Status Register	NRDYSTS	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 004Ah	USB0	BEMP Interrupt Status Register	BEMPSTS	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.

Table 4.1 List of I/O Registers (Address Order) (32/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
000A 006Ch	USB0	Pipe Maximum Packet Size Register	PIPEMAXP	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1	USBa	Not present in versions with 112, 100, 64, or 48 pins.
000A 006Eh	USB0	Pipe Cycle Control Register	PIPEPERI	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 0070h	USB0	PIPE1 Control Register	PIPE1CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 0072h	USB0	PIPE2 Control Register	PIPE2CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 0074h	USB0	PIPE3 Control Register	PIPE3CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 0076h	USB0	PIPE4 Control Register	PIPE4CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 0078h	USB0	PIPE5 Control Register	PIPE5CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 007Ah	USB0	PIPE6 Control Register	PIPE6CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 007Ch	USB0	PIPE7 Control Register	PIPE7CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 007Eh	USB0	PIPE8 Control Register	PIPE8CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 0080h	USB0	PIPE9 Control Register	PIPE9CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 0090h	USB0	PIPE1 Transaction Counter Enable Register	PIPE1TRE	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.

Table 4.1 List of I/O Registers (Address Order) (36/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
000C 1A28h	MTU7	Timer General Register C	TGRC	16	16, 32	4, 5 PCLKA	2, 3 ICLK	MTU3	
000C 1A2Ah	MTU7	Timer General Register D	TGRD	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1A2Ch	MTU6	Timer Status Register	TSR	8	8, 16	4, 5 PCLKA	2, 3 ICLK		
000C 1A2Dh	MTU7	Timer Status Register	TSR	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1A30h	MTU	Timer Interrupt Skipping Set Register 1B	TITCR1B	8	8, 16	4, 5 PCLKA	2, 3 ICLK		
000C 1A31h	MTU	Timer Interrupt Skipping Counters 1B	TITCNT1B	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1A32h	MTU	Timer Buffer Transfer Set Register B	TBTERB	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1A34h	MTU	Timer Dead Time Enable Register B	TDERB	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1A36h	MTU	Timer Output Level Buffer Register B	TOLBRB	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1A38h	MTU6	Timer Buffer Operation Transfer Mode Register	TBTM	8	8, 16	4, 5 PCLKA	2, 3 ICLK		
000C 1A39h	MTU7	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1A3Ah	MTU	Timer Interrupt Skipping Mode Register B	TITMRB	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1A3Bh	MTU	Timer Interrupt Skipping Set Register 2B	TITCR2B	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1A3Ch	MTU	Timer Interrupt Skipping Counters 2B	TITCNT2B	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1A40h	MTU7	Timer A/D Converter Start Request Control Register	TADCR	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1A44h	MTU7	Timer A/D Converter Start Request Cycle Set Register A	TADCORA	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1A46h	MTU7	Timer A/D Converter Start Request Cycle Set Register B	TADCORB	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1A48h	MTU7	Timer A/D Converter Start Request Cycle Set Buffer Register A	TADCOBRA	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1A4Ah	MTU7	Timer A/D Converter Start Request Cycle Set Buffer Register B	TADCOBRB	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1A50h	MTU	Timer Synchronous Clear Register	TSYCR	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1A60h	MTU	Timer Waveform Control Register B	TWCRB	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1A70h	MTU	Timer Mode Register 2B	TMDR2B	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1A72h	MTU6	Timer General Register E	TGRE	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1A74h	MTU7	Timer General Register E	TGRE	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1A76h	MTU7	Timer General Register F	TGRF	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1A80h	MTU	Timer Start Register B	TSTRB	8	8, 16	4, 5 PCLKA	2, 3 ICLK		
000C 1A81h	MTU	Timer Synchronous Register B	TSYRB	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1A84h	MTU	Timer Read/Write Enable Register B	TRWERB	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1C80h	MTU5	Timer Counter U	TCNTU	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1C82h	MTU5	Timer General Register U	TGRU	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1C84h	MTU5	Timer Control Register U	TCRU	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1C86h	MTU5	Timer I/O Control Register U	TIORU	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1C90h	MTU5	Timer Counter V	TCNTV	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1C92h	MTU5	Timer General Register V	TGRV	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1C94h	MTU5	Timer Control Register V	TCRV	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1C96h	MTU5	Timer I/O Control Register V	TIORV	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1CA0h	MTU5	Timer Counter W	TCNTW	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1CA2h	MTU5	Timer General Register W	TGRW	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1CA4h	MTU5	Timer Control Register W	TCRW	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1CA6h	MTU5	Timer I/O Control Register W	TIORW	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1CB0h	MTU5	Timer Status Register	TSR	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1CB2h	MTU5	Timer Interrupt Enable Register	TIER	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1CB4h	MTU5	Timer Start Register	TSTR	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1CB6h	MTU5	Timer Compare Match Clear Register	TCNTCMPCLR	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 2000h	GPT	General PWM Timer Software Start Register	GTSTR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK	GPT	
000C 2004h	GPT	General PWM Timer Hardware Source Start Control Register	GTHSCR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		

Table 4.1 List of I/O Registers (Address Order) (39/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
000C 21A6h	GPT1	A/D Converter Start Request Timing Buffer Register A	GTADTBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK	GPT	
000C 21A8h	GPT1	A/D Converter Start Request Timing Double-Buffer Register A	GTADTDBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 21ACh	GPT1	A/D Converter Start Request Timing Register B	GTADTRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 21AEh	GPT1	A/D Converter Start Request Timing Buffer Register B	GTADTBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 21B0h	GPT1	A/D Converter Start Request Timing Double-Buffer Register B	GTADTDBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 21B4h	GPT1	General PWM Timer Output Negate Control Register	GTONCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 21B6h	GPT1	General PWM Timer Dead Time Control Register	GTDTCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 21B8h	GPT1	General PWM Timer Dead Time Value Register U	GTDVU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 21BAh	GPT1	General PWM Timer Dead Time Value Register D	GTDVD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 21BCh	GPT1	General PWM Timer Dead Time Buffer Register U	GTDBU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 21BEh	GPT1	General PWM Timer Dead Time Buffer Register D	GTDBD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 21C0h	GPT1	General PWM Timer Output Protection Function Status Register	GTSOS	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 21C2h	GPT1	General PWM Timer Output Protection Function Temporary Release Register	GTSOTR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2200h	GPT2	General PWM Timer I/O Control Register	GTIOR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2202h	GPT2	General PWM Timer Interrupt Output Setting Register	GTINTAD	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2204h	GPT2	General PWM Timer Control Register	GTCR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2206h	GPT2	General PWM Timer Buffer Enable Register	GTBER	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2208h	GPT2	General PWM Timer Count Direction Register	GTUDC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 220Ah	GPT2	General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register	GTITC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 220Ch	GPT2	General PWM Timer Status Register	GTST	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 220Eh	GPT2	General PWM Timer Counter	GTCNT	16	16	2 to 5 PCLKA	2, 3 ICLK		
000C 2210h	GPT2	General PWM Timer Compare Capture Register A	GTCCRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2212h	GPT2	General PWM Timer Compare Capture Register B	GTCCRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2214h	GPT2	General PWM Timer Compare Capture Register C	GTCCRC	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2216h	GPT2	General PWM Timer Compare Capture Register D	GTCCRD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2218h	GPT2	General PWM Timer Compare Capture Register E	GTCCRE	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 221Ah	GPT2	General PWM Timer Compare Capture Register F	GTCCRF	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 221Ch	GPT2	General PWM Timer Cycle Setting Register	GTPR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 221Eh	GPT2	General PWM Timer Cycle Setting Buffer Register	GTPBR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2220h	GPT2	General PWM Timer Cycle Setting Double-Buffer Register	GTPDBR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2224h	GPT2	A/D Converter Start Request Timing Register A	GTADTRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2226h	GPT2	A/D Converter Start Request Timing Buffer Register A	GTADTBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2228h	GPT2	A/D Converter Start Request Timing Double-Buffer Register A	GTADTDBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 222Ch	GPT2	A/D Converter Start Request Timing Register B	GTADTRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 222Eh	GPT2	A/D Converter Start Request Timing Buffer Register B	GTADTBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		

Table 4.1 List of I/O Registers (Address Order) (42/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
000C 2884h	GPTB	LOCO Count Value Register	LCNT	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK	GPT	Not present in versions with 64, or 48 pins.
000C 2886h	GPTB	LOCO Count Result Average Register	LCNTA	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64, or 48 pins.
000C 2888h	GPTB	LOCO Count Result Register 0	LCNT00	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64, or 48 pins.
000C 288Ah	GPTB	LOCO Count Result Register 1	LCNT01	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64, or 48 pins.
000C 288Ch	GPTB	LOCO Count Result Register 2	LCNT02	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 288Eh	GPTB	LOCO Count Result Register 3	LCNT03	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2890h	GPTB	LOCO Count Result Register 4	LCNT04	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2892h	GPTB	LOCO Count Result Register 5	LCNT05	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2894h	GPTB	LOCO Count Result Register 6	LCNT06	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2896h	GPTB	LOCO Count Result Register 7	LCNT07	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2898h	GPTB	LOCO Count Result Register 8	LCNT08	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 289Ah	GPTB	LOCO Count Result Register 9	LCNT09	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 289Ch	GPTB	LOCO Count Result Register 10	LCNT10	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 289Eh	GPTB	LOCO Count Result Register 11	LCNT11	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 28A0h	GPTB	LOCO Count Result Register 12	LCNT12	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 28A2h	GPTB	LOCO Count Result Register 13	LCNT13	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 28A4h	GPTB	LOCO Count Result Register 14	LCNT14	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 28A6h	GPTB	LOCO Count Result Register 15	LCNT15	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 28A8h	GPTB	LOCO Count Upper Permissible Deviation Register	LCNTDU	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 28AAh	GPTB	LOCO Count Lower Permissible Deviation Register	LCNTDL	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2900h	GPT4	General PWM Timer I/O Control Register	GTIOR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2902h	GPT4	General PWM Timer Interrupt Output Setting Register	GTINTAD	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2904h	GPT4	General PWM Timer Control Register	GTCR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2906h	GPT4	General PWM Timer Buffer Enable Register	GTBER	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2908h	GPT4	General PWM Timer Count Direction Register	GTUDC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 290Ah	GPT4	General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register	GTITC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 290Ch	GPT4	General PWM Timer Status Register	GTST	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 290Eh	GPT4	General PWM Timer Counter	GTCNT	16	16	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2910h	GPT4	General PWM Timer Compare Capture Register A	GTCCRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2912h	GPT4	General PWM Timer Compare Capture Register B	GTCCRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2914h	GPT4	General PWM Timer Compare Capture Register C	GTCCRC	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2916h	GPT4	General PWM Timer Compare Capture Register D	GTCCRD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2918h	GPT4	General PWM Timer Compare Capture Register E	GTCCRE	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.

Table 4.1 List of I/O Registers (Address Order) (43/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
000C 291Ah	GPT4	General PWM Timer Compare Capture Register F	GTCCRF	16	16, 32	2 to 5 PCLKA	2, 3 ICLK	GPT	Not present in versions with 64 or 48 pins.
000C 291Ch	GPT4	General PWM Timer Cycle Setting Register	GTPR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 291Eh	GPT4	General PWM Timer Cycle Setting Buffer Register	GTPBR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2920h	GPT4	General PWM Timer Cycle Setting Double-Buffer Register	GTPDBR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2924h	GPT4	A/D Converter Start Request Timing Register A	GTADTRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2926h	GPT4	A/D Converter Start Request Timing Buffer Register A	GTADTBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2928h	GPT4	A/D Converter Start Request Timing Double-Buffer Register A	GTADTDBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 292Ch	GPT4	A/D Converter Start Request Timing Register B	GTADTRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 292Eh	GPT4	A/D Converter Start Request Timing Buffer Register B	GTADTBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2930h	GPT4	A/D Converter Start Request Timing Double-Buffer Register B	GTADTDBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2934h	GPT4	General PWM Timer Output Negate Control Register	GTONCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2936h	GPT4	General PWM Timer Dead Time Control Register	GTDTCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2938h	GPT4	General PWM Timer Dead Time Value Register U	GTDVU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 293Ah	GPT4	General PWM Timer Dead Time Value Register D	GTDVD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 293Ch	GPT4	General PWM Timer Dead Time Buffer Register U	GTDBU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 293Eh	GPT4	General PWM Timer Dead Time Buffer Register D	GTDBD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2940h	GPT4	General PWM Timer Output Protection Function Status Register	GTSOS	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2942h	GPT4	General PWM Timer Output Protection Function Temporary Release Register	GTSOTR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2980h	GPT5	General PWM Timer I/O Control Register	GTIOR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2982h	GPT5	General PWM Timer Interrupt Output Setting Register	GTINTAD	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2984h	GPT5	General PWM Timer Control Register	GTCR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2986h	GPT5	General PWM Timer Buffer Enable Register	GTBER	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2988h	GPT5	General PWM Timer Count Direction Register	GTUDC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 298Ah	GPT5	General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register	GTITC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 298Ch	GPT5	General PWM Timer Status Register	GTST	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 298Eh	GPT5	General PWM Timer Counter	GTCNT	16	16	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2990h	GPT5	General PWM Timer Compare Capture Register A	GTCCRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2992h	GPT5	General PWM Timer Compare Capture Register B	GTCCRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2994h	GPT5	General PWM Timer Compare Capture Register C	GTCCRC	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2996h	GPT5	General PWM Timer Compare Capture Register D	GTCCRD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2998h	GPT5	General PWM Timer Compare Capture Register E	GTCCRE	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 299Ah	GPT5	General PWM Timer Compare Capture Register F	GTCCRF	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 299Ch	GPT5	General PWM Timer Cycle Setting Register	GTPR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.

Table 4.1 List of I/O Registers (Address Order) (44/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
000C 299Eh	GPT5	General PWM Timer Cycle Setting Buffer Register	GTPBR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK	GPT	Not present in versions with 64 or 48 pins.
000C 29A0h	GPT5	General PWM Timer Cycle Setting Double-Buffer Register	GTPDBR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 29A4h	GPT5	A/D Converter Start Request Timing Register A	GTADTRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 29A6h	GPT5	A/D Converter Start Request Timing Buffer Register A	GTADTBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 29A8h	GPT5	A/D Converter Start Request Timing Double-Buffer Register A	GTADTDBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 29ACh	GPT5	A/D Converter Start Request Timing Register B	GTADTRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 29AEh	GPT5	A/D Converter Start Request Timing Buffer Register B	GTADTBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 29B0h	GPT5	A/D Converter Start Request Timing Double-Buffer Register B	GTADTDBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 29B4h	GPT5	General PWM Timer Output Negate Control Register	GTONCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 29B6h	GPT5	General PWM Timer Dead Time Control Register	GTDTCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 29B8h	GPT5	General PWM Timer Dead Time Value Register U	GTDVU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 29BAh	GPT5	General PWM Timer Dead Time Value Register D	GTDVD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 29BCh	GPT5	General PWM Timer Dead Time Buffer Register U	GTDBU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 29BEh	GPT5	General PWM Timer Dead Time Buffer Register D	GTDBD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 29C0h	GPT5	General PWM Timer Output Protection Function Status Register	GTSOS	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 29C2h	GPT5	General PWM Timer Output Protection Function Temporary Release Register	GTSOTR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A00h	GPT6	General PWM Timer I/O Control Register	GTIOR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A02h	GPT6	General PWM Timer Interrupt Output Setting Register	GTINTAD	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A04h	GPT6	General PWM Timer Control Register	GTCR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A06h	GPT6	General PWM Timer Buffer Enable Register	GTBER	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A08h	GPT6	General PWM Timer Count Direction Register	GTUDC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A0Ah	GPT6	General PWM Timer Interrupt, A/D Converter Start Request Skipping Setting Register	GTITC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A0Ch	GPT6	General PWM Timer Status Register	GTST	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A0Eh	GPT6	General PWM Timer Counter	GTCNT	16	16	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A10h	GPT6	General PWM Timer Compare Capture Register A	GTCCRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A12h	GPT6	General PWM Timer Compare Capture Register B	GTCCRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A14h	GPT6	General PWM Timer Compare Capture Register C	GTCCRC	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A16h	GPT6	General PWM Timer Compare Capture Register D	GTCCRD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A18h	GPT6	General PWM Timer Compare Capture Register E	GTCCRE	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A1Ah	GPT6	General PWM Timer Compare Capture Register F	GTCCRF	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A1Ch	GPT6	General PWM Timer Cycle Setting Register	GTPR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A1Eh	GPT6	General PWM Timer Cycle Setting Buffer Register	GTPBR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A20h	GPT6	General PWM Timer Cycle Setting Double-Buffer Register	GTPDBR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.

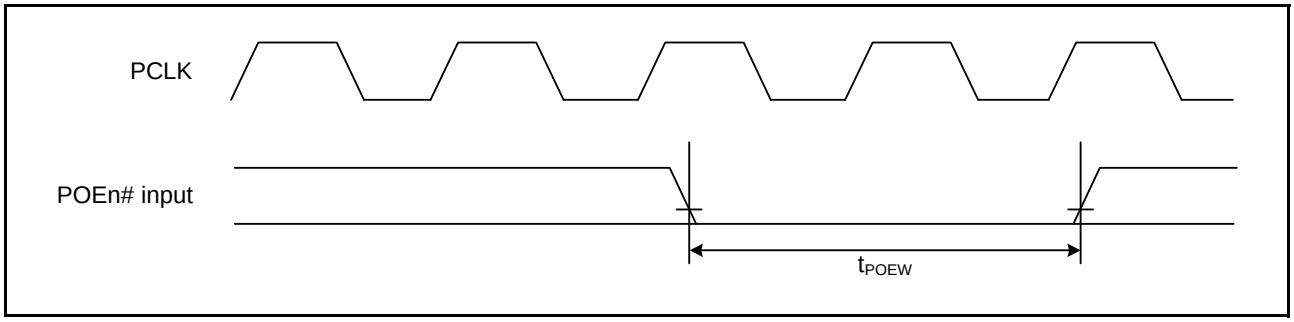

Figure 5.25 POE3# Input Timing

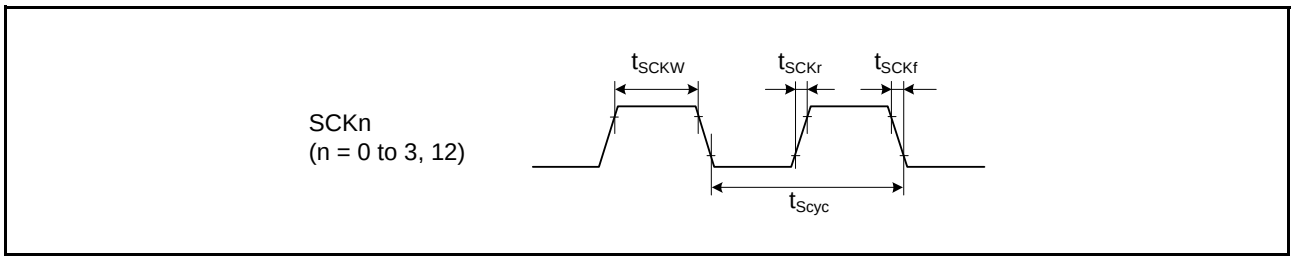

Figure 5.26 SCK Clock Input Timing

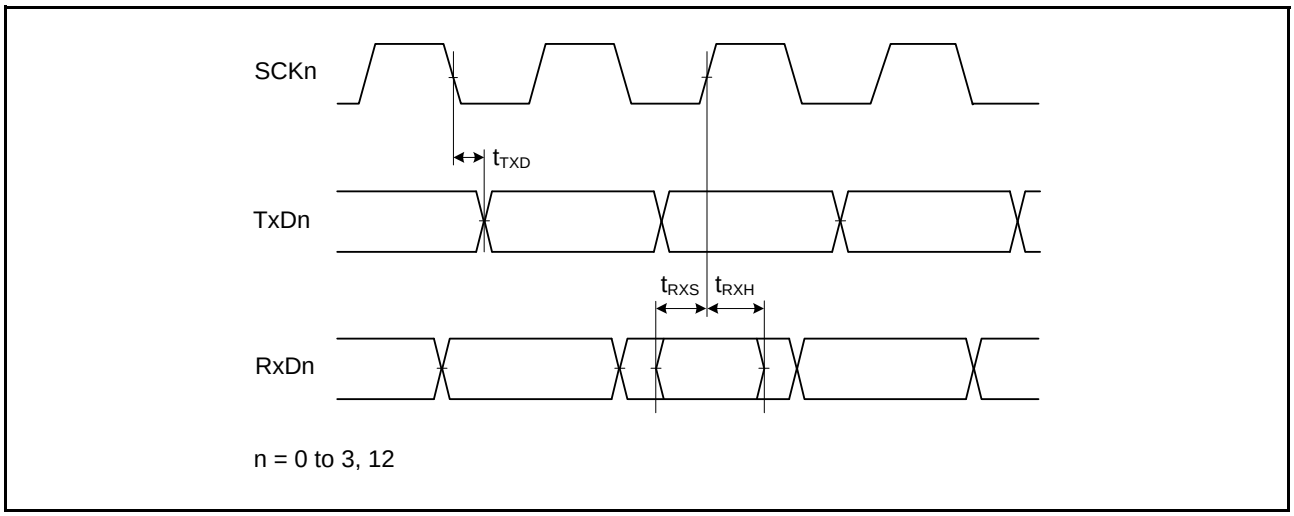

Figure 5.27 SCI Input/Output Timing: Clock Synchronous Mode

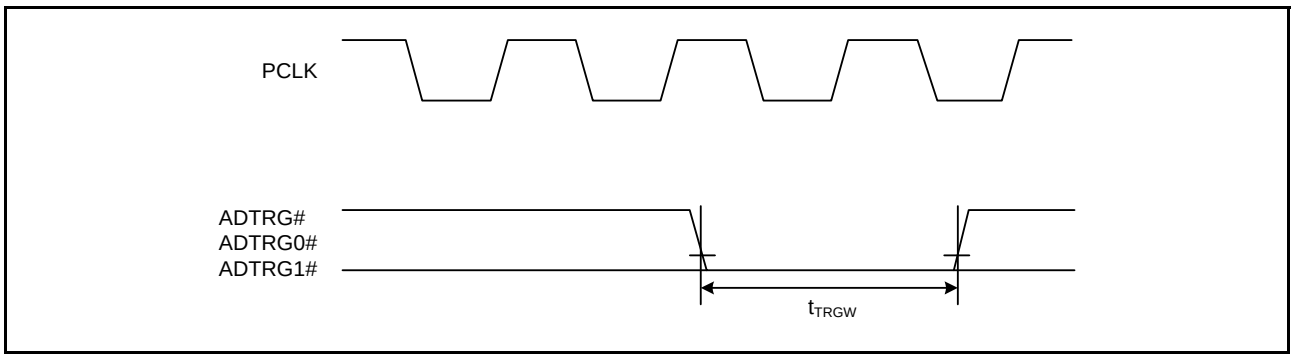

Figure 5.28 AD Converter External Trigger Input Timing

Table 5.24 Comparator Characteristics

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Analog input capacitance	C_{in}	—	—	8	pF	
REFH pin offset voltage	V_{off}	—	—	5	mV	
REFL pin offset voltage		—	—	5	mV	
REFH input voltage range	V_{in}	1.7	—	AVcc – 0.3	V	
REFL input voltage range		0.3	—	AVcc – 1.7	V	
REFH reply time	t_{CR}	—	—	500	ns	VI = VREF±25mV
REFL reply time	t_{CF}	—	—	500	ns	

Table 6.12 Timing of On-Chip Peripheral Modules (2)

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
RSPI	RSPCK clock cycle	Master	t_{SPcyc}	2	4096	t_{Pcyc}	Figure 6.20
		Slave		8	4096		
	RSPCK clock high pulse width	Master	t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2 - 3$	—	ns	
		Slave		$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2$	—		
	RSPCK clock low pulse width	Master	t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2 - 3$	—	ns	
		Slave		$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2$	—		
	RSPCK clock rise/fall time	Output	t_{SPCKR}, t_{SPCKF}	—	5	ns	
		Input		—	1	µs	
	Data input setup time	Master	t_{SU}	15	—	ns	Figure 6.21 to Figure 6.24
				20	—		
		Slave		$20 - t_{Pcyc}$	—		
	Data input hold time	Master	t_H	0	—	ns	
		Slave		$20 + 2 \times t_{Pcyc}$	—		
	SSL setup time	Master	t_{LEAD}	1	8	t_{SPcyc}	
		Slave		4	—	t_{Pcyc}	
	SSL hold time	Master	t_{LAG}	1	8	t_{SPcyc}	
		Slave		4	—	t_{Pcyc}	
	Data output delay time	Master	t_{OD}	—	18	ns	
		Slave		—	$3 \times t_{Pcyc} + 40$		
	Data output hold time	Master	t_{OH}	0	—	ns	
		Slave		0	—		
	Successive transmission delay time	Master	t_{TD}	$t_{SPcyc} + 2 \times t_{Pcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	ns	
		Slave		$4 \times t_{Pcyc}$	—		
	MOSI rise/fall time	Output	t_{MODR}, t_{MODF}	—	5	ns	
		Input		—	1	µs	
	MISO rise/fall time	Output	t_{MODR}, t_{MODF}	—	5	ns	
		Input		—	1	µs	
	SSL rise/fall time	Output	t_{SSLr}, t_{SSLf}	—	15	ns	
		Input		—	1	µs	
	Slave access time		t_{SA}	—	4	t_{Pcyc}	Figure 6.23 and Figure 6.24
	Slave output release time		t_{REL}	—	3	t_{Pcyc}	

Note 1. t_{Pcyc}: PCLK cycle

Rev.	Date	Description	
		Page	Summary
2.10	Sep 26, 2013	36 to 39	Table 1.7 List of Pins and Pin Functions (112-Pin LQFP), changed
		40 to 42	Table 1.8 List of Pins and Pin Functions (100-Pin LQFP), changed
		43 to 45	Table 1.9 List of Pins and Pin Functions (64-Pin LQFP), changed
		46 to 47	Table 1.10 List of Pins and Pin Functions (48-Pin LQFP), changed
		4. I/O Registers	
		56 to 103	Table 4.1 List of I/O Registers (Address Order), changed
		5. Electrical Characteristics [144-, 120-, 112- and 100-Pin Versions]	
		104	Table 5.1 Absolute Maximum Ratings, changed
		107	Table 5.4 DC Characteristics (3), Note 7, deleted
		108	Table 5.6 Permissible Power Consumption, added
		128	5.3.7 Timing of PWM Delay Generation Circuit, added
		128	Table 42.21 Timing of the PWM Delay Generation Circuit, added
		132	Figure 5.32 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKB Division Ratio Set to a Value Other Than 1/2) and Simple SPI Timing (Master, CKPH = 1), changed
		133	Figure 5.34 RSPI Timing (Slave, CPHA = 0) and Simple SPI Timing (Slave, CKPH = 0), changed
		134	Figure 5.35 RSPI Timing (Slave, CPHA = 1) and Simple SPI Timing (Slave, CKPH = 1), changed
		6. Electrical Characteristics [64- and 48-Pin Versions]	
		149	Table 6.1 Absolute Maximum Ratings, changed
		151	Table 6.3 DC Characteristics (2), Note 3, changed
		152	Table 6.5 Permissible Power Consumption, added

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   ¾ The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   ¾ The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   ¾ The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   ¾ When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   ¾ The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.