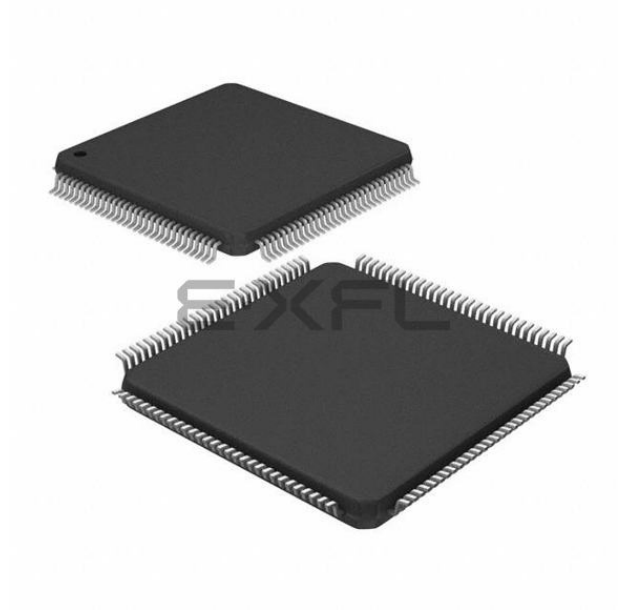
Renesas Electronics America Inc - R5F563TBDDFA#V0 Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	EBI/EMI, I²C, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	72
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x10b, 8x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	120-LQFP
Supplier Device Package	120-LQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f563tbddfa-v0

Table 1.1 Outline of Specifications (3/7)

Classification	Module/Function	Description
I/O ports	General I/O ports	• 144-pin LQFP I/O pins: 81 Input pins: 29 Open-drain outputs: 27 • 120-pin LQFP I/O pins: 72 Input pin: 21 Open-drain outputs: 26 • 112-pin LQFP I/O pins: 69 Input pins: 21 Open-drain outputs: 20 • 100-pin LQFP I/O pins: 57 Input pins: 21 Open-drain outputs: 16 • 64-pin LQFP I/O pins: 39 Input pins: 9 Open-drain outputs: 10 5-V tolerance: 39 • 48-pin LQFP I/O pins: 25 Input pins: 7 Open-drain outputs: 8 5-V tolerance: 25
Timers	Multi-function timer pulse unit 3 (MTU3)	• (16 bits × 8 channels) • Maximum of 16 pulse-input/output and 3 pulse-input possible • Select eight clocks from among ten count clocks (PCLKA/1, PCLKA/4, PCLKA/16, PCLKA/64, PCLKA/256, PCLKA/1024, MTCLKA, MTCLKB, MTCLKC, and MTCLKD) for each channel (seven clocks for channel 1, four clocks for channel 5, and six clocks for channel 6 or 7) • 24 output compare/input capture registers • Counter-clearing operation (simultaneous clearing on compare match or input capture) • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous input and output to registers in synchronization with counter operations • Buffer operation specifiable • Capable of cascade-connected operation • Interrupts: 38 sources • Automatic transfer of register data • Pulse output modes Topple, PWM, complementary PWM, and reset-synchronous PWM modes • Complementary PWM output mode Outputs non-overlapping waveforms for controlling 3-phase inverters Automatic specification of dead times PWM duty cycle: Selectable as any value from 0% to 100% Delay can be applied to requests for A/D conversion. Non-generation of interrupt requests at peak or trough values of counters can be selected. Double buffering • Reset-synchronous PWM mode Three PWM waveforms and corresponding inverse waveforms are output with the desired duty cycles. • Phase-counting mode • Counter functionality for dead-time compensation • Generation of triggers for A/D converters • Differential timing for initiation of A/D conversion
	Port output enable 3 (POE3)	• Control of the high-impedance state of the MTU3 and GPT's waveform output pins • Six pins for input from signal sources: POE0, POE4, POE8, POE10, POE11, and POE12 • Initiation on detection of short-circuited outputs (detection of PWM outputs having simultaneously become an active level.) • Initiation by comparator-detection, oscillation-stoppage detection, or software • Software control of the states of pins for output control can also be added.

Table 1.9 List of Pins and Pin Functions (64-Pin LQFP) (2/3)

Pin Number 64-Pin LQFP	Power Supply Clock System Control	I/O Port	POE3	Timer (MTU3, GPT, CAC)	Communications (SCIc, SCId)	Communications (RSPI, RIIC)	Interrupt	S12ADB
27		PA3		MTIOC2A		SSLA0		
28		PA2		MTIOC2B		SSLA1		
29		P94			TXD1 SMOSI1 SSDA1			
30		P93			RXD1 SMISO1 SSCL1		IRQ1	
31		P92			SCK1			
32		P91			CTS1# RTS1# SS1#			
33		P76		MTIOC4D GTIOC2B MTIOC7D				
34		P75		MTIOC4C GTIOC1B MTIOC7C				
35		P74		MTIOC3D GTIOC0B MTIOC6D				
36		P73		MTIOC4B GTIOC2A MTIOC7B				
37		P72		MTIOC4A GTIOC1A MTIOC7A				
38		P71		MTIOC3B GTIOC0A MTIOC6B				
39		P70	POE0#		CTS1# RTS1# SS1#		IRQ5-DS	
40		P33		MTIOC3A MTIOC6A		SSLA3		
41		P32		MTIOC3C MTIOC6C		SSLA2		
42	VCC							
43		P31		MTIOC0A		SSLA1		
44	VSS							
45		P30		MTIOC0B MTCLKD	TXD0 SMOSI0 SSDA0	SSLA0		
46		P24		MTIC5U MTCLKC	RXD0 SMISO0 SSCL0	RSPCKA		
47		P23		MTIC5V MTCLKB CACREF	SCK0	MOSIA		
48		P22		MTIC5W MTCLKA	CTS0# RTS0# SS0#	MISOA		
49		P47						AN007 CVREFH

- Longword-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.L  #SFR_DATA, [R1]
CMP    [R1].L, R1
;; Next process
```

If multiple registers are written to and a subsequent instruction should be executed after the write operations are entirely completed, only read the I/O register that was last written to and execute the operation using the value; it is not necessary to read or execute operation for all the registers that were written to.

(3) Number of Access Cycles to I/O Registers

For the number of I/O register access cycles, refer to Table 4.1, List of I/O Registers (Address Order).
The number of access cycles to I/O registers is obtained by following equation.*1

Number of access cycles to I/O registers = Number of bus cycles for internal main bus 1 +
Number of divided clock synchronization cycles +
Number of bus cycles for internal peripheral bus 1 to 6

The number of bus cycles of internal peripheral bus 1 to 6 differs according to the register to be accessed.
When peripheral functions connected to internal peripheral bus 2 to 6 are accessed, the number of divided clock synchronization cycles is added.
The number of divided clock synchronization cycles differs depending on the frequency ratio between ICLK and PCLK (or FCLK, BCLK) or bus access timing.
In the peripheral function unit, when the frequency ratio of ICLK is equal to or greater than that of PCLK (or FCLK), the sum of the number of bus cycles for internal main bus 1 and the number of the divided clock synchronization cycles will be one cycle of PCLK (or FCLK) at a maximum. Therefore, one PCLK (or FCLK) has been added to the number of access states shown in Table 4.1.
When the frequency ratio of ICLK is lower than that of PCLK (or FCLK), the subsequent bus access is started from the ICLK cycle following the completion of the access to the peripheral functions. Therefore, the access cycles are described on an ICLK basis.
In the external bus control unit, the sum of the number of bus cycles for internal main bus 1 and the number of divided clock synchronization cycles will be one cycle of BCLK at a maximum. Therefore, one BCLK is added to the number of access cycles shown in Table 4.1.

Note 1. This applies to the number of cycles when the access from the CPU does not conflict with the instruction fetching to the external memory or bus access from the different bus master (DMAC or DTC).

(4) Note on Sleep Mode and Mode Transition

During sleep mode or a mode transition, do not write to the system control related registers (indicated by 'SYSTEM' in the Module Symbol column in Table 4.1, List of I/O Registers (Address Order)).

Table 4.1 List of I/O Registers (Address Order) (4/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 7010h	ICU	Interrupt Request Register 016	IR016	8	8	2 ICLK		ICUb	
0008 7015h	ICU	Interrupt Request Register 021	IR021	8	8	2 ICLK			
0008 7017h	ICU	Interrupt Request Register 023	IR023	8	8	2 ICLK			
0008 701Bh	ICU	Interrupt Request Register 027	IR027	8	8	2 ICLK			
0008 701Ch	ICU	Interrupt Request Register 028	IR028	8	8	2 ICLK			
0008 701Dh	ICU	Interrupt Request Register 029	IR029	8	8	2 ICLK			
0008 701Eh	ICU	Interrupt Request Register 030	IR030	8	8	2 ICLK			
0008 701Fh	ICU	Interrupt Request Register 031	IR031	8	8	2 ICLK			
0008 7021h	ICU	Interrupt Request Register 033	IR033	8	8	2 ICLK			Not present in versions with 112, 100, 64 or 48 pins.
0008 7022h	ICU	Interrupt Request Register 034	IR034	8	8	2 ICLK			Not present in versions with 112, 100, 64 or 48 pins.
0008 7023h	ICU	Interrupt Request Register 035	IR035	8	8	2 ICLK			Not present in versions with 112, 100, 64 or 48 pins.
0008 7024h	ICU	Interrupt Request Register 036	IR036	8	8	2 ICLK			
0008 7025h	ICU	Interrupt Request Register 037	IR037	8	8	2 ICLK			
0008 7026h	ICU	Interrupt Request Register 038	IR038	8	8	2 ICLK			
0008 7027h	ICU	Interrupt Request Register 039	IR039	8	8	2 ICLK			
0008 7028h	ICU	Interrupt Request Register 040	IR040	8	8	2 ICLK			
0008 7029h	ICU	Interrupt Request Register 041	IR041	8	8	2 ICLK			
0008 702Ah	ICU	Interrupt Request Register 042	IR042	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 702Bh	ICU	Interrupt Request Register 043	IR043	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 702Ch	ICU	Interrupt Request Register 044	IR044	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 702Dh	ICU	Interrupt Request Register 045	IR045	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 702Eh	ICU	Interrupt Request Register 046	IR046	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 702Fh	ICU	Interrupt Request Register 047	IR047	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7030h	ICU	Interrupt Request Register 048	IR048	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7031h	ICU	Interrupt Request Register 049	IR049	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7032h	ICU	Interrupt Request Register 050	IR050	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7033h	ICU	Interrupt Request Register 051	IR051	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7034h	ICU	Interrupt Request Register 052	IR052	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7035h	ICU	Interrupt Request Register 053	IR053	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7036h	ICU	Interrupt Request Register 054	IR054	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7037h	ICU	Interrupt Request Register 055	IR055	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7038h	ICU	Interrupt Request Register 056	IR056	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7039h	ICU	Interrupt Request Register 057	IR057	8	8	2 ICLK			
0008 703Ah	ICU	Interrupt Request Register 058	IR058	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 703Bh	ICU	Interrupt Request Register 059	IR059	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 703Ch	ICU	Interrupt Request Register 060	IR060	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 703Dh	ICU	Interrupt Request Register 061	IR061	8	8	2 ICLK			Not present in versions with 64 or 48 pins.

Table 4.1 List of I/O Registers (Address Order) (11/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 7206h	ICU	Interrupt Request Enable Register 06	IER06	8	8	2 ICLK		ICUb	Not present in versions with 64 or 48 pins.
0008 7207h	ICU	Interrupt Request Enable Register 07	IER07	8	8	2 ICLK			
0008 7208h	ICU	Interrupt Request Enable Register 08	IER08	8	8	2 ICLK			
0008 720Bh	ICU	Interrupt Request Enable Register 0B	IER0B	8	8	2 ICLK			Not present in versions with 112, 100, 64 or 48 pins.
0008 720Ch	ICU	Interrupt Request Enable Register 0C	IER0C	8	8	2 ICLK			
0008 720Dh	ICU	Interrupt Request Enable Register 0D	IER0D	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 720Eh	ICU	Interrupt Request Enable Register 0E	IER0E	8	8	2 ICLK			
0008 720Fh	ICU	Interrupt Request Enable Register 0F	IER0F	8	8	2 ICLK			
0008 7210h	ICU	Interrupt Request Enable Register 10	IER10	8	8	2 ICLK			
0008 7211h	ICU	Interrupt Request Enable Register 11	IER11	8	8	2 ICLK			
0008 7212h	ICU	Interrupt Request Enable Register 12	IER12	8	8	2 ICLK			
0008 7213h	ICU	Interrupt Request Enable Register 13	IER13	8	8	2 ICLK			
0008 7214h	ICU	Interrupt Request Enable Register 14	IER14	8	8	2 ICLK			
0008 7215h	ICU	Interrupt Request Enable Register 15	IER15	8	8	2 ICLK			
0008 7216h	ICU	Interrupt Request Enable Register 16	IER16	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7217h	ICU	Interrupt Request Enable Register 17	IER17	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7218h	ICU	Interrupt Request Enable Register 18	IER18	8	8	2 ICLK			
0008 7219h	ICU	Interrupt Request Enable Register 19	IER19	8	8	2 ICLK			
0008 721Ah	ICU	Interrupt Request Enable Register 1A	IER1A	8	8	2 ICLK			
0008 721Bh	ICU	Interrupt Request Enable Register 1B	IER1B	8	8	2 ICLK			
0008 721Ch	ICU	Interrupt Request Enable Register 1C	IER1C	8	8	2 ICLK			
0008 721Dh	ICU	Interrupt Request Enable Register 1D	IER1D	8	8	2 ICLK			
0008 721Eh	ICU	Interrupt Request Enable Register 1E	IER1E	8	8	2 ICLK			
0008 721Fh	ICU	Interrupt Request Enable Register 1F	IER1F	8	8	2 ICLK			
0008 72E0h	ICU	Software Interrupt Activation Register	SWINTR	8	8	2 ICLK			
0008 72F0h	ICU	Fast Interrupt Set Register	FIR	16	16	2 ICLK			
0008 7300h	ICU	Interrupt Source Priority Register 000	IPR000	8	8	2 ICLK			
0008 7301h	ICU	Interrupt Source Priority Register 001	IPR001	8	8	2 ICLK			
0008 7302h	ICU	Interrupt Source Priority Register 002	IPR002	8	8	2 ICLK			
0008 7303h	ICU	Interrupt Source Priority Register 003	IPR003	8	8	2 ICLK			
0008 7304h	ICU	Interrupt Source Priority Register 004	IPR004	8	8	2 ICLK			
0008 7305h	ICU	Interrupt Source Priority Register 005	IPR005	8	8	2 ICLK			
0008 7306h	ICU	Interrupt Source Priority Register 006	IPR006	8	8	2 ICLK			
0008 7307h	ICU	Interrupt Source Priority Register 007	IPR007	8	8	2 ICLK			
0008 7321h	ICU	Interrupt Source Priority Register 033	IPR033	8	8	2 ICLK			Not present in versions with 112, 100, 64 or 48 pins.
0008 7322h	ICU	Interrupt Source Priority Register 034	IPR034	8	8	2 ICLK			Not present in versions with 112, 100, 64 or 48 pins.
0008 7323h	ICU	Interrupt Source Priority Register 035	IPR035	8	8	2 ICLK			Not present in versions with 112, 100, 64 or 48 pins.
0008 7324h	ICU	Interrupt Source Priority Register 036	IPR036	8	8	2 ICLK			
0008 7327h	ICU	Interrupt Source Priority Register 039	IPR039	8	8	2 ICLK			
0008 7328h	ICU	Interrupt Source Priority Register 040	IPR040	8	8	2 ICLK			
0008 7329h	ICU	Interrupt Source Priority Register 041	IPR041	8	8	2 ICLK			
0008 732Ah	ICU	Interrupt Source Priority Register 042	IPR042	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 732B	ICU	Interrupt Source Priority Register 043	IPR043	8	8	2 ICLK			Not present in versions with 64 or 48 pins.

Table 4.1 List of I/O Registers (Address Order) (32/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
000A 006Ch	USB0	Pipe Maximum Packet Size Register	PIPEMAXP	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1	USBa	Not present in versions with 112, 100, 64, or 48 pins.
000A 006Eh	USB0	Pipe Cycle Control Register	PIPEPERI	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 0070h	USB0	PIPE1 Control Register	PIPE1CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 0072h	USB0	PIPE2 Control Register	PIPE2CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 0074h	USB0	PIPE3 Control Register	PIPE3CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 0076h	USB0	PIPE4 Control Register	PIPE4CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 0078h	USB0	PIPE5 Control Register	PIPE5CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 007Ah	USB0	PIPE6 Control Register	PIPE6CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 007Ch	USB0	PIPE7 Control Register	PIPE7CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 007Eh	USB0	PIPE8 Control Register	PIPE8CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 0080h	USB0	PIPE9 Control Register	PIPE9CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 0090h	USB0	PIPE1 Transaction Counter Enable Register	PIPE1TRE	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.

Table 4.1 List of I/O Registers (Address Order) (40/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
000C 2230h	GPT2	A/D Converter Start Request Timing Double-Buffer Register B	GTADTDBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK	GPT	
000C 2234h	GPT2	General PWM Timer Output Negate Control Register	GTONCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2236h	GPT2	General PWM Timer Dead Time Control Register	GTDTCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2238h	GPT2	General PWM Timer Dead Time Value Register U	GTDVU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 223Ah	GPT2	General PWM Timer Dead Time Value Register D	GTDVD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 223Ch	GPT2	General PWM Timer Dead Time Buffer Register U	GTDBU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 223Eh	GPT2	General PWM Timer Dead Time Buffer Register D	GTDBD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2240h	GPT2	General PWM Timer Output Protection Function Status Register	GTSOS	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2242h	GPT2	General PWM Timer Output Protection Function Temporary Release Register	GTSOTR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2280h	GPT3	General PWM Timer I/O Control Register	GTIOR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2282h	GPT3	General PWM Timer Interrupt Output Setting Register	GTINTAD	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2284h	GPT3	General PWM Timer Control Register	GTCR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2286h	GPT3	General PWM Timer Buffer Enable Register	GTBER	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2288h	GPT3	General PWM Timer Count Direction Register	GTUDC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 228Ah	GPT3	General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register	GTITC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 228Ch	GPT3	General PWM Timer Status Register	GTST	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 228Eh	GPT3	General PWM Timer Counter	GTCNT	16	16	2 to 5 PCLKA	2, 3 ICLK		
000C 2290h	GPT3	General PWM Timer Compare Capture Register A	GTCCRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2292h	GPT3	General PWM Timer Compare Capture Register B	GTCCRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2294h	GPT3	General PWM Timer Compare Capture Register C	GTCCRC	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2296h	GPT3	General PWM Timer Compare Capture Register D	GTCCRD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2298h	GPT3	General PWM Timer Compare Capture Register E	GTCCRE	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 229Ah	GPT3	General PWM Timer Compare Capture Register F	GTCCRF	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 229Ch	GPT3	General PWM Timer Cycle Setting Register	GTPR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 229Eh	GPT3	General PWM Timer Cycle Setting Buffer Register	GTPBR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 22A0h	GPT3	General PWM Timer Cycle Setting Double-Buffer Register	GTPDBR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 22A4h	GPT3	A/D Converter Start Request Timing Register A	GTADTRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 22A6h	GPT3	A/D Converter Start Request Timing Buffer Register A	GTADTBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 22A8h	GPT3	A/D Converter Start Request Timing Double-Buffer Register A	GTADTDBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 22ACh	GPT3	A/D Converter Start Request Timing Register B	GTADTRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 22AEh	GPT3	A/D Converter Start Request Timing Buffer Register B	GTADTBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 22B0h	GPT3	A/D Converter Start Request Timing Double-Buffer Register B	GTADTDBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 22B4h	GPT3	General PWM Timer Output Negate Control Register	GTONCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 22B6h	GPT3	General PWM Timer Dead Time Control Register	GTDTCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 22B8h	GPT3	General PWM Timer Dead Time Value Register U	GTDVU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		

Table 4.1 List of I/O Registers (Address Order) (43/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
000C 291Ah	GPT4	General PWM Timer Compare Capture Register F	GTCCRF	16	16, 32	2 to 5 PCLKA	2, 3 ICLK	GPT	Not present in versions with 64 or 48 pins.
000C 291Ch	GPT4	General PWM Timer Cycle Setting Register	GTPR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 291Eh	GPT4	General PWM Timer Cycle Setting Buffer Register	GTPBR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2920h	GPT4	General PWM Timer Cycle Setting Double-Buffer Register	GTPDBR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2924h	GPT4	A/D Converter Start Request Timing Register A	GTADTRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2926h	GPT4	A/D Converter Start Request Timing Buffer Register A	GTADTBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2928h	GPT4	A/D Converter Start Request Timing Double-Buffer Register A	GTADTDBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 292Ch	GPT4	A/D Converter Start Request Timing Register B	GTADTRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 292Eh	GPT4	A/D Converter Start Request Timing Buffer Register B	GTADTBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2930h	GPT4	A/D Converter Start Request Timing Double-Buffer Register B	GTADTDBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2934h	GPT4	General PWM Timer Output Negate Control Register	GTONCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2936h	GPT4	General PWM Timer Dead Time Control Register	GTDTCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2938h	GPT4	General PWM Timer Dead Time Value Register U	GTDVU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 293Ah	GPT4	General PWM Timer Dead Time Value Register D	GTDVD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 293Ch	GPT4	General PWM Timer Dead Time Buffer Register U	GTDBU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 293Eh	GPT4	General PWM Timer Dead Time Buffer Register D	GTDBD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2940h	GPT4	General PWM Timer Output Protection Function Status Register	GTSOS	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2942h	GPT4	General PWM Timer Output Protection Function Temporary Release Register	GTSOTR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2980h	GPT5	General PWM Timer I/O Control Register	GTIOR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2982h	GPT5	General PWM Timer Interrupt Output Setting Register	GTINTAD	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2984h	GPT5	General PWM Timer Control Register	GTCR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2986h	GPT5	General PWM Timer Buffer Enable Register	GTBER	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2988h	GPT5	General PWM Timer Count Direction Register	GTUDC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 298Ah	GPT5	General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register	GTITC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 298Ch	GPT5	General PWM Timer Status Register	GTST	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 298Eh	GPT5	General PWM Timer Counter	GTCNT	16	16	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2990h	GPT5	General PWM Timer Compare Capture Register A	GTCCRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2992h	GPT5	General PWM Timer Compare Capture Register B	GTCCRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2994h	GPT5	General PWM Timer Compare Capture Register C	GTCCRC	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2996h	GPT5	General PWM Timer Compare Capture Register D	GTCCRD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2998h	GPT5	General PWM Timer Compare Capture Register E	GTCCRE	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 299Ah	GPT5	General PWM Timer Compare Capture Register F	GTCCRF	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 299Ch	GPT5	General PWM Timer Cycle Setting Register	GTPR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.

Table 5.3 DC Characteristics (2)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

The following relation applies when the USB is in use under condition 1 or condition 2: Vcc = PLLVcc = Vcc_USB = 3.0 to 3.6 V.

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output high voltage	All output pins (except for P52, P53, P60 to P65, P71 to P76, P90 to P95, and USB0_DPUPE)	V_{OH}	VCC – 0.5	—	—	V	I_{OH} = –1 mA
	P52, P53, and P60 to P65		AVCC – 0.5	—	—		I_{OH} = –1 mA
	USB0_DPUPE		VCC_USB – 0.5				I_{OH} = –1 mA
	P71 to P76, and P90 to P95		VCC – 1.0	—	—		I_{OH} = –5 mA
Output low voltage	All output pins (except for P71 to P76, P90 to P95, and RIIC pins)	V_{OL}	—	—	0.5	V	I_{OL} = 1.0 mA
	P71 to P76, and P90 to P95		—	—	1.1		I_{OL} = 15 mA
	RIIC pins		—	—	0.4		I_{OL} = 3 mA
			—	—	0.6		I_{OL} = 6 mA
Input leakage current	RES#, MD pin, EMLE, Port 4, Ports P50, P51, P54 to P57, and Port C	$\lvert I_{in} \rvert$	—	—	1.0	µA	V_{in} = 0 V, V_{in} = VCC
Three-state leakage current (off state)	Port 0, Port 1, Ports P20 to P24, Port 3, Ports P52, P53, Ports 6 to A, Ports PB0, PB3 to PB7, and Ports D to G	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	V_{in} = 0 V, V_{in} = VCC
	Ports P25, P26, PB1, and PB2		—	—	5.0		
Input capacitance	All output pins (except for P25, P26, PB1, and PB2)	C_{in}	—	—	15	pF	V_{in} = 0 V, f = 1 MHz, T_a = 25 ºC
	Ports P25, P26, PB1, and PB2		—	—	30		

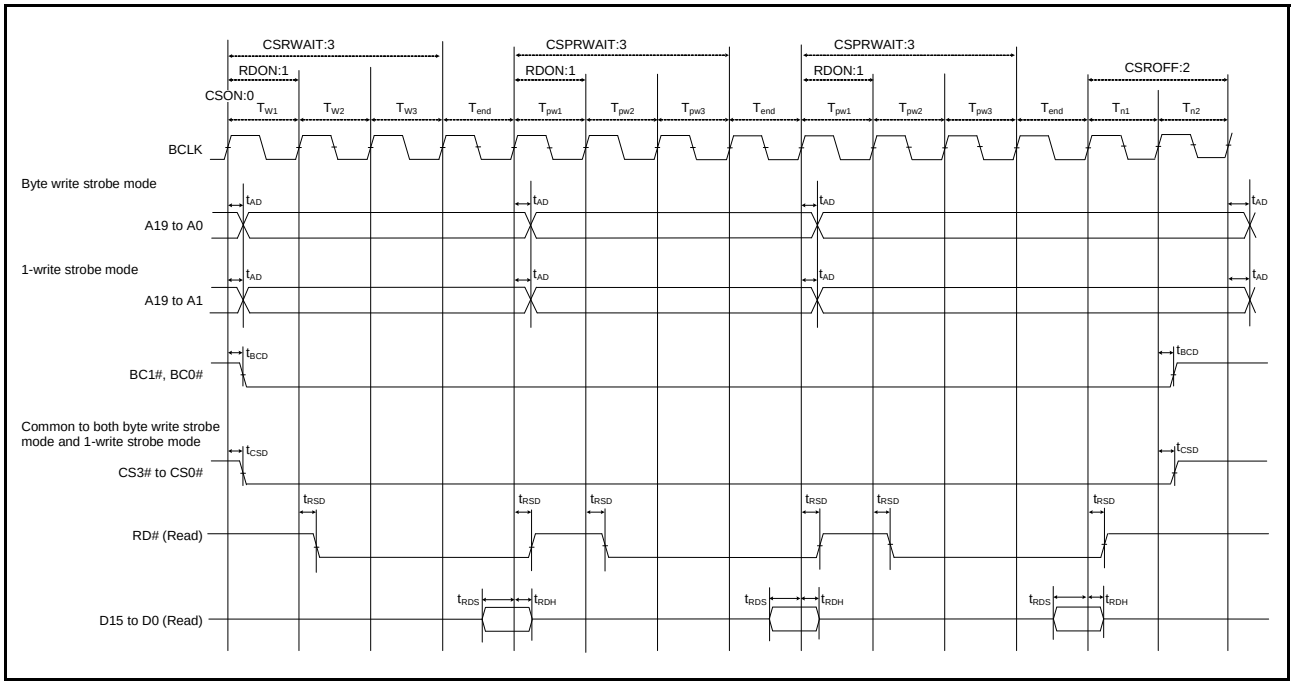
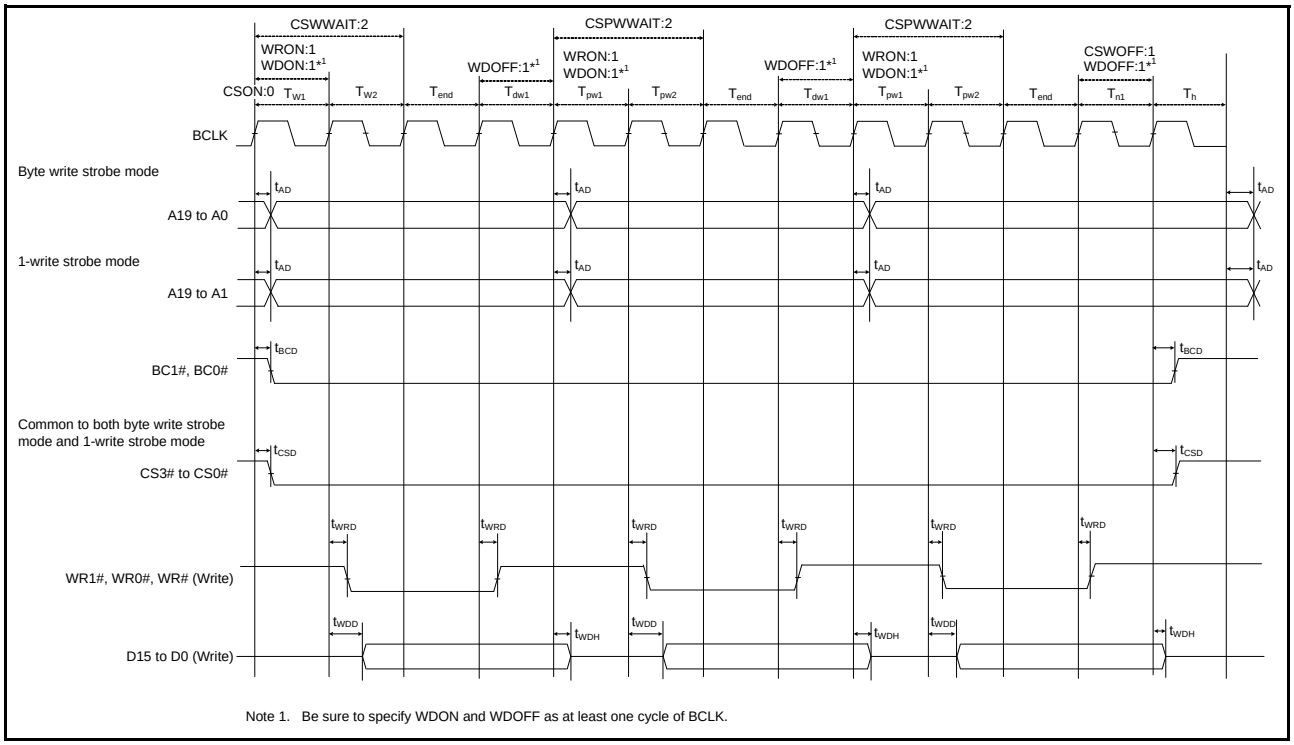


Figure 5.15 External Bus Timing/Page Read Cycle (Bus Clock Synchronized)



Note 1. Be sure to specify WDON and WDOFF as at least one cycle of BCLK.

Figure 5.16 External Bus Timing/Page Write Cycle (Bus Clock Synchronized)

Table 5.21 12-Bit A/D Conversion Characteristics (1)

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

$T_a = T_{opr}$

Item		Min.	Typ.	Max.	Unit	Test Conditions
Resolution		12	12	12	Bit	
Conversion time*1 (ADCLK = 25 MHz)	Without 0.1-µF external capacitor Permissible signal source impedance (max.) = 1.0 kΩ	2.0	—	—	µs	Sampling in 20 states
Analog input capacitance		—	—	8	pF	
Sample and hold circuit in use	Integral nonlinearity error	—	—	±4.0	LSB	AVin = 0.25 to AV_{REFH}–0.25
	Offset error	—	—	±4.0	LSB	
	Full-scale error	—	—	±4.0	LSB	
	Quantization error	—	±0.5	—	LSB	
	Absolute accuracy	—	—	±8.0	LSB	
Sample and hold circuit not in use	Integral nonlinearity error	—	—	±3.0	LSB	AVin = AV_{REFL} to AV_{REFH}
	Offset error	—	—	±3.0	LSB	
	Full-scale error	—	—	±3.0	LSB	
	Quantization error	—	±0.5	—	LSB	
	Absolute accuracy	—	—	±6.0	LSB	

Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Table 5.22 12-Bit A/D Conversion Characteristics (2)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” and “Condition 2” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 2: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. T_a is common to conditions 2 and 3.

Item		Min.	Typ.	Max.	Unit	Test Conditions
Resolution		12	12	12	Bit	
Conversion time*1 (ADCLK = 50 MHz)	Without 0.1-µF external capacitor Permissible signal source impedance (max.) = 1.0 kΩ	1.0	—	—	µs	Sampling in 20 states
Analog input capacitance		—	—	6	pF	
Sample and hold circuit in use	Integral nonlinearity error	—	—	±6.0	LSB	AVin = 0.25 to AV_{REFH}–0.25
	Offset error	—	—	±6.0	LSB	
	Full-scale error	—	—	±6.0	LSB	
	Quantization error	—	±0.5	—	LSB	
	Absolute accuracy	—	—	±8.0	LSB	
Sample and hold circuit not in use	Integral nonlinearity error	—	—	±3.0	LSB	AVin = AV_{REFL} to AV_{REFH}
	Offset error	—	—	±3.0	LSB	
	Full-scale error	—	—	±3.0	LSB	
	Quantization error	—	±0.5	—	LSB	
	Absolute accuracy	—	—	±6.0	LSB	

Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

5.6 D/A Conversion Characteristics

Table 5.25 D/A Conversion Characteristics

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	10	10	10	Bit	
Conversion time	—	—	3.0	µs	20-pF capacitive load
Absolute accuracy	—	±2.0	±4.0	LSB	2-MΩ resistive load
	—	—	±3.0	LSB	4-MΩ resistive load
	—	—	±2.0	LSB	10-MΩ resistive load
RO output resistance	—	3.6	—	kΩ	

5.8 Oscillation Stop Detection Circuit Characteristics

Table 5.28 Oscillation Stop Detection Circuit Characteristics

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection time	t_{dr}	—	—	1.0	ms	Figure 5.43

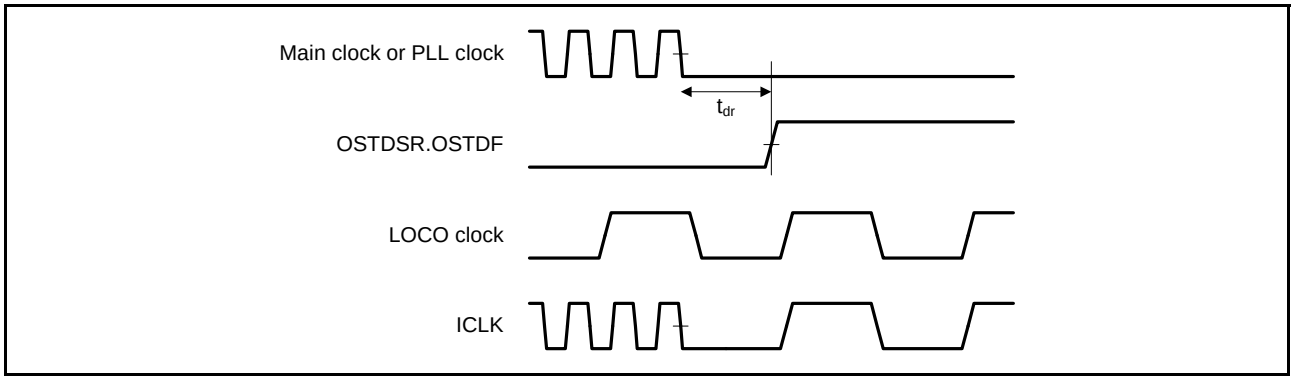


Figure 5.43 Oscillation Stop Detection Timing

Table 6.3 DC Characteristics (2)

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Supply current*1	During operation	Max. *2	I_{CC}*3	—	—	60	mA	ICLK = 100MHz PCLKA = 100MHz PCLKB = 50MHz PCLKD = 50MHz FCLK = 50MHz
		Normal *4		—	25	—		
		Increased by BGO operation*5		—	15	—		
	Sleep mode				25	35		
	All-module-clock-stop mode*6				14	25		
	During standby	Software standby mode		—	0.2	6	mA	
		Deep software standby mode		—	16	40	µA	
Analog power supply current	During 12-bit A/D conversion (sample & hold circuit in use)		AI_{CC0}	—	3	4	mA	
	During 12-bit A/D conversion (sample & hold circuit not in use)			—	2	3	mA	
	Window comparator (1-channel operation)				0.4	1	mA	
	Window comparator (3-channel operation)			—	0.5	1	mA	
	Waiting for 12-bit AD conversion			—	25	32	µA	
Reference power supply current	During 12-bit A/D conversion		AI_{REFH0}	—	0.6	0.7	mA	
	Waiting for 12-bit A/D conversion			—	0.6	0.7	mA	
VCC rising gradient			SrVcc	—	—	20000	ms/V	

Note 1. Supply current values are with all output pins unloaded.
Note 2. Measured with clocks supplied to the peripheral functions. This does not include the BGO operation.
Note 3. I_{CC} depends on f (ICLK) as follows. (ICLK: PCLK = 8:4)
ICC max = 0.45 × f + 15 (Max)
ICC typ = 0.18 × f + 7 (Normal)
ICC max = 0.22 × f + 13 (sleep mode)
Note 4. Measured with clocks not supplied to the peripheral functions. This does not include the BGO operation.
Note 5. Incremented if data is written to or erased from the on-chip ROM or on-chip data-flash memory for data storage during the program execution.
Note 6. The values are for reference.

Table 6.4 Permissible Output Currents

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item	Symbol	Min.	Typ.	Max.	Unit
Permissible output low current (average value per pin)	I_{OL}	—	—	2.0*1	mA
Permissible output low current (max. value per pin)	I_{OL}	—	—	4.0*1	mA
Permissible output low current (total)	ΣI_{OL}	—	—	32	mA
Permissible output high current (average value per pin)	$-I_{OH}$	—	—	2.0	mA
Permissible output high current (max. value per pin)	$-I_{OH}$	—	—	4.0	mA
Permissible output high current (total)	$\Sigma-I_{OH}$	—	—	32	mA

Caution: To protect the MCU's reliability, the output current values should not exceed the values in this table.
Note 1. RIIC pin: IOL = 6 mA (max.)

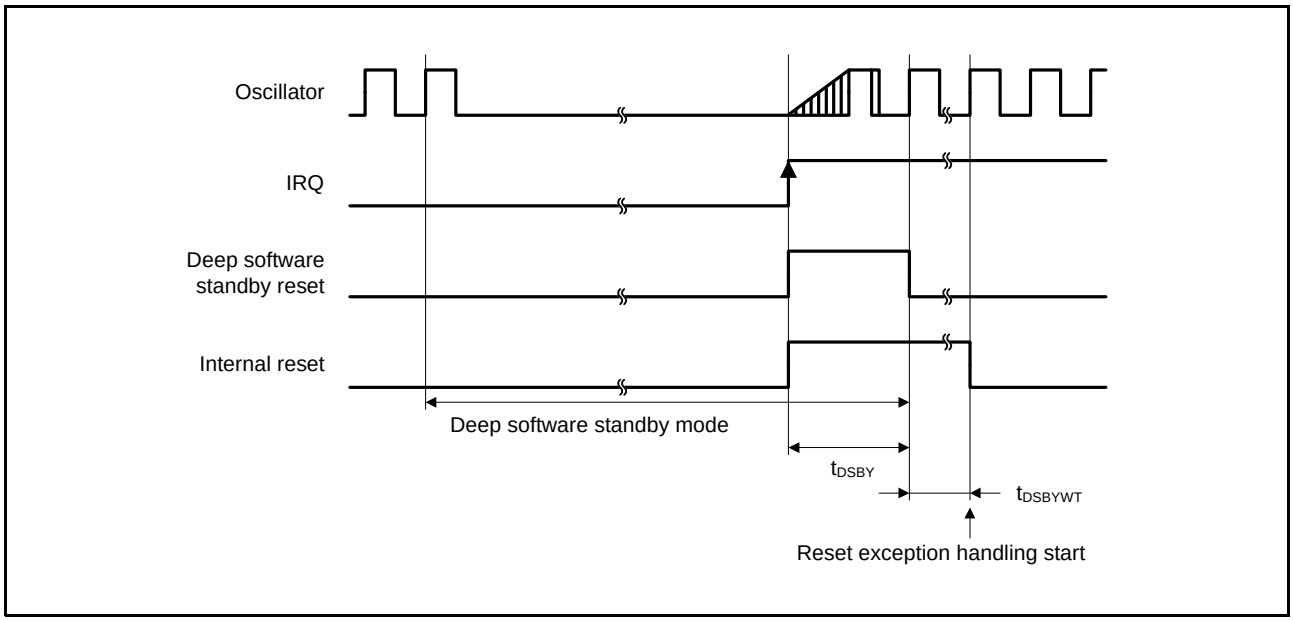


Figure 6.9 Deep Software Standby Mode Cancellation Timing

6.3.4 Control Signal Timing

Table 6.10 Control Signal Timing

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
NMI pulse width	t_{NMIW}	200	—	—	ns	t_{Pcyc} × 2 ≤ 200ns, Figure 6.10
		2			t_{Pcyc}	t_{Pcyc} × 2 > 200ns, Figure 6.10
IRQ pulse width	t_{IRQW}	200	—	—	ns	t_{Pcyc} × 2 ≤ 200ns, Figure 6.11
		2			t_{Pcyc}	t_{Pcyc} × 2 > 200ns, Figure 6.11

Note 1. t_{Pcyc}: PCLK cycle

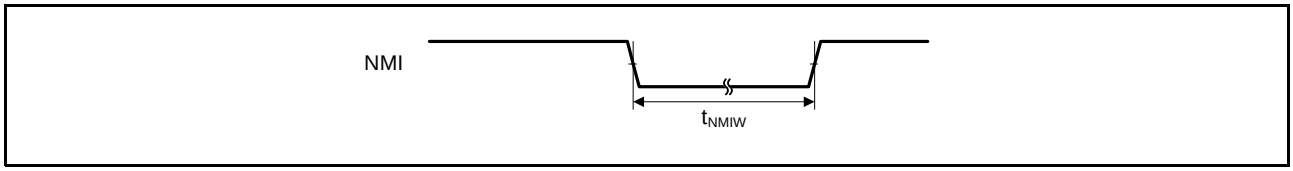


Figure 6.10 NMI Interrupt Input Timing

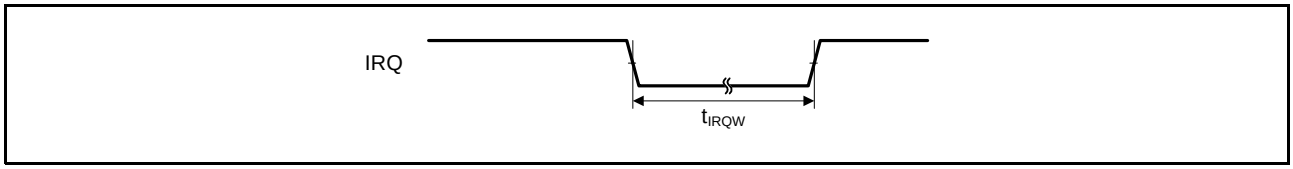


Figure 6.11 IRQ Interrupt Input Timing

Table 6.15 Timing of On-Chip Peripheral Modules (5)

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item		Symbol	Min.*1, *2	Max.	Unit	Test Conditions
Simple IIC (Standard-mode)	SCL, SDAinput rise time	t_{Sr}	—	1000	ns	Figure 6.25
	SCL, SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	4 × t_{IICcyc}	ns	
	Data input setup time	t_{SDAS}	250	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
Simple IIC (Fast-mode)	SCL, SDA input rise time	t_{Sr}	20 + 0.1C_b	300	ns	
	SCL, SDA input fall time	t_{Sf}	20 + 0.1C_b	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	4 × t_{IICcyc}	ns	
	Data input setup time	t_{SDAS}	100	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note 1. The value in parentheses is used when ICMR3.NF[1:0] are set to 11b while a digital filter is enabled with ICFER.NFE = 1.
Note 2. Cb indicates the total capacity of the bus line.

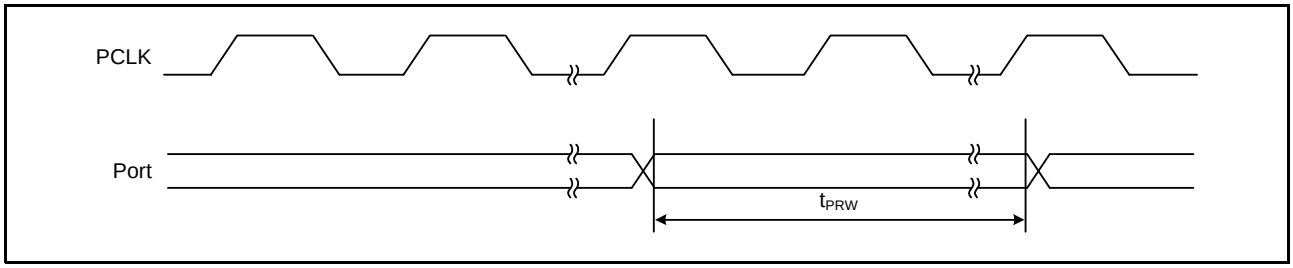


Figure 6.12 I/O port Input Timing

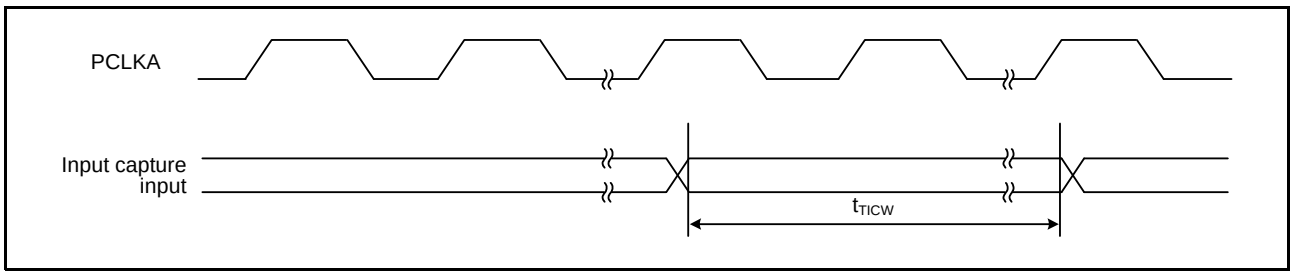


Figure 6.13 MTU3 Input/Output Timing

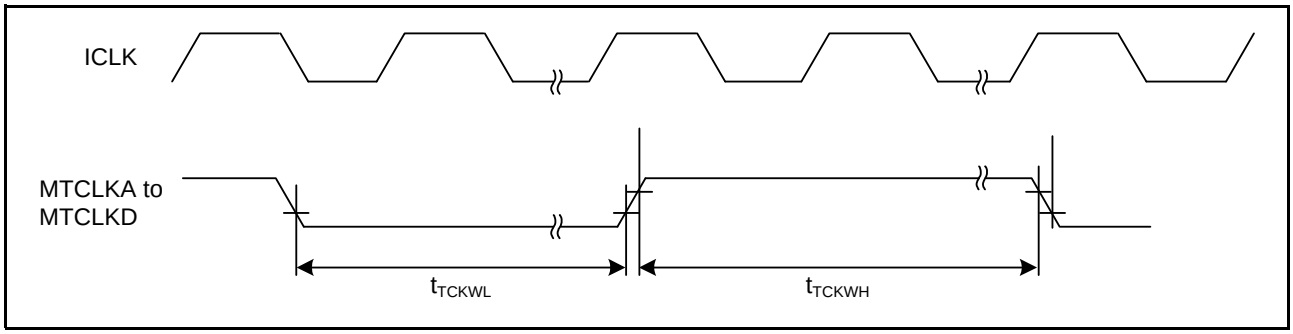


Figure 6.14 MTU3 Clock Input Timing

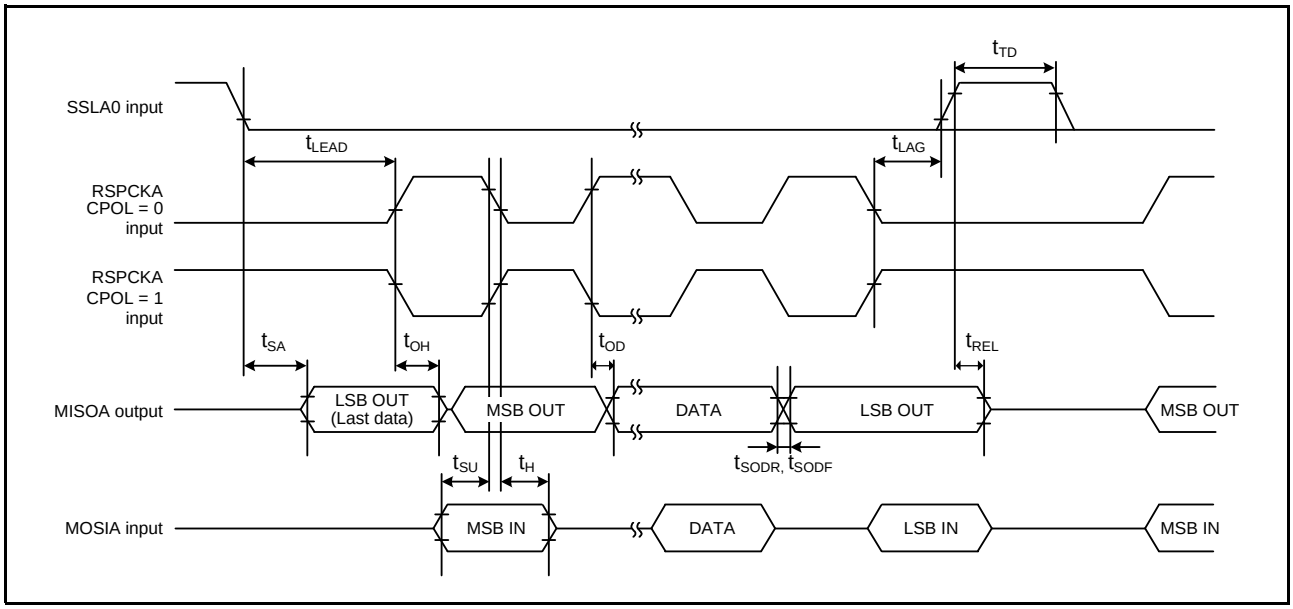
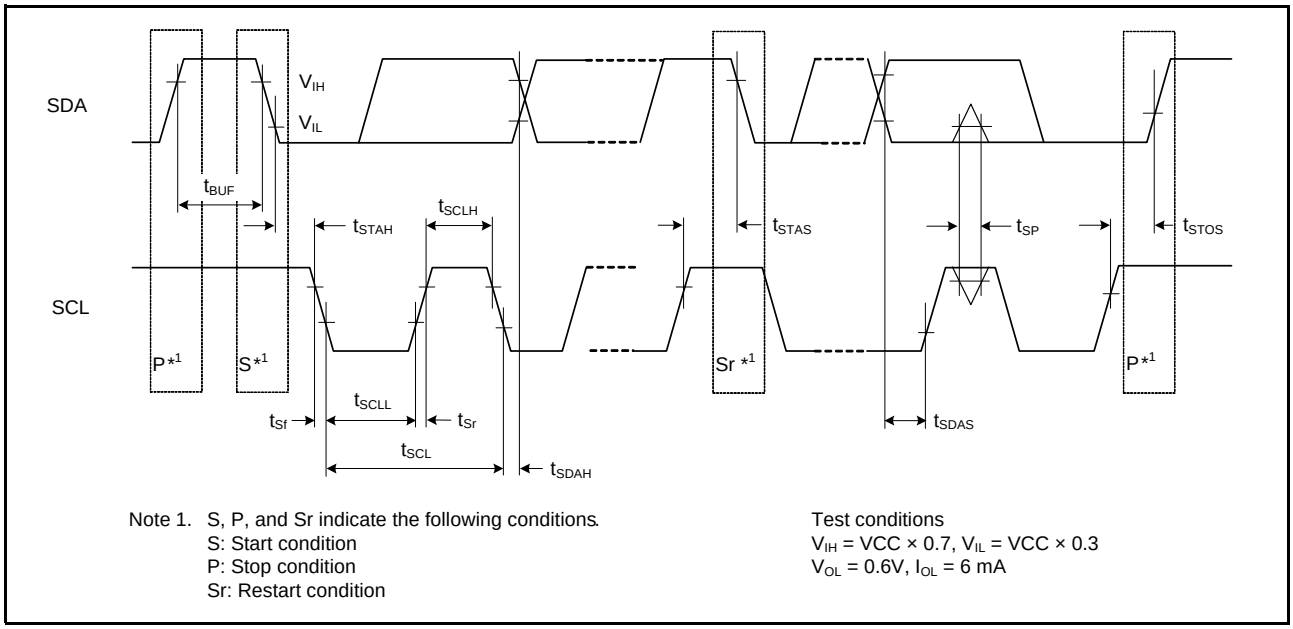


Figure 6.24 RSPI Timing (Slave, CPHA = 1) and Simple SPI Timing (Slave, CKPH = 0)

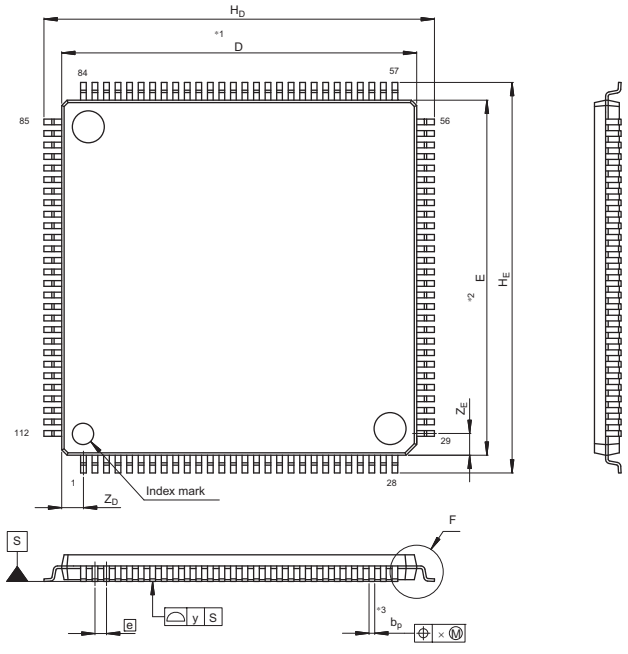


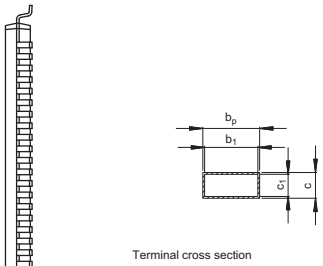
Note 1. S, P, and Sr indicate the following conditions.
S: Start condition
P: Stop condition
Sr: Restart condition

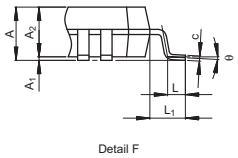
Test conditions
V_{IH} = VCC × 0.7, V_{IL} = VCC × 0.3
V_{OL} = 0.6V, I_{OL} = 6 mA

Figure 6.25 RIIC Bus Interface Input/Output Timing and Simple IIC Bus Interface Input/Output Timing

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP112-20x20-0.65	PLQP0112JA-A	FP-112E/FP-112EV	1.2g







NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	19.9	20.0	20.1
E	19.9	20.0	20.1
A_2	—	1.4	—
H_D	21.8	22.0	22.2
H_E	21.8	22.0	22.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.27	0.32	0.37
b_1	—	0.30	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z_D	—	1.225	—
Z_E	—	1.225	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure C 112-Pin LQFP (PLQP0112JA-A)

Rev.	Date	Description	
		Page	Summary
2.10	Sep 26, 2013	36 to 39	Table 1.7 List of Pins and Pin Functions (112-Pin LQFP), changed
		40 to 42	Table 1.8 List of Pins and Pin Functions (100-Pin LQFP), changed
		43 to 45	Table 1.9 List of Pins and Pin Functions (64-Pin LQFP), changed
		46 to 47	Table 1.10 List of Pins and Pin Functions (48-Pin LQFP), changed
		4. I/O Registers	
		56 to 103	Table 4.1 List of I/O Registers (Address Order), changed
		5. Electrical Characteristics [144-, 120-, 112- and 100-Pin Versions]	
		104	Table 5.1 Absolute Maximum Ratings, changed
		107	Table 5.4 DC Characteristics (3), Note 7, deleted
		108	Table 5.6 Permissible Power Consumption, added
		128	5.3.7 Timing of PWM Delay Generation Circuit, added
		128	Table 42.21 Timing of the PWM Delay Generation Circuit, added
		132	Figure 5.32 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKB Division Ratio Set to a Value Other Than 1/2) and Simple SPI Timing (Master, CKPH = 1), changed
		133	Figure 5.34 RSPI Timing (Slave, CPHA = 0) and Simple SPI Timing (Slave, CKPH = 0), changed
		134	Figure 5.35 RSPI Timing (Slave, CPHA = 1) and Simple SPI Timing (Slave, CKPH = 1), changed
		6. Electrical Characteristics [64- and 48-Pin Versions]	
		149	Table 6.1 Absolute Maximum Ratings, changed
		151	Table 6.3 DC Characteristics (2), Note 3, changed
		152	Table 6.5 Permissible Power Consumption, added

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