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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	EBI/EMI, I ² C, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	81
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 20x10b, 8x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f563tbddfb-v0

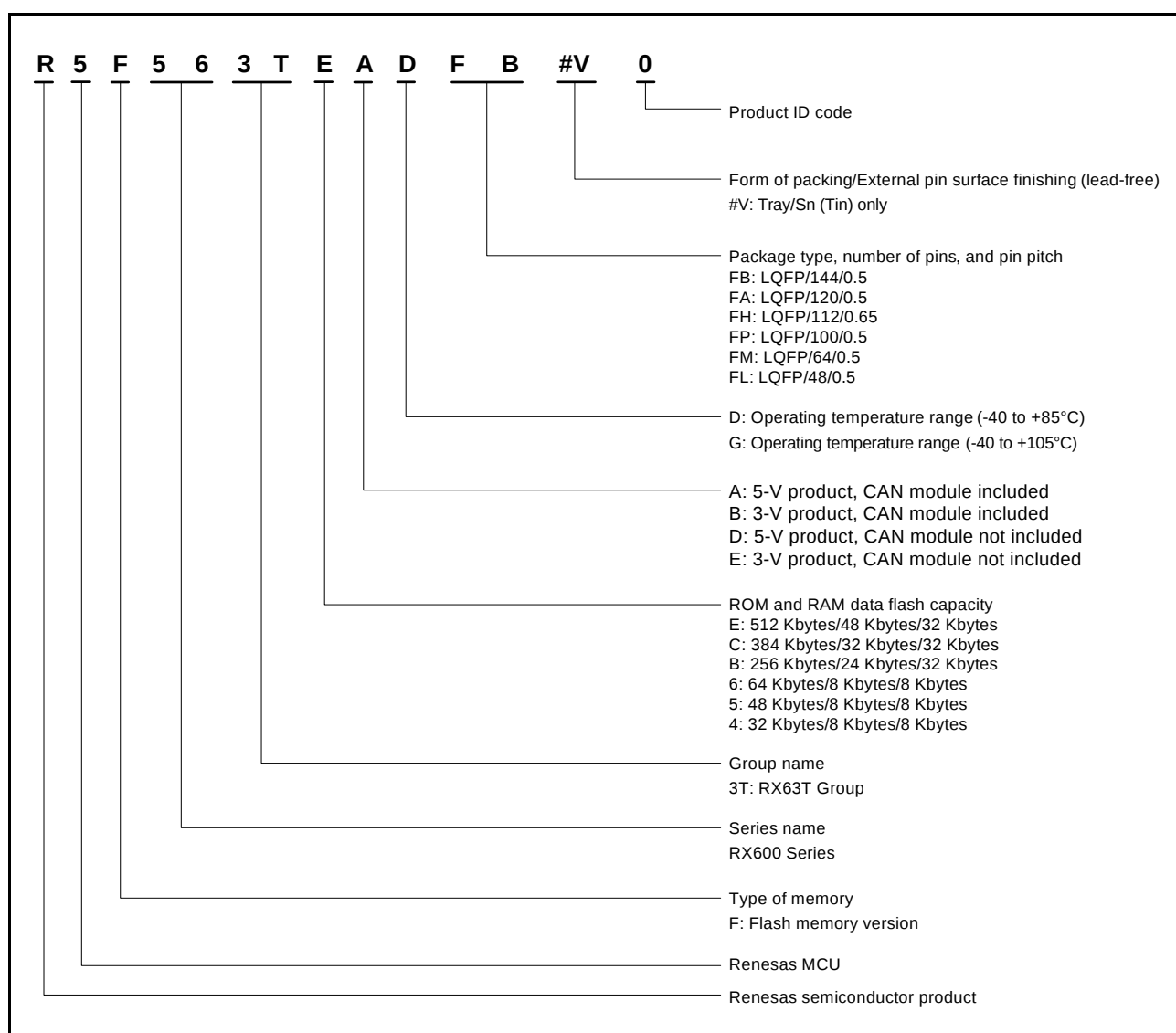


Figure 1.1 How to Read the Product Part Number

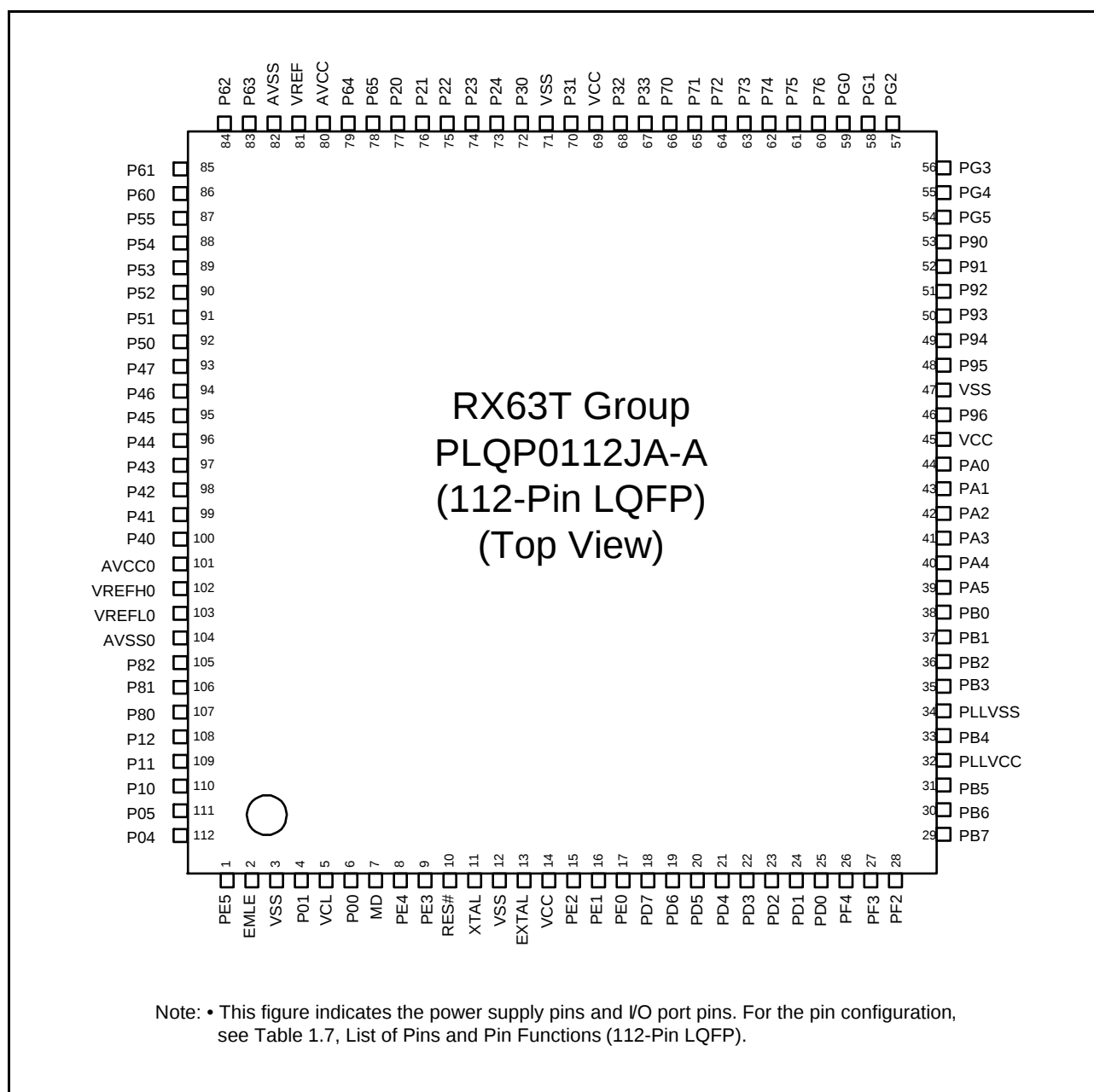


Figure 1.5 Pin Assignment (112-Pin LQFP)

Table 1.5 List of Pins and Pin Functions (144-Pin LQFP) (2/4)

Pin Number 144-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3, GPT, POE3, CAC)	Communications (SClC, SClD, RSPI, RIIC, CAN, USB)	Interrupt	S12ADB, AD, DA
39		PB6	A18		RXD12/SMISO12/ SSCL12/RXDX12/ CRX1	IRQ2	
40		PB5	A17		TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/ CTX1		
41	PLL VCC						
42		PB4	A16	POE8#/ GTETRG0		IRQ3-DS	
43	PLL VSS						
44	TDI				RXD1*1		
45	TCK/FINEC						
46	TDO				TXD1*1		
47		PB3	A15	MTIOC0A/CACREF	SCK0		
48		PB2		MTIOC0B	TXD0/SMOSI0/ SSDA0/SDA0		
49		PB1		MTIOC0C	RXD0/SMISO0/ SSCL0/SCL0	IRQ4	
50		PB0	A14	MTIOC0D	MOSIA/MOSIB		
51	TRDATA1	PA6	CS3#		CTS3#/RTS3#/SS3#		
52		PA5		MTIOC1A	RXD0/SMISO0/ SSCL0/ MISOA/MISOB		ADTRG1#
53		PA4		MTIOC1B	TXD0/SMOSI0/ SSDA0/SMOSI0/ RSPCKA/RSPCKB		ADTRG0#
54		PA3		MTIOC2A	SCK0/SSLA0/SSLB0		
55		PA2		MTIOC2B	RXD2/SMISO2/ SSCL2/ SSLA1/SSLB1		
56		PA1		MTIOC6A	TXD2/SMOSI2/ SSDA2/SMOSI2/ SSLA2/SSLB2		
57		PA0		MTIOC6C	SCK2/SSLA3/SSLB3		
58	TRDATA0	P35			TXD3/SMOSI3/SSDA3		
59	TRCLK	P34		GTETRG1	RXD3/SMISO3/SSCL3	IRQ3	
60	VCC						
61		P96	A13	POE4#	RXD1/SMISO1/SSCL1	IRQ4-DS	
62		PG6	CS2#		SCK1		
63	VSS						
64		P95		MTIOC6B/GTIOC4A	TXD1/SMOSI1/SSDA1		
65		P94		MTIOC7A/GTIOC5A	CTS1#/RTS1#/SS1#		
66		P93		MTIOC7B/GTIOC6A	CTS2#/RTS2#/SS2#		
67		P92		MTIOC6D/GTIOC4B			
68		P91		MTIOC7C/GTIOC5B			
69		P90		MTIOC7D/GTIOC6B			
70		PG5		POE12#	SCK3		ADTRG#
71		PG4		GTIOC6B	RXD3/SMISO3/SSCL3	IRQ6	

Table 1.7 List of Pins and Pin Functions (112-Pin LQFP) (2/4)

Pin Number 112-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3, GPT, POE3, CAC)	Communications (SCIC, SCID, RSPI, RIIC, CAN)	Interrupt	S12ADB, AD, DA
38		PB0	A14	MTIOC0D	MOSIA/MOSIB		
39		PA5		MTIOC1A	RXD0/SMISO0/ SSCL0/ MISOA/MISOB		ADTRG1#
40		PA4		MTIOC1B	TXD0/SMOSI0/ SSDA0/RSPCKA/ RSPCKB		ADTRG0#
41		PA3		MTIOC2A	SCK0/SSLA0/SSLB0		
42		PA2		MTIOC2B	RXD2/SMISO2/ SSCL2/ SSLA1/SSLB1		
43		PA1		MTIOC6A	TXD2/SMOSI2/ SSDA2/SSLA2/SSLB2		
44		PA0		MTIOC6C	SCK2/SSLA3/SSLB3		
45	VCC						
46		P96	A13	POE4#	RXD1/SMISO1/SSCL1	IRQ4-DS	
47	VSS						
48		P95		MTIOC6B/ GTIOC4A	TXD1/SMOSI1/SSDA1		
49		P94		MTIOC7A/ GTIOC5A	CTS1#/RTS1#/SS1#		
50		P93		MTIOC7B/ GTIOC6A	CTS2#/RTS2#/SS2#		
51		P92		MTIOC6D/GTIOC4B			
52		P91		MTIOC7C/GTIOC5B			
53		P90		MTIOC7D/GTIOC6B			
54	TRCLK	PG5		POE12#	SCK3		ADTRG#
55	TRDATA3	PG4		GTIOC6B	RXD3/SMISO3/SSCL3	IRQ6	
56	TRDATA2	PG3		GTIOC6A	TXD3/SMOSI3/SSDA3		
57	TRDATA1	PG2			SCK2	IRQ2	
58	TRDATA0	PG1		GTIOC7B	RXD2/SMISO2/SSCL2	IRQ1	
59	TRSYNC	PG0		GTIOC7A	TXD2/SMOSI2/SSDA2	IRQ0	
60		P76	D0/[A0/D0]	MTIOC4D/GTIOC2B			
61		P75	D1/[A1/D1]	MTIOC4C/GTIOC1B			
62		P74	D2/[A2/D2]	MTIOC3D/GTIOC0B			
63		P73	D3/[A3/D3]	MTIOC4B/GTIOC2A			
64		P72	D4/[A4/D4]	MTIOC4A/GTIOC1A			
65		P71	D5/[A5/D5]	MTIOC3B/GTIOC0A			
66		P70	D6/[A6/D6]	POE0#	CTS1#/RTS1#/SS1#	IRQ5-DS	
67		P33	D7/[A7/D7]	MTIOC3A/MTCLKA	SSLA3/SSLB3		
68		P32	D8/[A8/D8]	MTIOC3C/MTCLKB	SSLA2/SSLB2		
69	VCC						
70		P31	D9/[A9/D9]	MTIOC0A/MTCLKC	SSLA1/SSLB1		
71	VSS						
72		P30	D10/[A10/ D10]	MTIOC0B/MTCLKD	SCK0/SSLA0/SSLB0		
73		P24	D11/[A11/D11]		CTS0#/RTS0#/SS0#/ RSPCKA/RSPCKB	IRQ4	

Table 1.7 List of Pins and Pin Functions (112-Pin LQFP) (3/4)

Pin Number 112-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3, GPT, POE3, CAC)	Communications (SCIC, SCID, RSPI, RIIC, CAN)	Interrupt	S12ADB, AD, DA
74		P23	D12/[A12/ D12]	CACREF	TXD0/SMOSI0/ SSDA0/MOSIA/ MOSIB/CTX1		
75		P22	D13/[A13/ D13]		RXD0/SMISO0/ SSCL0/MISOA/ MISOB/CRX1		ADTRG#
76		P21	D14/[A14/ D14]	MTCLKA		IRQ6-DS	ADTRG1#
77		P20	D15/[A15/ D15]	MTCLKB		IRQ7-DS	ADTRG0#
78		P65	A0/BC0#				AN5
79		P64	A1				AN4
80	AVCC						
81	VREF						
82	AVSS						
83		P63	A2				AN3
84		P62	A3				AN2
85		P61	A4				AN1
86		P60	A5				AN0
87		P55					AN11/DA1
88		P54					AN10/ DA0
89		P53	A6				AN9
90		P52	A7				AN8
91		P51					AN7
92		P50					AN6
93		P47					AN103/ CVREFH
94		P46					AN102
95		P45					AN101
96		P44					AN100
97		P43					AN003/ CVREFL
98		P42					AN002
99		P41					AN001
100		P40					AN000
101	AVCC0						
102	VREFH0						
103	VREFL0						
104	AVSS0						
105		P82	WAIT#	MTIC5U	SCK12	IRQ3	
106		P81	A8	MTIC5V	TXD12/SMOSI12/ SSDA12/TXD12/ SIOX12		
107		P80	A9	MTIC5W	RXD12/SMISO12/ SSCL12/RXD12	IRQ5	
108		P12	CS3#				
109		P11	ALE	MTCLKC		IRQ1-DS	

2.1 General-Purpose Registers (R0 to R15)

This CPU has sixteen general-purpose registers (R0 to R15). R1 to R15 can be used as data registers or address registers. R0, a general-purpose register, also functions as the stack pointer (SP).

The stack pointer is switched to operate as the interrupt stack pointer (ISP) or user stack pointer (USP) by the value of the stack pointer select bit (U) in the processor status word (PSW).

2.2 Control Registers

(1) Interrupt Stack Pointer (ISP)/User Stack Pointer (USP)

The stack pointer (SP) can be either of two types, the interrupt stack pointer (ISP) or the user stack pointer (USP). Whether the stack pointer operates as the ISP or USP depends on the value of the stack pointer select bit (U) in the processor status word (PSW).

Set the ISP or USP to a multiple of four, as this reduces the numbers of cycles required to execute interrupt sequences and instructions entailing stack manipulation.

(2) Interrupt Table Register (INTB)

The interrupt table register (INTB) specifies the address where the relocatable vector table starts.

(3) Program Counter (PC)

The program counter (PC) indicates the address of the instruction being executed.

(4) Processor Status Word (PSW)

The processor status word (PSW) indicates the results of instruction execution or the state of the CPU.

(5) Backup PC (BPC)

The backup PC (BPC) is provided to speed up response to interrupts.

After a fast interrupt has been generated, the contents of the program counter (PC) are saved in the BPC register.

(6) Backup PSW (BPSW)

The backup PSW (BPSW) is provided to speed up response to interrupts.

After a fast interrupt has been generated, the contents of the processor status word (PSW) are saved in the BPSW. The allocation of bits in the BPSW corresponds to that in the PSW.

(7) Fast Interrupt Vector Register (FINTV)

The fast interrupt vector register (FINTV) is provided to speed up response to interrupts.

The FINTV register specifies a branch destination address when a fast interrupt has been generated.

(8) Floating-Point Status Word (FPSW)

The floating-point status word (FPSW) indicates the results of floating-point operations.

When an exception handling enable bit (Ej) enables the exception handling (Ej = 1), the exception cause can be identified by checking the corresponding Cj flag in the exception handling routine. If the exception handling is masked (Ej = 0), the occurrence of exception can be checked by reading the Fj flag at the end of a series of processing. Once the Fj flag has been set to 1, this value is retained until it is cleared to 0 by software (j = X, U, Z, O, or V).

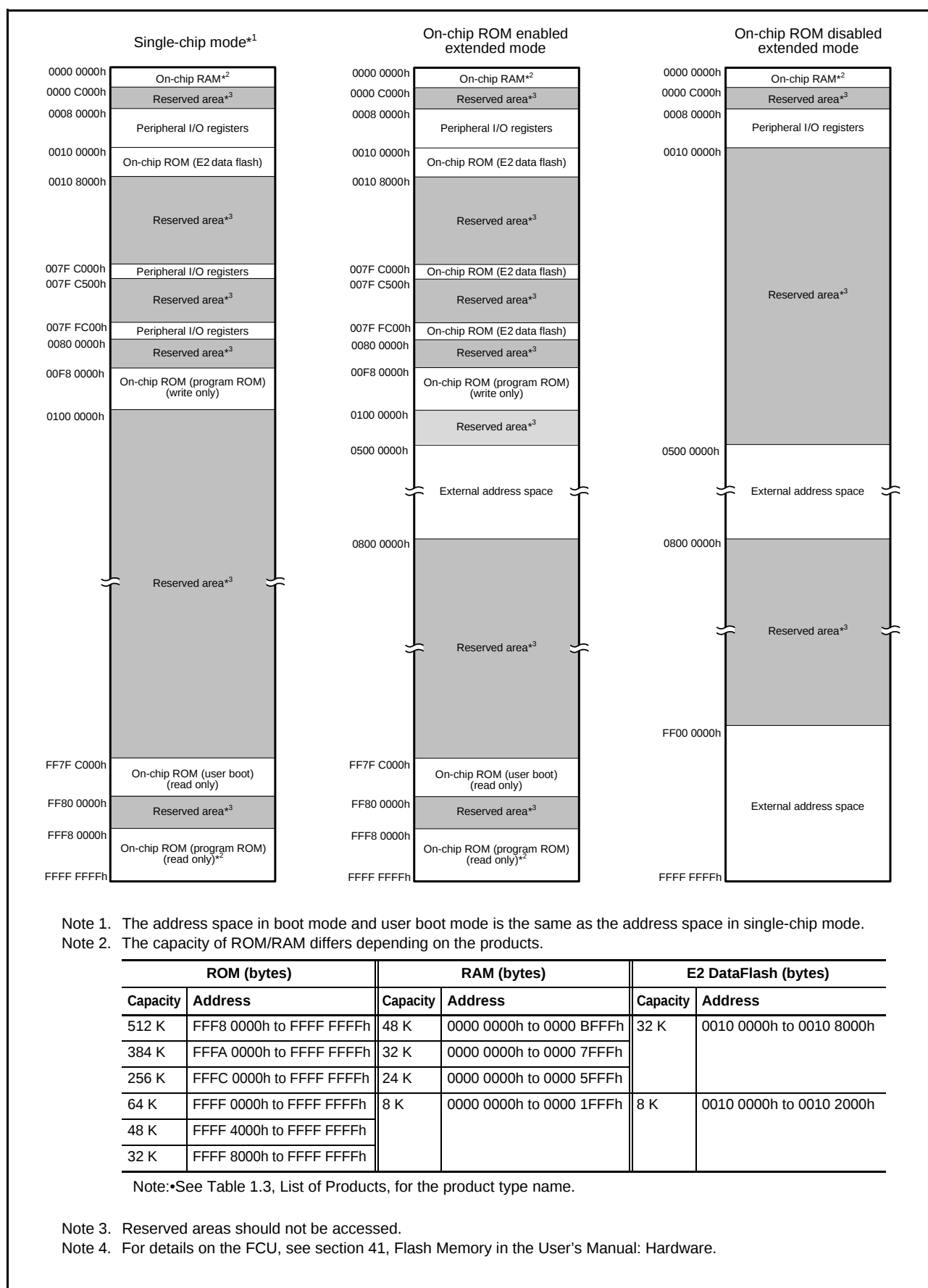


Figure 3.1 Memory Map in Each Operating Mode

Table 4.1 List of I/O Registers (Address Order) (18/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 90E0h	S12AD	Comparator Operating Mode Selection Register 0	ADCMPPMD0	16	16	2, 3 PCLKB	2 ICLK	S12ADB	
0008 90E2h	S12AD	Comparator Operating-Mode Selection Register 1	ADCMPPMD1	16	16	2, 3 PCLKB	2 ICLK		
0008 90E4h	S12AD	Comparator Filter-Mode Register	ADCMPPNR0	16	16	2, 3 PCLKB	2 ICLK		
0008 90E8h	S12AD	Comparator Detection Flag Register	ADCMPPFR	8	8	2, 3 PCLKB	2 ICLK		
0008 90EAh	S12AD	Comparator Interrupt Selection Register	ADCMPPSEL	16	16	2, 3 PCLKB	2 ICLK		
0008 90FCh	S12AD	A/D Group Scan Priority Control Register	ADGSPMR	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9100h	S12AD1	A/D Control Register	ADCSR	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9104h	S12AD1	A/D Channel Select Register A	ADANSA	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9108h	S12AD1	A/D-Converted Value Addition Mode Select Register (ADADS)	ADADS	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 910Ch	S12AD1	A/D-Converted Value Addition Count Select Register	ADADC	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 910Eh	S12AD1	A/D Control Extended Register	ADCER	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9110h	S12AD1	A/D Start Trigger Select Register	ADSTRGR	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9114h	S12AD1	A/D Channel Select Register B	ADANSB	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9118h	S12AD1	A/D Data-Doubling Register	ADDBLDR	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 911Eh	S12AD1	A/D Self-Diagnosis Data Register	ADRD	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9120h	S12AD1	A/D Data Register 0	ADDR0	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9122h	S12AD1	A/D Data Register 1	ADDR1	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9124h	S12AD1	A/D Data Register 2	ADDR2	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9126h	S12AD1	A/D Data Register 3	ADDR3	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9160h	S12AD1	A/D Sampling State Register 0	ADSSTR0	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9166h	S12AD1	A/D Sample and Hold Circuit Control Register	ADSHCR	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9173h	S12AD1	A/D Sampling State Register 1	ADSSTR1	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9174h	S12AD1	A/D Sampling State Register 2	ADSSTR2	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9175h	S12AD1	A/D Sampling State Register 3	ADSSTR3	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9180h	S12AD1	A/D Group Scan Priority Control Register	ADGSPCR	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9184h	S12AD1	A/D Data-Doubling Register A	ADDBLDRA	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9186h	S12AD1	A/D Data-Doubling Register B	ADDBLDRB	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 918Ah	S12AD1	A/D Programmable Gain Amplifier Register	ADPG	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 91E0h	S12AD1	Comparator Operating Mode Selection Register 0	ADCMPPMD0	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 91E2h	S12AD1	Comparator Operating-Mode Selection Register 1	ADCMPPMD1	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 91E4h	S12AD1	Comparator Filter-Mode Register	ADCMPPNR0	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 91E8h	S12AD1	Comparator Detection Flag Register	ADCMPPFR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 91EAh	S12AD1	Comparator Interrupt Selection Register	ADCMPPSEL	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9800h	AD	A/D Control Register	ADCSR	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.

Table 4.1 List of I/O Registers (Address Order) (35/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
000C 1308h	MTU0	Timer General Register A	TGRA	16	16, 32	4, 5 PCLKA	2, 3 ICLK	MTU3	
000C 130Ah	MTU0	Timer General Register B	TGRB	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 130Ch	MTU0	Timer General Register C	TGRC	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 130Eh	MTU0	Timer General Register D	TGRD	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1320h	MTU0	Timer General Register E	TGRE	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1322h	MTU0	Timer General Register F	TGRF	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1324h	MTU0	Timer Interrupt Enable Register 2	TIER2	8	8, 16	4, 5 PCLKA	2, 3 ICLK		
000C 1325h	MTU0	Timer Status Register 2	TSR2	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1326h	MTU0	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1380h	MTU1	Timer Control Register	TCR	8	8, 16	4, 5 PCLKA	2, 3 ICLK		
000C 1381h	MTU1	Timer Mode Register 1	TMDR1	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1382h	MTU1	Timer I/O Control Register	TIOR	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1384h	MTU1	Timer Interrupt Enable Register	TIER	8	8, 16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1385h	MTU1	Timer Status Register	TSR	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1386h	MTU1	Timer Counter	TCNT	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1388h	MTU1	Timer General Register A	TGRA	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 138Ah	MTU1	Timer General Register B	TGRB	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1390h	MTU1	Timer Input Capture Control Register	TICCR	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1400h	MTU2	Timer Control Register	TCR	8	8, 16	4, 5 PCLKA	2, 3 ICLK		
000C 1401h	MTU2	Timer Mode Register 1	TMDR1	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1402h	MTU2	Timer I/O Control Register	TIOR	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1404h	MTU2	Timer Interrupt Enable Register	TIER	8	8, 16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1405h	MTU2	Timer Status Register	TSR	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1406h	MTU2	Timer Counter	TCNT	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1408h	MTU2	Timer General Register A	TGRA	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 140Ah	MTU2	Timer General Register B	TGRB	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1A00h	MTU6	Timer Control Register	TCR	8	8, 16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1A01h	MTU7	Timer Control Register	TCR	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1A02h	MTU6	Timer Mode Register 1	TMDR1	8	8, 16	4, 5 PCLKA	2, 3 ICLK		
000C 1A03h	MTU7	Timer Mode Register 1	TMDR1	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1A04h	MTU6	Timer I/O Control Register H	TIORH	8	8, 16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1A05h	MTU6	Timer I/O Control Register L	TIORL	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1A06h	MTU7	Timer I/O Control Register H	TIORH	8	8, 16	4, 5 PCLKA	2, 3 ICLK		
000C 1A07h	MTU7	Timer I/O Control Register L	TIORL	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1A08h	MTU6	Timer Interrupt Enable Register	TIER	8	8, 16	4, 5 PCLKA	2, 3 ICLK		
000C 1A09h	MTU7	Timer Interrupt Enable Register	TIER	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1A0Ah	MTU	Timer Output Master Enable Register B	TOERB	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1A0Eh	MTU	Timer Output Control Register 1B	TOCR1B	8	8, 16	4, 5 PCLKA	2, 3 ICLK		
000C 1A0Fh	MTU	Timer Output Control Register 2B	TOCR2B	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1A10h	MTU6	Timer Counter	TCNT	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1A12h	MTU7	Timer Counter	TCNT	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1A14h	MTU	Timer Cycle Data Register B	TCDRB	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1A16h	MTU	Timer Dead Time Data Register B	TDDRB	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1A18h	MTU6	Timer General Register A	TGRA	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1A1Ah	MTU6	Timer General Register B	TGRB	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1A1Ch	MTU7	Timer General Register A	TGRA	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1A1Eh	MTU7	Timer General Register B	TGRB	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1A20h	MTU	Timer Subcounter B	TCNTSB	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1A22h	MTU	Timer Cycle Buffer Register B	TCBRB	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1A24h	MTU6	Timer General Register C	TGRC	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1A26h	MTU6	Timer General Register D	TGRD	16	16	4, 5 PCLKA	2, 3 ICLK		

Table 4.1 List of I/O Registers (Address Order) (46/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK $\geq$ PCLK	ICLK $<$ PCLK		
000C 2AA8h	GPT7	A/D Converter Start Request Timing Double-Buffer Register A	GTADTDBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK	GPT	Not present in versions with 64 or 48 pins.
000C 2AACh	GPT7	A/D Converter Start Request Timing Register B	GTADTRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2AAEh	GPT7	A/D Converter Start Request Timing Buffer Register B	GTADTBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2AB0h	GPT7	A/D Converter Start Request Timing Double-Buffer Register B	GTADTDBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2AB4h	GPT7	General PWM Timer Output Negate Control Register	GTONCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2AB6h	GPT7	General PWM Timer Dead Time Control Register	GTDTCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2AB8h	GPT7	General PWM Timer Dead Time Value Register U	GTDVU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2ABAh	GPT7	General PWM Timer Dead Time Value Register D	GTDVD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2ABCh	GPT7	General PWM Timer Dead Time Buffer Register U	GTDBU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2ABEh	GPT7	General PWM Timer Dead Time Buffer Register D	GTDBD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2AC0h	GPT7	General PWM Timer Output Protection Function Status Register	GTSOS	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2AC2h	GPT7	General PWM Timer Output Protection Function Temporary Release Register	GTSOTR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3002h	DPC	Software Start Setting Register 0	SOFTSTART 0	16	16	3 to 5 PCLKA	2, 3 ICLK	DPC	Not present in versions with 64 or 48 pins.
000C3006h	DPC	Software Start Setting Register 1	SOFTSTART 1	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C300Ah	DPC	Software Start Setting Register 2	SOFTSTART 2	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C300Eh	DPC	Software Start Setting Register 3	SOFTSTART 3	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3012h	DPC	Reference Value Setting Register 0	VOTARGET 0	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3016h	DPC	Reference Value Setting Register 1	VOTARGET 1	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C301Ah	DPC	Reference Value Setting Register 2	VOTARGET 2	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C301Eh	DPC	Reference Value Setting Register 3	VOTARGET 3	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3022h	DPC	Reference Value Select Register	REFSEL	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3026h	DPC	PWM Channel Setting Register	CHLSEL	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C302Ah	DPC	Control Enable Setting Register	ENABLE	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C302Eh	DPC	Control Calculation Parameter Setting Register KP0	PARAMKP0	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3032h	DPC	Control Calculation Parameter Setting Register KI0	PARAMKI0	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3036h	DPC	Control Calculation Parameter Setting Register KQ0	PARAMKQ0	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C303Ah	DPC	Control Calculation Parameter Setting Register KF0	PARAMKF0	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C303Eh	DPC	Control Calculation Parameter Setting Register KP1	PARAMKP1	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3042h	DPC	Control Calculation Parameter Setting Register KI1	PARAMKI1	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3046h	DPC	Control Calculation Parameter Setting Register KQ1	PARAMKQ1	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C304Ah	DPC	Control Calculation Parameter Setting Register KF1	PARAMKF1	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C304Eh	DPC	Control Calculation Parameter Setting Register KP2	PARAMKP2	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3052h	DPC	Control Calculation Parameter Setting Register KI2	PARAMKI2	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.

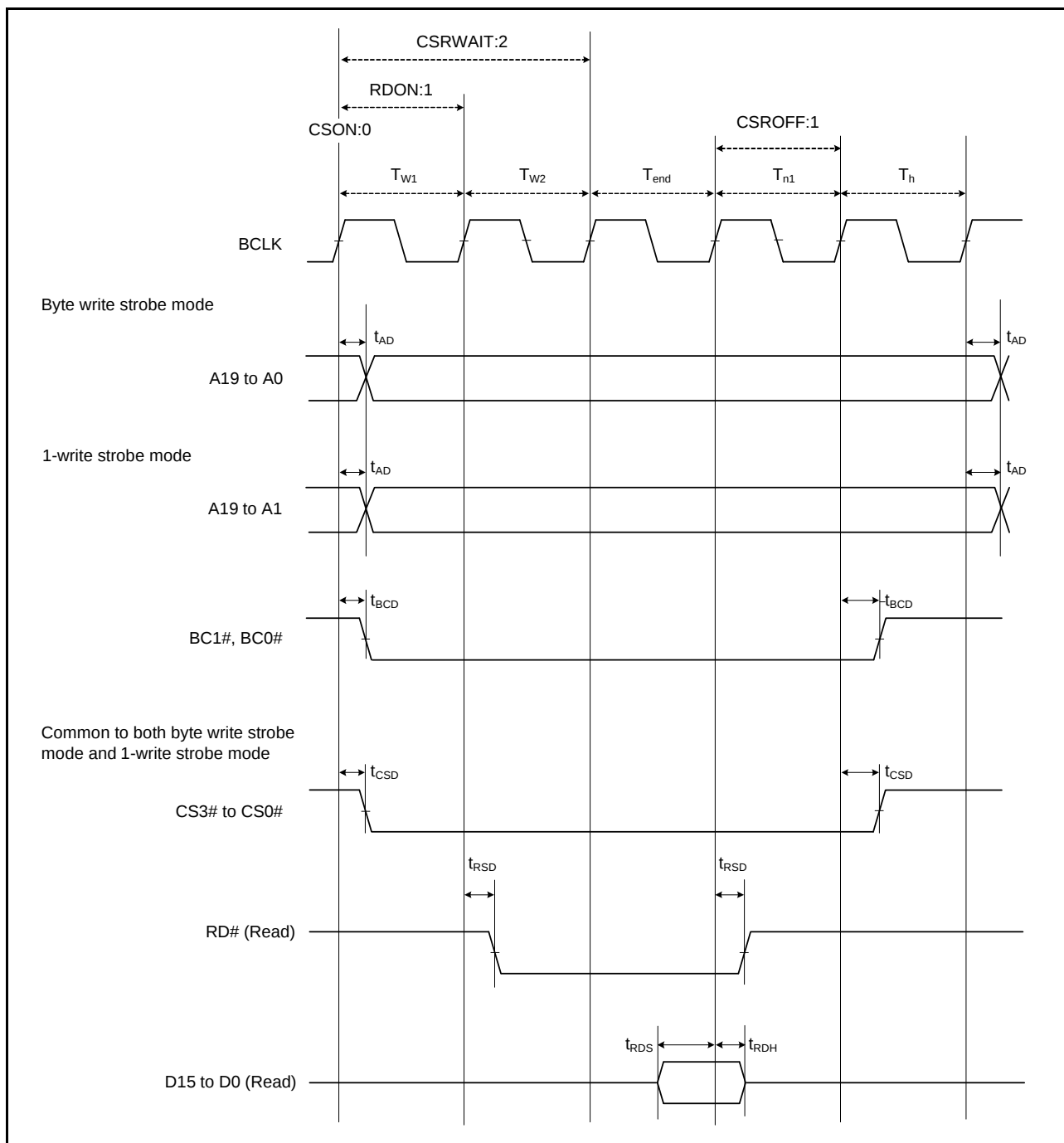


Figure 5.13 External Bus Timing/Normal Read Cycle (Bus Clock Synchronized)

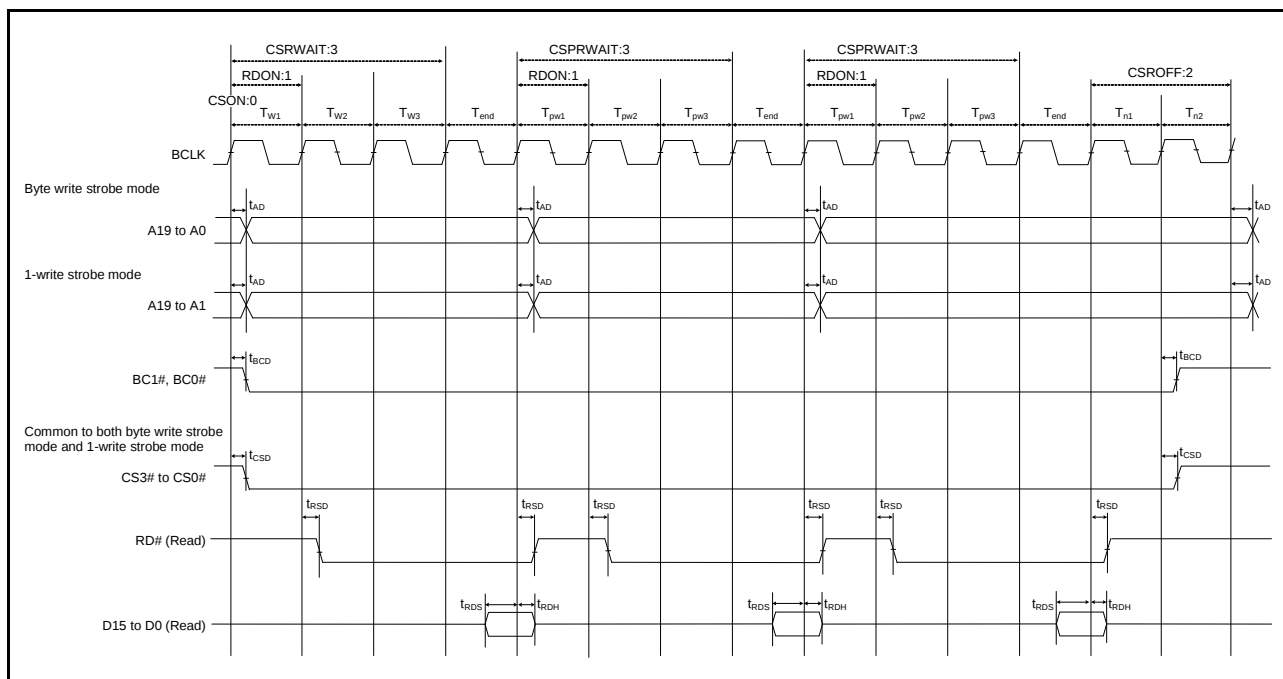


Figure 5.15 External Bus Timing/Page Read Cycle (Bus Clock Synchronized)

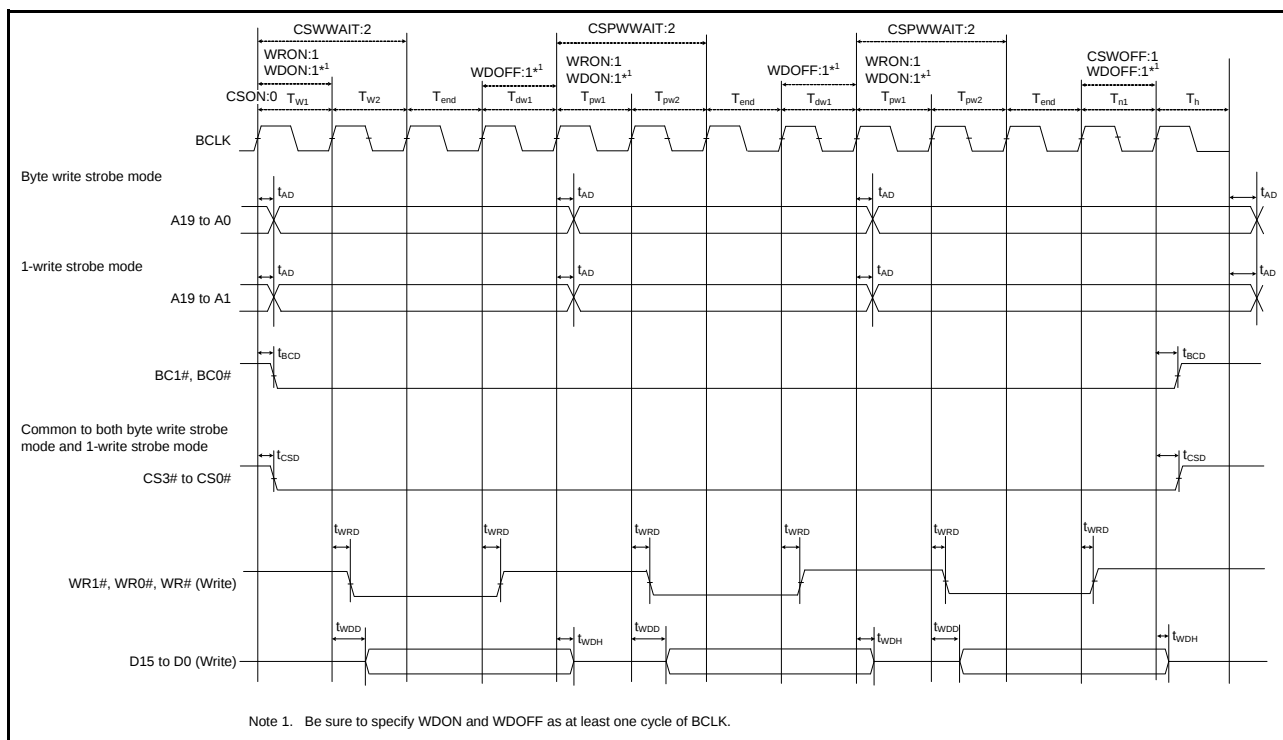


Figure 5.16 External Bus Timing/Page Write Cycle (Bus Clock Synchronized)

5.3.6 Timing of On-Chip Peripheral Modules

Table 5.16 Timing of On-Chip Peripheral Modules (1)

Note: Common standard values for conditions not given in the table are listed as "Condition 1" to "Condition 3" below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

T_a = T_{opr}. T_a is common to conditions 1 to 3.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
I/O ports	Input data pulse width		t _{PRW}	1.5	—	t _{PCyc}	Figure 5.22
MTU3	Input capture input pulse width	Single-edge setting	t _{TICW}	3	—	t _{PAcyc}	Figure 5.23
		Both-edge setting		5	—		
	Input capture input fall time		t _{TICTF}	—	0.1	μs/V	When Input capture at rising edge, or Input capture at both edges is selected.
	Timer clock pulse width	Single-edge setting	t _{TCKWH} , t _{TCKWL}	3	—	t _{PAcyc}	Figure 5.25
		Both-edge setting		5	—		
		Phase counting mode		5	—		
	Timer clock input fall time		t _{TCKTF}	—	0.1	μs/V	
POE3	POE# input pulse width		t _{POEW}	1.5	—	t _{PCyc}	Figure 5.28
GPT	Input capture input pulse width	Single-edge setting	t _{GTICW}	3	—	t _{PAcyc}	Figure 5.26
		Both-edge setting		5	—		
	Input capture input fall time		t _{GTICTF}	—	0.1	μs/V	When Input capture at rising edge, or Input capture at both edges is selected. When Count operation is started at rising edge, or Count operation is started at both edges is selected. When Count operation is stopped at rising edge, or Count operation is stopped at both edges is selected. When Counter is cleared at rising edge, or Counter is cleared at both edges is selected.
	External trigger input pulse width	Single-edge setting	t _{OTETW}	3	—	t _{PAcyc}	Figure 5.27
		Both-edge setting		5	—		
	External trigger input fall time		t _{GTETRGTF}	—	0.1	μs/V	When Count operation is started at rising edge, or Count operation is started at both edges is selected. When Count operation is stopped at rising edge, or Count operation is stopped at both edges is selected. When Counter is cleared at rising edge, or Counter is cleared at both edges is selected.

Table 5.16 Timing of On-Chip Peripheral Modules (5)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$ T_a is common to conditions 1 to 3.

Item		Symbol	Min.*1,*2	Max.	Unit	Test Conditions
RIIC (Standard-mode)	SCL input cycle time	t_{SCL}	$6(12) \times t_{IICcyc} + 1300$	—	ns	Figure 5.36
	SCL input high pulse width	t_{SCLH}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	SCL input low pulse width	t_{SCLL}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	SCL, SDA input rise time	t_{Sr}	—	1000	ns	
	SCL, SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	$1(4) \times t_{IICcyc}$	ns	
	SDA input bus free time	t_{BUF}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	Start condition input hold time	t_{STAH}	$t_{IICcyc} + 300$	—	ns	
	Restart condition input setup time	t_{STAS}	1000	—	ns	
	Stop condition input setup time	t_{STOS}	1000	—	ns	
	Data input setup time	t_{SDAS}	$t_{IICcyc} + 50$	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
RIIC (Fast-mode)	SCL input cycle time	t_{SCL}	$6(12) \times t_{IICcyc} + 600$	—	ns	
	SCL input high pulse width	t_{SCLH}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	SCL input low pulse width	t_{SCLL}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	SCL, SDA input rise time	t_{Sr}	$20 + 0.1C_b$	300	ns	
	SCL, SDA input fall time	t_{Sf}	$20 + 0.1C_b$	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	$1(4) \times t_{IICcyc}$	ns	
	SDA input bus free time	t_{BUF}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	Start condition input hold time	t_{STAH}	$t_{IICcyc} + 300$	—	ns	
	Restart condition input setup time	t_{STAS}	300	—	ns	
	Stop condition input setup time	t_{STOS}	300	—	ns	
	Data input setup time	t_{SDAS}	$t_{IICcyc} + 50$	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note: • t_{IICcyc} : RIIC internal reference clock (IIC ϕ) cycle

Note 1. The value within parentheses is applicable when the value of the ICMR3.NF[1:0] bits is 11b while the digital filter is enabled by the setting ICFER.NFE = 1.

Note 2. C_b is the total capacitance of the bus lines.

Table 5.27 Power-on Reset Circuit and Voltage Detection Circuit Characteristics (2)

Condition: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$

	Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	V_{POR}	3.6	3.8	4.0	V	Figure 5.41
	Voltage detection circuit (LVD0)	V_{DET0}	4.0	4.2	4.4		Figure 5.42
	Voltage detection circuit (LVD1)*1	V_{DET1_8}	4.59	4.77	4.95		Figure 5.43
		V_{DET1_9}	4.05	4.23	4.41		
		V_{DET1_A}	4.32	4.50	4.68		
	Voltage detection circuit (LVD2)*2	V_{DET2_8}	4.59	4.77	4.95		Figure 5.44
		V_{DET2_9}	4.05	4.23	4.41		
		V_{DET2_A}	4.32	4.50	4.68		
Internal reset time	Power-on reset (POR)	t_{POR}		9.7		ms	Figure 5.41
	Voltage detection circuit (LVD0)	t_{LVD0}		9.7			Figure 5.42
	Voltage detection circuit (LVD1)	t_{LVD1}		0.9			Figure 5.43
	Voltage detection circuit (LVD2)	t_{LVD2}		0.9			Figure 5.44
Minimum VCC down time*3		t_{VOFF}	200	—	—	μ s	Figure 5.41 to Figure 5.44
Response delay time		t_{DET}			200	μ s	
LVD operation stabilization time (after LVD is enabled)		$T_{d(E-A)}$			3	μ s	Figure 5.41 to Figure 5.44
Hysteresis width (LVD1 and LVD2)		V_{LVH}		80		mV	

Note 1. # in symbol $V_{DET1_#}$ indicates the value of the LVDLVLRLVD1LVL[3:0] bits.

Note 2. # in symbol $V_{DET2_#}$ indicates the value of the LVDLVLRLVD2LVL[3:0] bits.

Note 3. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR} , V_{DET1} , and V_{DET2} for the POR/ LVD.

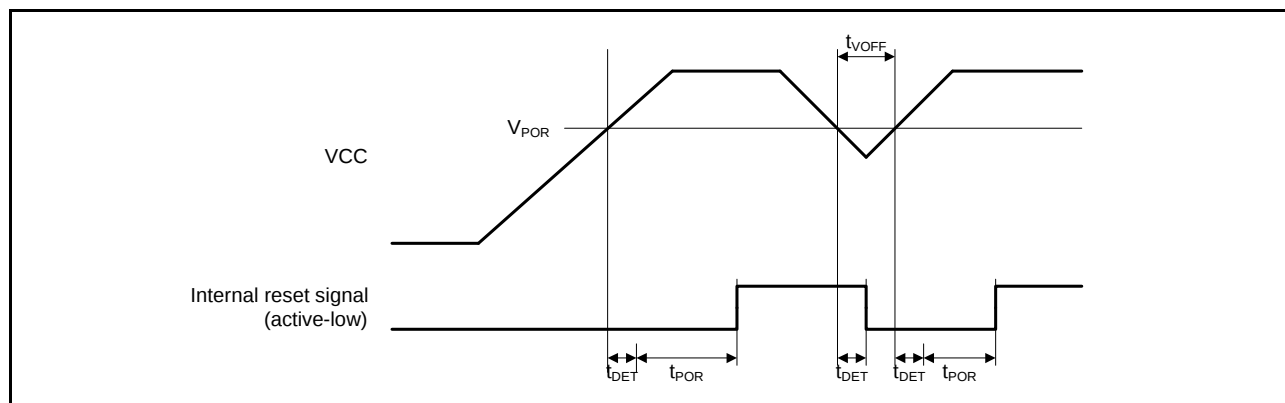
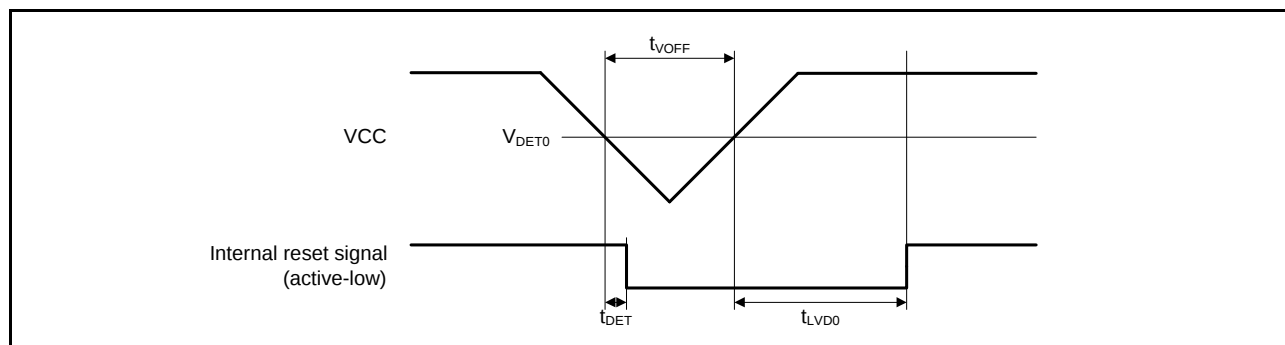
**Figure 5.39 Power-on Reset Timing****Figure 5.40 Voltage Detection Circuit Timing (V_{DET0})**

Table 6.13 Timing of On-Chip Peripheral Modules (3)

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
 AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
 Ta = T_{opr}

Item		Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI	SCK clock cycle output (master)	t _{SPcyc}	4	65536	t _{Pcyc}	Figure 6.20
	SCK clock cycle input (slave)		8	65536		
	SCK clock high pulse width	t _{SPCKWH}	0.4	0.6	t _{SPcyc}	
	SCK clock low pulse width	t _{SPCKWL}	0.4	0.6	t _{SPcyc}	
	SCK clock rise/fall time	t _{SPCKR} , t _{SPCKF}	—	20	ns	
	Data input setup time	t _{SU}	40	—	ns	Figure 6.21 to Figure 6.24
	Data input hold time	t _H	40	—	ns	
	SS input setup time	t _{LEAD}	6	—	t _{Pcyc}	
	SS input hold time	t _{LAG}	6	—	t _{Pcyc}	
	Data output delay time	t _{OD}	—	40	ns	
	Data output hold time	t _{OH}	−10	—	ns	
	Data rise/fall time	t _{DR} , t _{DF}	—	20	ns	
	SS input rise/fall time	t _{SSLr} , t _{SSLf}	—	20	ns	
	Slave access time	t _{SA}	—	5	t _{Pcyc}	Figure 6.23 and Figure 6.24
	Slave output release time	t _{REL}	—	5	t _{Pcyc}	

Note 1. t_{Pcyc}: PCLK cycle

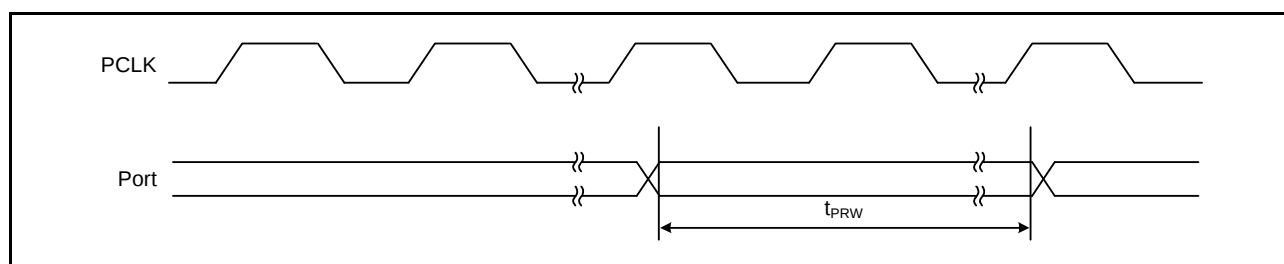
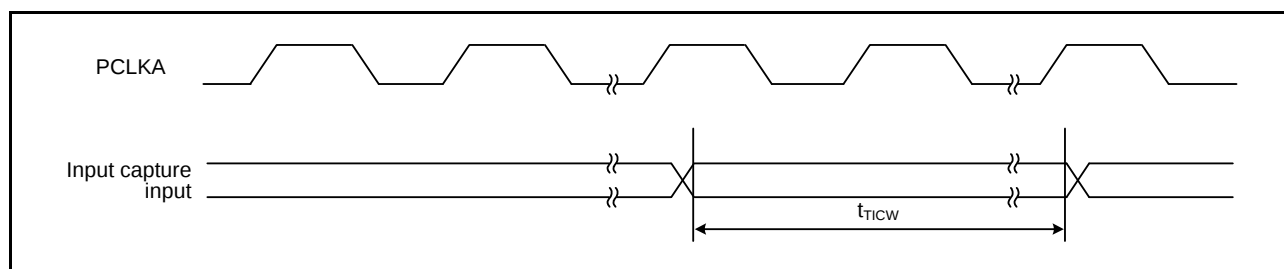
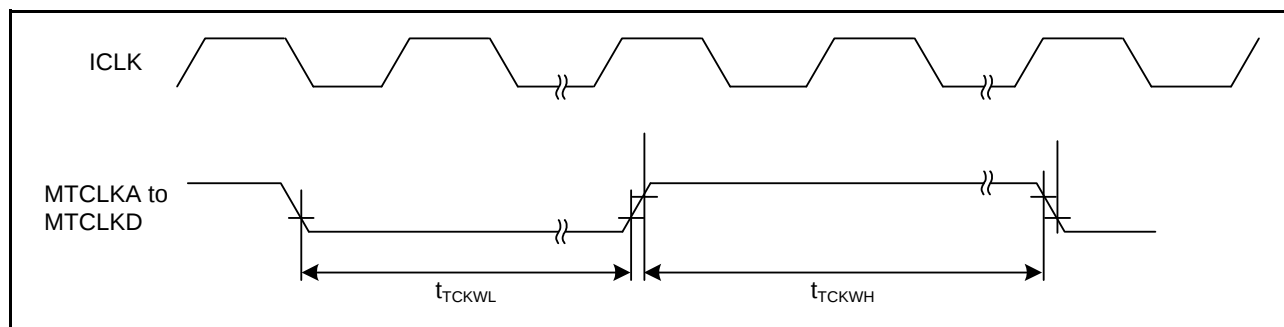
Table 6.15 Timing of On-Chip Peripheral Modules (5)

Conditions: $V_{CC} = 2.7$ to 3.6 V, $V_{SS} = AVSS0 = VREFL0 = 0$ V,
 $AVCC0 = 3.0$ to 3.6 V, $VREFH0 = 3.0$ V to $AVCC0$,
 $T_a = T_{opr}$

	Item	Symbol	Min.*1, *2	Max.	Unit	Test Conditions
Simple IIC (Standard-mode)	SCL, SDA input rise time	t_{Sr}	—	1000	ns	Figure 6.25
	SCL, SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	$4 \times t_{IICcyc}$	ns	
	Data input setup time	t_{SDAS}	250	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
Simple IIC (Fast-mode)	SCL, SDA input rise time	t_{Sr}	$20 + 0.1C_b$	300	ns	
	SCL, SDA input fall time	t_{Sf}	$20 + 0.1C_b$	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	$4 \times t_{IICcyc}$	ns	
	Data input setup time	t_{SDAS}	100	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note 1. The value in parentheses is used when ICMR3.NF[1:0] are set to 11b while a digital filter is enabled with ICFER.NFE = 1.

Note 2. C_b indicates the total capacity of the bus line.

**Figure 6.12 I/O port Input Timing****Figure 6.13 MTU3 Input/Output Timing****Figure 6.14 MTU3 Clock Input Timing**

6.7 ROM (Flash Memory for Code Storage) Characteristics

Table 6.20 ROM (Flash Memory for Code Storage) Characteristics (1)

Condition: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V

AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,

Temperature range for the programming/erasure operation: $T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Reprogram/erase cycle*1	N_{pec}	1000	—	—	Times	
Data hold time	t_{DRP}	30*2	—	—	Year	$T_a = +85^{\circ}\text{C}$

Note 1. Definition of reprogram/erase cycle:

The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times ($n = 1000$), erasing can be performed n times for each block. For instance, when 128-byte programming is performed 16 times for different addresses in 2-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. The value is obtained from the reliability test.

Table 6.21 ROM (Flash Memory for Code Storage) Characteristics (2)

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,

AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,

Temperature range for the programming/erasure operation: $T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item		Symbol	min	typ	max	Unit	Test Conditions
Programming time	128 bytes	t _{P128}	—	1	10	ms	FCLK = 50MHz N _{PEC} ≤ 100
	4 Kbytes	t _{P4K}	—	23	50	ms	
	16 Kbytes	t _{P16K}	—	90	200	ms	
	128 bytes	t _{P128}	—	1.2	12	ms	FCLK=50MHz N _{PEC} > 100
	4 Kbytes	t _{P4K}	—	27.6	60	ms	
	16 Kbytes	t _{P16K}	—	108	240	ms	
Erasure time	4 Kbytes	t _{E4K}	—	25	60	ms	FCLK=50MHz N _{PEC} ≤ 100
	16 Kbytes	t _{E16K}	—	100	240	ms	
	4 Kbytes	t _{E4K}	—	30	72	ms	FCLK=50MHz N _{PEC} > 100
	16 Kbytes	t _{E16K}	—	120	288	ms	
Suspend delay time during programming		t _{SPD}	—	—	120	μs	Figure 6.31 FCLK = 50MHz
First suspend delay time during erasing (in suspend priority mode)		t _{SESD1}	—	—	120	μs	
Second suspend delay time during erasing (in suspend priority mode)		t _{SESD2}	—	—	1.7	ms	
Suspend delay time during erasing (in erasure priority mode)		t _{SEED}	—	—	1.7	ms	
FCU reset time		t _{FCUR}	35	—	—	μs	

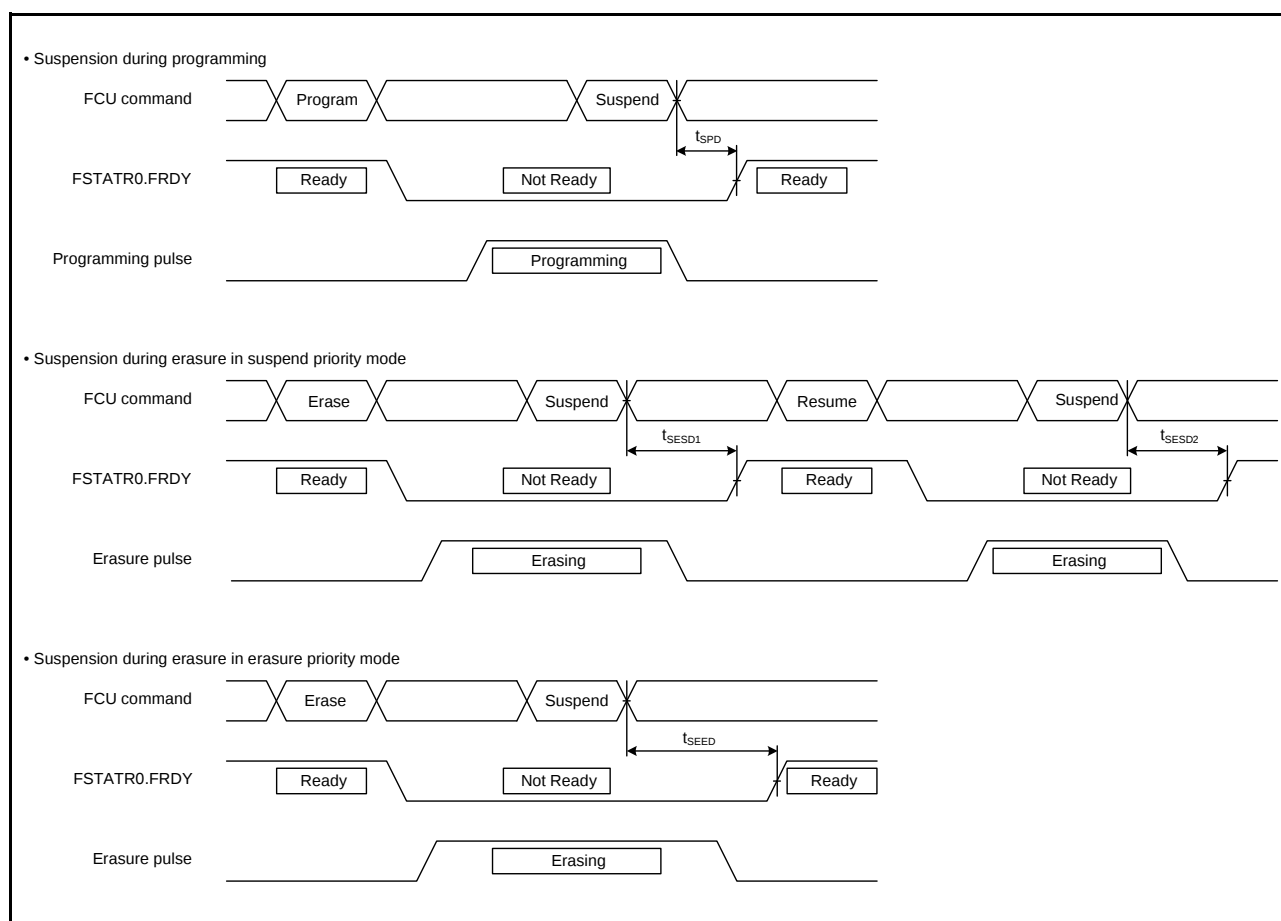


Figure 6.31 Flash Memory Program/Erase Suspend Timing

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

- ¾ The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- ¾ The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- ¾ The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- ¾ When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

- ¾ The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.