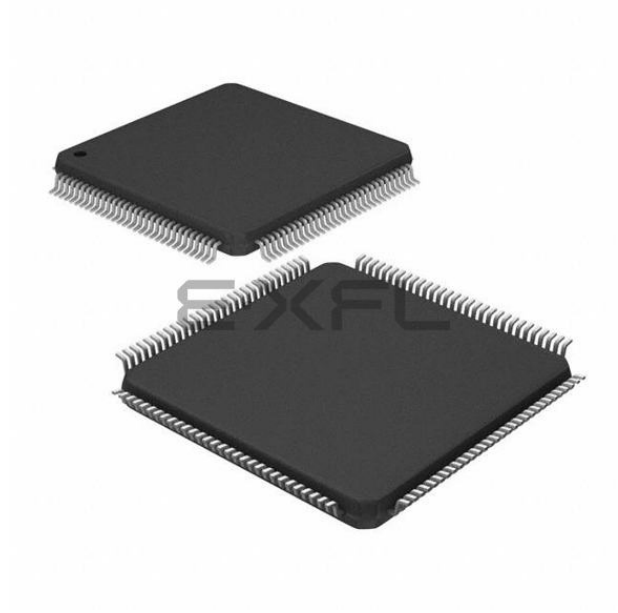

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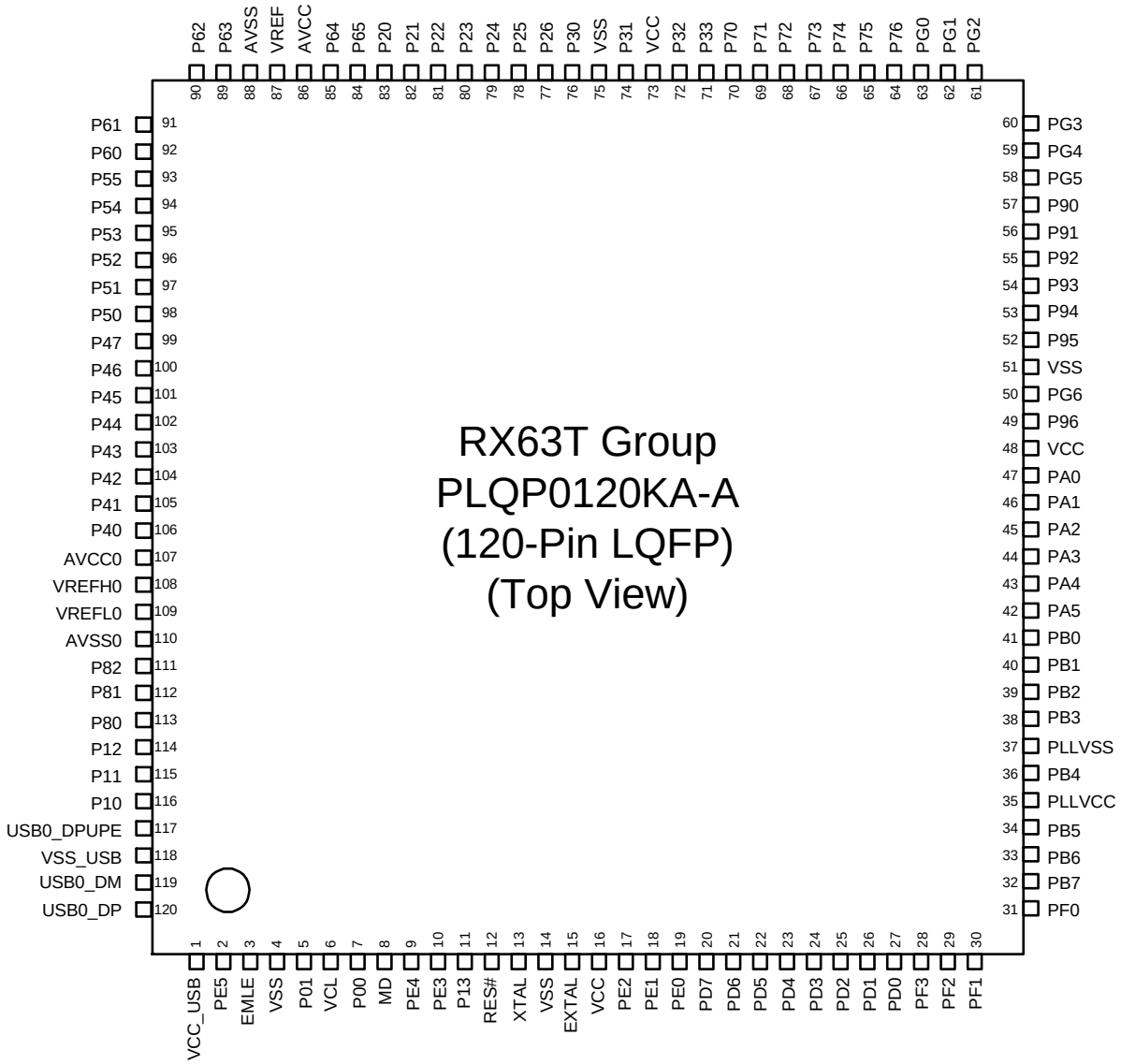
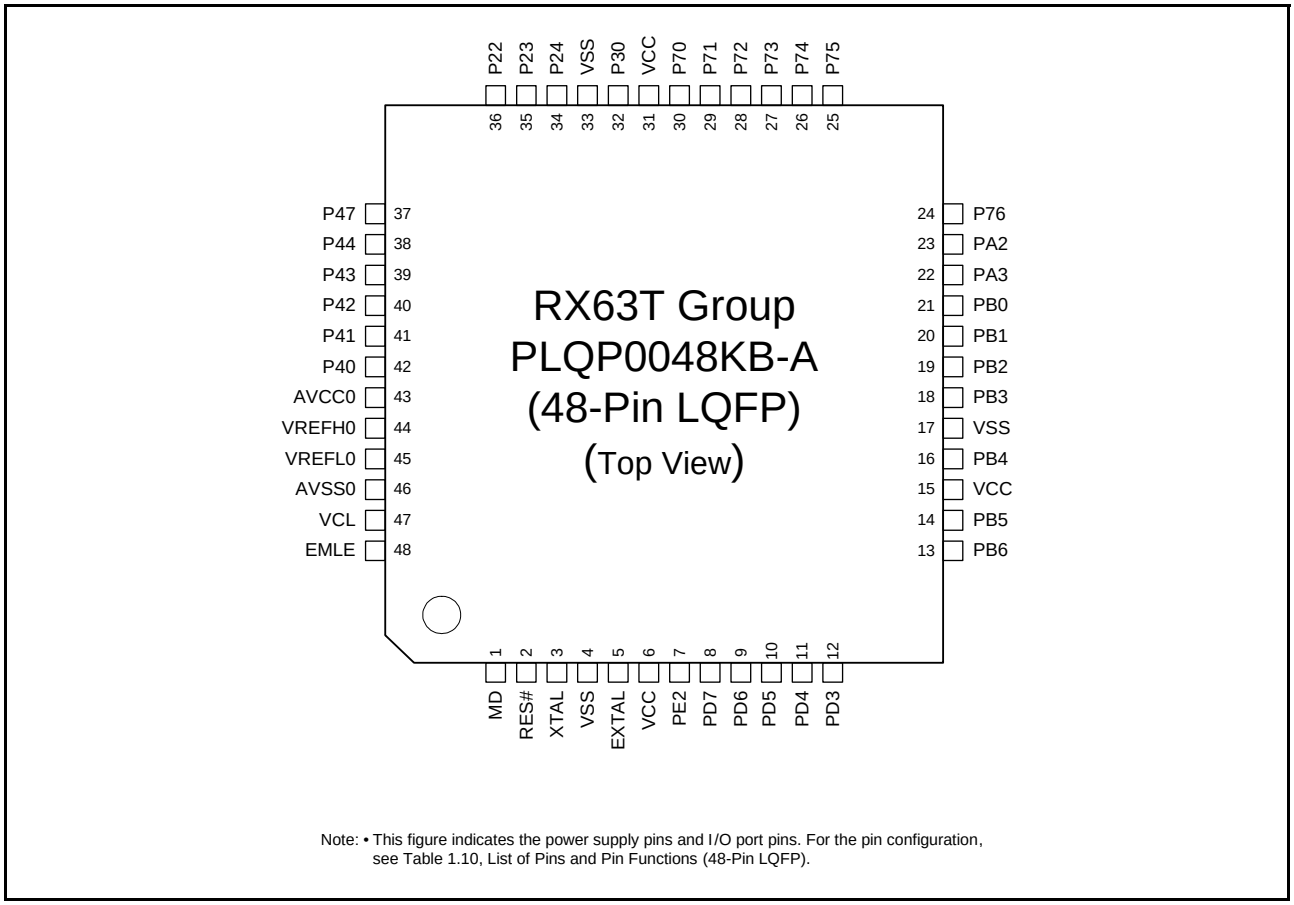
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	EBI/EMI, I²C, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	72
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 12x10b, 8x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	120-LQFP
Supplier Device Package	120-LQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f563tbedfa-v0



Note: • This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.6, List of Pins and Pin Functions (120-Pin LQFP).

Figure 1.4 Pin Assignment (120-Pin LQFP)



Note: • This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.10, List of Pins and Pin Functions (48-Pin LQFP).

Figure 1.8 Pin Assignment (48-Pin LQFP)

Table 1.6 List of Pins and Pin Functions (120-Pin LQFP) (1/4)

Pin Number 120-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3, GPT, POE3, CAC)	Communications (SCIc, SCId, RSPI, RIIC, CAN, USB)	Interrupt	S12ADB, AD, DA
1	VCC_USB						
2		PE5	BCLK		USB0_VBUS	IRQ0	
3	EMLE						
4	VSS						
5		P01	RD#		CTS0#/RTS0#/SS0#/ USB0_DRPD		
6	VCL						
7		P00	CS1#	CACREF			
8	MD/FINED						
9		PE4	A10	POE10#/MTCLKC		IRQ1	
10		PE3	A11	POE11#/MTCLKD		IRQ2-DS	
11		P13			CTS2#/RTS2#/SS2#/ USB0_VBUSEN		
12	RES#						
13	XTAL						
14	VSS						
15	EXTAL						
16	VCC						
17		PE2		POE10#		NMI	
18		PE1	WR0#/WR#		CTS12#/RTS12#/ SS12#/SSLA3/SSLB3/ USB0_OVRCURA		
19		PE0	WR1#/BC1#/ WAIT#		SSLA2/SSLB2/CRX1/ USB0_OVRCURB	IRQ7	
20	TRST#	PD7		GTIOC0A	CTS0#/RTS0#/SS0#/ SSLA1/SSLB1/CTX1		
21	TMS	PD6		GTIOC0B	SSLA0/SSLB0		
22	TDI	PD5		GTIOC1A	RXD1/SMISO1/SSCL1	IRQ6	
23	TCK/FINEC	PD4		GTIOC1B	SCK1		
24	TDO	PD3		GTIOC2A	TXD1/SMOSI1/SSDA1		
25		PD2	CS2#	GTIOC2B	MOSIA/MOSIB/ USB0_ID		
26		PD1	CS0#	GTIOC3A	MISOA/MISOB/ USB0_EXICEN		
27		PD0	A12	GTIOC3B	RSPCKA/RSPCKB		
28		PF3			TXD1/SMOSI1/SSDA1		
29		PF2	CS1#		RXD1/SMISO1/SSCL1	IRQ5	
30		PF1					
31		PF0					
32		PB7	A19		SCK12		
33		PB6	A18		RXD12/SMISO12/ SSCL12/RXDX12/ CRX1	IRQ2	
34		PB5	A17		TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/CTX1		
35	PLLVCC						
36		PB4	A16	POE8#/GTETRG0		IRQ3-DS	

Table 1.7 List of Pins and Pin Functions (112-Pin LQFP) (2/4)

Pin Number 112-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3, GPT, POE3, CAC)	Communications (SCIc, SCId, RSPI, RIIC, CAN)	Interrupt	S12ADB, AD, DA
38		PB0	A14	MTIOC0D	MOSIA/MOSIB		
39		PA5		MTIOC1A	RXD0/SMISO0/ SSCL0/ MISOA/MISOB		ADTRG1#
40		PA4		MTIOC1B	TXD0/SMOSI0/ SSDA0/RSPCKA/ RSPCKB		ADTRG0#
41		PA3		MTIOC2A	SCK0/SSLA0/SSLB0		
42		PA2		MTIOC2B	RXD2/SMISO2/ SSCL2/ SSLA1/SSLB1		
43		PA1		MTIOC6A	TXD2/SMOSI2/ SSDA2/SSLA2/SSLB2		
44		PA0		MTIOC6C	SCK2/SSLA3/SSLB3		
45	VCC						
46		P96	A13	POE4#	RXD1/SMISO1/SSCL1	IRQ4-DS	
47	VSS						
48		P95		MTIOC6B/ GTIOC4A	TXD1/SMOSI1/SSDA1		
49		P94		MTIOC7A/ GTIOC5A	CTS1#/RTS1#/SS1#		
50		P93		MTIOC7B/ GTIOC6A	CTS2#/RTS2#/SS2#		
51		P92		MTIOC6D/GTIOC4B			
52		P91		MTIOC7C/GTIOC5B			
53		P90		MTIOC7D/GTIOC6B			
54	TRCLK	PG5		POE12#	SCK3		ADTRG#
55	TRDATA3	PG4		GTIOC6B	RXD3/SMISO3/SSCL3	IRQ6	
56	TRDATA2	PG3		GTIOC6A	TXD3/SMOSI3/SSDA3		
57	TRDATA1	PG2			SCK2	IRQ2	
58	TRDATA0	PG1		GTIOC7B	RXD2/SMISO2/SSCL2	IRQ1	
59	TRSYNC	PG0		GTIOC7A	TXD2/SMOSI2/SSDA2	IRQ0	
60		P76	D0/[A0/D0]	MTIOC4D/GTIOC2B			
61		P75	D1/[A1/D1]	MTIOC4C/GTIOC1B			
62		P74	D2/[A2/D2]	MTIOC3D/GTIOC0B			
63		P73	D3/[A3/D3]	MTIOC4B/GTIOC2A			
64		P72	D4/[A4/D4]	MTIOC4A/GTIOC1A			
65		P71	D5/[A5/D5]	MTIOC3B/GTIOC0A			
66		P70	D6/[A6/D6]	POE0#	CTS1#/RTS1#/SS1#	IRQ5-DS	
67		P33	D7/[A7/D7]	MTIOC3A/MTCLKA	SSLA3/SSLB3		
68		P32	D8/[A8/D8]	MTIOC3C/MTCLKB	SSLA2/SSLB2		
69	VCC						
70		P31	D9/[A9/D9]	MTIOC0A/MTCLKC	SSLA1/SSLB1		
71	VSS						
72		P30	D10/[A10/ D10]	MTIOC0B/MTCLKD	SCK0/SSLA0/SSLB0		
73		P24	D11/[A11/D11]		CTS0#/RTS0#/SS0#/ RSPCKA/RSPCKB	IRQ4	

2. CPU

The RX CPU has sixteen general-purpose registers, nine control registers, and one accumulator used for DSP instructions.

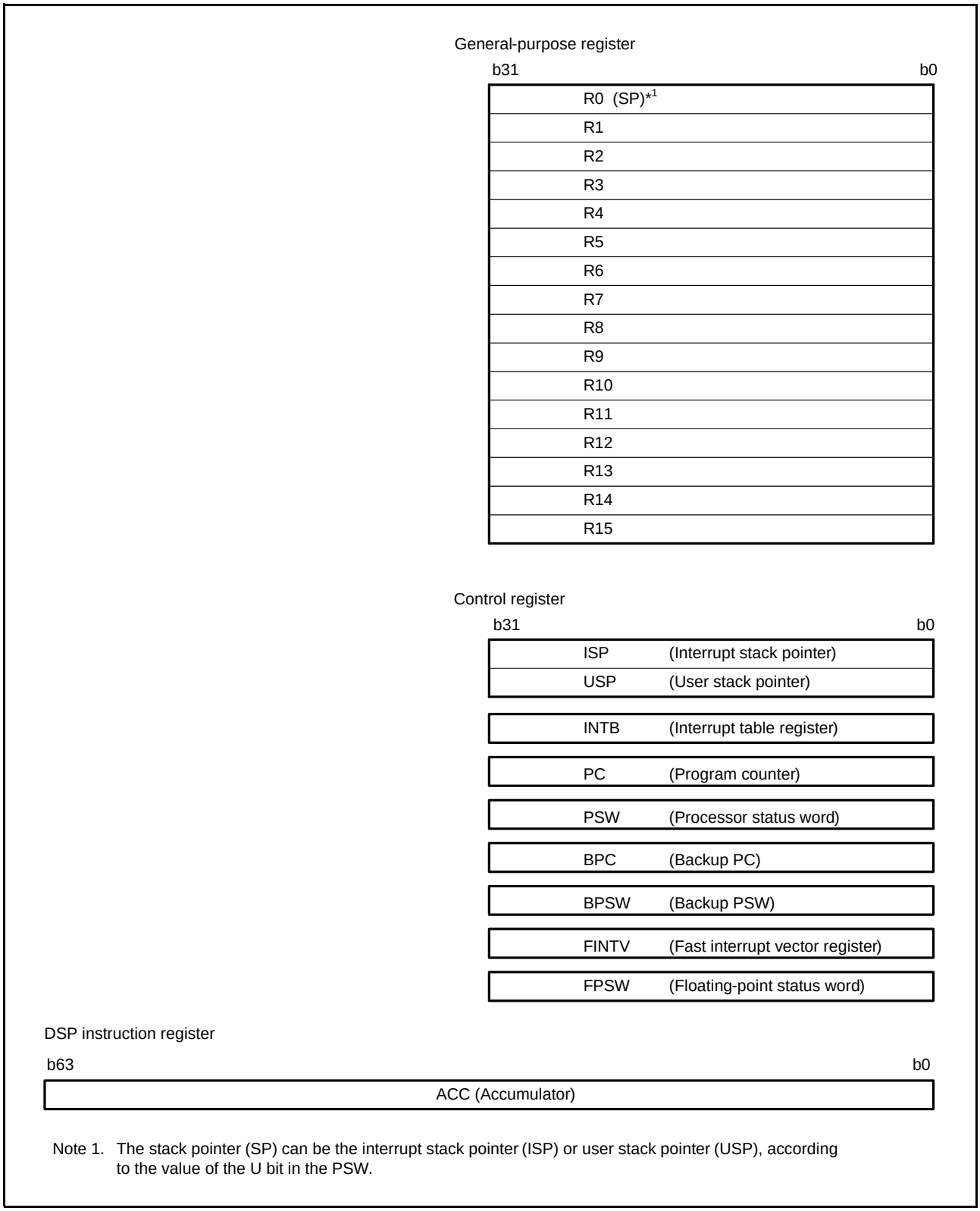


Figure 2.1 Register Set of the CPU

Table 4.1 List of I/O Registers (Address Order) (4/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 7010h	ICU	Interrupt Request Register 016	IR016	8	8	2 ICLK		ICUb	
0008 7015h	ICU	Interrupt Request Register 021	IR021	8	8	2 ICLK			
0008 7017h	ICU	Interrupt Request Register 023	IR023	8	8	2 ICLK			
0008 701Bh	ICU	Interrupt Request Register 027	IR027	8	8	2 ICLK			
0008 701Ch	ICU	Interrupt Request Register 028	IR028	8	8	2 ICLK			
0008 701Dh	ICU	Interrupt Request Register 029	IR029	8	8	2 ICLK			
0008 701Eh	ICU	Interrupt Request Register 030	IR030	8	8	2 ICLK			
0008 701Fh	ICU	Interrupt Request Register 031	IR031	8	8	2 ICLK			
0008 7021h	ICU	Interrupt Request Register 033	IR033	8	8	2 ICLK			Not present in versions with 112, 100, 64 or 48 pins.
0008 7022h	ICU	Interrupt Request Register 034	IR034	8	8	2 ICLK			Not present in versions with 112, 100, 64 or 48 pins.
0008 7023h	ICU	Interrupt Request Register 035	IR035	8	8	2 ICLK			Not present in versions with 112, 100, 64 or 48 pins.
0008 7024h	ICU	Interrupt Request Register 036	IR036	8	8	2 ICLK			
0008 7025h	ICU	Interrupt Request Register 037	IR037	8	8	2 ICLK			
0008 7026h	ICU	Interrupt Request Register 038	IR038	8	8	2 ICLK			
0008 7027h	ICU	Interrupt Request Register 039	IR039	8	8	2 ICLK			
0008 7028h	ICU	Interrupt Request Register 040	IR040	8	8	2 ICLK			
0008 7029h	ICU	Interrupt Request Register 041	IR041	8	8	2 ICLK			
0008 702Ah	ICU	Interrupt Request Register 042	IR042	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 702Bh	ICU	Interrupt Request Register 043	IR043	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 702Ch	ICU	Interrupt Request Register 044	IR044	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 702Dh	ICU	Interrupt Request Register 045	IR045	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 702Eh	ICU	Interrupt Request Register 046	IR046	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 702Fh	ICU	Interrupt Request Register 047	IR047	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7030h	ICU	Interrupt Request Register 048	IR048	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7031h	ICU	Interrupt Request Register 049	IR049	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7032h	ICU	Interrupt Request Register 050	IR050	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7033h	ICU	Interrupt Request Register 051	IR051	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7034h	ICU	Interrupt Request Register 052	IR052	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7035h	ICU	Interrupt Request Register 053	IR053	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7036h	ICU	Interrupt Request Register 054	IR054	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7037h	ICU	Interrupt Request Register 055	IR055	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7038h	ICU	Interrupt Request Register 056	IR056	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7039h	ICU	Interrupt Request Register 057	IR057	8	8	2 ICLK			
0008 703Ah	ICU	Interrupt Request Register 058	IR058	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 703Bh	ICU	Interrupt Request Register 059	IR059	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 703Ch	ICU	Interrupt Request Register 060	IR060	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 703Dh	ICU	Interrupt Request Register 061	IR061	8	8	2 ICLK			Not present in versions with 64 or 48 pins.

Table 4.1 List of I/O Registers (Address Order) (9/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 717Fh	ICU	DTC Activation Enable Register 127	DTCER127	8	8	2 ICLK		ICUb	
0008 7180h	ICU	DTC Activation Enable Register 128	DTCER128	8	8	2 ICLK			
0008 7181h	ICU	DTC Activation Enable Register 129	DTCER129	8	8	2 ICLK			
0008 7185h	ICU	DTC Activation Enable Register 133	DTCER133	8	8	2 ICLK			
0008 7186h	ICU	DTC Activation Enable Register 134	DTCER134	8	8	2 ICLK			
0008 7189h	ICU	DTC Activation Enable Register 137	DTCER137	8	8	2 ICLK			
0008 718Ah	ICU	DTC Activation Enable Register 138	DTCER138	8	8	2 ICLK			
0008 718Dh	ICU	DTC Activation Enable Register 141	DTCER141	8	8	2 ICLK			
0008 718Eh	ICU	DTC Activation Enable Register 142	DTCER142	8	8	2 ICLK			
0008 718Fh	ICU	DTC Activation Enable Register 143	DTCER143	8	8	2 ICLK			
0008 7190h	ICU	DTC Activation Enable Register 144	DTCER144	8	8	2 ICLK			
0008 7192h	ICU	DTC Activation Enable Register 146	DTCER146	8	8	2 ICLK			
0008 7193h	ICU	DTC Activation Enable Register 147	DTCER147	8	8	2 ICLK			
0008 7194h	ICU	DTC Activation Enable Register 148	DTCER148	8	8	2 ICLK			
0008 7195h	ICU	DTC Activation Enable Register 149	DTCER149	8	8	2 ICLK			
0008 7196h	ICU	DTC Activation Enable Register 150	DTCER150	8	8	2 ICLK			
0008 7197h	ICU	DTC Activation Enable Register 151	DTCER151	8	8	2 ICLK			
0008 7198h	ICU	DTC Activation Enable Register 152	DTCER152	8	8	2 ICLK			
0008 7199h	ICU	DTC Activation Enable Register 153	DTCER153	8	8	2 ICLK			
0008 719Ah	ICU	DTC Activation Enable Register 154	DTCER154	8	8	2 ICLK			
0008 719Bh	ICU	DTC Activation Enable Register 155	DTCER155	8	8	2 ICLK			
0008 719Ch	ICU	DTC Activation Enable Register 156	DTCER156	8	8	2 ICLK			
0008 719Dh	ICU	DTC Activation Enable Register 157	DTCER157	8	8	2 ICLK			
0008 71A1h	ICU	DTC Activation Enable Register 161	DTCER161	8	8	2 ICLK			
0008 71A2h	ICU	DTC Activation Enable Register 162	DTCER162	8	8	2 ICLK			
0008 71A3h	ICU	DTC Activation Enable Register 163	DTCER163	8	8	2 ICLK			
0008 71A4h	ICU	DTC Activation Enable Register 164	DTCER164	8	8	2 ICLK			
0008 71A5h	ICU	DTC Activation Enable Register 165	DTCER165	8	8	2 ICLK			
0008 71ABh	ICU	DTC Activation Enable Register 171	DTCER171	8	8	2 ICLK			
0008 71ACh	ICU	DTC Activation Enable Register 172	DTCER172	8	8	2 ICLK			
0008 71ADh	ICU	DTC Activation Enable Register 173	DTCER173	8	8	2 ICLK			
0008 71AEh	ICU	DTC Activation Enable Register 174	DTCER174	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 71AFh	ICU	DTC Activation Enable Register 175	DTCER175	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 71B0h	ICU	DTC Activation Enable Register 176	DTCER176	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 71B1h	ICU	DTC Activation Enable Register 177	DTCER177	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 71B2h	ICU	DTC Activation Enable Register 178	DTCER178	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 71B3h	ICU	DTC Activation Enable Register 179	DTCER179	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 71B4h	ICU	DTC Activation Enable Register 180	DTCER180	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 71B5h	ICU	DTC Activation Enable Register 181	DTCER181	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 71B6h	ICU	DTC Activation Enable Register 182	DTCER182	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 71B7h	ICU	DTC Activation Enable Register 183	DTCER183	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 71B8h	ICU	DTC Activation Enable Register 184	DTCER184	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 71B9h	ICU	DTC Activation Enable Register 185	DTCER185	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 71BAh	ICU	DTC Activation Enable Register 186	DTCER186	8	8	2 ICLK			Not present in versions with 64 or 48 pins.

Table 4.1 List of I/O Registers (Address Order) (24/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 C086h	PORT3	Open Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK	I/O Ports	Not present in versions with 144, 120, 112, or 100 pins.
0008 C087h	PORT3	Open Drain Control Register 1	ODR1	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64 or 48 pins.
0008 C090h	PORT8	Open Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C092h	PORT9	Open Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 144, 120, 112, 100 or 48 pins.
0008 C093h	PORT9	Open Drain Control Register 1	ODR1	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 48 pins.
0008 C094h	PORTA	Open Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C095h	PORTA	Open Drain Control Register 1	ODR1	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C096h	PORTB	Open Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK		
0008 C097h	PORTB	Open Drain Control Register 1	ODR1	8	8	2, 3 PCLKB	2 ICLK		
0008 C09Ah	PORTD	Open Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK		
0008 C09Bh	PORTD	Open Drain Control Register 1	ODR1	8	8	2, 3 PCLKB	2 ICLK		
0008 C09Eh	PORTF	Open Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 100, 64, or 48 pins.
0008 C0A0h	PORTG	Open Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 100, 64, or 48 pins.
0008 C0A1h	PORTG	Open Drain Control Register 1	ODR1	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 100, 64, or 48 pins.
0008 C0F2h	PORT	Driving Ability Control Register 1	DSCR1	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C0F3h	PORT	Driving Ability Control Register 2	DSCR2	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C100h	MPC	CS Output Enable Register	PFCSE	8	8	2, 3 PCLKB	2 ICLK	MPC	Not present in versions with 64 or 48 pins.
0008 C102h	MPC	CS Output Pin Select Register 0	PFCSS0	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C104h	MPC	Address Output Enable Register 0	PFAOE0	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C105h	MPC	Address Output Enable Register 1	PFAOE1	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C106h	MPC	External Bus Control Register 0	PFBCR0	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C107h	MPC	External Bus Control Register 1	PFBCR1	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C114h	MPC	USB0 Control Register	PFUSB0	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
0008 C11Fh	MPC	Write-Protect Register	PWPR	8	8	2, 3 PCLKB	2 ICLK		
0008 C140h	MPC	P00 Pin Function Control Register	P00PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 48 pins.
0008 C141h	MPC	P01 Pin Function Control Register	P01PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 48 pins.
0008 C142h	MPC	P02 Pin Function Control Register	P02PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 C143h	MPC	P03 Pin Function Control Register	P03PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 C148h	MPC	P10 Pin Function Control Register	P10PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 48 pins.
0008 C149h	MPC	P11 Pin Function Control Register	P11PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 48 pins.
0008 C14Ah	MPC	P12 Pin Function Control Register	P12PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 100, 64, or 48 pins.
0008 C14Bh	MPC	P13 Pin Function Control Register	P13PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 112, 100, 64, or 48 pins.

Table 4.1 List of I/O Registers (Address Order) (41/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
000C 22BAh	GPT3	General PWM Timer Dead Time Value Register D	GTDVD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK	GPT	
000C 22BCh	GPT3	General PWM Timer Dead Time Buffer Register U	GTDBU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 22BEh	GPT3	General PWM Timer Dead Time Buffer Register D	GTDBD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 22C0h	GPT3	General PWM Timer Output Protection Function Status Register	GTSOS	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 22C2h	GPT3	General PWM Timer Output Protection Function Temporary Release Register	GTSOTR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2318h	GPT0	GTIOCA Rising Output Delay Register	GTDLYRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64, or 48 pins.
000C 231Ah	GPT0	GTIOCB Rising Output Delay Register	GTDLYRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64, or 48 pins.
000C 231Ch	GPT1	GTIOCA Rising Output Delay Register	GTDLYRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64, or 48 pins.
000C 231Eh	GPT1	GTIOCB Rising Output Delay Register	GTDLYRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64, or 48 pins.
000C 2320h	GPT2	GTIOCA Rising Output Delay Register	GTDLYRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64, or 48 pins.
000C 2322h	GPT2	GTIOCB Rising Output Delay Register	GTDLYRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64, or 48 pins.
000C 2324h	GPT3	GTIOCA Rising Output Delay Register	GTDLYRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64, or 48 pins.
000C 2326h	GPT3	GTIOCB Rising Output Delay Register	GTDLYRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64, or 48 pins.
000C 2328h	GPT0	GTIOCA Falling Output Delay Register	GTDLYFA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64, or 48 pins.
000C 232Ah	GPT0	GTIOCB Falling Output Delay Register	GTDLYFB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64, or 48 pins.
000C 232Ch	GPT1	GTIOCA Falling Output Delay Register	GTDLYFA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64, or 48 pins.
000C 232Eh	GPT1	GTIOCB Falling Output Delay Register	GTDLYFB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64, or 48 pins.
000C 2330h	GPT2	GTIOCA Falling Output Delay Register	GTDLYFA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64, or 48 pins.
000C 2332h	GPT2	GTIOCB Falling Output Delay Register	GTDLYFB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64, or 48 pins.
000C 2334h	GPT3	GTIOCA Falling Output Delay Register	GTDLYFA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64, or 48 pins.
000C 2336h	GPT3	GTIOCB Falling Output Delay Register	GTDLYFB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64, or 48 pins.
000C 2800h	GPTB	General PWM Timer Software Start Register	GTSTR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64, or 48 pins.
000C 2804h	GPTB	General PWM Timer Hardware Source Start Control Register	GTHSCR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64, or 48 pins.
000C 2806h	GPTB	General PWM Timer Hardware Source Clear Control Register	GTHCCR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64, or 48 pins.
000C 2808h	GPTB	General PWM Timer Hardware Start Source Select Register	GTHSSR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64, or 48 pins.
000C 280Ah	GPTB	General PWM Timer Hardware Stop/Clear Source Select Register	GTHPSR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64, or 48 pins.
000C 280Ch	GPTB	General PWM Timer Write-Protection Register	GTWP	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64, or 48 pins.
000C 280Eh	GPTB	General PWM Timer Sync Register	GTSYNC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64, or 48 pins.
000C 2810h	GPTB	General PWM Timer External Trigger Input Interrupt Register	GTETINT	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64, or 48 pins.
000C 2814h	GPTB	General PWM Timer Buffer Operation Disable Register	GTBDR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64, or 48 pins.
000C 2818h	GPTB	General PWM Timer Start Write-Protection Register	GTSWP	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64, or 48 pins.
000C 2880h	GPTB	LOCO Count Control Register	LCCR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64, or 48 pins.
000C 2882h	GPTB	LOCO Count Status Register	LCST	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64, or 48 pins.

Table 4.1 List of I/O Registers (Address Order) (45/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
000C 2A24h	GPT6	A/D Converter Start Request Timing Register A	GTADTRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK	GPT	Not present in versions with 64 or 48 pins.
000C 2A26h	GPT6	A/D Converter Start Request Timing Buffer Register A	GTADTBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A28h	GPT6	A/D Converter Start Request Timing Double-Buffer Register A	GTADTDBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A2Ch	GPT6	A/D Converter Start Request Timing Register B	GTADTRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A2Eh	GPT6	A/D Converter Start Request Timing Buffer Register B	GTADTBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A30h	GPT6	A/D Converter Start Request Timing Double-Buffer Register B	GTADTDBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A34h	GPT6	General PWM Timer Output Negate Control Register	GTONCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A36h	GPT6	General PWM Timer Dead Time Control Register	GTDTCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A38h	GPT6	General PWM Timer Dead Time Value Register U	GTDVU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A3Ah	GPT6	General PWM Timer Dead Time Value Register D	GTDVD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A3Ch	GPT6	General PWM Timer Dead Time Buffer Register U	GTDBU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A3Eh	GPT6	General PWM Timer Dead Time Buffer Register D	GTDBD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A40h	GPT6	General PWM Timer Output Protection Function Status Register	GTSOS	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A42h	GPT6	General PWM Timer Output Protection Function Temporary Release Register	GTSOTR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A80h	GPT7	General PWM Timer I/O Control Register	GTIOR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A82h	GPT7	General PWM Timer Interrupt Output Setting Register	GTINTAD	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A84h	GPT7	General PWM Timer Control Register	GTCR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A86h	GPT7	General PWM Timer Buffer Enable Register	GTBER	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A88h	GPT7	General PWM Timer Count Direction Register	GTUDC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A8Ah	GPT7	General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register	GTITC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A8Ch	GPT7	General PWM Timer Status Register	GTST	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A8Eh	GPT7	General PWM Timer Counter	GTCNT	16	16	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A90h	GPT7	General PWM Timer Compare Capture Register A	GTCCRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A92h	GPT7	General PWM Timer Compare Capture Register B	GTCCRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A94h	GPT7	General PWM Timer Compare Capture Register C	GTCCRC	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A96h	GPT7	General PWM Timer Compare Capture Register D	GTCCRD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A98h	GPT7	General PWM Timer Compare Capture Register E	GTCCRE	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A9Ah	GPT7	General PWM Timer Compare Capture Register F	GTCCRF	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A9Ch	GPT7	General PWM Timer Cycle Setting Register	GTPR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A9Eh	GPT7	General PWM Timer Cycle Setting Buffer Register	GTPBR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2AA0h	GPT7	General PWM Timer Cycle Setting Double-Buffer Register	GTPDBR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2AA4h	GPT7	A/D Converter Start Request Timing Register A	GTADTRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2AA6h	GPT7	A/D Converter Start Request Timing Buffer Register A	GTADTBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.

Table 4.1 List of I/O Registers (Address Order) (47/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
000C3056h	DPC	Control Calculation Parameter Setting Register KQ2	PARAMKQ2	16	16	3 to 5 PCLKA	2, 3 ICLK	DPC	Not present in versions with 64 or 48 pins.
000C305Ah	DPC	Control Calculation Parameter Setting Register KF2	PARAMKF2	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C305Eh	DPC	Control Calculation Parameter Setting Register KP3	PARAMKP3	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3062h	DPC	Control Calculation Parameter Setting Register KI3	PARAMKI3	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3066h	DPC	Control Calculation Parameter Setting Register KQ3	PARAMKQ3	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C306Ah	DPC	Control Calculation Parameter Setting Register KF3	PARAMKF3	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C306Ch	DPC	Control Calculation Result Higher-Order Bits Store Register 0	RESULTU0	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C306Eh	DPC	Control Calculation Result Lower-Order Bits Store Register 0	RESULTL0	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3070h	DPC	Control Calculation Result Higher-Order Bits Store Register 1	RESULTU1	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3072h	DPC	Control Calculation Result Lower-Order Bits Store Register 1	RESULTL1	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3074h	DPC	Control Calculation Result Higher-Order Bits Store Register 2	RESULTU2	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3076h	DPC	Control Calculation Result Lower-Order Bits Store Register 2	RESULTL2	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3078h	DPC	Control Calculation Result Higher-Order Bits Store Register 3	RESULTU3	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C307Ah	DPC	Control Calculation Result Lower-Order Bits Store Register 3	RESULTL3	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C307Eh	DPC	Input Code Monitor Enable Register	TMONEN	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3082h	DPC	Maximum Input Code Monitor Register 0	TMONMAX0	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3086h	DPC	Minimum Input Code Monitor Register 0	TMONMIN0	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C308Ah	DPC	Maximum Input Code Monitor Register 1	TMONMAX1	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C308Eh	DPC	Minimum Input Code Monitor Register 1	TMONMIN1	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3092h	DPC	Maximum Input Code Monitor Register 2	TMONMAX2	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3096h	DPC	Minimum Input Code Monitor Register 2	TMONMIN2	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C309Ah	DPC	Maximum Input Code Monitor Register 3	TMONMAX3	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C309Eh	DPC	Minimum Input Code Monitor Register 3	TMONMIN3	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C30A2h	DPC	Overvoltage Output Error Judgment Threshold Setting Register 0	ERRVTH0	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C30A6h	DPC	Overvoltage Output Error Judgment Threshold Setting Register 1	ERRVTH1	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C30AAh	DPC	Overvoltage Output Error Judgment Threshold Setting Register 2	ERRVTH2	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C30AEh	DPC	Overvoltage Output Error Judgment Threshold Setting Register 3	ERRVTH3	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C30B2h	DPC	PWM Shut-Down at Overvoltage Output Error Setting Register	ERRDWN	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
007F C402h	FLASH	Flash Mode Register	FMODR	8	8	2, 3 FCLK	2, 3 ICLK	ROM/ E2 DataFlash Memory	
007F C410h	FLASH	Flash Access Status Register	FASTAT	8	8	2, 3 FCLK	2, 3 ICLK		
007F C411h	FLASH	Flash Access Error Interrupt Enable Register	FAEINT	8	8	2, 3 FCLK	2, 3 ICLK		
007F C412h	FLASH	Flash Ready Interrupt Enable Register	FRDYIE	8	8	2, 3 FCLK	2, 3 ICLK	ROM	
007F C440h	FLASH	E2 DataFlash Read Enable Register 0	DFLRE0	16	16	2, 3 FCLK	2, 3 ICLK	E2 DataFlash Memory	
007F C442h	FLASH	E2 DataFlash Read Enable Register 1	DFLRE1	16	16	2, 3 FCLK	2, 3 ICLK		
007F C450h	FLASH	E2 DataFlash P/E Enable Register 0	DFLWE0	16	16	2, 3 FCLK	2, 3 ICLK		
007F C452h	FLASH	E2 DataFlash P/E Enable Register 1	DFLWE1	16	16	2, 3 FCLK	2, 3 ICLK		

5.3.6 Timing of On-Chip Peripheral Modules

Table 5.16 Timing of On-Chip Peripheral Modules (1)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
I/O ports	Input data pulse width		t_{PRW}	1.5	—	t_{Pcyc}	Figure 5.22
MTU3	Input capture input pulse width	Single-edge setting	t_{TICW}	3	—	t_{PAcyc}	Figure 5.23
		Both-edge setting		5	—		
	Input capture input fall time		t_{TICTF}	—	0.1	µs/V	When Input capture at rising edge, or Input capture at both edges is selected.
	Timer clock pulse width	Single-edge setting	t_{TCKWH}, t_{TCKWL}	3	—	t_{PAcyc}	Figure 5.25
		Both-edge setting		5	—		
		Phase counting mode		5	—		
	Timer clock input fall time		t_{TCKTF}	—	0.1	µs/V	
POE3	POE# input pulse width		t_{POEW}	1.5	—	t_{Pcyc}	Figure 5.28
GPT	Input capture input pulse width	Single-edge setting	t_{GTICW}	3	—	t_{PAcyc}	Figure 5.26
		Both-edge setting		5	—		
	Input capture input fall time		t_{GTICTF}	—	0.1	µs/V	When Input capture at rising edge, or Input capture at both edges is selected. When Count operation is started at rising edge, or Count operation is started at both edges is selected. When Count operation is stopped at rising edge, or Count operation is stopped at both edges is selected. When Counter is cleared at rising edge, or Counter is cleared at both edges is selected.
	External trigger input pulse width	Single-edge setting	t_{OTETW}	3	—	t_{PAcyc}	Figure 5.27
		Both-edge setting		5	—		
	External trigger input fall time		$t_{GTETRGTF}$	—	0.1	µs/V	When Count operation is started at rising edge, or Count operation is started at both edges is selected. When Count operation is stopped at rising edge, or Count operation is stopped at both edges is selected. When Counter is cleared at rising edge, or Counter is cleared at both edges is selected.

Table 5.16 Timing of On-Chip Peripheral Modules (2)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
SCI	Input clock cycle	Asynchronous	t_{Scyc}	4	—	t_{Pcyc}	C = 30 pF Figure 5.29
		Clock synchronous		6	—		
	Input clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time		t_{SCKr}	—	20	ns	
	Input clock fall time		t_{SCKf}	—	20	ns	
	Output clock cycle	Asynchronous	t_{Scyc}	16	—	t_{Pcyc}	
		Clock synchronous		4	—		
	Output clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time		t_{SCKr}	—	20	ns	
	Output clock fall time		t_{SCKf}	—	20	ns	
	Transmit data delay time	Clock synchronous	t_{TXD}	—	40	ns	Figure 5.30
	Receive data setup time	Clock synchronous	t_{RXS}	40	—	ns	
	Receive data hold time	Clock synchronous	t_{RXH}	40	—	ns	
	Receive data fall time		t_{TICTF}	—	0.1	µs/V	When Noise Cancellation Function is not used.
A/D converter	10-bit A/D converter trigger input pulse width		t_{TRGW}	1.5	—	t_{Pcyc}	Figure 5.31
	12-bit A/D converter trigger input pulse width			1.5	—		
CAC	CACREF input pulse width	$t_{Pcyc} \leq t_{cac}$*2	t_{CACREF}	4.5 t_{cac} + 3 t_{Pcyc}	—	ns	
		$t_{Pcyc} > t_{cac}$*2		5 t_{cac} + 6.5 t_{Pcyc}	—	ns	
	CACREF input fall time		$t_{CACREFTF}$	—	0.1	µs/V	

Note 1. t_{Pcyc}: PCLK cycle, t_{PAcye}: PCLKA cycle
Note 2. t_{cac}: CAC count clock source cycle.

Table 5.16 Timing of On-Chip Peripheral Modules (3)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS =PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

High drive output is selected by the drive capacity control register.

Item				Symbol	Min.	Max.	Unit*1	Test Conditions
RSPI	RSPCK clock cycle	Master		t_{SPcyc}	2	4096	t_{Pcyc}	C = 30 pF, Figure 5.32
		Slave			8	4096		
	RSPCK clock high pulse width	Master		t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2 - 3$	—	ns	
		Slave			$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2$	—		
	RSPCK clock low pulse width	Master		t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2 - 3$	—	ns	
		Slave			$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2$	—		
	RSPCK clock rise/fall time	Output		t_{SPCKR}, t_{SPCKF}	—	5	ns	
		Input			—	1	µs	
	RSPCK clock fall time	Input		t_{SPCKF}	—	0.1	µs/V	
	Data input setup time	Master		t_{SU}	4	—	ns	C = 30 pF, Figure 5.33 to Figure 5.40
		Slave			$20 - t_{Pcyc}$	—		
	Data input hold time	Master	PCLKB division ratio set to a value other than 1/2	t_H	t_{Pcyc}	—	ns	
			PCLKB division ratio set to 1/2	t_{HF}	0	—		
		Slave		t_H	$20 + 2 \times t_{Pcyc}$	—		
	SSL setup time	Master		t_{LEAD}	1	8	t_{SPcyc}	
		Slave			4	—	t_{Pcyc}	
	SSL hold time	Master		t_{LAG}	1	8	t_{SPcyc}	
		Slave			4	—	t_{Pcyc}	
	Data output delay time	Master		t_{OD}	—	10	ns	
		Slave			—	$3 \times t_{Pcyc} + 40$		
	Data output hold time	Master		t_{OH}	0	—	ns	
		Slave			0	—		
	Successive transmission delay time	Master		t_{TD}	$t_{SPcyc} + 2 \times t_{Pcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	ns	
		Slave			$4 \times t_{Pcyc}$	—		
	MOSI and MISO rise/fall time	Output		t_{DR}, t_{DF}	—	5	ns	
		Input			—	1	µs	
	SSL rise/fall time	Output		t_{SSLr}, t_{SSLf}	—	15	ns	
		Input			—	1	µs	
	Slave access time			t_{SA}	—	4	t_{Pcyc}	Figure 5.39 and Figure 5.40
	Slave output release time			t_{REL}	—	3	t_{Pcyc}	

Note 1. t_{Pcyc}: PCLK cycle

Table 5.16 Timing of On-Chip Peripheral Modules (4)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item		Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI	SCK clock cycle output (master)	t_{SPcyc}	4	65536	t_{Pcyc}	C = 30 pF, Figure 5.30
	SCK clock cycle input (slave)		8	65536		
	SCK clock high pulse width	t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width	t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise/fall time	t_{SPCKR}, t_{SPCKF}	—	20	ns	
	Data input setup time	t_{SU}	40	—	ns	C = 30 pF, Figure 5.31 to Figure 5.38
	Data input hold time	t_H	40	—	ns	
	SS input setup time	t_{LEAD}	6	—	t_{Pcyc}	
	SS input hold time	t_{LAG}	6	—	t_{Pcyc}	
	Data output delay time	t_{OD}	—	40	ns	
	Data output hold time	t_{OH}	–10	—	ns	
	Data rise/fall time	t_{DR}, t_{DF}	—	20	ns	
	SS input rise/fall time	t_{SSLr}, t_{SSLf}	—	20	ns	
	Slave access time	t_{SA}	—	5	t_{Pcyc}	C = 30 pF, Figure 5.37 and Figure 5.38
	Slave output release time	t_{REL}	—	5	t_{Pcyc}	

Note 1. t_{Pcyc}: PCLK cycle

Table 5.16 Timing of On-Chip Peripheral Modules (6)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item		Symbol	Min.*1, *2	Max.	Unit	Test Conditions
Simple IIC (Standard-mode)	SCL, SDA input rise time	t_{Sr}	—	1000	ns	Figure 5.36
	SCL, SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	$4 \times t_{Pcyc}$	ns	
	Data input setup time	t_{SDAS}	250	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
Simple IIC (Fast-mode)	SCL, SDA input rise time	t_{Sr}	$20 + 0.1C_b$	300	ns	
	SCL, SDA input fall time	t_{Sf}	$20 + 0.1C_b$	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	$4 \times t_{Pcyc}$	ns	
	Data input setup time	t_{SDAS}	100	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note 1. The value in parentheses is used when ICMR3.NF[1:0] are set to 11b while a digital filter is enabled with ICFER.NFE = 1.
Note 2. Cb indicates the total capacity of the bus line.
Note 3. t_{Pcyc}: PCLK cycle

5.3.7 Timing of PWM Delay Generation Circuit

Table 5.17 Timing of the PWM Delay Generation Circuit

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Ta = Topr. Ta is common to conditions 1 to 3.

Item	Symbol	Typ.	Max.	Unit	Test Conditions
Resolution	—	312.5	—	ps	PCLKA = 100 MHz
DNL*1	—	±2.0	—	LSB	

Note 1. This value is correct when the difference between each code and the next is a resolution of one bit (1 LSB).

Table 6.3 DC Characteristics (2)

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Supply current*1	During operation	Max. *2	I_{CC}*3	—	—	60	mA	ICLK = 100MHz PCLKA = 100MHz PCLKB = 50MHz PCLKD = 50MHz FCLK = 50MHz
		Normal *4		—	25	—		
		Increased by BGO operation*5		—	15	—		
	Sleep mode				25	35		
	All-module-clock-stop mode*6				14	25		
	During standby	Software standby mode		—	0.2	6	mA	
		Deep software standby mode		—	16	40	µA	
Analog power supply current	During 12-bit A/D conversion (sample & hold circuit in use)		AI_{CC0}	—	3	4	mA	
	During 12-bit A/D conversion (sample & hold circuit not in use)			—	2	3	mA	
	Window comparator (1-channel operation)				0.4	1	mA	
	Window comparator (3-channel operation)			—	0.5	1	mA	
	Waiting for 12-bit AD conversion			—	25	32	µA	
Reference power supply current	During 12-bit A/D conversion		AI_{REFH0}	—	0.6	0.7	mA	
	Waiting for 12-bit A/D conversion			—	0.6	0.7	mA	
VCC rising gradient			SrVcc	—	—	20000	ms/V	

Note 1. Supply current values are with all output pins unloaded.
Note 2. Measured with clocks supplied to the peripheral functions. This does not include the BGO operation.
Note 3. I_{CC} depends on f (ICLK) as follows. (ICLK: PCLK = 8:4)
ICC max = 0.45 × f + 15 (Max)
ICC typ = 0.18 × f + 7 (Normal)
ICC max = 0.22 × f + 13 (sleep mode)
Note 4. Measured with clocks not supplied to the peripheral functions. This does not include the BGO operation.
Note 5. Incremented if data is written to or erased from the on-chip ROM or on-chip data-flash memory for data storage during the program execution.
Note 6. The values are for reference.

Table 6.4 Permissible Output Currents

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item	Symbol	Min.	Typ.	Max.	Unit
Permissible output low current (average value per pin)	I_{OL}	—	—	2.0*1	mA
Permissible output low current (max. value per pin)	I_{OL}	—	—	4.0*1	mA
Permissible output low current (total)	ΣI_{OL}	—	—	32	mA
Permissible output high current (average value per pin)	$-I_{OH}$	—	—	2.0	mA
Permissible output high current (max. value per pin)	$-I_{OH}$	—	—	4.0	mA
Permissible output high current (total)	$\Sigma-I_{OH}$	—	—	32	mA

Caution: To protect the MCU's reliability, the output current values should not exceed the values in this table.
Note 1. RIIC pin: IOL = 6 mA (max.)

6.3 AC Characteristics

Table 6.6 Operation Frequency Value

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item		Symbol	Min.	Typ	Max.	Unit
Operation frequency	System clock (ICLK)	f	—	—	100	MHz
	Peripheral module clock PCLK		—	—	50	
	Timer module clock (PCLKA)		—	—	100	
	S12AD clock (PCLKD)		—	—	50	
	Flash clock (FCLK)		—*1	—	50	

Note 1. The FCLK must run at a frequency of at least 4 MHz when changing the ROM or E2 DataFlash memory contents.

6.3.1 Clock Timing

Table 6.7 Clock Timing

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item		Symbol	Min	Typ	Max.	Unit	Test Conditions
EXTAL external clock input cycle time		t_{EXcyc}	50	—	—	ns	Figure 6.1
EXTAL external clock input high pulse width		t_{EXH}	20	—	—	ns	
EXTAL external clock input low pulse width		t_{EXL}	20	—	—	ns	
EXTAL external clock rising time		t_{EXr}	—	—	5	ns	
EXTAL external clock falling time		t_{EXf}	—	—	5	ns	
EXTAL external clock input wait time*1		t_{EXWT}	1	—	—	ms	
Main clock oscillator oscillation frequency		f_{MAIN}	4	—	16	MHz	
Main clock oscillation stabilization time (crystal)		$t_{MAINOSC}$	—	—	—*2	ms	Figure 6.2
Main clock oscillation stabilization wait time (crystal)		$t_{MAINOSCWT}$	—	—	—*3	ms	
LOCO, IWDTCLK clock cycle time		t_{cyc}	6.96	8	9.4	µs	
LOCO, IWDTCLK clock oscillation frequency		f_{LOCO}	106.25	125	143.75	kHz	
LOCO, IWDTCLK clock oscillation stabilization wait time		t_{LOCOWT}	—	—	20	µs	Figure 6.2
PLL clock oscillation stabilization time	PLL operation started after main clock oscillation has settled	t_{PLL1}	—	—	500	µs	Figure 6.4
PLL clock oscillation stabilization wait time		t_{PLLWT1}	—	—	—*4	ms	
PLL clock oscillation stabilization time PLL	PLL operation started before main clock oscillation has settled	t_{PLL2}	—	—	$t_{MAINOSC}$ + t_{PLL1}	ms	Figure 6.5
PLL clock oscillation stabilization wait time		t_{PLLWT2}	—	—	—*4	ms	

Note 1. This is the time until the clock is used after clearing the main clock oscillator stop bit (MOSCCR.MOSTP) to 0 (selecting operation).
Note 2. When using a main clock, ask the manufacturer of the oscillator to evaluate its oscillation. Refer to the results of evaluation provided by the manufacturer for the oscillation stabilization time.
Note 3. This is calculated from the formula below, where n is the number of cycles set by the MOSCWTCR.MSTS[4:0] bits.

$$t_{MAINOSCWT} = t_{MAINOSC} + \frac{n + 16384}{f_{MAIN}}$$

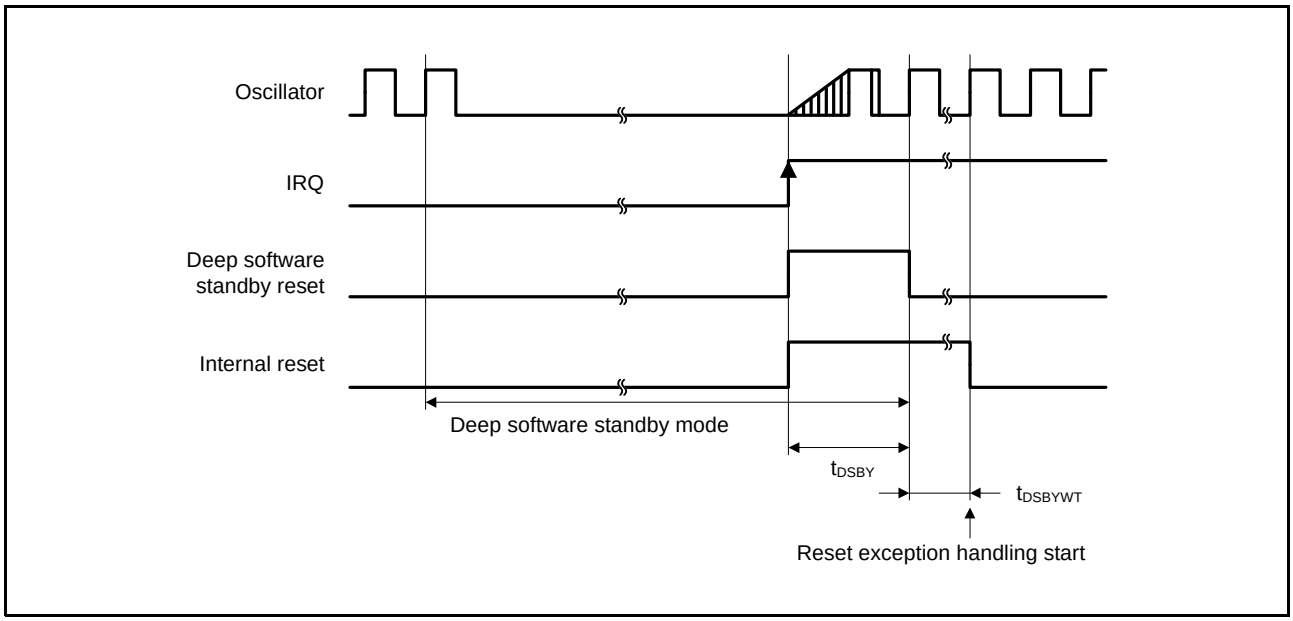


Figure 6.9 Deep Software Standby Mode Cancellation Timing

6.3.4 Control Signal Timing

Table 6.10 Control Signal Timing

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
NMI pulse width	t_{NMIW}	200	—	—	ns	t_{Pcyc} × 2 ≤ 200ns, Figure 6.10
		2			t_{Pcyc}	t_{Pcyc} × 2 > 200ns, Figure 6.10
IRQ pulse width	t_{IRQW}	200	—	—	ns	t_{Pcyc} × 2 ≤ 200ns, Figure 6.11
		2			t_{Pcyc}	t_{Pcyc} × 2 > 200ns, Figure 6.11

Note 1. t_{Pcyc}: PCLK cycle

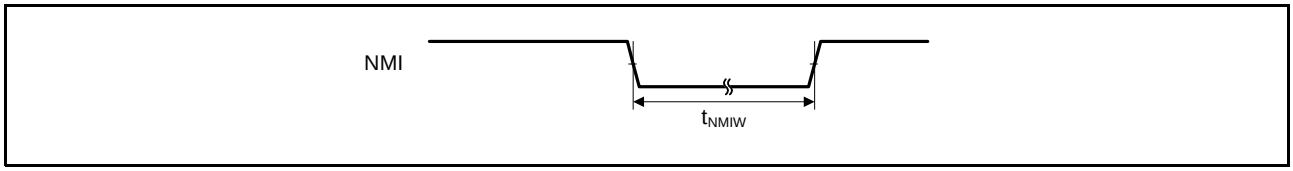


Figure 6.10 NMI Interrupt Input Timing

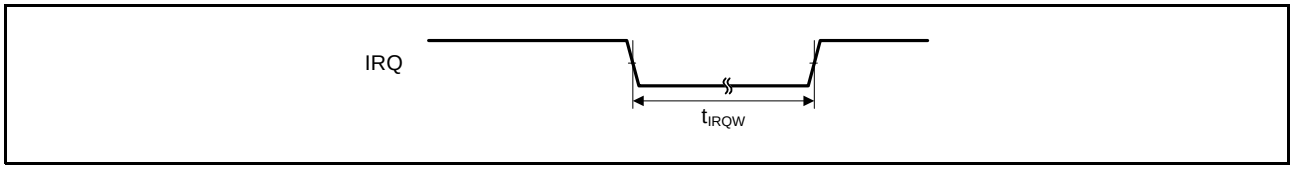


Figure 6.11 IRQ Interrupt Input Timing

Table 6.14 Timing of On-Chip Peripheral Modules (4)

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item		Symbol	Min.	Max.	Unit	Test Conditions
RIIC (Standard-mode)	SCL input cycle time	t_{SCL}	6(12) × t_{IICcyc} + 1300	—	ns	Figure 6.25
	SCL input high pulse width	t_{SCLH}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA input rise time	t_{Sr}	—	1000	ns	
	SCL, SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	3(6) × t_{IICcyc} + 300	—	ns	
	Start condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Restart condition input setup time	t_{STAS}	1000	—	ns	
	Stop condition input setup time	t_{STOS}	1000	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
RIIC (Fast-mode)	SCL input cycle time	t_{SCL}	6(12) × t_{IICcyc} + 600	—	ns	
	SCL input high pulse width	t_{SCLH}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA input rise time	t_{Sr}	20 + 0.1C_b	300	ns	
	SCL, SDA input fall time	t_{Sf}	20 + 0.1C_b	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	3(6) × t_{IICcyc} + 300	—	ns	
	Start condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Restart condition input setup time	t_{STAS}	300	—	ns	
	Stop condition input setup time	t_{STOS}	300	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note 1. t_{IICcyc}: RIIC internal reference clock (IICϕ) Cycle
Note 2. The value within parentheses is applicable when the value of the ICMR3.NF[1:0] bits is 11b while the digital filter is enabled by the setting ICFER.NFE = 1.
Note 3. Cb is the total capacitance of the bus lines.