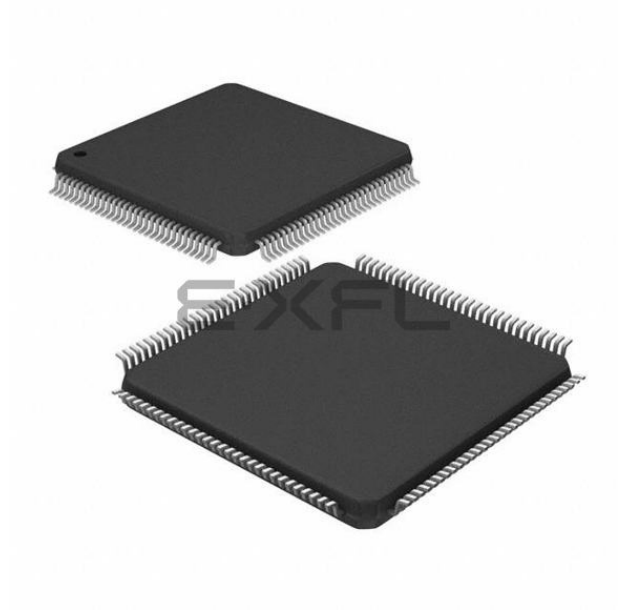
Renesas Electronics America Inc - R5F563TCADFA#V1 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	72
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x10b, 8x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	120-LQFP
Supplier Device Package	120-LQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f563tcadfa-v1

1.2 List of Products

Table 1.3 is a list of products, and Figure 1.1 shows how to read the product part number.

Table 1.3 List of Products (1/4)

Group	Part No.	Order Part No.	Package	On-chip ROM Capacity	On-chip RAM Capacity	Option	Operating Voltage	Operating Temperature
RX63T	R5F563TEADFB	R5F563TEADFB#V0	PLQP0144KA-A	512 Kbytes	48 Kbytes	CAN module included	VCC/ PLLVCC 4.0 to 5.5V VCC_USB 3.0 to 3.6V AVCC/ AVCC0 4.0 to 5.5V	-40 to +85°C (D Version)
	R5F563TEADFB	R5F563TEADFB#V1	PLQP0144KA-A	512 Kbytes	48 Kbytes	CAN module included		
	R5F563TEADFA	R5F563TEADFA#V0	PLQP0120KA-A	512 Kbytes	48 Kbytes	CAN module included		
	R5F563TEADFA	R5F563TEADFA#V1	PLQP0120KA-A	512 Kbytes	48 Kbytes	CAN module included		
	R5F563TEADFH	R5F563TEADFH#V0	PLQP0112JA-A	512 Kbytes	48 Kbytes	CAN module included		
	R5F563TEADFH	R5F563TEADFH#V1	PLQP0112JA-A	512 Kbytes	48 Kbytes	CAN module included		
	R5F563TEADFP	R5F563TEADFP#V0	PLQP0100KB-A	512 Kbytes	48 Kbytes	CAN module included		
	R5F563TEADFP	R5F563TEADFP#V1	PLQP0100KB-A	512 Kbytes	48 Kbytes	CAN module included		
	R5F563TCADFB	R5F563TCADFB#V0	PLQP0144KA-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TCADFB	R5F563TCADFB#V1	PLQP0144KA-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TCADFA	R5F563TCADFA#V0	PLQP0120KA-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TCADFA	R5F563TCADFA#V1	PLQP0120KA-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TCADFH	R5F563TCADFH#V0	PLQP0112JA-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TCADFH	R5F563TCADFH#V1	PLQP0112JA-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TCADFP	R5F563TCADFP#V0	PLQP0100KB-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TCADFP	R5F563TCADFP#V1	PLQP0100KB-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TBADFB	R5F563TBADFB#V0	PLQP0144KA-A	256 Kbytes	24 Kbytes	CAN module included		
	R5F563TBADFB	R5F563TBADFB#V1	PLQP0144KA-A	256 Kbytes	24 Kbytes	CAN module included		
	R5F563TBADFA	R5F563TBADFA#V0	PLQP0120KA-A	256 Kbytes	24 Kbytes	CAN module included		
	R5F563TBADFA	R5F563TBADFA#V1	PLQP0120KA-A	256 Kbytes	24 Kbytes	CAN module included		
	R5F563TBADFH	R5F563TBADFH#V0	PLQP0112JA-A	256 Kbytes	24 Kbytes	CAN module included		
	R5F563TBADFH	R5F563TBADFH#V1	PLQP0112JA-A	256 Kbytes	24 Kbytes	CAN module included		
	R5F563TBADFP	R5F563TBADFP#V0	PLQP0100KB-A	256 Kbytes	24 Kbytes	CAN module included		
	R5F563TBADFP	R5F563TBADFP#V1	PLQP0100KB-A	256 Kbytes	24 Kbytes	CAN module included		
	R5F563TEDDFB	R5F563TEDDFB#V0	PLQP0144KA-A	512 Kbytes	48 Kbytes	CAN module not included		
	R5F563TEDDFA	R5F563TEDDFA#V0	PLQP0120KA-A	512 Kbytes	48 Kbytes	CAN module not included		
	R5F563TEDDFH	R5F563TEDDFH#V0	PLQP0112JA-A	512 Kbytes	48 Kbytes	CAN module not included		
	R5F563TEDDFP	R5F563TEDDFP#V0	PLQP0100KB-A	512 Kbytes	48 Kbytes	CAN module not included		

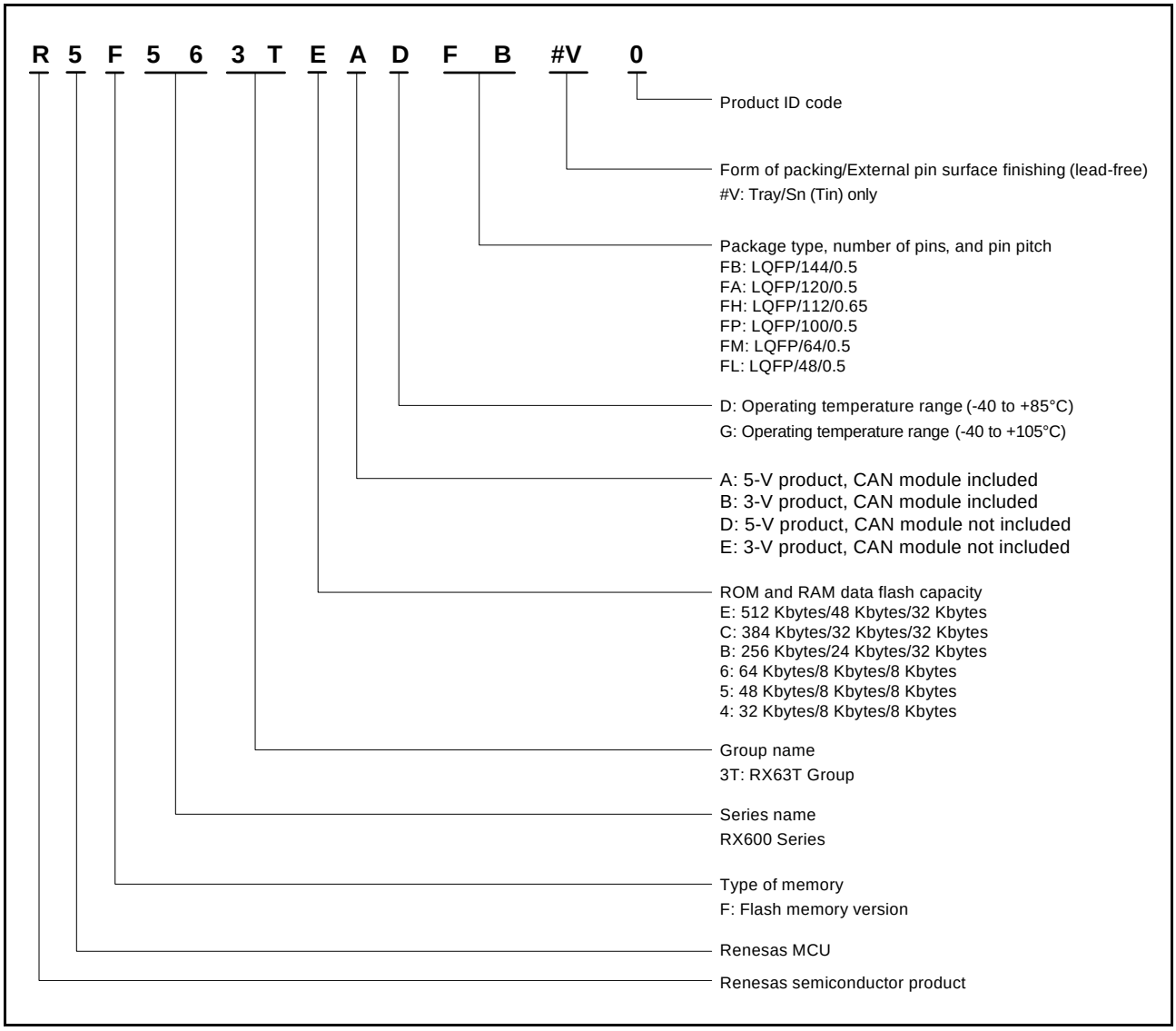


Figure 1.1 How to Read the Product Part Number

Table 1.4 Pin Functions (2/5)

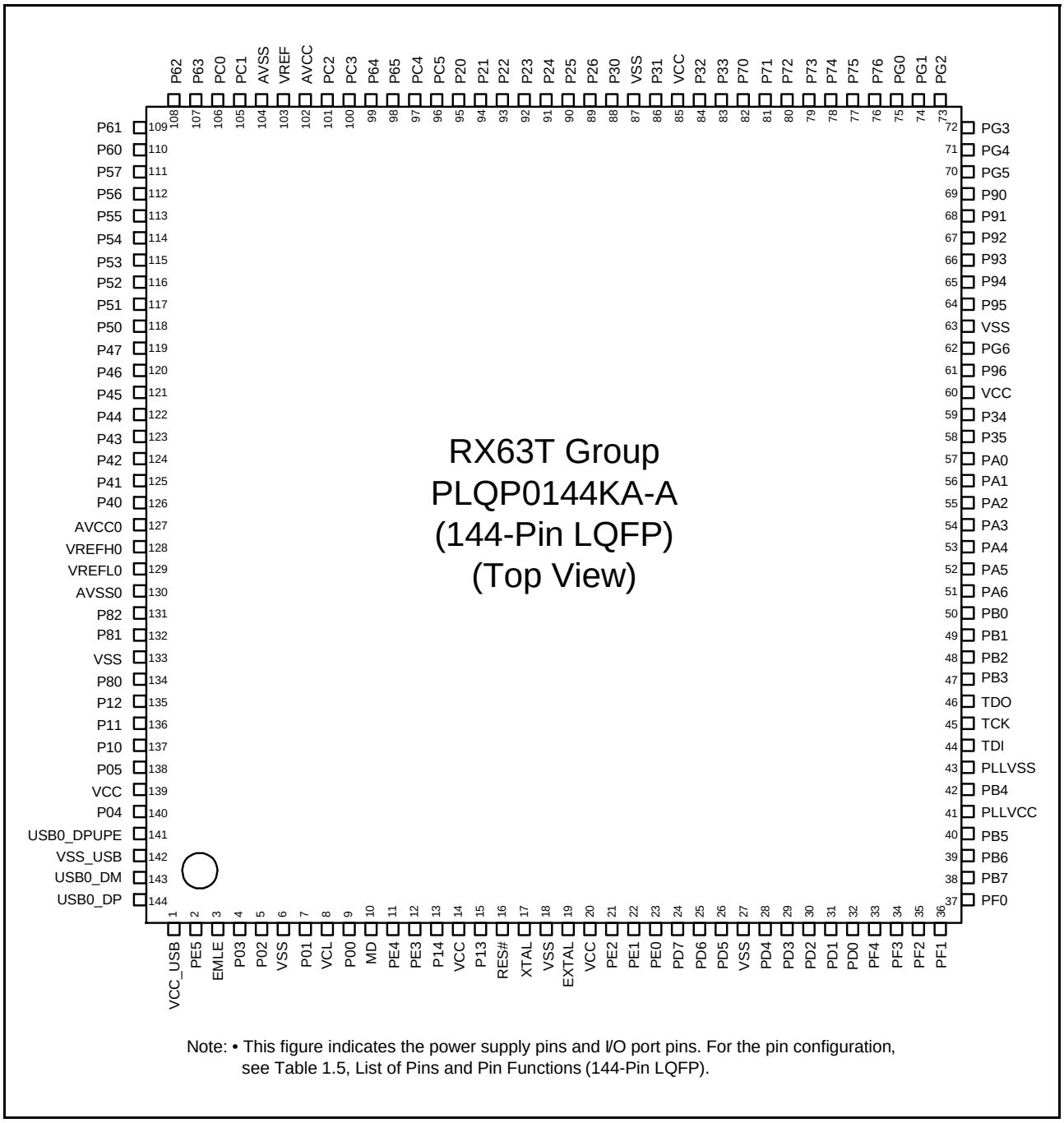
Classifications	Pin Name	I/O	Description
Interrupt	NMI	Input	Non-maskable interrupt request pin
	IRQ0 to IRQ7	Input	Maskable interrupt request pin
Multi-function timer pulse unit 3	MTIOC0A, MTIOC0B MTIOC0C, MTIOC0D	I/O	The TGRA0 to TGRD0 input capture input/output compare output/ PWM output pins
	MTIOC1A, MTIOC1B	I/O	The TGRA1 and TGRB1 input capture input/output compare output/ PWM output pins
	MTIOC2A, MTIOC2B	I/O	The TGRA2 and TGRB2 input capture input/output compare output/ PWM output pins
	MTIOC3A, MTIOC3B MTIOC3C, MTIOC3D	I/O	The TGRA3 to TGRD3 input capture input/output compare output/ PWM output pins
	MTIOC4A, MTIOC4B MTIOC4C, MTIOC4D	I/O	The TGRA4 to TGRD4 input capture input/output compare output/ PWM output pins
	MTIC5U, MTIC5V MTIC5W	Input	The TGRU5, TGRV5, and TGRW5 input capture input/dead time compensation input pins
	MTIOC6A, MTIOC6B MTIOC6C, MTIOC6D	I/O	The TGRA6 to TGRD6 input capture input/output compare output/ PWM output pins
	MTIOC7A, MTIOC7B MTIOC7C, MTIOC7D	I/O	The TGRA7 to TGRD7 input capture input/output compare output/ PWM output pins
	MTCLKA, MTCLKB MTCLKC, MTCLKD	Input	Input pins for external clock
Port output enable 3	POE0#, POE4# POE8#, POE10# POE11#, POE12#	Input	Input pins for request signals to place the MTU/GPT large-current pins in the high impedance state
General PWM timer	GTIOC0A, GTIOC0B	I/O	The GPT0.GTGRA and GPT0.GTGRB input capture input/output compare output/PWM output pins.
	GTIOC1A, GTIOC1B	I/O	The GPT1.GTGRA and GPT1.GTGRB input capture input/output compare output/PWM output pins.
	GTIOC2A, GTIOC2B	I/O	The GPT2.GTGRA and GPT2.GTGRB input capture input/output compare output/PWM output pins.
	GTIOC3A, GTIOC3B	I/O	The GPT3.GTGRA and GPT3.GTGRB input capture input/output compare output/PWM output pins.
	GTETRG0	Input	External trigger input pin for the GPT0 to GPT3
	GTIOC4A, GTIOC4B	I/O	The GPT4.GTGRA and GPT4.GTGRB input capture input/output compare output/PWM output pins.
	GTIOC5A, GTIOC5B	I/O	The GPT5.GTGRA and GPT5.GTGRB input capture input/output compare output/PWM output pins.
	GTIOC6A, GTIOC6B	I/O	The GPT6.GTGRA and GPT6.GTGRB input capture input/output compare output/PWM output pins.
	GTIOC7A, GTIOC7B	I/O	The GPT7.GTGRA and GPT7.GTGRB input capture input/output compare output/PWM output pins.
	GTETRG1	Input	External trigger input pin for the GPT4 to GPT7

Table 1.4 Pin Functions (4/5)

Classifications	Pin Name	I/O	Description
USB 2.0 host/function module	VCC_USB	Input	Power supply pin for USB
	VSS_USB	Input	Ground pin for USB
	USB0_DP	I/O	USB internal transceiver D + input and output pins
	USB0_DM	I/O	USB internal transceiver D - input and output pins
	USB0_EXICEN	Output	Low power control signal for OTG chip
	USB0_VBUSEN	Output	Supply enable signal of VBUS (5 V) to OTG chip
	USB0_ID	Input	Mini AB connector ID input pin for use in OTG operation
	USB0_DPRPD	Output	D+ signal pull-down control pin for use during host operation
	USB0_DRPD	Output	D- signal pull-down control pin for use during host operation
	USB0_DPUPE	Output	D+ signal pull-up control pin for use during function operation
	USB0_VBUS	Input	Pin for monitoring USB cable connection
	USB0_OVRCURA, USB0_OVRCURB	Input	Pin for detecting external over current
CAN module	CRX1	Input	Input pins
	CTX1	Output	Output pins
Serial peripheral interface	RSPCKA, RSPCKB	I/O	Clock input/output pins
	MOSIA, MOSIB	I/O	Inputs or outputs data output from the master
	MISOA, MISOB	I/O	Inputs or outputs data output from the slave
	SSLA0, SSLB0	I/O	Input or output pins for slave selection
	SSLA1 to SSLA3 SSLB1 to SSLB3	Output	Output pins for slave selection
12-bit A/D converter	AN000 to AN007 AN100 to AN103	Input	Input pins for the analog signals to be processed by the A/D converter
	ADTRG0#, ADTRG1#	Input	Input pins for the external trigger signals that start the A/D conversion
	CVREFH	Input	Input pin for the high-level reference voltage to the comparator
	CVREFL	Input	Input pin for the low-level reference voltage to the comparator
10-bit A/D converter	AN0 to AN19	Input	Input pins for the analog signals to be processed by the 10-bit A/D converter
	ADTRG#	Input	Input pins for the external trigger signals that start the A/D conversion
D/A converter	DA0, DA1	Output	Output pins for the analog signals to be processed by the 10-bit A/D converter
Analog power supply	AVCC0	—	Analog voltage supply pin for the 12-bit A/D converter. Connect this pin to VCC if the 12-bit A/D converter is not to be used
	AVSS0	—	Analog ground pin for the 12-bit A/D converter. Connect this pin to VSS if the 12-bit A/D converter is not to be used
	VREFH0	—	Reference voltage supply pin for the 12-bit A/D converter. Connect this pin to VCC if the 12-bit A/D converter is not to be used
	VREFL0	—	Reference ground pin for the 12-bit A/D converter. Connect this pin to VSS if the 12-bit A/D converter is not to be used
	AVCC	—	Analog voltage supply pin for the 10-bit A/D converter and the 10-bit D/A converter. Connect this pin to the power supply of the system if the A/D converter and the D/A converter are not to be used.
	AVSS	—	Ground pin for the 10-bit A/D converter and 10-bit D/A converter. Connect this pin to the power-supply ground for the system (0 V).
	VREF	—	Reference-voltage input pin for the 10-bit A/D converter and the 10-bit D/A converter. Connect this pin to the power supply for the system if the A/D converter and the D/A converter are not to be used.

1.5 Pin Assignments

Figure 1.3 to Figure 1.8 show the pin assignments. Table 1.5 to Table 1.10 show the lists of pins and pin functions.



Note: • This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.5, List of Pins and Pin Functions (144-Pin LQFP).

Figure 1.3 Pin Assignment (144-Pin LQFP)

Table 1.6 List of Pins and Pin Functions (120-Pin LQFP) (4/4)

Pin Number 120-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3, GPT, POE3, CAC)	Communications (SCIc, SCId, RSPI, RIIC, CAN, USB)	Interrupt	S12ADB, AD, DA
111		P82	WAIT#	MTIC5U	SCK12	IRQ3	
112		P81	A8	MTIC5V	TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12		
113		P80	A9	MTIC5W	RXD12/SMISO12/ SSCL12/RXDX12	IRQ5	
114		P12	CS3#		USB0_DPRPD		
115		P11	ALE	MTCLKC		IRQ1-DS	
116		P10		MTCLKD		IRQ0-DS	
117					USB0_DPUPE		
118	VSS_USB						
119					USB0_DM		
120					USB0_DP		

2. CPU

The RX CPU has sixteen general-purpose registers, nine control registers, and one accumulator used for DSP instructions.

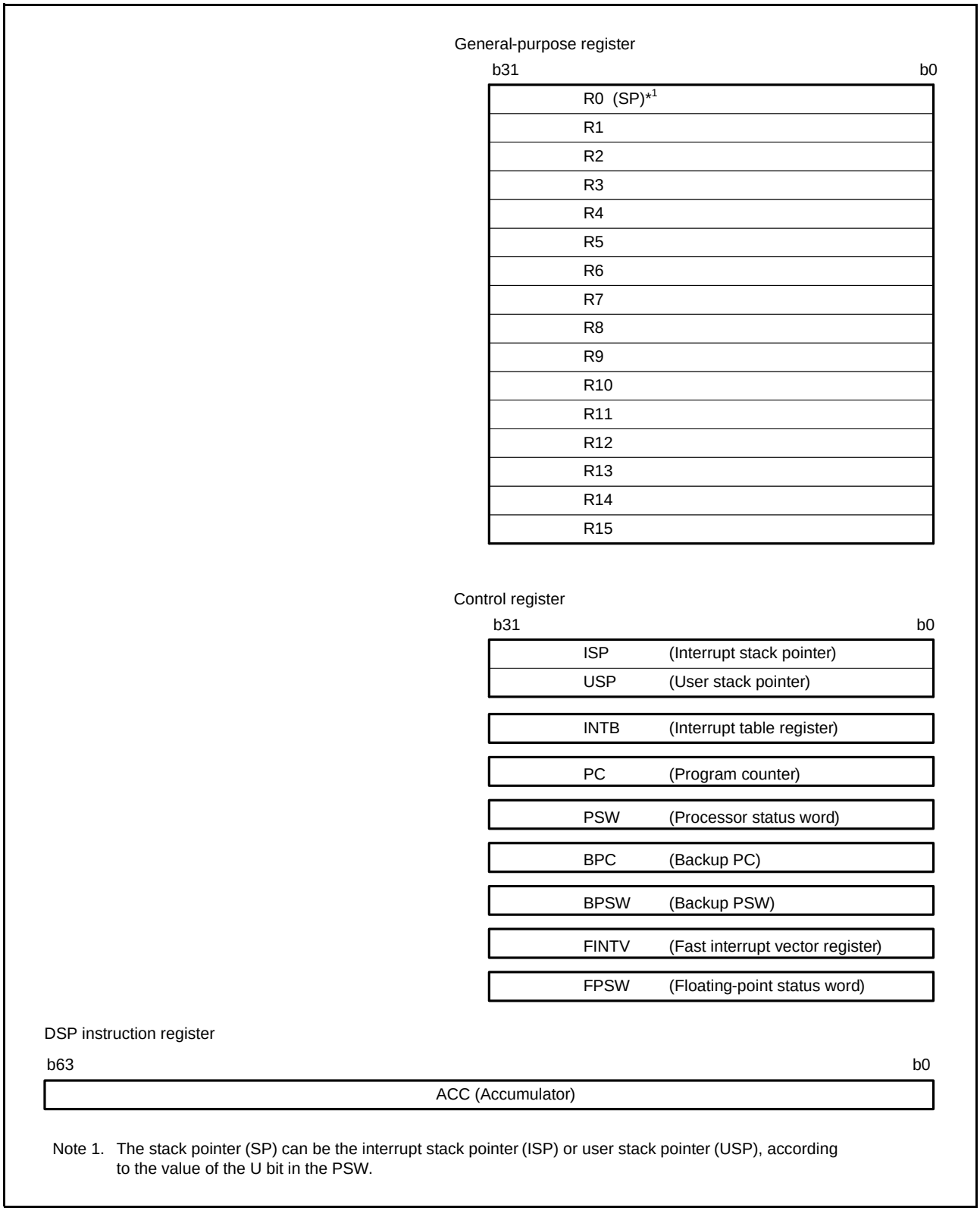


Figure 2.1 Register Set of the CPU

Table 4.1 List of I/O Registers (Address Order) (12/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 732C	ICU	Interrupt Source Priority Register 044	IPR044	8	8	2 ICLK		ICUb	Not present in versions with 64 or 48 pins.
0008 732Dh	ICU	Interrupt Source Priority Register 045	IPR045	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7331h	ICU	Interrupt Source Priority Register 049	IPR049	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7334h	ICU	Interrupt Source Priority Register 052	IPR052	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7336h	ICU	Interrupt Source Priority Register 054	IPR054	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7337h	ICU	Interrupt Source Priority Register 055	IPR055	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7338h	ICU	Interrupt Source Priority Register 056	IPR056	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7339h	ICU	Interrupt Source Priority Register 057	IPR057	8	8	2 ICLK			
0008 733Ah	ICU	Interrupt Source Priority Register 058	IPR058	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 733Bh	ICU	Interrupt Source Priority Register 059	IPR059	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 733Ch	ICU	Interrupt Source Priority Register 060	IPR060	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 733Dh	ICU	Interrupt Source Priority Register 061	IPR061	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 733Eh	ICU	Interrupt Source Priority Register 062	IPR062	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7340h	ICU	Interrupt Source Priority Register 064	IPR064	8	8	2 ICLK			
0008 7341h	ICU	Interrupt Source Priority Register 065	IPR065	8	8	2 ICLK			
0008 7342h	ICU	Interrupt Source Priority Register 066	IPR066	8	8	2 ICLK			
0008 7343h	ICU	Interrupt Source Priority Register 067	IPR067	8	8	2 ICLK			
0008 7344h	ICU	Interrupt Source Priority Register 068	IPR068	8	8	2 ICLK			
0008 7345h	ICU	Interrupt Source Priority Register 069	IPR069	8	8	2 ICLK			
0008 7346h	ICU	Interrupt Source Priority Register 070	IPR070	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7347h	ICU	Interrupt Source Priority Register 071	IPR071	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 735Ah	ICU	Interrupt Source Priority Register 090	IPR090	8	8	2 ICLK			Not present in versions with 112, 100, 64 or 48 pins.
0008 7362h	ICU	Interrupt Source Priority Register 098	IPR098	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7366h	ICU	Interrupt Source Priority Register 102	IPR102	8	8	2 ICLK			
0008 7367h	ICU	Interrupt Source Priority Register 103	IPR103	8	8	2 ICLK			
0008 7368h	ICU	Interrupt Source Priority Register 104	IPR104	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7369h	ICU	Interrupt Source Priority Register 105	IPR105	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 736Ah	ICU	Interrupt Source Priority Register 106	IPR106	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7372h	ICU	Interrupt Source Priority Register 114	IPR114	8	8	2 ICLK			
0008 737Ah	ICU	Interrupt Source Priority Register 122	IPR122	8	8	2 ICLK			
0008 737Eh	ICU	Interrupt Source Priority Register 126	IPR126	8	8	2 ICLK			
0008 7382h	ICU	Interrupt Source Priority Register 130	IPR130	8	8	2 ICLK			
0008 7385h	ICU	Interrupt Source Priority Register 133	IPR133	8	8	2 ICLK			
0008 7387h	ICU	Interrupt Source Priority Register 135	IPR135	8	8	2 ICLK			
0008 7389h	ICU	Interrupt Source Priority Register 137	IPR137	8	8	2 ICLK			
0008 738Bh	ICU	Interrupt Source Priority Register 139	IPR139	8	8	2 ICLK			
0008 738Dh	ICU	Interrupt Source Priority Register 141	IPR141	8	8	2 ICLK			
0008 7391h	ICU	Interrupt Source Priority Register 145	IPR145	8	8	2 ICLK			
0008 7392h	ICU	Interrupt Source Priority Register 146	IPR146	8	8	2 ICLK			
0008 7396h	ICU	Interrupt Source Priority Register 150	IPR150	8	8	2 ICLK			
0008 7397h	ICU	Interrupt Source Priority Register 151	IPR151	8	8	2 ICLK			

Table 4.1 List of I/O Registers (Address Order) (18/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 90E0h	S12AD	Comparator Operating Mode Selection Register 0	ADCMPMD0	16	16	2, 3 PCLKB	2 ICLK	S12ADB	
0008 90E2h	S12AD	Comparator Operating-Mode Selection Register 1	ADCMPMD1	16	16	2, 3 PCLKB	2 ICLK		
0008 90E4h	S12AD	Comparator Filter-Mode Register	ADCMPNR0	16	16	2, 3 PCLKB	2 ICLK		
0008 90E8h	S12AD	Comparator Detection Flag Register	ADCMPFR	8	8	2, 3 PCLKB	2 ICLK		
0008 90EAh	S12AD	Comparator Interrupt Selection Register	ADCMPSEL	16	16	2, 3 PCLKB	2 ICLK		
0008 90FCh	S12AD	A/D Group Scan Priority Control Register	ADGSPMR	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9100h	S12AD1	A/D Control Register	ADCSR	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9104h	S12AD1	A/D Channel Select Register A	ADANSA	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9108h	S12AD1	A/D-Converted Value Addition Mode Select Register (ADADS)	ADADS	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 910Ch	S12AD1	A/D-Converted Value Addition Count Select Register	ADADC	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 910Eh	S12AD1	A/D Control Extended Register	ADCER	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9110h	S12AD1	A/D Start Trigger Select Register	ADSTRGR	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9114h	S12AD1	A/D Channel Select Register B	ADANSB	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9118h	S12AD1	A/D Data-Doubling Register	ADDBLDR	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 911Eh	S12AD1	A/D Self-Diagnosis Data Register	ADRD	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9120h	S12AD1	A/D Data Register 0	ADDR0	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9122h	S12AD1	A/D Data Register 1	ADDR1	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9124h	S12AD1	A/D Data Register 2	ADDR2	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9126h	S12AD1	A/D Data Register 3	ADDR3	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9160h	S12AD1	A/D Sampling State Register 0	ADSSTR0	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9166h	S12AD1	A/D Sample and Hold Circuit Control Register	ADSHCR	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9173h	S12AD1	A/D Sampling State Register 1	ADSSTR1	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9174h	S12AD1	A/D Sampling State Register 2	ADSSTR2	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9175h	S12AD1	A/D Sampling State Register 3	ADSSTR3	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9180h	S12AD1	A/D Group Scan Priority Control Register	ADGSPCR	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9184h	S12AD1	A/D Data-Doubling Register A	ADDBLDRA	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9186h	S12AD1	A/D Data-Doubling Register B	ADDBLDRB	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 918Ah	S12AD1	A/D Programmable Gain Amplifier Register	ADPG	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 91E0h	S12AD1	Comparator Operating Mode Selection Register 0	ADCMPMD0	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 91E2h	S12AD1	Comparator Operating-Mode Selection Register 1	ADCMPMD1	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 91E4h	S12AD1	Comparator Filter-Mode Register	ADCMPNR0	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 91E8h	S12AD1	Comparator Detection Flag Register	ADCMPFR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 91EAh	S12AD1	Comparator Interrupt Selection Register	ADCMPSEL	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9800h	AD	A/D Control Register	ADCSR	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.

5.2 DC Characteristics

Table 5.2 DC Characteristics (1)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

The following relation applies when the USB is in use under condition 1 or condition 2: Vcc = PLLVcc = Vcc_USB = 3.0 to 3.6 V.

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	CAN input pin IRQ input pin MTU3 input pin POE3 input pin SCI input pin A/D trigger input pin GPT input pin RES#, NMI	V_{IH}	VCC × 0.8	—	VCC + 0.3	V	
		V_{IL}	–0.3	—	VCC × 0.2		
		ΔV_T	VCC × 0.06	—	—		
	RIIC input pin (IICBus operating)	V_{IH}	VCC × 0.7	—	VCC + 0.3		
		V_{IL}	–0.3	—	VCC × 0.3		
		ΔV_T	VCC × 0.05	—	—		
	USB0_VBUS input pin	V_{IH}	VCC × 0.7	—	VCC + 0.3		
		V_{IL}	–0.3	—	VCC × 0.2		
		ΔV_T	VCC × 0.06	—	—		
	Port 4*1 (also used as an analog port)	V_{IH}	AVCC0 × 0.8	—	AVCC0 + 0.3		
		V_{IL}	–0.3	—	AVCC0 × 0.2		
	Ports 5, 6, and C*1 (also used as an analog port)	V_{IH}	AVCC × 0.8	—	AVCC + 0.3		
		V_{IL}	–0.3	—	AVCC × 0.2		
	Ports 0 to 3*1 Ports 7 to B*1 Ports D to G*1	V_{IH}	VCC × 0.8	—	VCC + 0.3		
		V_{IL}	–0.3	—	VCC × 0.2		
Input high voltage (except for Schmitt trigger input pin)	MD pin, EMLE	V_{IH}	VCC × 0.9	—	VCC + 0.3	V	
	EXTAL, WAIT#, TCK RSPI input pin		VCC × 0.8	—	VCC + 0.3		
	D0 to D15		VCC × 0.7	—	VCC + 0.3		
	RIIC input pin (SMBus operating)		2.1	—	VCC + 0.3		Conditions 1 and 2
Input low voltage (except for Schmitt trigger input pin)	MD pin, EMLE	V_{IL}	–0.3	—	VCC × 0.1	V	
	EXTAL, WAIT#, TCK RSPI input pin		–0.3	—	VCC × 0.2		
	D0 to D15		–0.3	—	VCC × 0.3		
	RIIC input pin (SMBus operating)		–0.3	—	0.8		Conditions 1 and 2

Note 1. This includes the multiplexed pin functions, except for P25, P26, PB1, or PB2 when the RIIC input functions are in use, P22 to P24, P30, PA3 to PA5, PB0, PD0 to PD2, or PD6 when the RSPI input functions are in use, and PD4 or PF3 when the TCK input function is in use.

5.3 AC Characteristics

Table 5.7 Operation Frequency Value

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS =PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

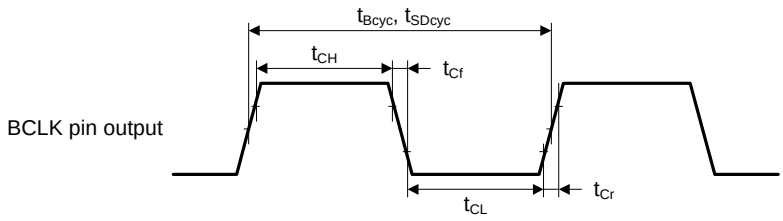
Item		Symbol	Min.	Typ.	Max.	Unit
Operation frequency	System clock (ICLK)	f	—	—	100	MHz
	Peripheral module clock (PCLK) *1		—	—	50	
	Timer module clock (PCLKA)		—	—	100	
	AD clock (PCLKC)		—	—	100	
	S12AD clock (PCLKD)		—	—	50	
	FlashIF clock (FCLK)		—	—	50	
	External bus clock (BCLK)		—	—	50	
	BCLK pin output		—	—	25	
	USB clock (UCLK)		—	—	48	

Note 1. The PCLK must run at a frequency of at least 24 MHz when the USB is in use.

Note 4. This is calculated from the formula below, where n is the number of cycles set by the PLLWTCR.PSTS[4:0] bits.

$$t_{PLLWT1} = t_{PLL1} + \frac{n + 131072}{f_{PLL}}$$

$$t_{PLLWT2} = t_{PLL2} + \frac{n + 131072}{f_{PLL}} = t_{MAINOSC} + t_{PLL1} + \frac{n + 131072}{f_{PLL}}$$



Test conditions: VOH = VCC × 0.7, VOL = VCC × 0.3, IOH = –1.0 mA, IOL = 1.0 mA, C = 30 pF

Figure 5.3 BCLK Pin Output Timing

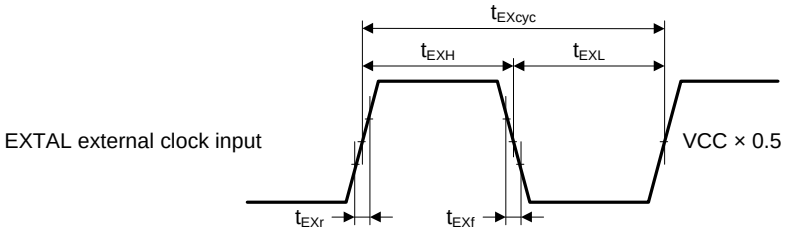


Figure 5.4 EXTAL External Clock Input Timing

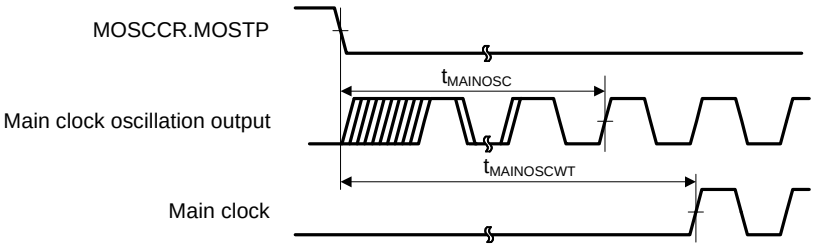


Figure 5.5 Main Clock Oscillation Start Timing

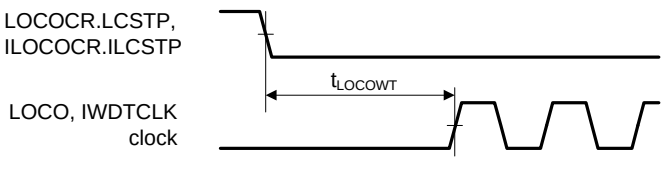


Figure 5.6 LOCO, IWDTCLK Clock Oscillation Start Timing

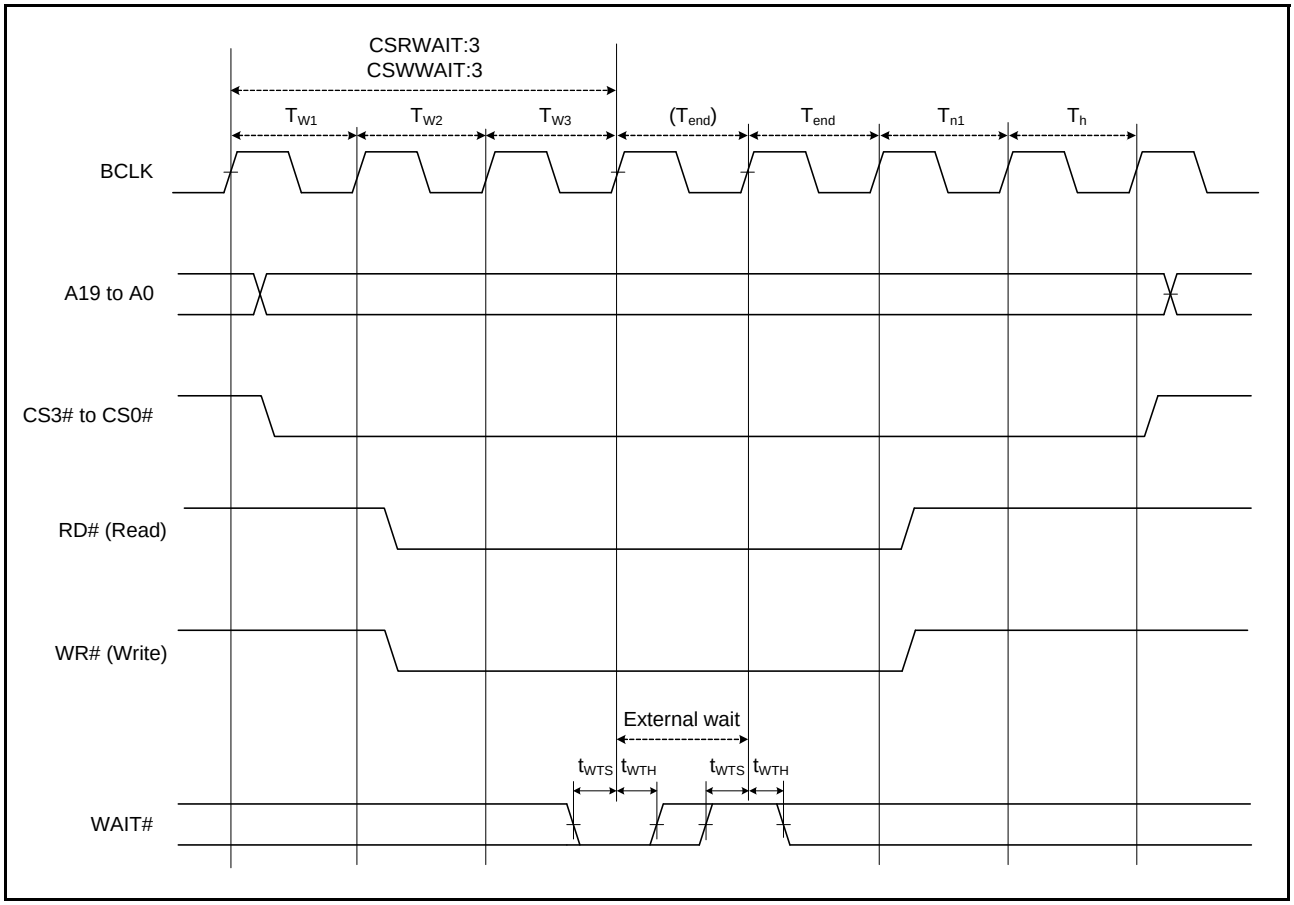


Figure 5.17 External Bus Timing/External Wait Control

Table 5.14 Bus Timing (Multiplexed Bus) (3)

Condition: PLLVCC = VCC_USB = AVCC0 = AVCC = VREF = 3.0 to 3.6 V
VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V, VREFH0 = 3.0 V to AVCC0
$T_a = T_{opr}$
Output load conditions: V_{OH} = VCC x 0.5, V_{OL} = VCC x 0.5, I_{OH} = –1.0 mA, I_{OL} = 1.0 mA, C = 30 pF

Item	Symbol	Min.	Max.	Unit	Test Conditions
Address delay time	t_{AD}	—	35	ns	Figure 5.18, Figure 5.19
Byte control delay time	t_{BCD}	—	30	ns	
CS# delay time	t_{CSD}	—	30	ns	
RD# delay time	t_{RSD}	—	30	ns	
ALE delay time	t_{ALED}	—	30	ns	
Read data setup time	t_{RDS}	20	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	—	30	ns	
Write data delay time	t_{WDD}	—	35	ns	
Write data hold time	t_{WDH}	0	—	ns	
WAIT# setup time	t_{WTS}	20	—	ns	Figure 5.17
WAIT# hold time	t_{WTH}	0.0	—	ns	

5.8 Oscillation Stop Detection Circuit Characteristics

Table 5.28 Oscillation Stop Detection Circuit Characteristics

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection time	t_{dr}	—	—	1.0	ms	Figure 5.43

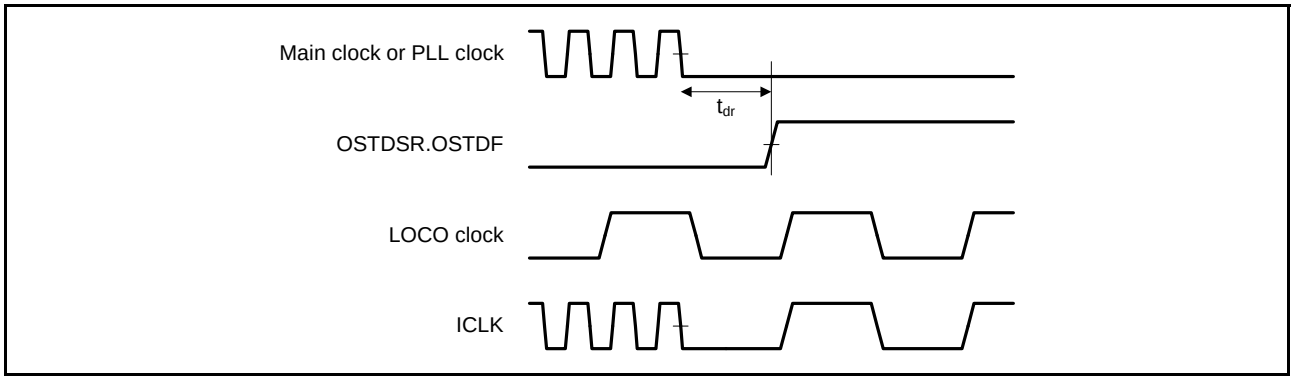


Figure 5.43 Oscillation Stop Detection Timing

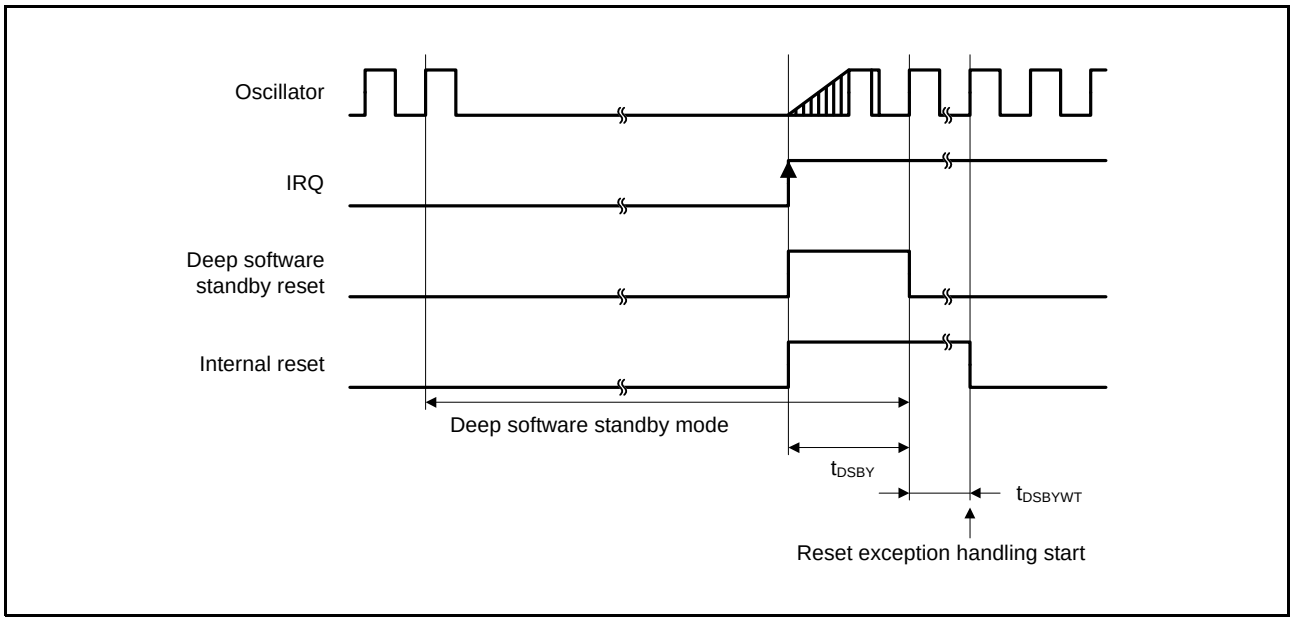


Figure 6.9 Deep Software Standby Mode Cancellation Timing

6.3.4 Control Signal Timing

Table 6.10 Control Signal Timing

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
NMI pulse width	t_{NMIW}	200	—	—	ns	t_{Pcyc} × 2 ≤ 200ns, Figure 6.10
		2			t_{Pcyc}	t_{Pcyc} × 2 > 200ns, Figure 6.10
IRQ pulse width	t_{IRQW}	200	—	—	ns	t_{Pcyc} × 2 ≤ 200ns, Figure 6.11
		2			t_{Pcyc}	t_{Pcyc} × 2 > 200ns, Figure 6.11

Note 1. t_{Pcyc}: PCLK cycle

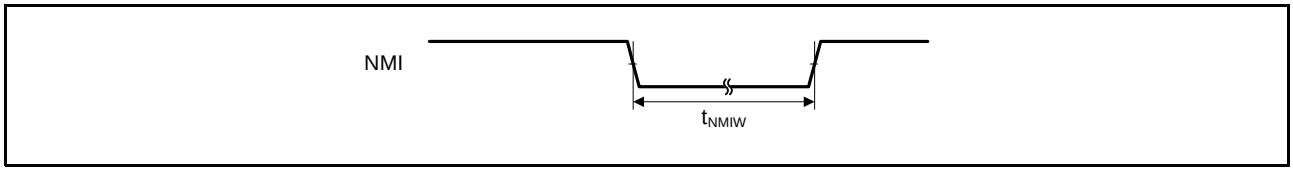


Figure 6.10 NMI Interrupt Input Timing

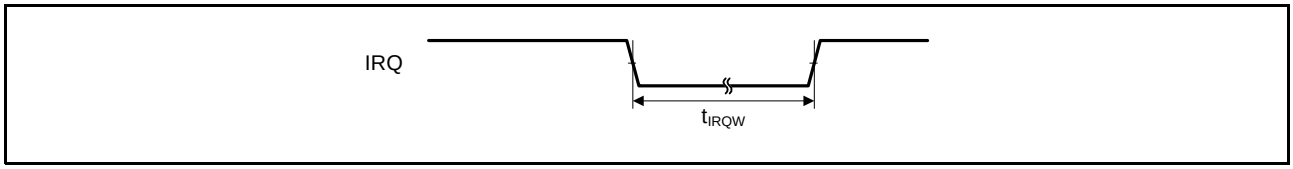


Figure 6.11 IRQ Interrupt Input Timing

6.3.5 Timing of On-Chip Peripheral Modules

Table 6.11 Timing of On-Chip Peripheral Modules (1)

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
I/O ports	Input data pulse width		t_{PRW}	1.5	—	t_{Pcyc}	Figure 6.12
MTU3	Input capture input pulse width	Single-edge setting	t_{TICW}	3	—	t_{PAcyc}	Figure 6.13
		Both-edge setting		5	—		
	Timer clock pulse width	Single-edge setting	t_{TCKWH}, t_{TCKWL}	3	—	t_{PAcyc}	Figure 6.14
		Both-edge setting		5	—		
		Phase counting mode		5	—		
POE3	POE# input pulse width		t_{POEW}	1.5	—	t_{Pcyc}	Figure 6.16
GPT	Input capture input pulse width	Single-edge setting	t_{GTICW}	3	—	t_{PAcyc}	Figure 6.15
		Both-edge setting		5	—		
	External trigger input pulse width	Single-edge setting	t_{OTETW}	3	—	t_{PAcyc}	Figure 6.18
		Both-edge setting		5	—		
SCI	Input clock cycle	Asynchronous	t_{Scyc}	4	—	t_{Pcyc}	Figure 6.17
		Clock synchronous		6	—		
	Input clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time		t_{SCKr}	—	20	ns	
	Input clock fall time		t_{SCKf}	—	20	ns	
	Output clock cycle	Asynchronous	t_{Scyc}	16	—	t_{Pcyc}	
		Clock synchronous		4	—		
	Output clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time		t_{SCKr}	—	20	ns	
	Output clock fall time		t_{SCKf}	—	20	ns	
	Transmit data delay time	Clock synchronous	t_{TXD}	—	40	ns	Figure 6.18
	Receive data setup time	Clock synchronous	t_{RXS}	40	—	ns	
	Receive data hold time	Clock synchronous	t_{RXH}	40	—	ns	
A/D converter	12-bit A/D converter trigger input pulse width		t_{TRGW}	1.5	—	t_{Pcyc}	Figure 6.19

Note 1. t_{Pcyc}: PCLK cycle, t_{PAcye}: PCLKA cycle

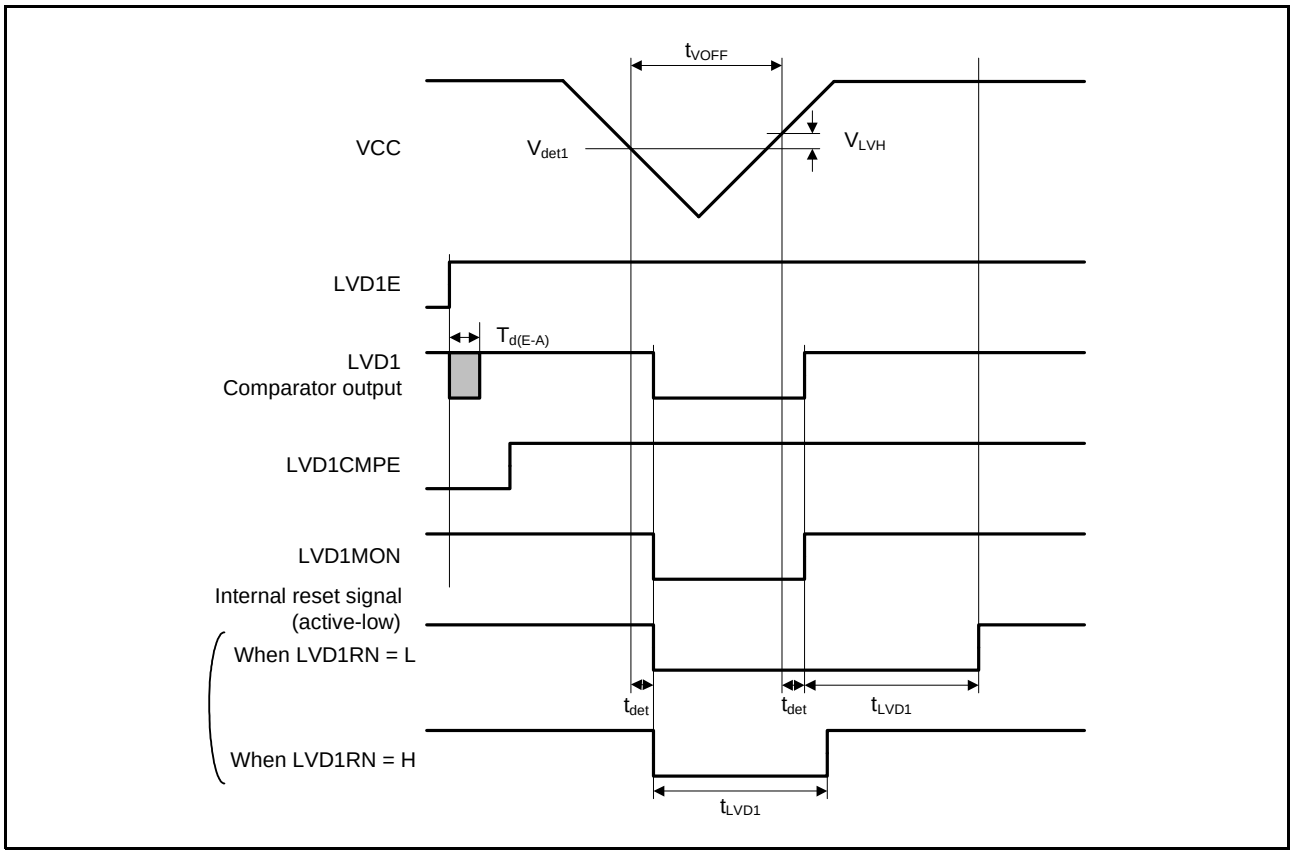


Figure 6.28 Voltage Detection Circuit Timing (V_{det1})

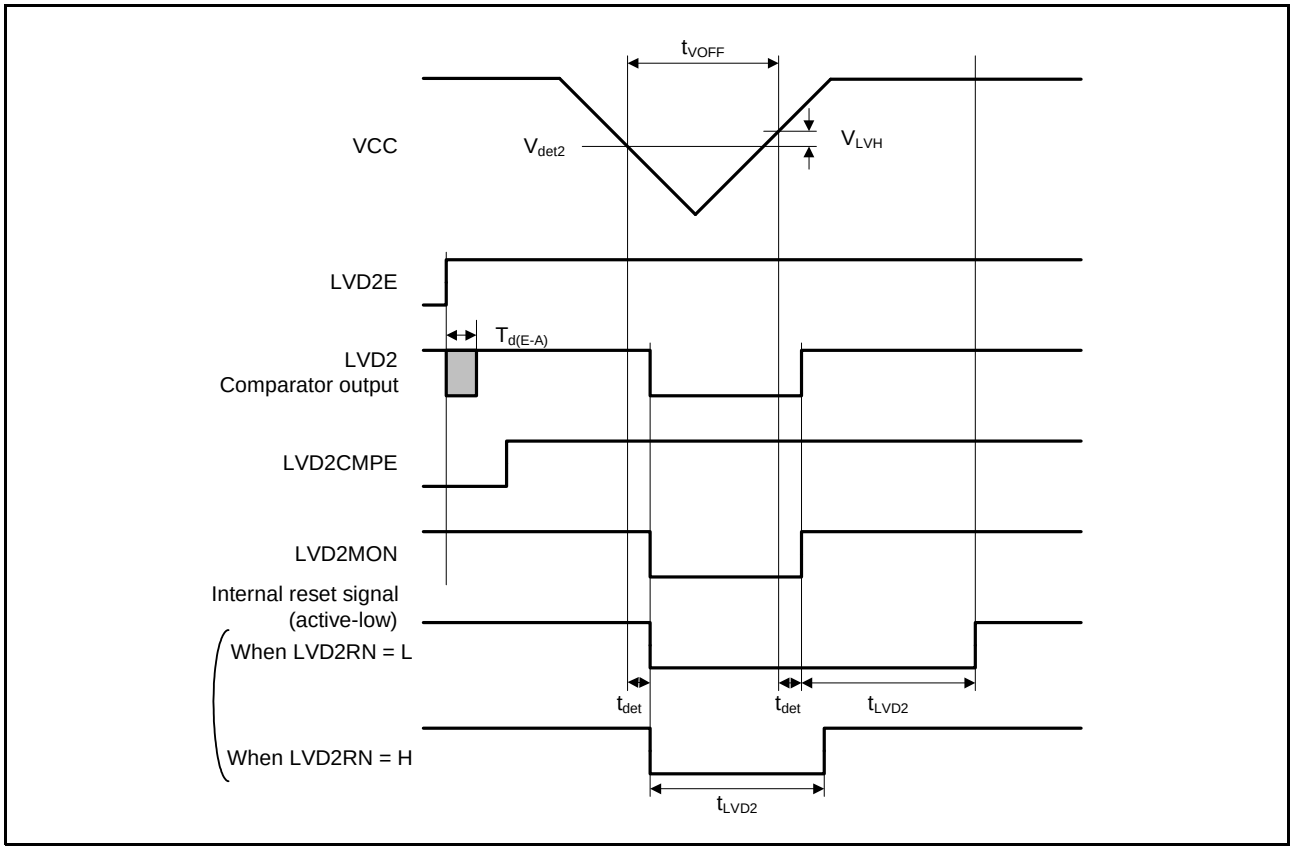
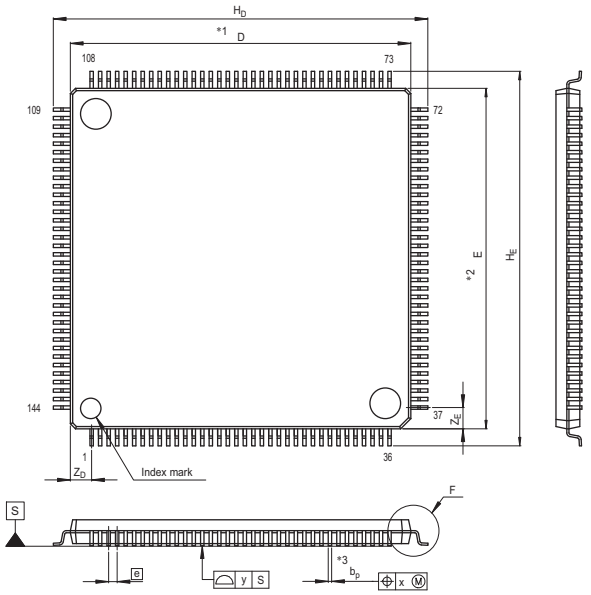


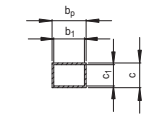
Figure 6.29 Voltage Detection Circuit Timing (V_{det2})

Appendix 1. Package Dimensions

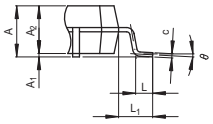
Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP144-20x20-0.50	PLQP0144KA-A	144P6Q-A / FP-144L / FP-144LV	1.2g





Terminal cross section



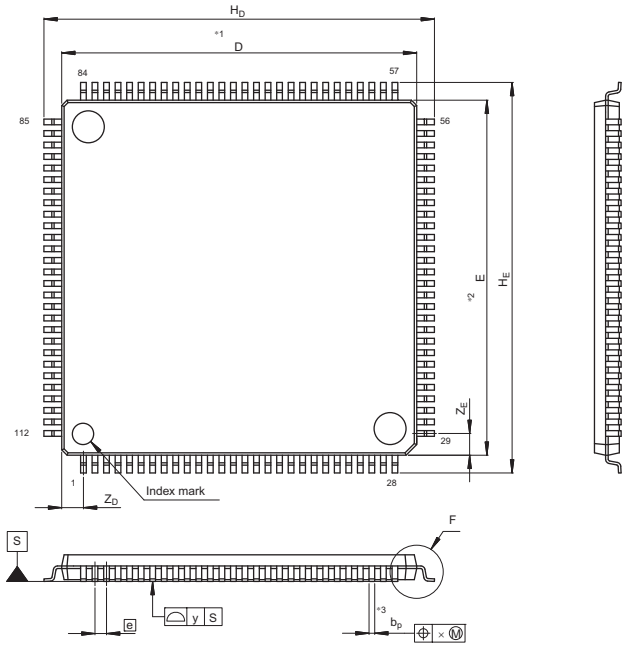
Detail F

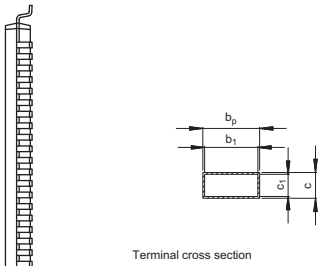
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

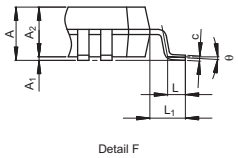
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	19.9	20.0	20.1
E	19.9	20.0	20.1
A_2	—	1.4	—
H_D	21.8	22.0	22.2
H_E	21.8	22.0	22.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.17	0.22	0.27
b_1	—	0.20	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure A 144-Pin LQFP (PLQP0144KA-A)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP112-20x20-0.65	PLQP0112JA-A	FP-112E/FP-112EV	1.2g







NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	19.9	20.0	20.1
E	19.9	20.0	20.1
A_2	—	1.4	—
H_D	21.8	22.0	22.2
H_E	21.8	22.0	22.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.27	0.32	0.37
b_1	—	0.30	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z_D	—	1.225	—
Z_E	—	1.225	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure C 112-Pin LQFP (PLQP0112JA-A)

Classifications

- Items with Technical Update document number: Changes according to the corresponding issued Technical Update
- Items without Technical Update document number: Minor changes that do not require Technical Update to be issued

Rev.	Date	Description		Classification
		Page	Summary	
2.20	Mar 31, 2016	1. Overview		
		2 to 8	Table 1.1 Outline of Specifications, Note 1 changed	TN-RX*-A086A/E
		10 to 13	Table 1.3 List of Products, changed	TN-RX*-A086A/E
		16	Table 1.4 Pin Functions, changed	
		27 to 30	Table 1.5 List of Pins and Pin Functions (144-Pin LQFP), changed	
		30	Table 1.5 List of Pins and Pin Functions (144-Pin LQFP), Note 1 added	
		31 to 34	Table 1.6 List of Pins and Pin Functions (120-Pin LQFP), changed	
		35 to 38	Table 1.7 List of Pins and Pin Functions (112-Pin LQFP), changed	
		38	Table 1.7 List of Pins and Pin Functions (112-Pin LQFP), Note 1 added	
		4. I/O Registers		
		54	(4) Notes on Sleep Mode and Mode Transition, added	TN-RX*-A140A/E
		55 to 102	Table 4.1 List of I/O Registers (Address Order), changed	TN-RX*-A086A/E, TN-RX*-A140A/E
		5. Electrical Characteristics [144-, 120-, 112- and 100-Pin Versions]		
		103	Table 5.1 Absolute Maximum Ratings, changed	TN-RX*-A086A/E
		106	Table 5.4 DC Characteristics (3), changed	
		107	Table 5.5 Permissible Output Currents, changed	
		108	Table 5.6 Permissible Power Consumption (G version product only), title changed, notes added	TN-RX*-A086A/E
		111	Table 5.9 Clock Timing, changed	TN-RX*-A097A/E
		112	Figure 5.6 LOCO, IWDTCLK Clock Oscillation Start Timing, title changed	TN-RX*-A097A/E
		112	Figure 5.6 LOCO, IWDTCLK Clock Oscillation Start Timing, changed	TN-RX*-A097A/E
		124	Table 5.16 Timing of On-Chip Peripheral Modules (1), changed	TN-RX*-A121A/E
		125	Table 5.16 Timing of On-Chip Peripheral Modules (2), changed	TN-RX*-A121A/E
		126	Table 5.16 Timing of On-Chip Peripheral Modules (3), changed	TN-RX*-A121A/E
		127	Table 5.16 Timing of On-Chip Peripheral Modules (4), changed	
		129	Table 5.17 Timing of the PWM Delay Generation Circuit	TN-RX*-A086A/E
		132	Figure 5.30 RSPI Timing (Master, CPHA = 0) (Bit Rate: PCLKB Division Ratio Set to a Value Other Than 1/2) and Simple SPI Timing (Master, CKPH = 1), title and figure changed	
		133	Figure 5.32 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKB Division Ratio Set to a Value Other Than 1/2) and Simple SPI Timing (Master, CKPH = 0), title changed	
		134	Figure 5.34 RSPI Timing (Slave, CPHA = 0) and Simple SPI Timing (Slave, CKPH = 1), title changed	
		135	Figure 5.35 RSPI Timing (Slave, CPHA = 1) and Simple SPI Timing (Slave, CKPH = 0), title changed	
		136	Table 5.18 On-Chip USB Full-Speed Characteristics (DP and DM Pin Characteristics), Condition 1, 2 changed	TN-RX*-A086A/E
		143	Table 5.26 Power-on Reset Circuit and Voltage Detection Circuit Characteristics (1), changed	
		6. Electrical Characteristics [64- and 48-Pin Versions]		
		150	Table 6.1 Absolute Maximum Ratings, changed	TN-RX*-A086A/E
		153	Table 6.5 Permissible Power Consumption (G version product only), title changed, note added	TN-RX*-A086A/E
		154	Table 6.7 Clock Timing, changed	TN-RX*-A097A/E
		155	Figure 6.3 LOCO, IWDTCLK Clock Oscillation Start Timing, title changed	TN-RX*-A097A/E
		155	Figure 6.3 LOCO, IWDTCLK Clock Oscillation Start Timing, changed	TN-RX*-A097A/E
		161	Table 6.12 Timing of On-Chip Peripheral Modules (2), changed	
		170	Table 6.18 Power-on Reset Circuit and Voltage Detection Circuit Characteristics, changed	