Renesas Electronics America Inc - R5F563TCADFH#V1 Datasheet

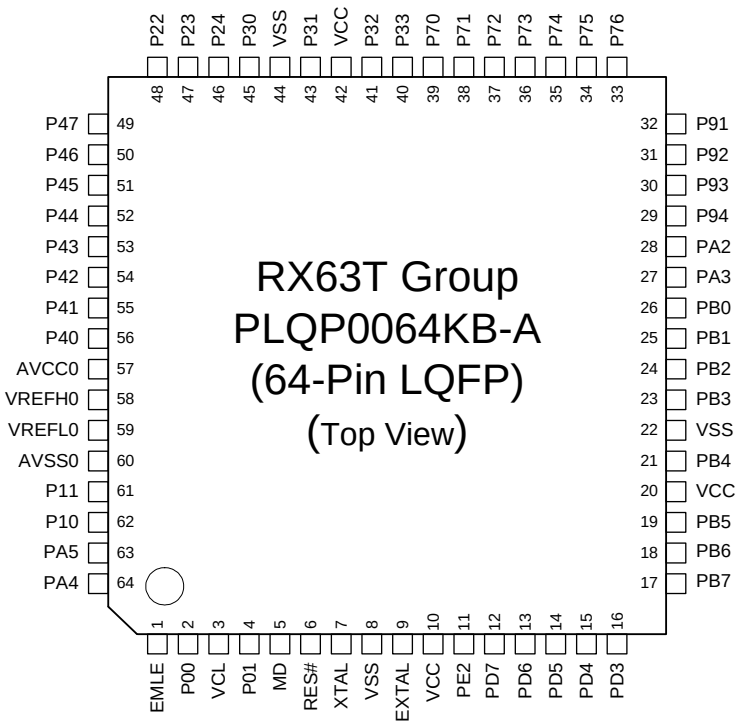
Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

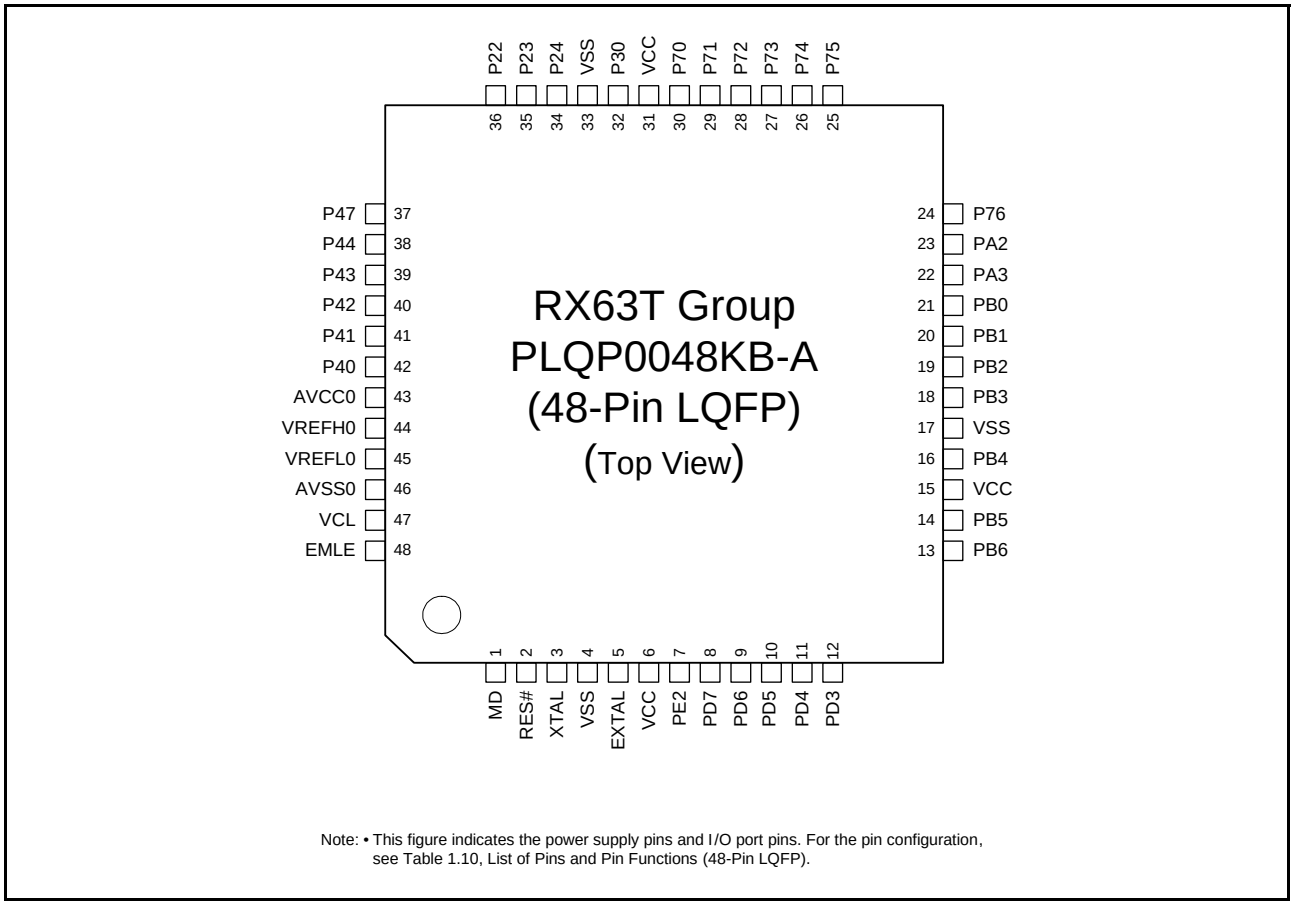
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	69
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x10b, 8x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f563tcadfh-v1



Note: • This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.9, List of Pins and Pin Functions (64-Pin LQFP).

Figure 1.7 Pin Assignment (64-Pin LQFP)



Note: • This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.10, List of Pins and Pin Functions (48-Pin LQFP).

Figure 1.8 Pin Assignment (48-Pin LQFP)

Table 1.5 List of Pins and Pin Functions (144-Pin LQFP) (3/4)

Pin Number 144-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3, GPT, POE3, CAC)	Communications (SCIc, SCId, RSPI, RIIC, CAN, USB)	Interrupt	S12ADB, AD, DA
72		PG3		GTIOC6A	TXD3/SMOSI3/SSDA3		
73		PG2			SCK2	IRQ2	
74		PG1		GTIOC7B	RXD2/SMISO2/SSCL2	IRQ1	
75		PG0		GTIOC7A	TXD2/SMOSI2/SSDA2	IRQ0	
76		P76	D0/[A0/D0]	MTIOC4D/GTIOC2B			
77		P75	D1/[A1/D1]	MTIOC4C/GTIOC1B			
78		P74	D2/[A2/D2]	MTIOC3D/GTIOC0B			
79		P73	D3/[A3/D3]	MTIOC4B/GTIOC2A			
80		P72	D4/[A4/D4]	MTIOC4A/GTIOC1A			
81		P71	D5/[A5/D5]	MTIOC3B/GTIOC0A			
82		P70	D6/[A6/D6]	POE0#	CTS1#/RTS1#/SS1#	IRQ5-DS	
83		P33	D7/[A7/D7]	MTIOC3A/MTCLKA	SSLA3/SSLB3		
84		P32	D8/[A8/D8]	MTIOC3C/MTCLKB	SSLA2/SSLB2		
85	VCC						
86		P31	D9/[A9/D9]	MTIOC0A/MTCLKC	SSLA1/SSLB1		
87	VSS						
88		P30	D10/[A10/D10]	MTIOC0B/MTCLKD	SCK0/SSLA0/SSLB0		
89		P26	CS0#		TXD1/SMOSI1/SSDA1/SDA1		
90		P25	CS1#		SCK1/SCL1		
91		P24	D11/[A11/D11]		CTS0#/RTS0#/SS0#/RSPCKA/RSPCKB	IRQ4	
92		P23	D12/[A12/D12]	CACREF	TXD0/SMOSI0/SSDA0/MOSIA/MOSIB/CTX1		
93		P22	D13/[A13/D13]		RXD0/SMISO0/SSCL0/MISOA/MISOB/CRX1		ADTRG#
94		P21	D14/[A14/D14]	MTCLKA		IRQ6-DS	ADTRG1#
95		P20	D15/[A15/D15]	MTCLKB		IRQ7-DS	ADTRG0#
96		PC5					AN19
97		PC4					AN18
98		P65	A0/BC0#				AN5
99		P64	A1				AN4
100		PC3					AN17
101		PC2					AN16
102	AVCC						
103	VREF						
104	AVSS						
105		PC1					AN15
106		PC0					AN14
107		P63	A2				AN3
108		P62	A3				AN2
109		P61	A4				AN1

Table 1.5 List of Pins and Pin Functions (144-Pin LQFP) (4/4)

Pin Number 144-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3, GPT, POE3, CAC)	Communications (SCIc, SCId, RSPI, RIIC, CAN, USB)	Interrupt	S12ADB, AD, DA
110		P60	A5				AN0
111		P57					AN13
112		P56					AN12
113		P55					AN11/DA1
114		P54					AN10/ DA0
115		P53	A6				AN9
116		P52	A7				AN8
117		P51					AN7
118		P50					AN6
119		P47					AN103/ CVREFH
120		P46					AN102
121		P45					AN101
122		P44					AN100
123		P43					AN003/ CVREFL
124		P42					AN002
125		P41					AN001
126		P40					AN000
127	AVCC0						
128	VREFH0						
129	VREFL0						
130	AVSS0						
131		P82	WAIT#	MTIC5U	SCK12	IRQ3	
132		P81	A8	MTIC5V	TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12		
133	VSS						
134		P80	A9	MTIC5W	RXD12/SMISO12/ SSCL12/RXDX12	IRQ5	
135		P12	CS3#		USB0_DPRPD		
136		P11	ALE	MTCLKC		IRQ1-DS	
137		P10		MTCLKD		IRQ0-DS	
138		P05	CS2#/WAIT#				
139	VCC						
140		P04					
141					USB0_DPUPE		
142	VSS_USB						
143					USB0_DM		
144					USB0_DP		

Note 1. Available for use as SCI pin only in boot mode.

Table 1.7 List of Pins and Pin Functions (112-Pin LQFP) (2/4)

Pin Number 112-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3, GPT, POE3, CAC)	Communications (SCIc, SCId, RSPI, RIIC, CAN)	Interrupt	S12ADB, AD, DA
38		PB0	A14	MTIOC0D	MOSIA/MOSIB		
39		PA5		MTIOC1A	RXD0/SMISO0/ SSCL0/ MISOA/MISOB		ADTRG1#
40		PA4		MTIOC1B	TXD0/SMOSI0/ SSDA0/RSPCKA/ RSPCKB		ADTRG0#
41		PA3		MTIOC2A	SCK0/SSLA0/SSLB0		
42		PA2		MTIOC2B	RXD2/SMISO2/ SSCL2/ SSLA1/SSLB1		
43		PA1		MTIOC6A	TXD2/SMOSI2/ SSDA2/SSLA2/SSLB2		
44		PA0		MTIOC6C	SCK2/SSLA3/SSLB3		
45	VCC						
46		P96	A13	POE4#	RXD1/SMISO1/SSCL1	IRQ4-DS	
47	VSS						
48		P95		MTIOC6B/ GTIOC4A	TXD1/SMOSI1/SSDA1		
49		P94		MTIOC7A/ GTIOC5A	CTS1#/RTS1#/SS1#		
50		P93		MTIOC7B/ GTIOC6A	CTS2#/RTS2#/SS2#		
51		P92		MTIOC6D/GTIOC4B			
52		P91		MTIOC7C/GTIOC5B			
53		P90		MTIOC7D/GTIOC6B			
54	TRCLK	PG5		POE12#	SCK3		ADTRG#
55	TRDATA3	PG4		GTIOC6B	RXD3/SMISO3/SSCL3	IRQ6	
56	TRDATA2	PG3		GTIOC6A	TXD3/SMOSI3/SSDA3		
57	TRDATA1	PG2			SCK2	IRQ2	
58	TRDATA0	PG1		GTIOC7B	RXD2/SMISO2/SSCL2	IRQ1	
59	TRSYNC	PG0		GTIOC7A	TXD2/SMOSI2/SSDA2	IRQ0	
60		P76	D0/[A0/D0]	MTIOC4D/GTIOC2B			
61		P75	D1/[A1/D1]	MTIOC4C/GTIOC1B			
62		P74	D2/[A2/D2]	MTIOC3D/GTIOC0B			
63		P73	D3/[A3/D3]	MTIOC4B/GTIOC2A			
64		P72	D4/[A4/D4]	MTIOC4A/GTIOC1A			
65		P71	D5/[A5/D5]	MTIOC3B/GTIOC0A			
66		P70	D6/[A6/D6]	POE0#	CTS1#/RTS1#/SS1#	IRQ5-DS	
67		P33	D7/[A7/D7]	MTIOC3A/MTCLKA	SSLA3/SSLB3		
68		P32	D8/[A8/D8]	MTIOC3C/MTCLKB	SSLA2/SSLB2		
69	VCC						
70		P31	D9/[A9/D9]	MTIOC0A/MTCLKC	SSLA1/SSLB1		
71	VSS						
72		P30	D10/[A10/ D10]	MTIOC0B/MTCLKD	SCK0/SSLA0/SSLB0		
73		P24	D11/[A11/D11]		CTS0#/RTS0#/SS0#/ RSPCKA/RSPCKB	IRQ4	

Table 1.8 List of Pins and Pin Functions (100-Pin LQFP) (2/3)

Pin Number 100-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3, GPT, POE3, CAC)	Communications (SCIc, SCId, RSPI, RIIC, CAN)	Interrupt	S12ADB, AD, DA
37		PA4		MTIOC1B	TXD0/SMOSI0/ SSDA0/ RSPCKA/RSPCKB		ADTRG0#
38		PA3		MTIOC2A	SCK0/SSLA0/SSLB0		
39		PA2		MTIOC2B	RXD2/SMISO2/ SSCL2/ SSLA1/SSLB1		
40		PA1		MTIOC6A	TXD2/SMOSI2/ SSDA2/ SSLA2/SSLB2		
41		PA0		MTIOC6C	SCK2/SSLA3/SSLB3		
42	VCC						
43		P96	A13	POE4#	RXD1/SMISO1/SSCL1	IRQ4-DS	
44	VSS						
45		P95		MTIOC6B/GTIOC4A	TXD1/SMOSI1/SSDA1		
46		P94		MTIOC7A/GTIOC5A	CTS1#/RTS1#/SS1#		
47		P93		MTIOC7B/GTIOC6A	CTS2#/RTS2#/SS2#		
48		P92		MTIOC6D/GTIOC4B			
49		P91		MTIOC7C/GTIOC5B			
50		P90		MTIOC7D/GTIOC6B			
51		P76	D0/[A0/D0]	MTIOC4D/GTIOC2B			
52		P75	D1/[A1/D1]	MTIOC4C/GTIOC1B			
53		P74	D2/[A2/D2]	MTIOC3D/GTIOC0B			
54		P73	D3/[A3/D3]	MTIOC4B/GTIOC2A			
55		P72	D4/[A4/D4]	MTIOC4A/GTIOC1A			
56		P71	D5/[A5/D5]	MTIOC3B/GTIOC0A			
57		P70	D6/[A6/D6]	POE0#	CTS1#/RTS1#/SS1#	IRQ5-DS	
58		P33	D7/[A7/D7]	MTIOC3A/MTCLKA	SSLA3/SSLB3		
59		P32	D8/[A8/D8]	MTIOC3C/MTCLKB	SSLA2/SSLB2		
60	VCC						
61		P31	D9/[A9/D9]	MTIOC0A/MTCLKC	SSLA1/SSLB1		
62	VSS						
63		P30	D10/[A10/ D10]	MTIOC0B/MTCLKD	SCK0/SSLA0/SSLB0		
64		P24	D11/[A11/D11]		CTS0#/RTS0#/SS0#/ RSPCKA/RSPCKB	IRQ4	
65		P23	D12/[A12/ D12]	CACREF	TXD0/SMOSI0/ SSDA0/MOSIA/ MOSIB/CTX1		
66		P22	D13/[A13/ D13]		RXD0/SMISO0/ SSCL0/MISOA/ MISOB/CRX1		ADTRG#
67		P21	D14/[A14/ D14]	MTCLKA		IRQ6-DS	ADTRG1#
68		P20	D15/[A15/ D15]	MTCLKB		IRQ7-DS	ADTRG0#
69		P65	A0/BC0#				AN5
70		P64	A1				AN4

3. Address Space

3.1 Address Space

This MCU has a 4-Gbyte address space, consisting of the range of addresses from 0000 0000h to FFFF FFFFh. That is, linear access to an address space of up to 4 Gbytes is possible, and this contains both program and data areas.
Figure 3.1 shows the memory maps in the respective operating modes. Accessible areas will differ according to the operating mode and states of control bits.

Table 4.1 List of I/O Registers (Address Order) (10/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 71BBh	ICU	DTC Activation Enable Register 187	DTCER187	8	8	2 ICLK		ICUb	Not present in versions with 64 or 48 pins.
0008 71BCh	ICU	DTC Activation Enable Register 188	DTCER188	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 71BDh	ICU	DTC Activation Enable Register 189	DTCER189	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 71BFh	ICU	DTC Activation Enable Register 191	DTCER191	8	8	2 ICLK			Not present in versions with 112, 100, 64 or 48 pins.
0008 71C0h	ICU	DTC Activation Enable Register 192	DTCER192	8	8	2 ICLK			Not present in versions with 112, 100, 64 or 48 pins.
0008 71C3h	ICU	DTC Activation Enable Register 195	DTCER195	8	8	2 ICLK			
0008 71C4h	ICU	DTC Activation Enable Register 196	DTCER196	8	8	2 ICLK			
0008 71C6h	ICU	DTC Activation Enable Register 198	DTCER198	8	8	2 ICLK			
0008 71C7h	ICU	DTC Activation Enable Register 199	DTCER199	8	8	2 ICLK			
0008 71C8h	ICU	DTC Activation Enable Register 200	DTCER200	8	8	2 ICLK			
0008 71C9h	ICU	DTC Activation Enable Register 201	DTCER201	8	8	2 ICLK			
0008 71D6h	ICU	DTC Activation Enable Register 214	DTCER214	8	8	2 ICLK			
0008 71D7h	ICU	DTC Activation Enable Register 215	DTCER215	8	8	2 ICLK			
0008 71D9h	ICU	DTC Activation Enable Register 217	DTCER217	8	8	2 ICLK			
0008 71DAh	ICU	DTC Activation Enable Register 218	DTCER218	8	8	2 ICLK			
0008 71DCh	ICU	DTC Activation Enable Register 220	DTCER220	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 71DDh	ICU	DTC Activation Enable Register 221	DTCER221	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 71DFh	ICU	DTC Activation Enable Register 223	DTCER223	8	8	2 ICLK			Not present in versions with 100, 64 or 48 pins.
0008 71E0h	ICU	DTC Activation Enable Register 224	DTCER224	8	8	2 ICLK			Not present in versions with 100, 64 or 48 pins.
0008 71E2h	ICU	DTC Activation Enable Register 226	DTCER226	8	8	2 ICLK			
0008 71E3h	ICU	DTC Activation Enable Register 227	DTCER227	8	8	2 ICLK			
0008 71E4h	ICU	DTC Activation Enable Register 228	DTCER228	8	8	2 ICLK			
0008 71E5h	ICU	DTC Activation Enable Register 229	DTCER229	8	8	2 ICLK			
0008 71E6h	ICU	DTC Activation Enable Register 230	DTCER230	8	8	2 ICLK			
0008 71E7h	ICU	DTC Activation Enable Register 231	DTCER231	8	8	2 ICLK			
0008 71E8h	ICU	DTC Activation Enable Register 232	DTCER232	8	8	2 ICLK			
0008 71E9h	ICU	DTC Activation Enable Register 233	DTCER233	8	8	2 ICLK			
0008 71EAh	ICU	DTC Activation Enable Register 234	DTCER234	8	8	2 ICLK			
0008 71EBh	ICU	DTC Activation Enable Register 235	DTCER235	8	8	2 ICLK			
0008 71ECh	ICU	DTC Activation Enable Register 236	DTCER236	8	8	2 ICLK			
0008 71EEh	ICU	DTC Activation Enable Register 238	DTCER238	8	8	2 ICLK			
0008 71EFh	ICU	DTC Activation Enable Register 239	DTCER239	8	8	2 ICLK			
0008 71F0h	ICU	DTC Activation Enable Register 240	DTCER240	8	8	2 ICLK			
0008 71F1h	ICU	DTC Activation Enable Register 241	DTCER241	8	8	2 ICLK			
0008 71F2h	ICU	DTC Activation Enable Register 242	DTCER242	8	8	2 ICLK			
0008 71F4h	ICU	DTC Activation Enable Register 244	DTCER244	8	8	2 ICLK			
0008 71F5h	ICU	DTC Activation Enable Register 245	DTCER245	8	8	2 ICLK			
0008 71F6h	ICU	DTC Activation Enable Register 246	DTCER246	8	8	2 ICLK			
0008 71F7h	ICU	DTC Activation Enable Register 247	DTCER247	8	8	2 ICLK			
0008 71F8h	ICU	DTC Activation Enable Register 248	DTCER248	8	8	2 ICLK			
0008 71FAh	ICU	DTC Activation Enable Register 250	DTCER250	8	8	2 ICLK			
0008 71FBh	ICU	DTC Activation Enable Register 251	DTCER251	8	8	2 ICLK			
0008 7202h	ICU	Interrupt Request Enable Register 02	IER02	8	8	2 ICLK			
0008 7203h	ICU	Interrupt Request Enable Register 03	IER03	8	8	2 ICLK			
0008 7204h	ICU	Interrupt Request Enable Register 04	IER04	8	8	2 ICLK			
0008 7205h	ICU	Interrupt Request Enable Register 05	IER05	8	8	2 ICLK			

Table 4.1 List of I/O Registers (Address Order) (15/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 8308h	RIIC0	I²C Bus Status Register 1	ICSR1	8	8	2, 3 PCLKB	2 ICLK	RIIC	
0008 8309h	RIIC0	I²C Bus Status Register 2	ICSR2	8	8	2, 3 PCLKB	2 ICLK		
0008 830Ah	RIIC0	Slave Address Register L0	SARL0	8	8	2, 3 PCLKB	2 ICLK		
0008 830Ah	RIIC0	Timeout Internal Counter L	TMOCNTL	8	8	2, 3 PCLKB	2 ICLK		
0008 830Bh	RIIC0	Slave Address Register U0	SARU0	8	8	2, 3 PCLKB	2 ICLK		
0008 830Bh	RIIC0	Timeout Internal Counter U	TMOCNTU	8	8*2	2, 3 PCLKB	2 ICLK		
0008 830Ch	RIIC0	Slave Address Register L1	SARL1	8	8	2, 3 PCLKB	2 ICLK		
0008 830Dh	RIIC0	Slave Address Register U1	SARU1	8	8	2, 3 PCLKB	2 ICLK		
0008 830Eh	RIIC0	Slave Address Register L2	SARL2	8	8	2, 3 PCLKB	2 ICLK		
0008 830Fh	RIIC0	Slave Address Register U2	SARU2	8	8	2, 3 PCLKB	2 ICLK		
0008 8310h	RIIC0	I²C Bus Bit Rate Low-Level Register	ICBRL	8	8	2, 3 PCLKB	2 ICLK		
0008 8311h	RIIC0	I²C Bus Bit Rate High-Level Register	ICBRH	8	8	2, 3 PCLKB	2 ICLK		
0008 8312h	RIIC0	I²C Bus Transmit Data Register	ICDRT	8	8	2, 3 PCLKB	2 ICLK		
0008 8313h	RIIC0	I²C Bus Receive Data Register	ICDRR	8	8	2, 3 PCLKB	2 ICLK		
0008 8320h	RIIC1	I²C Bus Control Register 1	ICCR1	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
0008 8321h	RIIC1	I²C Bus Control Register 2	ICCR2	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
0008 8322h	RIIC1	I²C Bus Mode Register 1	ICMR1	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
0008 8323h	RIIC1	I²C Bus Mode Register 2	ICMR2	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
0008 8324h	RIIC1	I²C Bus Mode Register 3	ICMR3	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
0008 8325h	RIIC1	I²C Bus Function Enable Register	ICFER	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
0008 8326h	RIIC1	I²C Bus Status Enable Register	ICSER	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
0008 8327h	RIIC1	I²C Bus Interrupt Enable Register	ICIER	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
0008 8328h	RIIC1	I²C Bus Status Register 1	ICSR1	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
0008 8329h	RIIC1	I²C Bus Status Register 2	ICSR2	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
0008 832Ah	RIIC1	Slave Address Register L0	SARL0	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
0008 832Ah	RIIC1	Timeout Internal Counter L	TMOCNTL	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
0008 832Bh	RIIC1	Slave Address Register U0	SARU0	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
0008 832Bh	RIIC1	Timeout Internal Counter U	TMOCNTU	8	8*2	2, 3 PCLKB	2 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
0008 832Ch	RIIC1	Slave Address Register L1	SARL1	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
0008 832Dh	RIIC1	Slave Address Register U1	SARU1	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
0008 832Eh	RIIC1	Slave Address Register L2	SARL2	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
0008 832Fh	RIIC1	Slave Address Register U2	SARU2	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 112, 100, 64, or 48 pins.

Table 4.1 List of I/O Registers (Address Order) (16/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 8330h	RIIC1	I²C Bus Bit Rate Low-Level Register	ICBRL	8	8	2, 3 PCLKB	2 ICLK	RIIC	Not present in versions with 112, 100, 64, or 48 pins.
0008 8331h	RIIC1	I²C Bus Bit Rate High-Level Register	ICBRH	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
0008 8332h	RIIC1	I²C Bus Transmit Data Register	ICDRT	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
0008 8333h	RIIC1	I²C Bus Receive Data Register	ICDRR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
0008 8380h	RSPI0	RSPI Control Register	SPCR	8	8	2, 3 PCLKB	2 ICLK	RSPI	
0008 8381h	RSPI0	RSPI Slave Select Polarity Register	SSLP	8	8	2, 3 PCLKB	2 ICLK		
0008 8382h	RSPI0	RSPI Pin Control Register	SPPCR	8	8	2, 3 PCLKB	2 ICLK		
0008 8383h	RSPI0	RSPI Status Register	SPSR	8	8	2, 3 PCLKB	2 ICLK		
0008 8384h	RSPI0	RSPI Data Register	SPDR	32	16, 32	2, 3 PCLKB	2 ICLK		
0008 8388h	RSPI0	RSPI Sequence Control Register	SPSCR	8	8	2, 3 PCLKB	2 ICLK		
0008 8389h	RSPI0	RSPI Sequence Status Register	SPSSR	8	8	2, 3 PCLKB	2 ICLK		
0008 838Ah	RSPI0	RSPI Bit Rate Register	SPBR	8	8	2, 3 PCLKB	2 ICLK		
0008 838Bh	RSPI0	RSPI Data Control Register	SPDCR	8	8	2, 3 PCLKB	2 ICLK		
0008 838Ch	RSPI0	RSPI Clock Delay Register	SPCKD	8	8	2, 3 PCLKB	2 ICLK		
0008 838Dh	RSPI0	RSPI Slave Select Negation Delay Register	SSLND	8	8	2, 3 PCLKB	2 ICLK		
0008 838Eh	RSPI0	RSPI Next-Access Delay Register	SPND	8	8	2, 3 PCLKB	2 ICLK		
0008 838Fh	RSPI0	RSPI Control Register 2	SPCR2	8	8	2, 3 PCLKB	2 ICLK		
0008 8390h	RSPI0	RSPI Command Register 0	SPCMD0	16	16	2, 3 PCLKB	2 ICLK		
0008 8392h	RSPI0	RSPI Command Register 1	SPCMD1	16	16	2, 3 PCLKB	2 ICLK		
0008 8394h	RSPI0	RSPI Command Register 2	SPCMD2	16	16	2, 3 PCLKB	2 ICLK		
0008 8396h	RSPI0	RSPI Command Register 3	SPCMD3	16	16	2, 3 PCLKB	2 ICLK		
0008 8398h	RSPI0	RSPI Command Register 4	SPCMD4	16	16	2, 3 PCLKB	2 ICLK		
0008 839Ah	RSPI0	RSPI Command Register 5	SPCMD5	16	16	2, 3 PCLKB	2 ICLK		
0008 839Ch	RSPI0	RSPI Command Register 6	SPCMD6	16	16	2, 3 PCLKB	2 ICLK		
0008 839Eh	RSPI0	RSPI Command Register 7	SPCMD7	16	16	2, 3 PCLKB	2 ICLK		
0008 83A0h	RSPI1	RSPI Control Register	SPCR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 83A1h	RSPI1	RSPI Slave Select Polarity Register	SSLP	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 83A2h	RSPI1	RSPI Pin Control Register	SPPCR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 83A3h	RSPI1	RSPI Status Register	SPSR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 83A4h	RSPI1	RSPI Data Register	SPDR	32	16, 32	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 83A8h	RSPI1	RSPI Sequence Control Register	SPSCR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 83A9h	RSPI1	RSPI Sequence Status Register	SPSSR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 83AAh	RSPI1	RSPI Bit Rate Register	SPBR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 83ABh	RSPI1	RSPI Data Control Register	SPDCR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 83ACh	RSPI1	RSPI Clock Delay Register	SPCKD	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 83ADh	RSPI1	RSPI Slave Select Negation Delay Register	SSLND	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 83AEh	RSPI1	RSPI Next-Access Delay Register	SPND	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 83AFh	RSPI1	RSPI Control Register 2	SPCR2	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 83B0h	RSPI1	RSPI Command Register 0	SPCMD0	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.

Table 4.1 List of I/O Registers (Address Order) (24/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 C086h	PORT3	Open Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK	I/O Ports	Not present in versions with 144, 120, 112, or 100 pins.
0008 C087h	PORT3	Open Drain Control Register 1	ODR1	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64 or 48 pins.
0008 C090h	PORT8	Open Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C092h	PORT9	Open Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 144, 120, 112, 100 or 48 pins.
0008 C093h	PORT9	Open Drain Control Register 1	ODR1	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 48 pins.
0008 C094h	PORTA	Open Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C095h	PORTA	Open Drain Control Register 1	ODR1	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C096h	PORTB	Open Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK		
0008 C097h	PORTB	Open Drain Control Register 1	ODR1	8	8	2, 3 PCLKB	2 ICLK		
0008 C09Ah	PORTD	Open Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK		
0008 C09Bh	PORTD	Open Drain Control Register 1	ODR1	8	8	2, 3 PCLKB	2 ICLK		
0008 C09Eh	PORTF	Open Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 100, 64, or 48 pins.
0008 C0A0h	PORTG	Open Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 100, 64, or 48 pins.
0008 C0A1h	PORTG	Open Drain Control Register 1	ODR1	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 100, 64, or 48 pins.
0008 C0F2h	PORT	Driving Ability Control Register 1	DSCR1	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C0F3h	PORT	Driving Ability Control Register 2	DSCR2	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C100h	MPC	CS Output Enable Register	PFCSE	8	8	2, 3 PCLKB	2 ICLK	MPC	Not present in versions with 64 or 48 pins.
0008 C102h	MPC	CS Output Pin Select Register 0	PFCSS0	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C104h	MPC	Address Output Enable Register 0	PFAOE0	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C105h	MPC	Address Output Enable Register 1	PFAOE1	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C106h	MPC	External Bus Control Register 0	PFBCR0	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C107h	MPC	External Bus Control Register 1	PFBCR1	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C114h	MPC	USB0 Control Register	PFUSB0	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
0008 C11Fh	MPC	Write-Protect Register	PWPR	8	8	2, 3 PCLKB	2 ICLK		
0008 C140h	MPC	P00 Pin Function Control Register	P00PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 48 pins.
0008 C141h	MPC	P01 Pin Function Control Register	P01PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 48 pins.
0008 C142h	MPC	P02 Pin Function Control Register	P02PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 C143h	MPC	P03 Pin Function Control Register	P03PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 C148h	MPC	P10 Pin Function Control Register	P10PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 48 pins.
0008 C149h	MPC	P11 Pin Function Control Register	P11PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 48 pins.
0008 C14Ah	MPC	P12 Pin Function Control Register	P12PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 100, 64, or 48 pins.
0008 C14Bh	MPC	P13 Pin Function Control Register	P13PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 112, 100, 64, or 48 pins.

Table 4.1 List of I/O Registers (Address Order) (26/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 C174h	MPC	P64 Pin Function Control Register	P64PFS	8	8	2, 3 PCLKB	2 ICLK	MPC	Not present in versions with 64 or 48 pins.
0008 C175h	MPC	P65 Pin Function Control Register	P65PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C178h	MPC	P70 Pin Function Control Register	P70PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C179h	MPC	P71 Pin Function Control Register	P71PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C17Ah	MPC	P72 Pin Function Control Register	P72PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C17Bh	MPC	P73 Pin Function Control Register	P73PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C17Ch	MPC	P74 Pin Function Control Register	P74PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C17Dh	MPC	P75 Pin Function Control Register	P75PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C17Eh	MPC	P76 Pin Function Control Register	P76PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C180h	MPC	P80 Pin Function Control Register	P80PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C181h	MPC	P81 Pin Function Control Register	P81PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C182h	MPC	P82 Pin Function Control Register	P82PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C188h	MPC	P90 Pin Function Control Register	P90PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C189h	MPC	P91 Pin Function Control Register	P91PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 48 pins.
0008 C18Ah	MPC	P92 Pin Function Control Register	P92PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 48 pins.
0008 C18Bh	MPC	P93 Pin Function Control Register	P93PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 48 pins.
0008 C18Ch	MPC	P94 Pin Function Control Register	P94PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 48 pins.
0008 C18Dh	MPC	P95 Pin Function Control Register	P95PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C18Eh	MPC	P96 Pin Function Control Register	P96PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C190h	MPC	PA0 Pin Function Control Register	PA0PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C191h	MPC	PA1 Pin Function Control Register	PA1PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C192h	MPC	PA2 Pin Function Control Register	PA2PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C193h	MPC	PA3 Pin Function Control Register	PA3PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C194h	MPC	PA4 Pin Function Control Register	PA4PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 48 pins.
0008 C195h	MPC	PA5 Pin Function Control Register	PA5PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 48 pins.
0008 C196h	MPC	PA6 Pin Function Control Register	PA6PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64 or 48 pins.
0008 C198h	MPC	PB0 Pin Function Control Register	PB0PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C199h	MPC	PB1 Pin Function Control Register	PB1PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C19Ah	MPC	PB2 Pin Function Control Register	PB2PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C19Bh	MPC	PB3 Pin Function Control Register	PB3PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C19Ch	MPC	PB4 Pin Function Control Register	PB4PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C19Dh	MPC	PB5 Pin Function Control Register	PB5PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C19Eh	MPC	PB6 Pin Function Control Register	PB6PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C19Fh	MPC	PB7 Pin Function Control Register	PB7PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 48 pins.
0008 C1A0h	MPC	PC0 Pin Function Control Register	PC0PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 C1A1h	MPC	PC1 Pin Function Control Register	PC1PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 C1A2h	MPC	PC2 Pin Function Control Register	PC2PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64, or 48 pins.

Table 4.1 List of I/O Registers (Address Order) (35/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
000C 1308h	MTU0	Timer General Register A	TGRA	16	16, 32	4, 5 PCLKA	2, 3 ICLK	MTU3	
000C 130Ah	MTU0	Timer General Register B	TGRB	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 130Ch	MTU0	Timer General Register C	TGRC	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 130Eh	MTU0	Timer General Register D	TGRD	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1320h	MTU0	Timer General Register E	TGRE	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1322h	MTU0	Timer General Register F	TGRF	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1324h	MTU0	Timer Interrupt Enable Register 2	TIER2	8	8, 16	4, 5 PCLKA	2, 3 ICLK		
000C 1325h	MTU0	Timer Status Register 2	TSR2	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1326h	MTU0	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1380h	MTU1	Timer Control Register	TCR	8	8, 16	4, 5 PCLKA	2, 3 ICLK		
000C 1381h	MTU1	Timer Mode Register 1	TMDR1	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1382h	MTU1	Timer I/O Control Register	TIOR	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1384h	MTU1	Timer Interrupt Enable Register	TIER	8	8, 16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1385h	MTU1	Timer Status Register	TSR	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1386h	MTU1	Timer Counter	TCNT	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1388h	MTU1	Timer General Register A	TGRA	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 138Ah	MTU1	Timer General Register B	TGRB	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1390h	MTU1	Timer Input Capture Control Register	TICCR	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1400h	MTU2	Timer Control Register	TCR	8	8, 16	4, 5 PCLKA	2, 3 ICLK		
000C 1401h	MTU2	Timer Mode Register 1	TMDR1	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1402h	MTU2	Timer I/O Control Register	TIOR	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1404h	MTU2	Timer Interrupt Enable Register	TIER	8	8, 16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1405h	MTU2	Timer Status Register	TSR	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1406h	MTU2	Timer Counter	TCNT	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1408h	MTU2	Timer General Register A	TGRA	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 140Ah	MTU2	Timer General Register B	TGRB	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1A00h	MTU6	Timer Control Register	TCR	8	8, 16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1A01h	MTU7	Timer Control Register	TCR	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1A02h	MTU6	Timer Mode Register 1	TMDR1	8	8, 16	4, 5 PCLKA	2, 3 ICLK		
000C 1A03h	MTU7	Timer Mode Register 1	TMDR1	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1A04h	MTU6	Timer I/O Control Register H	TIORH	8	8, 16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1A05h	MTU6	Timer I/O Control Register L	TIORL	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1A06h	MTU7	Timer I/O Control Register H	TIORH	8	8, 16	4, 5 PCLKA	2, 3 ICLK		
000C 1A07h	MTU7	Timer I/O Control Register L	TIORL	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1A08h	MTU6	Timer Interrupt Enable Register	TIER	8	8, 16	4, 5 PCLKA	2, 3 ICLK		
000C 1A09h	MTU7	Timer Interrupt Enable Register	TIER	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1A0Ah	MTU	Timer Output Master Enable Register B	TOERB	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1A0Eh	MTU	Timer Output Control Register 1B	TOCR1B	8	8, 16	4, 5 PCLKA	2, 3 ICLK		
000C 1A0Fh	MTU	Timer Output Control Register 2B	TOCR2B	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1A10h	MTU6	Timer Counter	TCNT	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1A12h	MTU7	Timer Counter	TCNT	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1A14h	MTU	Timer Cycle Data Register B	TCDRB	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1A16h	MTU	Timer Dead Time Data Register B	TDDRB	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1A18h	MTU6	Timer General Register A	TGRA	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1A1Ah	MTU6	Timer General Register B	TGRB	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1A1Ch	MTU7	Timer General Register A	TGRA	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1A1Eh	MTU7	Timer General Register B	TGRB	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1A20h	MTU	Timer Subcounter B	TCNTSB	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1A22h	MTU	Timer Cycle Buffer Register B	TCBRB	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1A24h	MTU6	Timer General Register C	TGRC	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1A26h	MTU6	Timer General Register D	TGRD	16	16	4, 5 PCLKA	2, 3 ICLK		

5.3.3 Timing of Recovery from Low Power Consumption Modes

Table 5.10 Timing of Recovery from Low Power Consumption Modes

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time after cancellation of software standby mode	Crystal resonator connected to main clock oscillator	Main clock oscillator operating	t_{SBYMC}	10	—	—	ms	Figure 5.9
		Main clock oscillator and PLL circuit operating	t_{SBYPC}	10	—	—	ms	
	External clock input to main clock oscillator	Main clock oscillator operating	t_{SBYEX}	1	—	—	ms	
		Main clock oscillator and PLL circuit operating	t_{SBYPE}	1	—	—	ms	
	Low-speed clock oscillator or IWDT-specific low-speed clock oscillator operating		t_{SBYLO}	—	—	800	µs	
Recovery time after cancellation of deep software standby mode			t_{DSBY}	—	—	1	ms	Figure 5.10
Wait time after cancellation of deep software standby mode			t_{DSBYWT}	45	—	46	t_{cyc}	

Note: • The wait time varies depending on the state in which each oscillator was when the WAIT instruction was executed. The recovery time when multiple oscillators are operating is the same period as that when the oscillator, which takes the longest time for recovery among the operating oscillators, is operating alone.

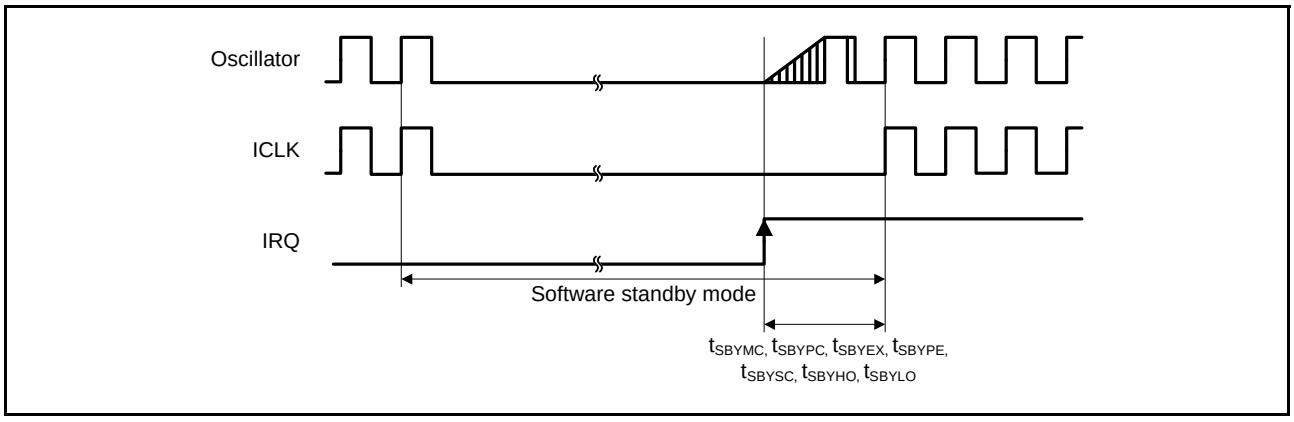


Figure 5.9 Software Standby Mode Cancellation Timing

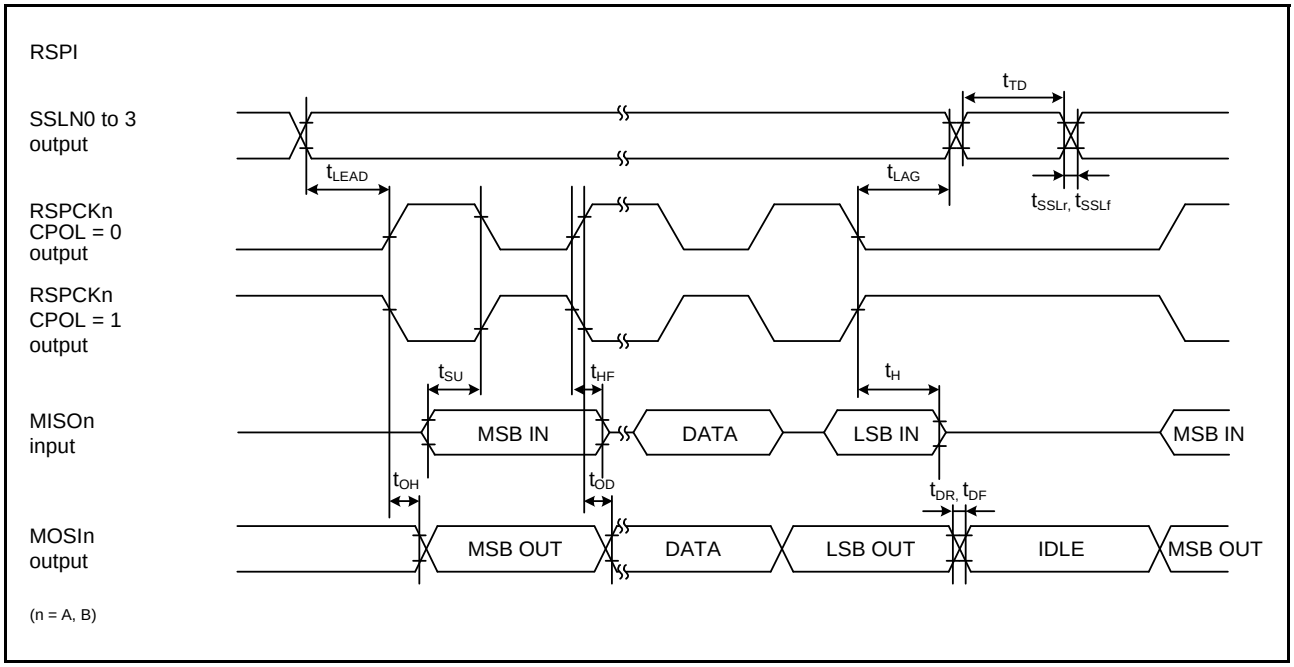


Figure 5.33 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKB Division Ratio Set to 1/2)

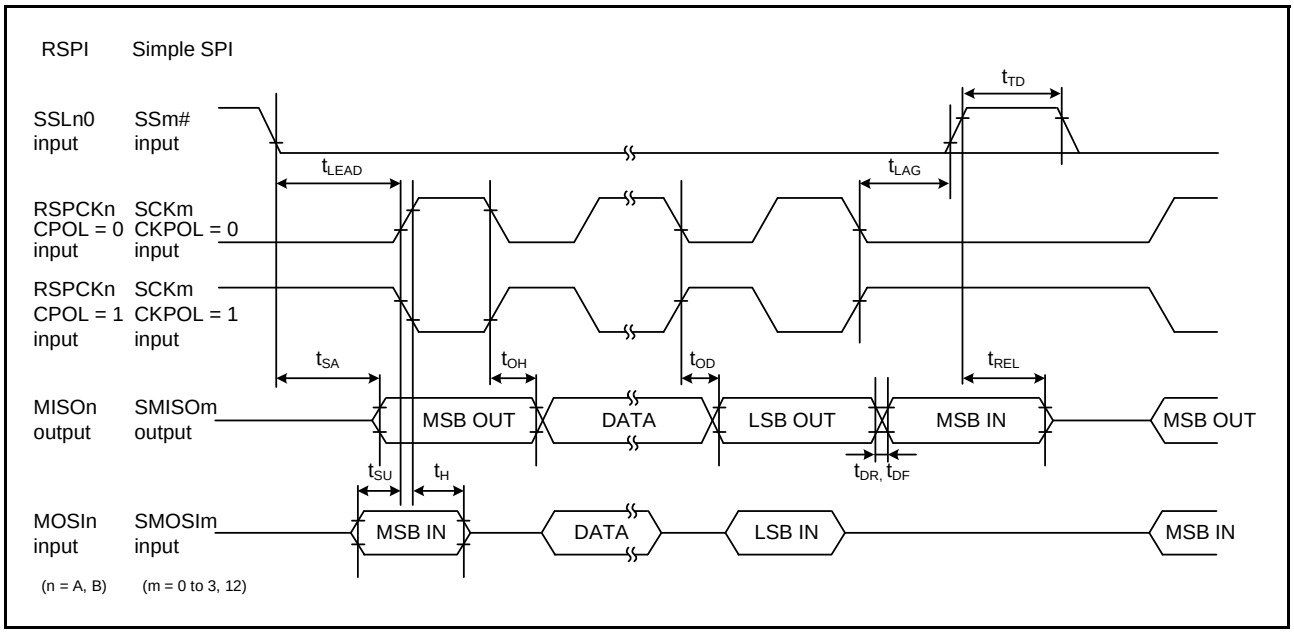


Figure 5.34 RSPI Timing (Slave, CPHA = 0) and Simple SPI Timing (Slave, CKPH = 1)

5.5 A/D Conversion Characteristics

Table 5.19 10-Bit A/D Conversion Characteristics (1)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item			Min.	Typ.	Max.	Unit	Test Conditions
Resolution			10	10	10	Bit	
Conversion time*1 (Operation at ADCLK = 100 MHz)	With 0.1-µF external capacitor	AN0 to AN7	0.5	—	—	µs	Sampling in 25 states
		Other channels	0.75	—	—	µs	Sampling in 50 states
	Without 0.1-µF external capacitor Permissible signal source impedance (max.) = 1 kΩ	AN0 to AN7	0.6	—	—	µs	Sampling in 35 states
		Other channels	0.75	—	—	µs	Sampling in 50 states
Analog input capacitance			—	—	6	pF	
Integral nonlinearity error			—	—	±3.0	LSB	
Offset error			—	—	±2.0	LSB	
Full-scale error			—	—	±3.0	LSB	
Quantization error			—	±0.5	—	LSB	
Absolute accuracy			—	—	±6.0	LSB	

Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

5.9 ROM (Flash Memory for Code Storage) Characteristics

Table 5.29 ROM (Flash Memory for Code Storage) Characteristics (1)

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Temperature range for the programming/erasure operation: $T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Reprogram/erase cycle*1	N_{pec}	1000	—	—	Times	
Data hold time	t_{DRP}	30*2	—	—	Year	Ta = +85°C

Note 1. Definition of reprogram/erase cycle:
The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 128-byte programming is performed 16 times for different addresses in 2-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).
Note 2. The value is obtained from the reliability test.

Table 5.30 ROM (Flash Memory for Code Storage) Characteristics (2)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Temperature range for the programming/erasure operation: $T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time $N_{PEC} \leq 100$ times	128 bytes	t_{P128}	—	2.8	28	—	1	10	ms
	4 Kbytes	t_{P4K}	—	63	140	—	23	50	ms
	16 Kbytes	t_{P16K}	—	252	560	—	90	200	ms
Programming time $N_{PEC} > 100$ times	128 bytes	t_{P128}	—	3.4	33.6	—	1.2	12	ms
	4 Kbytes	t_{P4K}	—	75.6	168	—	27.6	60	ms
	16 Kbytes	t_{P16K}	—	302.4	672	—	108	240	ms
Erasure time $N_{PEC} \leq 100$ times	4 Kbytes	t_{E4K}	—	50	120	—	25	60	ms
	16 Kbytes	t_{E16K}	—	200	480	—	100	240	ms
Erasure time $N_{PEC} > 100$ times	4 Kbytes	t_{E4K}	—	60	144	—	30	72	ms
	16 Kbytes	t_{E16K}	—	240	576	—	120	288	ms
Suspend delay time during programming		t_{SPD}	—	—	400	—	—	120	µs
First suspend delay time during erasing (in suspend priority mode)		t_{SESD1}	—	—	300	—	—	120	µs
Second suspend delay time during erasing (in suspend priority mode)		t_{SESD2}	—	—	1.7	—	—	1.7	ms
Suspend delay time during erasing (in erasure priority mode)		t_{SEED}	—	—	1.7	—	—	1.7	ms
FCU reset time		t_{FCUR}	35	—	—	35	—	—	µs

6.5 Power-on Reset Circuit and Voltage Detection Circuit Characteristics

Table 6.18 Power-on Reset Circuit and Voltage Detection Circuit Characteristics

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	V_{POR}	2.5	2.6	2.7	V	Figure 6.26
	Voltage detection circuit (LVD0)	V_{DET0}	2.7	2.8	2.9		Figure 6.27
	Voltage detection circuit (LVD1)	V_{DET1}	2.80	2.95	3.10		
	Voltage detection circuit (LVD2)	V_{DET2}	2.80	2.95	3.10		
Internal reset time	Power-on reset (POR)	t_{POR}	—	4.6		ms	Figure 6.26
	Voltage detection circuit (LVD0)	t_{LVD0}	—	4.6			Figure 6.27
	Voltage detection circuit (LVD1)	t_{LVD1}	—	0.9			Figure 6.28
	Voltage detection circuit (LVD2)	t_{LVD2}	—	0.9			Figure 6.29
Minimum VCC down time*1		t_{VOFF}	200	—	—	µs	Figure 6.26, Figure 6.27
Response delay time		t_{det}			200	µs	Figure 6.26 to Figure 6.29
LVD operation stabilization time (after LVD is enabled)		$Td_{(E-A)}$			3	µs	Figure 6.28 Figure 6.29
Hysteresis width (LVD1 and LVD2)		V_{LVH}		80		mV	

Note 1. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{DET1}, and V_{DET2} for the POR/ LVD.

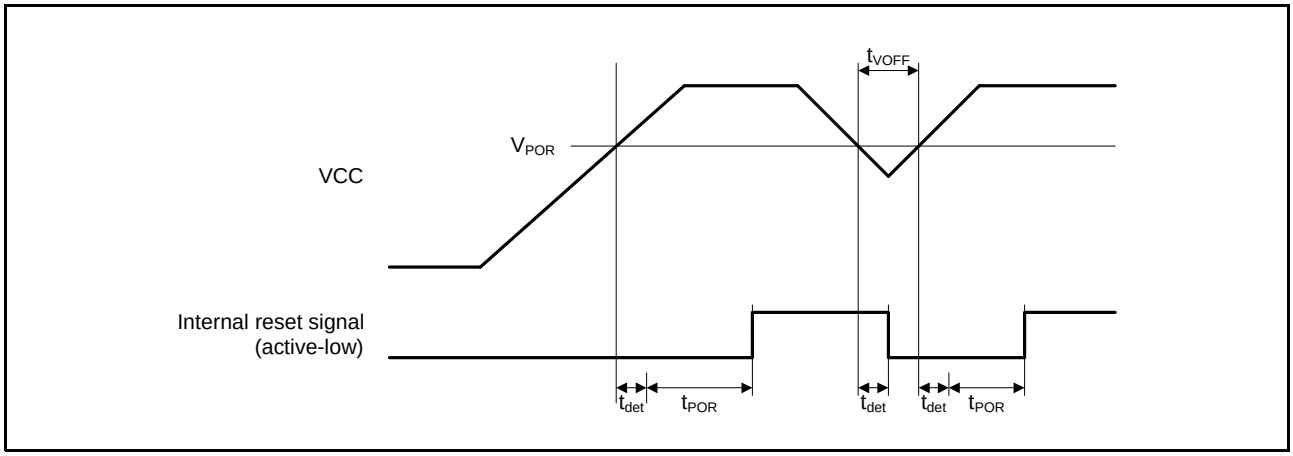


Figure 6.26 Power-on Reset Timing

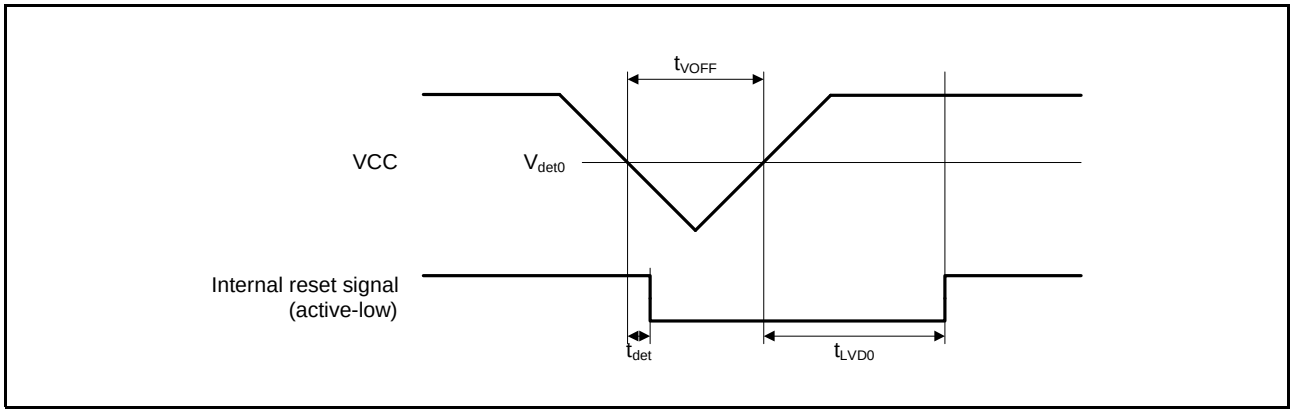


Figure 6.27 Voltage Detection Circuit Timing (V_{det0})

6.7 ROM (Flash Memory for Code Storage) Characteristics

Table 6.20 ROM (Flash Memory for Code Storage) Characteristics (1)

Condition: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Temperature range for the programming/erasure operation: $T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Reprogram/erase cycle*1	N_{pec}	1000	—	—	Times	
Data hold time	t_{DRP}	30*2	—	—	Year	Ta = +85°C

Note 1. Definition of reprogram/erase cycle:
The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 128-byte programming is performed 16 times for different addresses in 2-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).
Note 2. The value is obtained from the reliability test.

Table 6.21 ROM (Flash Memory for Code Storage) Characteristics (2)

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Temperature range for the programming/erasure operation: $T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item		Symbol	min	typ	max	Unit	Test Conditions
Programming time	128 bytes	t_{P128}	—	1	10	ms	FCLK = 50MHz $N_{PEC} \leq 100$
	4 Kbytes	t_{P4K}	—	23	50	ms	
	16 Kbytes	t_{P16K}	—	90	200	ms	
	128 bytes	t_{P128}	—	1.2	12	ms	FCLK=50MHz $N_{PEC} > 100$
	4 Kbytes	t_{P4K}	—	27.6	60	ms	
	16 Kbytes	t_{P16K}	—	108	240	ms	
Erasure time	4 Kbytes	t_{E4K}	—	25	60	ms	FCLK=50MHz $N_{PEC} \leq 100$
	16 Kbytes	t_{E16K}	—	100	240	ms	
	4 Kbytes	t_{E4K}	—	30	72	ms	FCLK=50MHz $N_{PEC} > 100$
	16 Kbytes	t_{E16K}	—	120	288	ms	
Suspend delay time during programming		t_{SPD}	—	—	120	µs	Figure 6.31 FCLK = 50MHz
First suspend delay time during erasing (in suspend priority mode)		t_{SESD1}	—	—	120	µs	
Second suspend delay time during erasing (in suspend priority mode)		t_{SESD2}	—	—	1.7	ms	
Suspend delay time during erasing (in erasure priority mode)		t_{SEED}	—	—	1.7	ms	
FCU reset time		t_{FCUR}	35	—	—	µs	

REVISION HISTORY — RX63T Group Datasheet

Rev.	Date	Description	
		Page	Summary
1.00	Aug 28, 2012	—	First Edition issued
2.00	Mar 11, 2013	Features	
		1	Changed
		1. Overview	
		2	1.1 Outline of Specifications, description changed
		2 to 8	Table 1.1 Outline of Specifications, changed
		9	Table 1.2 Comparison of Functions for Different Packages, changed
		10 to 12	Table 1.3 List of Products, changed
		12	Figure 1.1 How to Read the Product Part Number, changed
		13	Figure 1.2 Block Diagram, changed
		14 to 18	Table 1.4 Pin Functions, changed
		19	Figure 1.3 Pin Assignment (144-Pin LQFP), added
		20	Figure 1.4 Pin Assignment (120-Pin LQFP), added
		21	Figure 1.5 Pin Assignment (112-Pin LQFP), added
		22	Figure 1.6 Pin Assignment (100-Pin LQFP), added
		23	Figure 1.7 Pin Assignment (64-Pin LQFP), notes changed
		24	Figure 1.8 Pin Assignment (48-Pin LQFP), notes changed
		25 to 28	Table 1.5 List of Pins and Pin Functions (144-Pin LQFP), added
		29 to 32	Table 1.6 List of Pins and Pin Functions (120-Pin LQFP), added
		33 to 36	Table 1.7 List of Pins and Pin Functions (112-Pin LQFP), added
		37 to 39	Table 1.8 List of Pins and Pin Functions (100-Pin LQFP), added
		3. Address Space	
		49	Figure 3.1 Memory Map in Each Operating Mode, changed
		50	3.2 External Address Space, added
		4. I/O Registers	
		52	(3) Number of Access Cycles to I/O Registers, description changed
		53 to 103	Table 4.1 List of I/O Registers (Address Order), changed
		5. Electrical Characteristics [144-, 120-, 112- and 100-Pin Versions]	
		104 to 148	Added
		6. Electrical Characteristics [64- and 48-Pin Versions]	
		149	Title changed
		152	Table 6.6 Clock Timing, changed
		158	Table 6.10 Timing of On-Chip Peripheral Modules (1), changed
		160	Table 6.12 Timing of On-Chip Peripheral Modules (3), changed
		170	6.6 Oscillation Stop Detection Circuit Characteristics, title changed
		170	Table 6.18 Oscillation Stop Detection Circuit Characteristics, title changed
		171	Table 6.19 ROM (Flash Memory for Code Storage) Characteristics (1), added
		171	Table 6.20 ROM (Flash Memory for Code Storage) Characteristics (2), title and description changed
		172	Table 6.21 DataFlash (Flash Memory for Data Storage) Characteristics (1), added
		172	Table 6.22 DataFlash (Flash Memory for Data Storage) Characteristics (2), title and description changed
		Appendix 1. Package Dimensions	
		174 to 177	Figure A 144-Pin LQFP (PLQP0144KA-A) to Figure D 100-Pin LQFP (PLQP0100KB-A), added
2.10	Sep 26, 2013	The RX63T Group and RX63T changed to this MCU	
		Features	
		1	Changed
		1. Overview	
		2 to 8	Table 1.1 Outline of Specifications, changed, Note 1, added.
		9	Table 1.2 Comparison of Functions for Different Packages, changed, Note 2, added.
		10 to 14	Table 1.3 List of Products, changed, Note 1, added
		15	Figure 1.1 How to Read the Product Part Number, changed
		28 to 31	Table 1.5 List of Pins and Pin Functions (144-Pin LQFP), changed
		32 to 35	Table 1.6 List of Pins and Pin Functions (120-Pin LQFP), changed