Renesas Electronics America Inc - R5F563TCBDFB#V0 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	81
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 20x10b, 8x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f563tcbdfb-v0

Table 1.1 Outline of Specifications (2/7)

Classification	Module/Function	Description
Clock	Clock generation circuit	• Main clock oscillator, low-speed on-chip oscillator, PLL frequency synthesizer, and dedicated on-chip oscillator for the IWDT • Main-clock oscillation stop detection • Separate frequency-division and multiplication settings for the system clock (ICLK), peripheral module clock (PCLKA), peripheral module clock (PCLKB), AD clock (PCLKC), FlashIF clock (FCLK) and S12AD clock (PCLKD). The CPU and other bus masters run in synchronization with the system clock (ICLK): Up to 100 MHz Multi-function timer pulse unit 3 and general PWM timer run in synchronization with PCLKA: Up to 100 MHz Peripheral modules run in synchronization with the peripheral module clock (PCLKB): Up to 50 MHz Flash IF run in synchronization with the FlashIF clock (FCLK): Up to 50 MHz Devices connected to the external bus run in synchronization with the external bus clock (BCLK): Up to 50 MHz 10-bit A/D converter runs in synchronization with the AD clock (PCLKC): Up to 100 MHz 12-bit A/D converter runs in synchronization with the S12AD clock (PCLKD): Up to 50 MHz
Clock	Clock frequency accuracy measurement circuit (CAC)	The frequency of the following clocks can be measured; the main clock oscillator, PLL circuit, and IWDT-dedicated on-chip oscillator.
Reset		RES# pin reset, power-on reset, voltage-monitoring reset, independent watchdog timer reset, watchdog timer reset, deep software standby reset, and software reset
Voltage detection circuit		When the voltage on VCC passes the voltage detection level (Vdet), an internal reset or internal interrupt is generated.
Low power consumption	Low power consumption facilities	• Module stop function • Four low power consumption modes Sleep mode, all-module clock stop mode, software standby mode, and deep software standby mode
Interrupt	Interrupt controller (ICUb)	• Peripheral function interrupts: Up to 169 sources • External interrupts: Up to 8 (pins IRQ0 to IRQ7) • Software interrupts: One source • Non-maskable interrupts: 6 sources • Sixteen levels specifiable for the order of priority
External bus extension		• The external address space can be divided into four areas (CS0 to CS3), each with independent control of access settings. Capacity of each area: 1 Mbyte (CS0 to CS3) A chip-select signal (CS0# to CS3#) can be output for each area. Each area is specifiable as an 8- or 16-bit bus space The data arrangement in each area is selectable as little or big endian (only for data). • Bus format: Separate bus, multiplex bus • Wait control • Write buffer facility
DMA	DMA controller (DMACA)	• 4 channels • Three transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Software trigger, external interrupts, and interrupt requests from peripheral functions
	Data transfer controller (DTCa)	• Three transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Software interrupt activation register settings, external interrupts, and interrupt requests from peripheral functions

Table 1.5 List of Pins and Pin Functions (144-Pin LQFP) (1/4)

Pin Number 144-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3, GPT, POE3, CAC)	Communications (SCIc, SCId, RSPI, RIIC, CAN, USB)	Interrupt	S12ADB, AD, DA
1	VCC_USB						
2		PE5	BCLK		USB0_VBUS	IRQ0	
3	EMLE						
4	TRSYNC	P03			RXD2/SMISO2/SSCL2	IRQ7	
5	TRDATA3	P02			TXD2/SMOSI2/SSDA2		
6	VSS						
7		P01	RD#		CTS0#/RTS0#/SS0#/ USB0_DRPD		
8	VCL						
9		P00	CS1#	CACREF			
10	MD/FINED						
11		PE4	A10	POE10#/MTCLKC		IRQ1	
12		PE3	A11	POE11#/MTCLKD		IRQ2-DS	
13	TRDATA2	P14			SCK2		
14	VCC						
15		P13			CTS2#/RTS2#/SS2#/ USB0_VBUSEN		
16	RES#						
17	XTAL						
18	VSS						
19	EXTAL						
20	VCC						
21		PE2		POE10#		NMI	
22		PE1	WR0#/WR#		CTS12#/RTS12#/ SS12#/SSLA3/SSLB3/ USB0_OVRCURA		
23		PE0	WR1#/BC1#/ WAIT#		SSLA2/SSLB2/CRX1/ USB0_OVRCURB	IRQ7	
24		PD7		GTIOC0A	CTS0#/RTS0#/SS0#/ SSLA1/SSLB1/CTX1		
25		PD6		GTIOC0B	SSLA0/SSLB0		
26		PD5		GTIOC1A	RXD1/SMISO1/SSCL1	IRQ6	
27	VSS						
28		PD4		GTIOC1B	SCK1		
29		PD3		GTIOC2A	TXD1/SMOSI1/SSDA1		
30		PD2	CS2#	GTIOC2B	MOSIA/MOSIB/ USB0_ID		
31		PD1	CS0#	GTIOC3A	MISOA/MISOB/ USB0_EXICEN		
32		PD0	A12	GTIOC3B	RSPCKA/RSPCKB		
33		PF4	CS3#				
34		PF3			TXD1/SMOSI1/SSDA1		
35		PF2	CS1#		RXD1/SMISO1/SSCL1	IRQ5	
36	TRST#	PF1					
37	TMS	PF0					
38		PB7	A19		SCK12		

Table 1.8 List of Pins and Pin Functions (100-Pin LQFP) (1/3)

Pin Number 100-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3, GPT, POE3, CAC)	Communications (SCIc, SCId, RSPI, RIIC, CAN)	Interrupt	S12ADB, AD, DA
1		PE5	BCLK			IRQ0	
2	EMLE						
3	VSS						
4		P01	RD#		CTS0#/RTS0#/SS0#		
5	VCL						
6		P00	CS1#	CACREF			
7	MD/FINED						
8		PE4	A10	POE10#/MTCLKC		IRQ1	
9		PE3	A11	POE11#/MTCLKD		IRQ2-DS	
10	RES#						
11	XTAL						
12	VSS						
13	EXTAL						
14	VCC						
15		PE2		POE10#		NMI	
16		PE1	WR0#/WR#		CTS12#/RTS12#/ SS12#/SSLA3/SSLB3		
17		PE0	WR1#/BC1#/ WAIT#		SSLA2/SSLB2/CRX1	IRQ7	
18	TRST#	PD7		GTIOC0A	CTS0#/RTS0#/SS0#/ SSLA1/SSLB1/CTX1		
19	TMS	PD6		GTIOC0B	SSLA0/SSLB0		
20	TDI	PD5		GTIOC1A	RXD1/SMISO1/SSCL1	IRQ6	
21	TCK/FINEC	PD4		GTIOC1B	SCK1		
22	TDO	PD3		GTIOC2A	TXD1/SMOSI1/SSDA1		
23		PD2	CS2#	GTIOC2B	MOSIA/MOSIB		
24		PD1	CS0#	GTIOC3A	MISOA/MISOB		
25		PD0	A12	GTIOC3B	RSPCKA/RSPCKB		
26		PB7	A19		SCK12		
27		PB6	A18		RXD12/SMISO12/ SSCL12/RXDX12/ CRX1	IRQ2	
28		PB5	A17		TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/CTX1		
29	PLLVCC						
30		PB4	A16	POE8#/GTETRG0		IRQ3-DS	
31	PLLVSS						
32		PB3	A15	MTIOC0A/CACREF	SCK0		
33		PB2		MTIOC0B	TXD0/SMOSI0/ SSDA0/SDA0		
34		PB1		MTIOC0C	RXD0/SMISO0/ SSCL0/SCL0	IRQ4	
35		PB0	A14	MTIOC0D	MOSIA/MOSIB		
36		PA5		MTIOC1A	RXD0/SMISO0/ SSCL0/ MISOA/MISOB		ADTRG1#

Table 1.8 List of Pins and Pin Functions (100-Pin LQFP) (2/3)

Pin Number 100-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3, GPT, POE3, CAC)	Communications (SCIc, SCId, RSPI, RIIC, CAN)	Interrupt	S12ADB, AD, DA
37		PA4		MTIOC1B	TXD0/SMOSI0/ SSDA0/ RSPCKA/RSPCKB		ADTRG0#
38		PA3		MTIOC2A	SCK0/SSLA0/SSLB0		
39		PA2		MTIOC2B	RXD2/SMISO2/ SSCL2/ SSLA1/SSLB1		
40		PA1		MTIOC6A	TXD2/SMOSI2/ SSDA2/ SSLA2/SSLB2		
41		PA0		MTIOC6C	SCK2/SSLA3/SSLB3		
42	VCC						
43		P96	A13	POE4#	RXD1/SMISO1/SSCL1	IRQ4-DS	
44	VSS						
45		P95		MTIOC6B/GTIOC4A	TXD1/SMOSI1/SSDA1		
46		P94		MTIOC7A/GTIOC5A	CTS1#/RTS1#/SS1#		
47		P93		MTIOC7B/GTIOC6A	CTS2#/RTS2#/SS2#		
48		P92		MTIOC6D/GTIOC4B			
49		P91		MTIOC7C/GTIOC5B			
50		P90		MTIOC7D/GTIOC6B			
51		P76	D0/[A0/D0]	MTIOC4D/GTIOC2B			
52		P75	D1/[A1/D1]	MTIOC4C/GTIOC1B			
53		P74	D2/[A2/D2]	MTIOC3D/GTIOC0B			
54		P73	D3/[A3/D3]	MTIOC4B/GTIOC2A			
55		P72	D4/[A4/D4]	MTIOC4A/GTIOC1A			
56		P71	D5/[A5/D5]	MTIOC3B/GTIOC0A			
57		P70	D6/[A6/D6]	POE0#	CTS1#/RTS1#/SS1#	IRQ5-DS	
58		P33	D7/[A7/D7]	MTIOC3A/MTCLKA	SSLA3/SSLB3		
59		P32	D8/[A8/D8]	MTIOC3C/MTCLKB	SSLA2/SSLB2		
60	VCC						
61		P31	D9/[A9/D9]	MTIOC0A/MTCLKC	SSLA1/SSLB1		
62	VSS						
63		P30	D10/[A10/ D10]	MTIOC0B/MTCLKD	SCK0/SSLA0/SSLB0		
64		P24	D11/[A11/D11]		CTS0#/RTS0#/SS0#/ RSPCKA/RSPCKB	IRQ4	
65		P23	D12/[A12/ D12]	CACREF	TXD0/SMOSI0/ SSDA0/MOSIA/ MOSIB/CTX1		
66		P22	D13/[A13/ D13]		RXD0/SMISO0/ SSCL0/MISOA/ MISOB/CRX1		ADTRG#
67		P21	D14/[A14/ D14]	MTCLKA		IRQ6-DS	ADTRG1#
68		P20	D15/[A15/ D15]	MTCLKB		IRQ7-DS	ADTRG0#
69		P65	A0/BC0#				AN5
70		P64	A1				AN4

Table 1.9 List of Pins and Pin Functions (64-Pin LQFP) (1/3)

Pin Number 64-Pin LQFP	Power Supply Clock System Control	I/O Port	POE3	Timer (MTU3, GPT, CAC)	Communications (SCIc, SCId)	Communications (RSPI, RIIC)	Interrupt	S12ADB
1	EMLE							
2		P00		GTIOC3A	CTS0# RTS0# SS0#		IRQ2-DS	
3	VCL							
4		P01		GTIOC3B CACREF			IRQ4-DS	
5	MD FINED							
6	RES#							
7	XTAL							
8	VSS							
9	EXTAL							
10	VCC							
11		PE2	POE10#				NMI	
12	TRST#	PD7		GTIOC0A	CTS0# RTS0# SS0#			
13	TMS	PD6		GTIOC0B				
14	TDI	PD5		GTIOC1A	RXD1 SMISO1 SSCL1			
15	TCK FINEC	PD4		GTIOC1B	SCK1			
16	TDO	PD3		GTIOC2A	TXD1 SMOSI1 SSDA1			
17		PB7		GTIOC2B	SCK12			
18		PB6		GTIOC2B	RXD12 SMISO12 SSCL12 RXDX12			
19		PB5	POE11#		TXD12 SMOSI12 SSDA12 TXDX12 SIOX12		IRQ0	
20	VCC							
21		PB4	POE8#	GTETRG	CTS12# RTS12# SS12#		IRQ3-DS	
22	VSS							
23		PB3		MTIOC0A MTCLKA CACREF	SCK0			
24		PB2		MTIOC0B MTCLKB	TXD0 SMOSI0 SSDA0	SDA		
25		PB1		MTIOC0C	RXD0 SMISO0 SSCL0	SCL		
26		PB0		MTIOC0D		MOSIA		

Table 4.1 List of I/O Registers (Address Order) (8/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 711Bh	ICU	DTC Activation Enable Register 027	DTCER027	8	8	2 ICLK		ICUb	
0008 711Ch	ICU	DTC Activation Enable Register 028	DTCER028	8	8	2 ICLK			
0008 711Dh	ICU	DTC Activation Enable Register 029	DTCER029	8	8	2 ICLK			
0008 711Eh	ICU	DTC Activation Enable Register 030	DTCER030	8	8	2 ICLK			
0008 711Fh	ICU	DTC Activation Enable Register 031	DTCER031	8	8	2 ICLK			
0008 7121h	ICU	DTC Activation Enable Register 033	DTCER033	8	8	2 ICLK			Not present in versions with 112, 100, 64 or 48 pins.
0008 7122h	ICU	DTC Activation Enable Register 034	DTCER034	8	8	2 ICLK			Not present in versions with 112, 100, 64 or 48 pins.
0008 7127h	ICU	DTC Activation Enable Register 039	DTCER039	8	8	2 ICLK			
0008 7128h	ICU	DTC Activation Enable Register 040	DTCER040	8	8	2 ICLK			
0008 712Ah	ICU	DTC Activation Enable Register 042	DTCER042	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 712Bh	ICU	DTC Activation Enable Register 043	DTCER043	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7131h	ICU	DTC Activation Enable Register 049	DTCER049	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7132h	ICU	DTC Activation Enable Register 050	DTCER050	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7133h	ICU	DTC Activation Enable Register 051	DTCER051	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7134h	ICU	DTC Activation Enable Register 052	DTCER052	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7135h	ICU	DTC Activation Enable Register 053	DTCER053	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7136h	ICU	DTC Activation Enable Register 054	DTCER054	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7137h	ICU	DTC Activation Enable Register 055	DTCER055	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7138h	ICU	DTC Activation Enable Register 056	DTCER056	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 713Ah	ICU	DTC Activation Enable Register 058	DTCER058	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 713Bh	ICU	DTC Activation Enable Register 059	DTCER059	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 713Ch	ICU	DTC Activation Enable Register 060	DTCER060	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 713Dh	ICU	DTC Activation Enable Register 061	DTCER061	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 713Eh	ICU	DTC Activation Enable Register 062	DTCER062	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7140h	ICU	DTC Activation Enable Register 064	DTCER064	8	8	2 ICLK			
0008 7141h	ICU	DTC Activation Enable Register 065	DTCER065	8	8	2 ICLK			
0008 7142h	ICU	DTC Activation Enable Register 066	DTCER066	8	8	2 ICLK			
0008 7143h	ICU	DTC Activation Enable Register 067	DTCER067	8	8	2 ICLK			
0008 7144h	ICU	DTC Activation Enable Register 068	DTCER068	8	8	2 ICLK			
0008 7145h	ICU	DTC Activation Enable Register 069	DTCER069	8	8	2 ICLK			
0008 7146h	ICU	DTC Activation Enable Register 070	DTCER070	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7147h	ICU	DTC Activation Enable Register 071	DTCER071	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7162h	ICU	DTC Activation Enable Register 098	DTCER098	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7166h	ICU	DTC Activation Enable Register 102	DTCER102	8	8	2 ICLK			
0008 7167h	ICU	DTC Activation Enable Register 103	DTCER103	8	8	2 ICLK			
0008 7168h	ICU	DTC Activation Enable Register 104	DTCER104	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7169h	ICU	DTC Activation Enable Register 105	DTCER105	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 717Eh	ICU	DTC Activation Enable Register 126	DTCER126	8	8	2 ICLK			

Table 4.1 List of I/O Registers (Address Order) (13/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 739Ah	ICU	Interrupt Source Priority Register 154	IPR154	8	8	2 ICLK		ICUb	
0008 739Eh	ICU	Interrupt Source Priority Register 158	IPR158	8	8	2 ICLK			
0008 73A1h	ICU	Interrupt Source Priority Register 161	IPR161	8	8	2 ICLK			
0008 73A3h	ICU	Interrupt Source Priority Register 163	IPR163	8	8	2 ICLK			
0008 73A5h	ICU	Interrupt Source Priority Register 165	IPR165	8	8	2 ICLK			
0008 73A6h	ICU	Interrupt Source Priority Register 166	IPR166	8	8	2 ICLK			
0008 73ABh	ICU	Interrupt Source Priority Register 171	IPR171	8	8	2 ICLK			
0008 73ACh	ICU	Interrupt Source Priority Register 172	IPR172	8	8	2 ICLK			
0008 73ADh	ICU	Interrupt Source Priority Register 173	IPR173	8	8	2 ICLK			
0008 73AEh	ICU	Interrupt Source Priority Register 174	IPR174	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 73B1h	ICU	Interrupt Source Priority Register 177	IPR177	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 73B4h	ICU	Interrupt Source Priority Register 180	IPR180	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 73B7h	ICU	Interrupt Source Priority Register 183	IPR183	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 73B9h	ICU	Interrupt Source Priority Register 185	IPR185	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 73BCh	ICU	Interrupt Source Priority Register 188	IPR188	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 73BEh	ICU	Interrupt Source Priority Register 190	IPR190	8	8	2 ICLK			Not present in versions with 112, 100, 64 or 48 pins.
0008 73C2h	ICU	Interrupt Source Priority Register 194	IPR194	8	8	2 ICLK			
0008 73C6h	ICU	Interrupt Source Priority Register 198	IPR198	8	8	2 ICLK			
0008 73C7h	ICU	Interrupt Source Priority Register 199	IPR199	8	8	2 ICLK			
0008 73C8h	ICU	Interrupt Source Priority Register 200	IPR200	8	8	2 ICLK			
0008 73C9h	ICU	Interrupt Source Priority Register 201	IPR201	8	8	2 ICLK			
0008 73D6h	ICU	Interrupt Source Priority Register 214	IPR214	8	8	2 ICLK			
0008 73D9h	ICU	Interrupt Source Priority Register 217	IPR217	8	8	2 ICLK			
0008 73DCh	ICU	Interrupt Source Priority Register 220	IPR220	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 73DFh	ICU	Interrupt Source Priority Register 223	IPR223	8	8	2 ICLK			Not present in versions with 100, 64 or 48 pins.
0008 73E2h	ICU	Interrupt Source Priority Register 226	IPR226	8	8	2 ICLK			
0008 73E5h	ICU	Interrupt Source Priority Register 229	IPR229	8	8	2 ICLK			
0008 73E8h	ICU	Interrupt Source Priority Register 232	IPR232	8	8	2 ICLK			
0008 73EBh	ICU	Interrupt Source Priority Register 235	IPR235	8	8	2 ICLK			
0008 73EEh	ICU	Interrupt Source Priority Register 238	IPR238	8	8	2 ICLK			
0008 73F1h	ICU	Interrupt Source Priority Register 241	IPR241	8	8	2 ICLK			
0008 73F4h	ICU	Interrupt Source Priority Register 244	IPR244	8	8	2 ICLK			
0008 73F7h	ICU	Interrupt Source Priority Register 247	IPR247	8	8	2 ICLK			
0008 73FAh	ICU	Interrupt Source Priority Register 250	IPR250	8	8	2 ICLK			
0008 7400h	ICU	DMAC Activation Request Select Register 0	DMRSR0	8	8	2 ICLK			
0008 7404h	ICU	DMAC Activation Request Select Register 1	DMRSR1	8	8	2 ICLK			
0008 7408h	ICU	DMAC Activation Request Select Register 2	DMRSR2	8	8	2 ICLK			
0008 740Ch	ICU	DMAC Activation Request Select Register 3	DMRSR3	8	8	2 ICLK			
0008 7500h	ICU	IRQ Control Register 0	IRQCR0	8	8	2 ICLK			
0008 7501h	ICU	IRQ Control Register 1	IRQCR1	8	8	2 ICLK			
0008 7502h	ICU	IRQ Control Register 2	IRQCR2	8	8	2 ICLK			
0008 7503h	ICU	IRQ Control Register 3	IRQCR3	8	8	2 ICLK			
0008 7504h	ICU	IRQ Control Register 4	IRQCR4	8	8	2 ICLK			
0008 7505h	ICU	IRQ Control Register 5	IRQCR5	8	8	2 ICLK			
0008 7506h	ICU	IRQ Control Register 6	IRQCR6	8	8	2 ICLK			Not present in versions with 64 or 48 pins.

Table 4.1 List of I/O Registers (Address Order) (26/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 C174h	MPC	P64 Pin Function Control Register	P64PFS	8	8	2, 3 PCLKB	2 ICLK	MPC	Not present in versions with 64 or 48 pins.
0008 C175h	MPC	P65 Pin Function Control Register	P65PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C178h	MPC	P70 Pin Function Control Register	P70PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C179h	MPC	P71 Pin Function Control Register	P71PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C17Ah	MPC	P72 Pin Function Control Register	P72PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C17Bh	MPC	P73 Pin Function Control Register	P73PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C17Ch	MPC	P74 Pin Function Control Register	P74PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C17Dh	MPC	P75 Pin Function Control Register	P75PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C17Eh	MPC	P76 Pin Function Control Register	P76PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C180h	MPC	P80 Pin Function Control Register	P80PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C181h	MPC	P81 Pin Function Control Register	P81PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C182h	MPC	P82 Pin Function Control Register	P82PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C188h	MPC	P90 Pin Function Control Register	P90PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C189h	MPC	P91 Pin Function Control Register	P91PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 48 pins.
0008 C18Ah	MPC	P92 Pin Function Control Register	P92PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 48 pins.
0008 C18Bh	MPC	P93 Pin Function Control Register	P93PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 48 pins.
0008 C18Ch	MPC	P94 Pin Function Control Register	P94PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 48 pins.
0008 C18Dh	MPC	P95 Pin Function Control Register	P95PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C18Eh	MPC	P96 Pin Function Control Register	P96PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C190h	MPC	PA0 Pin Function Control Register	PA0PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C191h	MPC	PA1 Pin Function Control Register	PA1PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C192h	MPC	PA2 Pin Function Control Register	PA2PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C193h	MPC	PA3 Pin Function Control Register	PA3PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C194h	MPC	PA4 Pin Function Control Register	PA4PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 48 pins.
0008 C195h	MPC	PA5 Pin Function Control Register	PA5PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 48 pins.
0008 C196h	MPC	PA6 Pin Function Control Register	PA6PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64 or 48 pins.
0008 C198h	MPC	PB0 Pin Function Control Register	PB0PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C199h	MPC	PB1 Pin Function Control Register	PB1PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C19Ah	MPC	PB2 Pin Function Control Register	PB2PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C19Bh	MPC	PB3 Pin Function Control Register	PB3PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C19Ch	MPC	PB4 Pin Function Control Register	PB4PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C19Dh	MPC	PB5 Pin Function Control Register	PB5PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C19Eh	MPC	PB6 Pin Function Control Register	PB6PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C19Fh	MPC	PB7 Pin Function Control Register	PB7PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 48 pins.
0008 C1A0h	MPC	PC0 Pin Function Control Register	PC0PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 C1A1h	MPC	PC1 Pin Function Control Register	PC1PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 C1A2h	MPC	PC2 Pin Function Control Register	PC2PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64, or 48 pins.

5. Electrical Characteristics [144-, 120-, 112- and 100-Pin Versions]

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

Conditions: VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V

Item		Symbol	Value	Unit
Power supply voltage		VCC, PLLVCC	–0.3 to +6.5	V
USB power supply voltage		VCC_USB*1	–0.3 to +6.5	V
Analog power supply voltage		AVCC0, AVCC*2	–0.3 to +6.5	V
Reference power supply voltage		VREFH0*2	–0.3 to AVCC0 + 0.3	V
		VREF*2	–0.3 to AVCC0 + 0.3	V
Input voltage (except for ports 4 to 6, C, USB0_DP, and USB0_DM)		V_{in}	–0.3 to VCC + 0.3	V
Input voltage (USB0_DP and USB0_DM)		V_{in}	–0.3 to VCC_USB + 0.3	V
Input voltage (port 4)		V_{in}	–0.3 to AVCC0 + 0.3	V
Input voltage (ports 5, 6, and C)		V_{in}	–0.3 to AVCC + 0.3	V
Analog input voltage (port 4)		V_{AN}	–0.3 to AVCC0 + 0.3	V
Analog input voltage (ports 5, 6, and C)		V_{AN}	–0.3 to AVCC + 0.3	V
Operating temperature	D version product	T_{opr}	–40 to +85	ºC
	G version product	T_{opr}	–40 to +105	ºC
Storage temperature		T_{stg}	–55 to +125	ºC

Caution: Permanent damage to the LSI may result if absolute maximum ratings are exceeded.

Note 1. When the USB is not in use, do not leave the VCC_USB and VSS_USB pins open.
Connect the VCC_USB pin to VCC, and the VSS_USB pin to VSS, respectively.

Note 2. When the A/D converter is not in use, do not leave the AVCC0, VREFH0, VREFL0, AVSS0, AVCC, VREF, and AVSS pins open.
- When the 12-bit A/D converter is not in use
  Connect the AVCC0 pin to AVCC, the VREFH0 pin to VREF, and the AVSS0 and VREFL0 pins to AVSS, respectively.
- When the 10-bit A/D converter is not in use
  Connect the AVCC pin to AVCC0, the VREF pin to VREFH0, and the AVSS pin to AVSS0, respectively.
- When the 12-bit A/D converter and 10-bit A/D converter are not in use
  Connect the AVCC0, VREFH0, AVCC, and VREF pins to VCC, and the AVSS0, VREFL0, and AVSS pins to VSS, respectively.

5.3 AC Characteristics

Table 5.7 Operation Frequency Value

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS =PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item		Symbol	Min.	Typ.	Max.	Unit
Operation frequency	System clock (ICLK)	f	—	—	100	MHz
	Peripheral module clock (PCLK) *1		—	—	50	
	Timer module clock (PCLKA)		—	—	100	
	AD clock (PCLKC)		—	—	100	
	S12AD clock (PCLKD)		—	—	50	
	FlashIF clock (FCLK)		—	—	50	
	External bus clock (BCLK)		—	—	50	
	BCLK pin output		—	—	25	
	USB clock (UCLK)		—	—	48	

Note 1. The PCLK must run at a frequency of at least 24 MHz when the USB is in use.

5.3.5 Bus Timing

Table 5.12 Bus Timing (1)

Condition: VCC = PLLVCC = VCC_USB = AVCC0 = AVCC = 3.0 to 3.6 V,
VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC
$T_a = T_{opr}$
Output load conditions: V_{OH} = VCC x 0.5, V_{OL} = VCC x 0.5, I_{OH} = –1.0 mA, I_{OL} = 1.0 mA, C = 30 pF

Item	Symbol	Min.	Max.	Unit	Test Conditions
Address delay time	t_{AD}	—	30	ns	Figure 5.13 to Figure 5.16
Byte control delay time	t_{BCD}	—	30	ns	
CS# delay time	t_{CSD}	—	30	ns	
RD# delay time	t_{RSD}	—	30	ns	
Read data setup time	t_{RDS}	20	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	—	30	ns	
Write data delay time	t_{WDD}	—	35	ns	
Write data hold time	t_{WDH}	0	—	ns	
WAIT# setup time	t_{WTS}	20	—	ns	Figure 5.17
WAIT# hold time	t_{WTH}	0	—	ns	

Table 5.13 Bus Timing (2)

Condition: VCC = PLLVCC = AVCC0 = AVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V,
VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
$T_a = T_{opr}$
Output load conditions: V_{OH} = VCC x 0.5, V_{OL} = VCC x 0.5, I_{OH} = –1.0 mA, I_{OL} = 1.0 mA, C = 30 pF

Item	Symbol	Min.	Max.	Unit	Test Conditions
Address delay time	t_{AD}	—	15	ns	Figure 5.13 to Figure 5.16
Byte control delay time	t_{BCD}	—	15	ns	
CS# delay time	t_{CSD}	—	15	ns	
RD# delay time	t_{RSD}	—	15	ns	
Read data setup time	t_{RDS}	15	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	—	15	ns	
Write data delay time	t_{WDD}	—	15	ns	
Write data hold time	t_{WDH}	0	—	ns	
WAIT# setup time	t_{WTS}	15	—	ns	Figure 5.17
WAIT# hold time	t_{WTH}	0	—	ns	

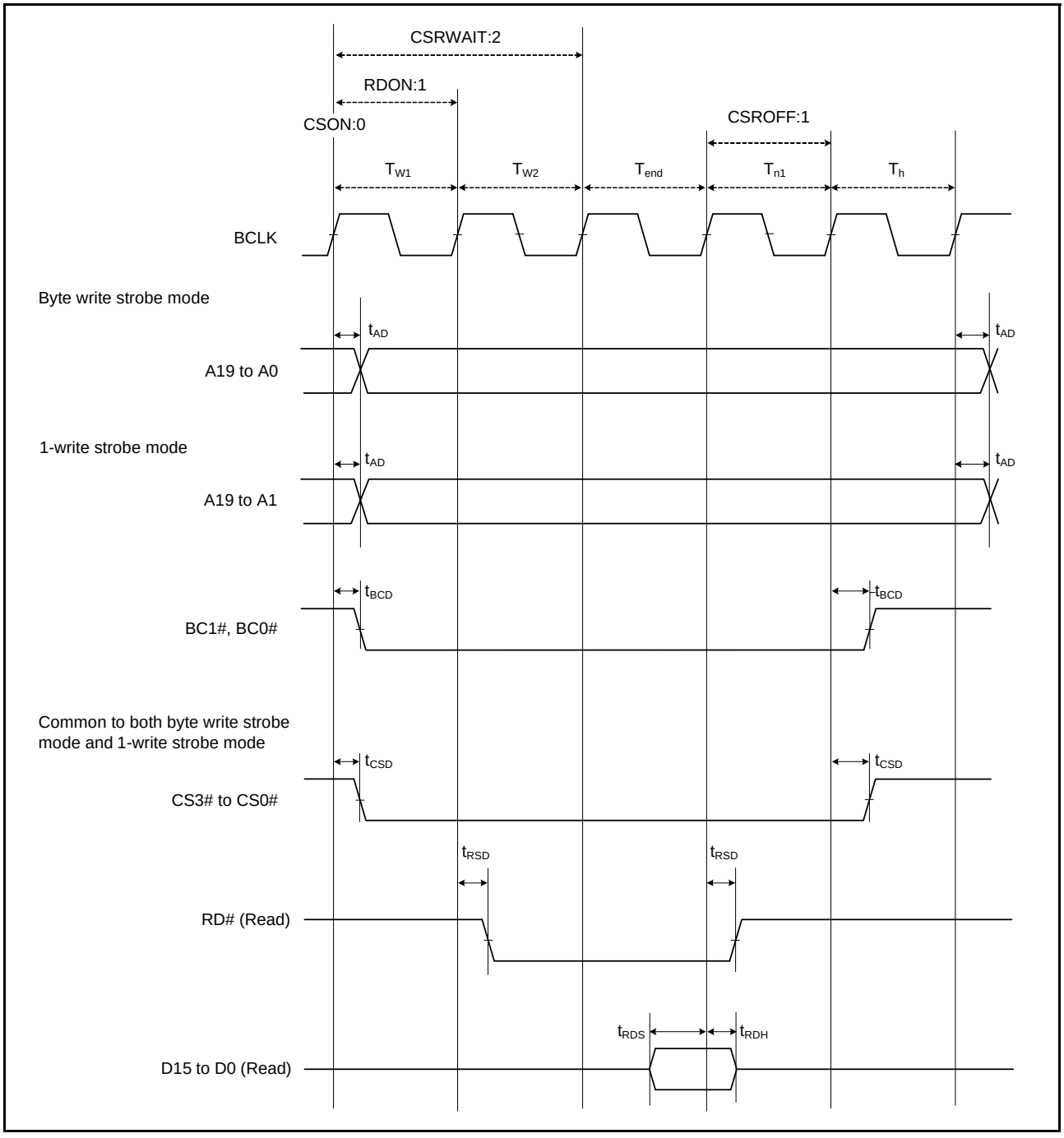


Figure 5.13 External Bus Timing/Normal Read Cycle (Bus Clock Synchronized)

Table 5.16 Timing of On-Chip Peripheral Modules (5)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item		Symbol	Min.*1,*2	Max.	Unit	Test Conditions
RIIC (Standard-mode)	SCL input cycle time	t_{SCL}	$6(12) \times t_{IICcyc} + 1300$	—	ns	Figure 5.36
	SCL input high pulse width	t_{SCLH}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	SCL input low pulse width	t_{SCLL}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	SCL, SDA input rise time	t_{Sr}	—	1000	ns	
	SCL, SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	$1(4) \times t_{IICcyc}$	ns	
	SDA input bus free time	t_{BUF}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	Start condition input hold time	t_{STAH}	$t_{IICcyc} + 300$	—	ns	
	Restart condition input setup time	t_{STAS}	1000	—	ns	
	Stop condition input setup time	t_{STOS}	1000	—	ns	
	Data input setup time	t_{SDAS}	$t_{IICcyc} + 50$	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
RIIC (Fast-mode)	SCL input cycle time	t_{SCL}	$6(12) \times t_{IICcyc} + 600$	—	ns	
	SCL input high pulse width	t_{SCLH}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	SCL input low pulse width	t_{SCLL}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	SCL, SDA input rise time	t_{Sr}	$20 + 0.1C_b$	300	ns	
	SCL, SDA input fall time	t_{Sf}	$20 + 0.1C_b$	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	$1(4) \times t_{IICcyc}$	ns	
	SDA input bus free time	t_{BUF}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	Start condition input hold time	t_{STAH}	$t_{IICcyc} + 300$	—	ns	
	Restart condition input setup time	t_{STAS}	300	—	ns	
	Stop condition input setup time	t_{STOS}	300	—	ns	
	Data input setup time	t_{SDAS}	$t_{IICcyc} + 50$	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note: • t_{IICcyc}: RIIC internal reference clock (IICϕ) cycle

Note 1. The value within parentheses is applicable when the value of the ICMR3.NF[1:0] bits is 11b while the digital filter is enabled by the setting ICFER.NFE = 1.

Note 2. Cb is the total capacitance of the bus lines.

6. Electrical Characteristics [64- and 48-Pin Versions]

6.1 Absolute Maximum Ratings

Table 6.1 Absolute Maximum Ratings

Item		Symbol	Value	Unit
Power supply voltage		VCC	–0.3 to +4.6	V
Input voltage (except for ports for 5 V tolerant*1 and port 4)		Vin	–0.3 to VCC+0.3	V
Input voltage (port 4)		Vin	–0.3 to AVCC0+0.3	V
Input voltage (ports for 5 V tolerant)*1		Vin	–0.3 to +5.8	V
Analog power supply voltage		AVCC0*2	–0.3 to +4.6	V
Reference power supply voltage		VREFH0*2	–0.3 to AVCC0+0.3	V
Analog input voltage (port 4)		V_{AN}	–0.3 to AVCC0+0.3	V
Operating temperature	D version product	Topr	–40 to +85	°C
	G version product	Topr	–40 to +105	°C
Storage temperature		Tstg	–55 to +125	°C

Caution: Permanent damage to the LSI may result if absolute maximum ratings are exceeded.

Note 1. Ports 0, 1, 2, 3, 7, 9, A, B, and D are 5 V tolerant.

Note 2. When the A/D converter is not in use, do not leave the AVCC0, VREFH0, VREFL0, and AVSS0 pins open. Connect the AVCC0 and VREFH0 pins to VCC, and the AVSS0 and VREFL0 pins to VSS, respectively.

Table 6.5 Permissible Power Consumption (G version product only)

Condition: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0
$T_a = T_{opr}$

Item	Symbol	Typ.	Max.	Unit	Test Conditions
Total permissible power consumption*1	Pd	—	150	mW	85°C < Ta ≤ 105°C 64-pin version
	Pd	—	120	mW	85°C < Ta ≤ 105 °C 48-pin version

Note: • Please contact Renesas Electronics sales office for derating of operation under Ta = +85°C to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.
Note 1. The total power consumption of the whole chip including output current.

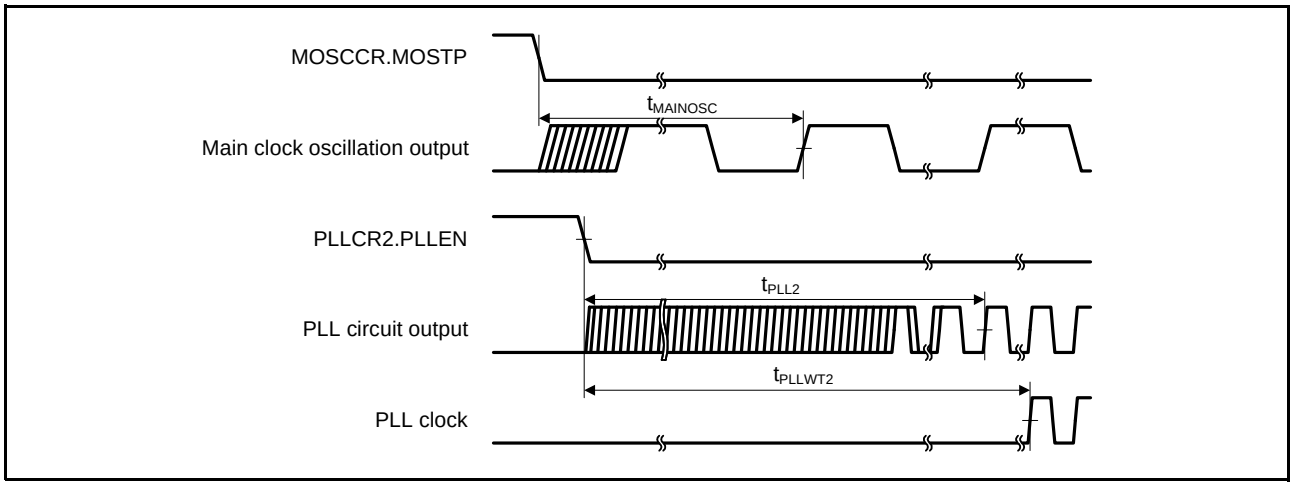


Figure 6.5 PLL Clock Oscillation Start Timing (PLL is Operated before Main Clock Oscillation Has Settled)

6.3.2 Reset Timing

Table 6.8 Reset Timing

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item		Symbol	Min	Typ	Max.	Unit	Test Conditions
RES# pulse width	Power-on	t_{RESWP}	2	—	—	ms	Figure 6.6
	Deep software standby mode	t_{RESWD}	1	—	—	ms	Figure 6.7
	Software standby mode	t_{RESWS}	1	—	—	ms	
	Other than above (except for programming or erasure of the ROM or E2 DataFlash memory or blank checking of the E2 DataFlash memory)	t_{RESW}	200	—	—	µs	
Wait time after RES# cancellation		t_{RESWT}	59	—	60	t_{cyc}	
Internal reset time (independent watchdog timer reset, watchdog timer reset, software reset)		t_{RESW2}	112	—	120	t_{cyc}	

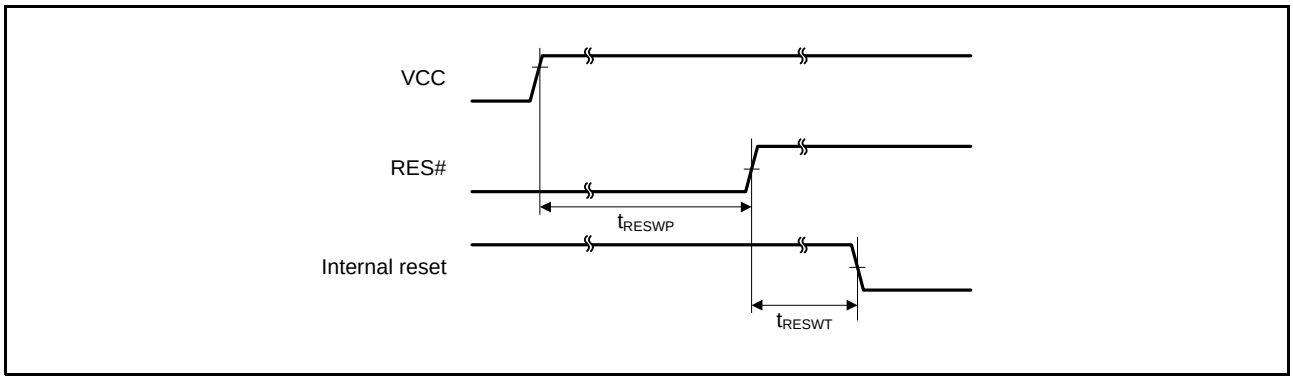


Figure 6.6 Reset Input Timing at Power-On

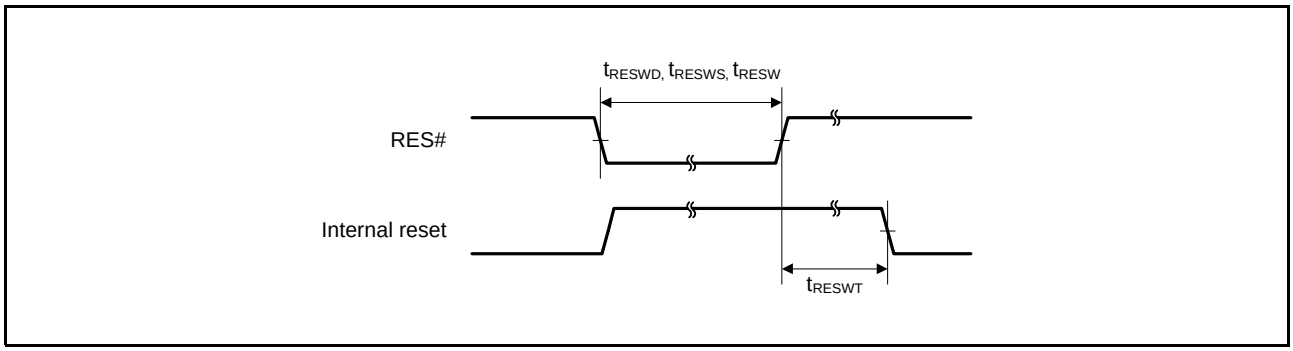


Figure 6.7 Reset Input Timing

6.3.3 Timing of Recovery from Low Power Consumption Modes

Table 6.9 Timing of Recovery from Low Power Consumption Modes

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time after cancellation of software standby mode	Crystal resonator connected to main clock oscillator	Main clock oscillator operating	t_{SBYMC}	10	—	—	ms	Figure 6.8
		Main clock oscillator and PLL circuit operating	t_{SBYPC}	10	—	—	ms	
	External clock input to main clock oscillator	Main clock oscillator operating	t_{SBYEX}	1	—	—	ms	
		Main clock oscillator and PLL circuit operating	t_{SBYPE}	1	—	—	ms	
	Low-speed clock oscillator or IWDT-specific low-speed clock oscillator operating		t_{SBYLO}	—	—	800	µs	
Recovery time after cancellation of deep software standby mode			t_{DSBY}	—	—	1	ms	Figure 6.9
Wait time after cancellation of deep software standby mode			t_{DSBYWT}	45	—	46	t_{cyc}	

Note: • The wait time varies depending on the state in which each oscillator was when the WAIT instruction was executed. The recovery time when multiple oscillators are operating is the same period as that when the oscillator, which takes the longest time for recovery among the operating oscillators, is operating alone.

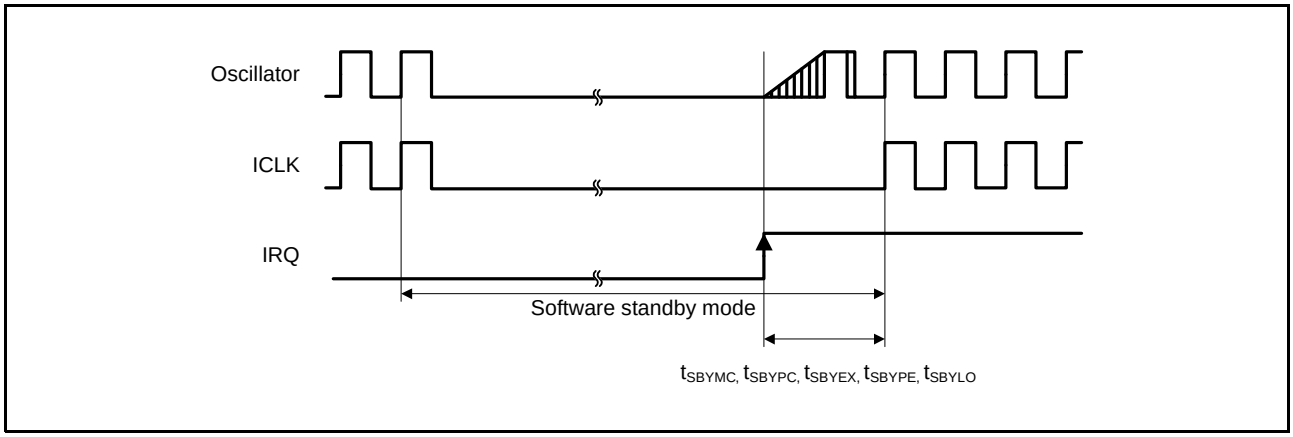


Figure 6.8 Software Standby Mode Cancellation Timing

6.8 E^2 DataFlash Characteristic

Table 6.22 E^2 DataFlash (Flash Memory for Data Storage) Characteristics (1)

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0
Temperature range for the programming/erasure operation: $T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Reprogram/erase cycle*1	N_{DPEC}	100000	—	—	Times	
Data hold time	t_{DDRP}	30*2	—	—	Year	Ta = +85°C

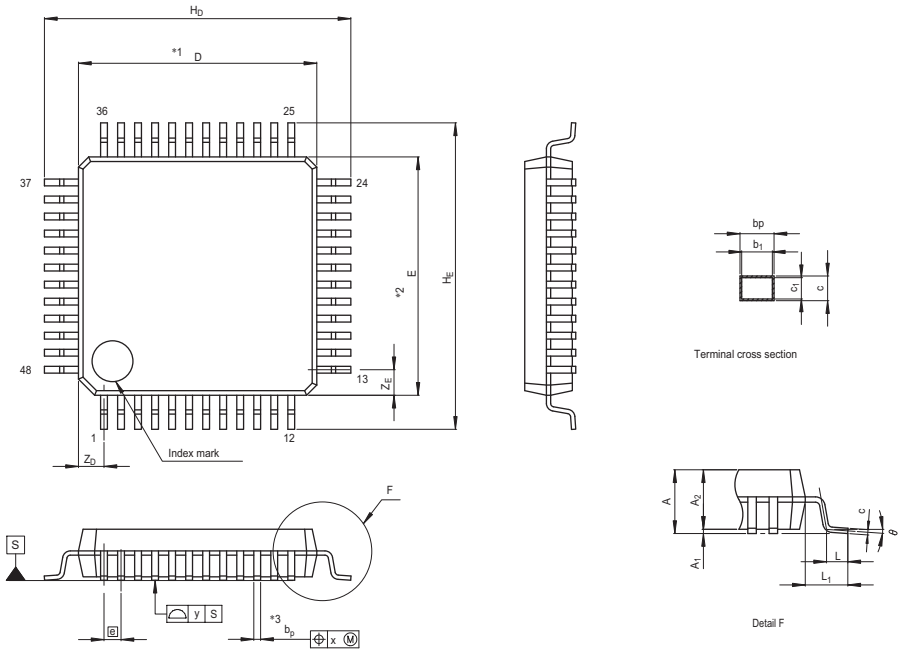
Note 1. Definition of reprogram/erase cycle:
The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 128-byte programming is performed 16 times for different addresses in 2-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).
Note 2. The value is obtained from the reliability test.

Table 6.23 E^2 DataFlash (Flash Memory for Data Storage) Characteristics (2)

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item		Symbol	min	typ	max	Unit	Test Condition
Programming time	2 bytes	t_{DP2}	—	0.25	2	ms	FCLK = 50 MHz
Erasure time	32 bytes	t_{DE32}	—	2	20	ms	FCLK = 50 MHz $N_{DPEC} \leq 100$
	32 bytes	t_{DE32}	—	4	20	ms	FCLK = 50 MHz $N_{DPEC} > 100$
Blank check time	2 bytes	t_{DBC2}	—	—	30	µs	FCLK = 50 MHz
Suspend delay time during programming		t_{DSPD}	—	—	120	µs	Figure 6.31 PCLKB = 50 MHz
First suspend delay time during erasing (in suspend priority mode)		t_{DSESD1}	—	—	120	µs	
Second suspend delay time during erasing (in suspend priority mode)		t_{DSESD2}	—	—	300	µs	
Suspend delay time during erasing (in erasure priority mode)		t_{DSEED}	—	—	300	µs	

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP48-7x7-0.50	PLQP0048KB-A	48P6Q-A	0.2g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A_2	—	1.4	—
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.17	0.22	0.27
b_1	—	0.20	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z_D	—	0.75	—
Z_E	—	0.75	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure F 48-Pin LQFP (PLQP0048KB-A)