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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	69
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 12x10b, 8x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f563tcbdfh-v0

Table 1.1 Outline of Specifications (2/7)

Classification	Module/Function	Description
Clock	Clock generation circuit	• Main clock oscillator, low-speed on-chip oscillator, PLL frequency synthesizer, and dedicated on-chip oscillator for the IWDT • Main-clock oscillation stop detection • Separate frequency-division and multiplication settings for the system clock (ICLK), peripheral module clock (PCLKA), peripheral module clock (PCLKB), AD clock (PCLKC), FlashIF clock (FCLK) and S12AD clock (PCLKD). The CPU and other bus masters run in synchronization with the system clock (ICLK): Up to 100 MHz Multi-function timer pulse unit 3 and general PWM timer run in synchronization with PCLKA: Up to 100 MHz Peripheral modules run in synchronization with the peripheral module clock (PCLKB): Up to 50 MHz Flash IF run in synchronization with the FlashIF clock (FCLK): Up to 50 MHz Devices connected to the external bus run in synchronization with the external bus clock (BCLK): Up to 50 MHz 10-bit A/D converter runs in synchronization with the AD clock (PCLKC): Up to 100 MHz 12-bit A/D converter runs in synchronization with the S12AD clock (PCLKD): Up to 50 MHz
Clock	Clock frequency accuracy measurement circuit (CAC)	The frequency of the following clocks can be measured; the main clock oscillator, PLL circuit, and IWDT-dedicated on-chip oscillator.
Reset		RES# pin reset, power-on reset, voltage-monitoring reset, independent watchdog timer reset, watchdog timer reset, deep software standby reset, and software reset
Voltage detection circuit		When the voltage on VCC passes the voltage detection level (Vdet), an internal reset or internal interrupt is generated.
Low power consumption	Low power consumption facilities	• Module stop function • Four low power consumption modes Sleep mode, all-module clock stop mode, software standby mode, and deep software standby mode
Interrupt	Interrupt controller (ICUb)	• Peripheral function interrupts: Up to 169 sources • External interrupts: Up to 8 (pins IRQ0 to IRQ7) • Software interrupts: One source • Non-maskable interrupts: 6 sources • Sixteen levels specifiable for the order of priority
External bus extension		• The external address space can be divided into four areas (CS0 to CS3), each with independent control of access settings. - Capacity of each area: 1 Mbyte (CS0 to CS3) - A chip-select signal (CS0# to CS3#) can be output for each area. - Each area is specifiable as an 8- or 16-bit bus space - The data arrangement in each area is selectable as little or big endian (only for data). • Bus format: Separate bus, multiplex bus • Wait control • Write buffer facility
DMA	DMA controller (DMACA)	• 4 channels • Three transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Software trigger, external interrupts, and interrupt requests from peripheral functions
	Data transfer controller (DTCa)	• Three transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Software interrupt activation register settings, external interrupts, and interrupt requests from peripheral functions

Table 1.1 Outline of Specifications (4/7)

Classification	Module/Function	Description
Timers	General PWM timer (GPT)	• 16 bits x 8 channels • Counting up or down (saw-wave), counting up and down (triangle-wave) selectable for all channels • Select from among four count clocks (PCLKA/1, PCLKA/4, PCLKA/8, and PCLKA/16) for each channel • 2 input/output pins per channel • 2 output compare/input capture registers per channel • For the 2 output compare/input capture registers of each channel, 4 registers are provided as buffer registers and are capable of operating as comparison registers when buffering is not in use. • In output compare operation, buffer switching can be at peaks or troughs, enabling the generation of laterally asymmetrically PWM waveforms. • Registers for setting up frame intervals on each channel (with capability for generating interrupts on overflow or underflow) • Synchronizable operation of the several counters • Modes of synchronized operation (synchronized, or displaced by desired times for phase shifting) • Generation of dead times in PWM operation • Through combination of three counters, generation of automatic three-phase PWM waveforms incorporating dead times • Starting, clearing, and stopping counters in response to external or internal triggers • Internal trigger sources: Output of the internal comparator detection, software, and compare-match • The main clock can be used as a counter clock for measuring the timing of the edges of signals produced by frequency-dividing the dedicated clock signal for the IWDt (to detect abnormal oscillation). • A PWM delay with an accuracy of up to 1/32 times the period of the system clock (ICLK) can be generated to control the timing with which signals from the two PWM output pins from each of channels 0 to 3 rise and fall.
	Compare match timer (CMT)	• (16 bits x 2 channels) x 2 units • Select from among four internal clock signals (PCLK/8, PCLK/32, PCLK/128, PCLK/512)
	Watchdog timer (WDTA)	• 14 bits x 1 channel • Select from among 6 counter-input clock signals (PCLK/4, PCLK/64, PCLK/128, PCLK/512, PCLK/2048, PCLK/8192)
	Independent watchdog timer (IWDtA)	• 14 bits x 1 channel • Counter-input clock: Dedicated on-chip oscillator • Dedicated clock/1, dedicated clock/16, dedicated clock/32, dedicated clock/64, dedicated clock/128, dedicated clock/256
Communication function	USB 2.0 host/function module (USBa)	• Includes a UDC (USB Device Controller) and transceiver for USB 2.0 • Single port • Compliance with the USB 2.0 specification • Transfer rate: Full speed (12 Mbps) • Self-power mode and bus power mode are selectable • Supports the OTG (On-The-Go) • Incorporates 2 Kbytes of RAM as a transfer buffer
	Serial communications interfaces (SCIC, SCID)	• 5 channels (SCIC: 4 channels + SCID: 1 channel) • SCIC - Serial communications modes: Asynchronous, clock synchronous, and smart-card interface - Multi-processor function - On-chip baud rate generator allows selection of the desired bit rate - Choice of LSB-first or MSB-first transfer - Simple I²C - Simple SPI • SCID (The following functions are added to SCIC) - Supports the serial communications protocol, which contains the start frame and information frame - Supports the LIN format

1.3 Block Diagram

Figure 1.2 shows a block diagram.

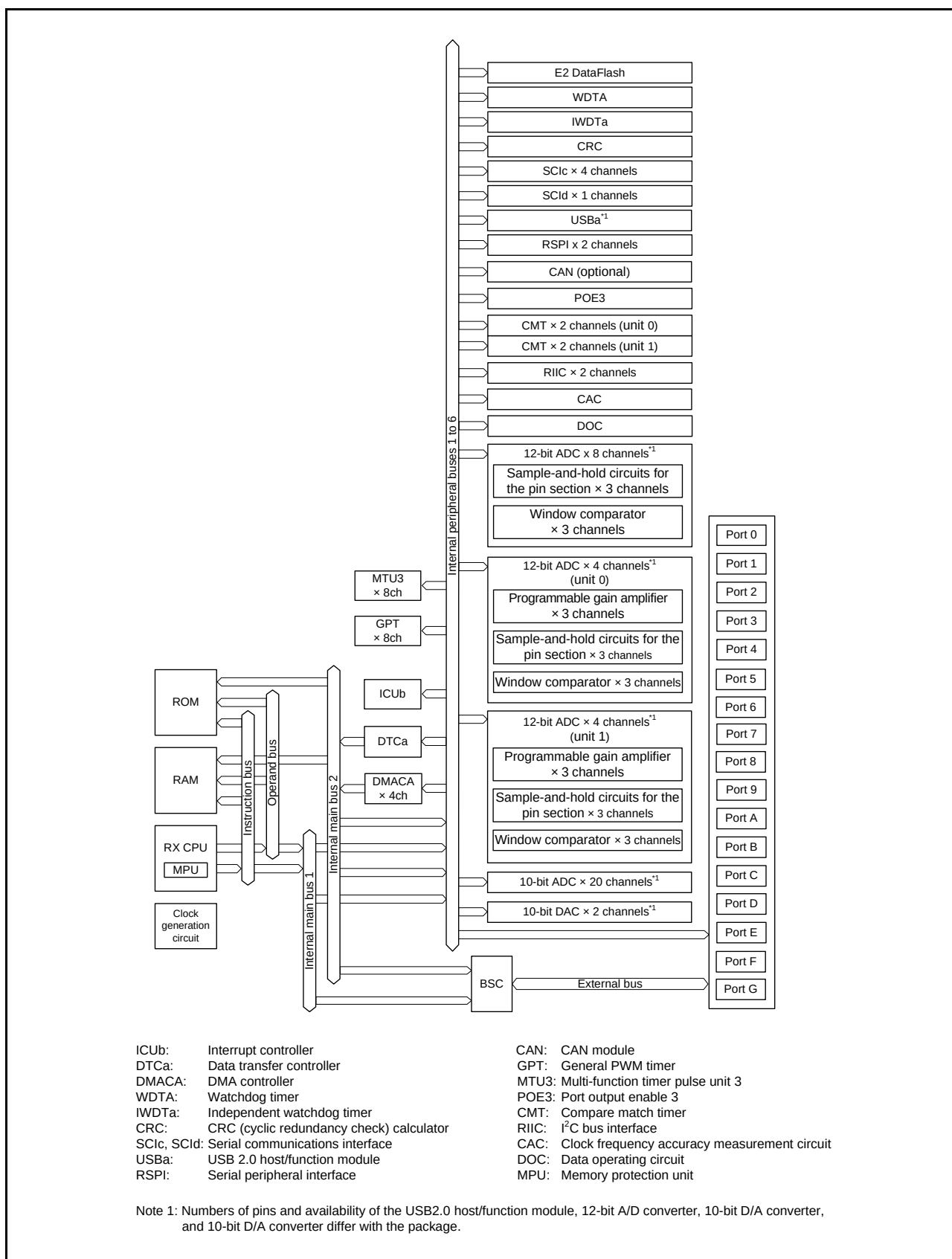


Figure 1.2 Block Diagram

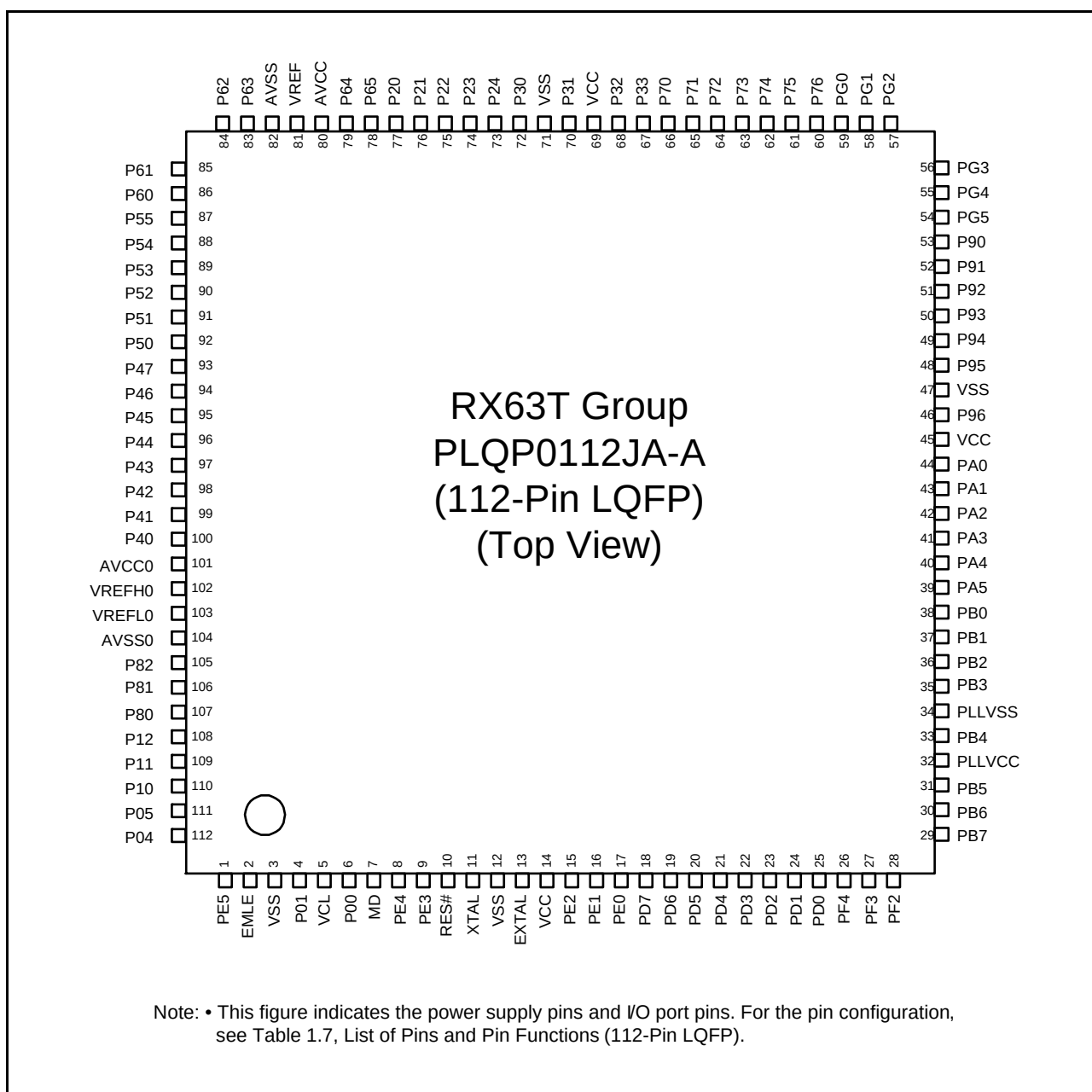


Figure 1.5 Pin Assignment (112-Pin LQFP)

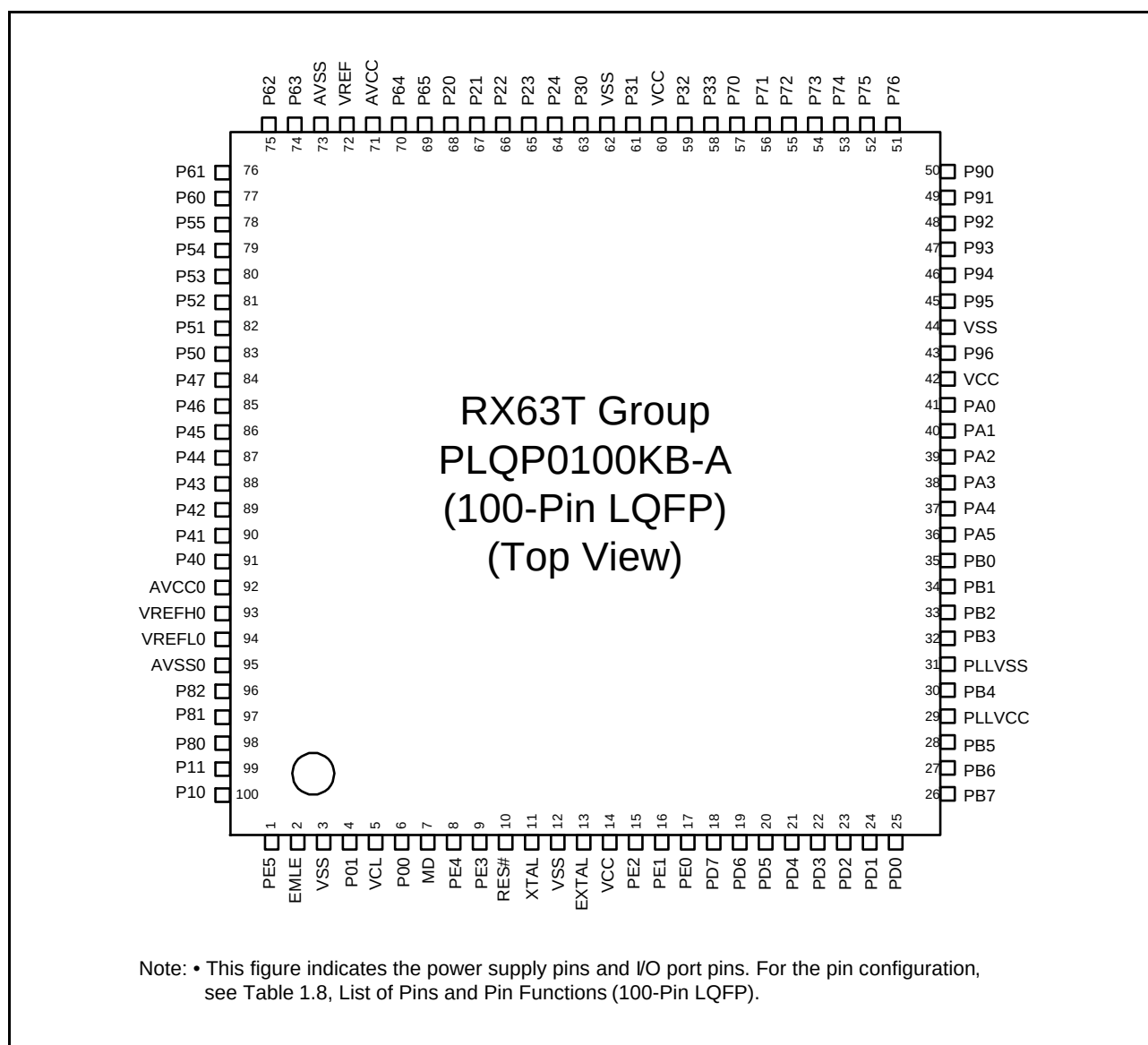


Figure 1.6 Pin Assignment (100-Pin LQFP)

Table 1.9 List of Pins and Pin Functions (64-Pin LQFP) (1/3)

Pin Number 64-Pin LQFP	Power Supply Clock System Control	I/O Port	POE3	Timer (MTU3, GPT, CAC)	Communications		Interrupt	S12ADB
					(SCIc, SCId)	(RSPI, RIIC)		
1	EMLE							
2		P00		GTIOC3A	CTS0# RTS0# SS0#		IRQ2-DS	
3	VCL							
4		P01		GTIOC3B CACREF			IRQ4-DS	
5	MD FINED							
6	RES#							
7	XTAL							
8	VSS							
9	EXTAL							
10	VCC							
11		PE2	POE10#				NMI	
12	TRST#	PD7		GTIOC0A	CTS0# RTS0# SS0#			
13	TMS	PD6		GTIOC0B				
14	TDI	PD5		GTIOC1A	RXD1 SMISO1 SSCL1			
15	TCK FINEC	PD4		GTIOC1B	SCK1			
16	TDO	PD3		GTIOC2A	TXD1 SMOSI1 SSDA1			
17		PB7		GTIOC2B	SCK12			
18		PB6		GTIOC2B	RXD12 SMISO12 SSCL12 RXDX12			
19		PB5	POE11#		TXD12 SMOSI12 SSDA12 TXDX12 SIOX12		IRQ0	
20	VCC							
21		PB4	POE8#	GTETRQ	CTS12# RTS12# SS12#		IRQ3-DS	
22	VSS							
23		PB3		MTIOC0A MTCLKA CACREF	SCK0			
24		PB2		MTIOC0B MTCLKB	TXD0 SMOSI0 SSDA0	SDA		
25		PB1		MTIOC0C	RXD0 SMISO0 SSCL0	SCL		
26		PB0		MTIOC0D		MOSIA		

Table 4.1 List of I/O Registers (Address Order) (9/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 717Fh	ICU	DTC Activation Enable Register 127	DTCER127	8	8	2 ICLK		ICUB	
0008 7180h	ICU	DTC Activation Enable Register 128	DTCER128	8	8	2 ICLK			
0008 7181h	ICU	DTC Activation Enable Register 129	DTCER129	8	8	2 ICLK			
0008 7185h	ICU	DTC Activation Enable Register 133	DTCER133	8	8	2 ICLK			
0008 7186h	ICU	DTC Activation Enable Register 134	DTCER134	8	8	2 ICLK			
0008 7189h	ICU	DTC Activation Enable Register 137	DTCER137	8	8	2 ICLK			
0008 718Ah	ICU	DTC Activation Enable Register 138	DTCER138	8	8	2 ICLK			
0008 718Dh	ICU	DTC Activation Enable Register 141	DTCER141	8	8	2 ICLK			
0008 718Eh	ICU	DTC Activation Enable Register 142	DTCER142	8	8	2 ICLK			
0008 718Fh	ICU	DTC Activation Enable Register 143	DTCER143	8	8	2 ICLK			
0008 7190h	ICU	DTC Activation Enable Register 144	DTCER144	8	8	2 ICLK			
0008 7192h	ICU	DTC Activation Enable Register 146	DTCER146	8	8	2 ICLK			
0008 7193h	ICU	DTC Activation Enable Register 147	DTCER147	8	8	2 ICLK			
0008 7194h	ICU	DTC Activation Enable Register 148	DTCER148	8	8	2 ICLK			
0008 7195h	ICU	DTC Activation Enable Register 149	DTCER149	8	8	2 ICLK			
0008 7196h	ICU	DTC Activation Enable Register 150	DTCER150	8	8	2 ICLK			
0008 7197h	ICU	DTC Activation Enable Register 151	DTCER151	8	8	2 ICLK			
0008 7198h	ICU	DTC Activation Enable Register 152	DTCER152	8	8	2 ICLK			
0008 7199h	ICU	DTC Activation Enable Register 153	DTCER153	8	8	2 ICLK			
0008 719Ah	ICU	DTC Activation Enable Register 154	DTCER154	8	8	2 ICLK			
0008 719Bh	ICU	DTC Activation Enable Register 155	DTCER155	8	8	2 ICLK			
0008 719Ch	ICU	DTC Activation Enable Register 156	DTCER156	8	8	2 ICLK			
0008 719Dh	ICU	DTC Activation Enable Register 157	DTCER157	8	8	2 ICLK			
0008 71A1h	ICU	DTC Activation Enable Register 161	DTCER161	8	8	2 ICLK			
0008 71A2h	ICU	DTC Activation Enable Register 162	DTCER162	8	8	2 ICLK			
0008 71A3h	ICU	DTC Activation Enable Register 163	DTCER163	8	8	2 ICLK			
0008 71A4h	ICU	DTC Activation Enable Register 164	DTCER164	8	8	2 ICLK			
0008 71A5h	ICU	DTC Activation Enable Register 165	DTCER165	8	8	2 ICLK			
0008 71ABh	ICU	DTC Activation Enable Register 171	DTCER171	8	8	2 ICLK			
0008 71ACh	ICU	DTC Activation Enable Register 172	DTCER172	8	8	2 ICLK			
0008 71ADh	ICU	DTC Activation Enable Register 173	DTCER173	8	8	2 ICLK			
0008 71AEh	ICU	DTC Activation Enable Register 174	DTCER174	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 71AFh	ICU	DTC Activation Enable Register 175	DTCER175	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 71B0h	ICU	DTC Activation Enable Register 176	DTCER176	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 71B1h	ICU	DTC Activation Enable Register 177	DTCER177	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 71B2h	ICU	DTC Activation Enable Register 178	DTCER178	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 71B3h	ICU	DTC Activation Enable Register 179	DTCER179	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 71B4h	ICU	DTC Activation Enable Register 180	DTCER180	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 71B5h	ICU	DTC Activation Enable Register 181	DTCER181	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 71B6h	ICU	DTC Activation Enable Register 182	DTCER182	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 71B7h	ICU	DTC Activation Enable Register 183	DTCER183	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 71B8h	ICU	DTC Activation Enable Register 184	DTCER184	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 71B9h	ICU	DTC Activation Enable Register 185	DTCER185	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 71BAh	ICU	DTC Activation Enable Register 186	DTCER186	8	8	2 ICLK			Not present in versions with 64 or 48 pins.

Table 4.1 List of I/O Registers (Address Order) (14/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 7507h	ICU	IRQ Control Register 7	IRQCR7	8	8	2 ICLK		ICUb	Not present in versions with 64 or 48 pins.
0008 7510h	ICU	IRQ Pin Digital Filter Enable Register 0	IRQFLTE0	8	8	2 ICLK			
0008 7514h	ICU	IRQ Pin Digital Filter Setting Register 0	IRQFLTC0	16	16	2 ICLK			
0008 7580h	ICU	Non-Maskable Interrupt Status Register	NMISR	8	8	2 ICLK			
0008 7581h	ICU	Non-Maskable Interrupt Enable Register	NMIER	8	8	2 ICLK			
0008 7582h	ICU	Non-Maskable Interrupt Status Clear Register	NMICLR	8	8	2 ICLK			
0008 7583h	ICU	NMI Pin Interrupt Control Register	NMICR	8	8	2 ICLK			
0008 7590h	ICU	NMI Pin Digital Filter Enable Register	NMIFLTE	8	8	2 ICLK			
0008 7594h	ICU	NMI Pin Digital Filter Setting Register	NMIFLTC	8	8	2 ICLK			
0008 8000h	CMT	Compare Match Timer Start Register 0	CMSTR0	16	16	2, 3 PCLKB	2 ICLK	CMT	
0008 8002h	CMT0	Compare Match Timer Control Register	CMCR	16	16	2, 3 PCLKB	2 ICLK		
0008 8004h	CMT0	Compare Match Timer Counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK		
0008 8006h	CMT0	Compare Match Timer Constant Register	CMCOR	16	16	2, 3 PCLKB	2 ICLK		
0008 8008h	CMT1	Compare Match Timer Control Register	CMCR	16	16	2, 3 PCLKB	2 ICLK		
0008 800Ah	CMT1	Compare Match Timer Counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK		
0008 800Ch	CMT1	Compare Match Timer Constant Register	CMCOR	16	16	2, 3 PCLKB	2 ICLK		
0008 8010h	CMT	Compare Match Timer Start Register 1	CMSTR1	16	16	2, 3 PCLKB	2 ICLK		
0008 8012h	CMT2	Compare Match Timer Control Register	CMCR	16	16	2, 3 PCLKB	2 ICLK		
0008 8014h	CMT2	Compare Match Timer Counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK		
0008 8016h	CMT2	Compare Match Timer Constant Register	CMCOR	16	16	2, 3 PCLKB	2 ICLK		
0008 8018h	CMT3	Compare Match Timer Control Register	CMCR	16	16	2, 3 PCLKB	2 ICLK		
0008 801Ah	CMT3	Compare Match Timer Counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK		
0008 801Ch	CMT3	Compare Match Timer Constant Register	CMCOR	16	16	2, 3 PCLKB	2 ICLK		
0008 8020h	WDT	WDT Refresh Register	WDTRR	8	8	2, 3 PCLKB	2 ICLK	WDTA	
0008 8022h	WDT	WDT Control Register	WDTCR	16	16	2, 3 PCLKB	2 ICLK		
0008 8024h	WDT	WDT Status Register	WDTSR	16	16	2, 3 PCLKB	2 ICLK		
0008 8026h	WDT	WDT Reset Control Register	WDTRCR	8	8	2, 3 PCLKB	2 ICLK		
0008 8030h	IWDT	IWDT Refresh Register	IWDTRR	8	8	2, 3 PCLKB	2 ICLK	IWDTa	
0008 8032h	IWDT	IWDT Control Register	IWDTCR	16	16	2, 3 PCLKB	2 ICLK		
0008 8034h	IWDT	IWDT Status Register	IWDTSR	16	16	2, 3 PCLKB	2 ICLK		
0008 8036h	IWDT	IWDT Reset Control Register	IWDTRCR	8	8	2, 3 PCLKB	2 ICLK		
0008 8038h	IWDT	IWDT Count Stop Control Register	IWDTCSTPR	8	8	2, 3 PCLKB	2 ICLK		
0008 80C0h	DA	D/A Data Register 0	DADR0	16	16	2, 3 PCLKB	2 ICLK	DAa	Not present in versions with 64 or 48 pins.
0008 80C2h	DA	D/A Data Register 1	DADR1	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 80C4h	DA	D/A Control Register	DACR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 80C5h	DA	DADRm Format Select Register	DADPR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 80C6h	DA	D/A A/D Synchronous Start Control Register	DAADSCR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 8280h	CRC	CRC Control Register	CRCCR	8	8	2, 3 PCLKB	2 ICLK	CRC	
0008 8281h	CRC	CRC Data Input Register	CRCDIR	8	8	2, 3 PCLKB	2 ICLK		
0008 8282h	CRC	CRC Data Output Register	CRCDOR	16	16	2, 3 PCLKB	2 ICLK		
0008 8300h	RIIC0	I ² C Bus Control Register 1	ICCR1	8	8	2, 3 PCLKB	2 ICLK	RIIC	
0008 8301h	RIIC0	I ² C Bus Control Register 2	ICCR2	8	8	2, 3 PCLKB	2 ICLK		
0008 8302h	RIIC0	I ² C Bus Mode Register 1	ICMR1	8	8	2, 3 PCLKB	2 ICLK		
0008 8303h	RIIC0	I ² C Bus Mode Register 2	ICMR2	8	8	2, 3 PCLKB	2 ICLK		
0008 8304h	RIIC0	I ² C Bus Mode Register 3	ICMR3	8	8	2, 3 PCLKB	2 ICLK		
0008 8305h	RIIC0	I ² C Bus Function Enable Register	ICFER	8	8	2, 3 PCLKB	2 ICLK		
0008 8306h	RIIC0	I ² C Bus Status Enable Register	ICSER	8	8	2, 3 PCLKB	2 ICLK		
0008 8307h	RIIC0	I ² C Bus Interrupt Enable Register	ICIER	8	8	2, 3 PCLKB	2 ICLK		

Table 4.1 List of I/O Registers (Address Order) (27/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 C1A3h	MPC	PC3 Pin Function Control Register	PC3PFS	8	8	2, 3 PCLKB	2 ICLK	MPC	Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 C1A4h	MPC	PC4 Pin Function Control Register	PC4PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 C1A5h	MPC	PC5 Pin Function Control Register	PC5PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 C1A8h	MPC	PD0 Pin Function Control Register	PD0PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C1A9h	MPC	PD1 Pin Function Control Register	PD1PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C1AAh	MPC	PD2 Pin Function Control Register	PD2PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C1ABh	MPC	PD3 Pin Function Control Register	PD3PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C1ACh	MPC	PD4 Pin Function Control Register	PD4PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C1ADh	MPC	PD5 Pin Function Control Register	PD5PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C1AEh	MPC	PD6 Pin Function Control Register	PD6PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C1AFh	MPC	PD7 Pin Function Control Register	PD7PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C1B0h	MPC	PE0 Pin Function Control Register	PE0PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C1B1h	MPC	PE1 Pin Function Control Register	PE1PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C1B2h	MPC	PE2 Pin Function Control Register	PE2PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C1B3h	MPC	PE3 Pin Function Control Register	PE3PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C1B4h	MPC	PE4 Pin Function Control Register	PE4PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C1B5h	MPC	PE5 Pin Function Control Register	PE5PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C1BAh	MPC	PF2 Pin Function Control Register	PF2PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 100, 64, or 48 pins.
0008 C1B8h	MPC	PF3 Pin Function Control Register	PF3PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 100, 64, or 48 pins.
0008 C1C0h	MPC	PG0 Pin Function Control Register	PG0PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 100, 64, or 48 pins.
0008 C1C1h	MPC	PG1 Pin Function Control Register	PG1PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 100, 64, or 48 pins.
0008 C1C2h	MPC	PG2 Pin Function Control Register	PG2PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 100, 64, or 48 pins.
0008 C1C3h	MPC	PG3 Pin Function Control Register	PG3PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 100, 64, or 48 pins.
0008 C1C4h	MPC	PG4 Pin Function Control Register	PG4PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 100, 64, or 48 pins.
0008 C1C5h	MPC	PG5 Pin Function Control Register	PG5PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 100, 64, or 48 pins.
0008 C1C6h	MPC	PG6 Pin Function Control Register	PG6PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
0008 C1D0h	MPC	USB0_DPUPE Pin Function Control Register	UDPUPEPFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
0008 C280h	SYSTEM	Deep Standby Control Register	DPSBYCR	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption	
0008 C282h	SYSTEM	Deep Standby Interrupt Enable Register 0	DPSIER0	8	8	4, 5 PCLKB	2, 3 ICLK		
0008 C284h	SYSTEM	Deep Standby Interrupt Enable Register 2	DPSIER2	8	8	4, 5 PCLKB	2, 3 ICLK		
0008 C286h	SYSTEM	Deep Standby Interrupt Flag Register 0	DPSIFR0	8	8	4, 5 PCLKB	2, 3 ICLK		
0008 C288h	SYSTEM	Deep Standby Interrupt Flag Register 2	DPSIFR2	8	8	4, 5 PCLKB	2, 3 ICLK		
0008 C28Ah	SYSTEM	Deep Standby Interrupt Edge Register 0	DPSIEGR0	8	8	4, 5 PCLKB	2, 3 ICLK		
0008 C28Ch	SYSTEM	Deep Standby Interrupt Edge Register 2	DPSIEGR2	8	8	4, 5 PCLKB	2, 3 ICLK		
0008 C290h	SYSTEM	Reset Status Register 0	RSTSR0	8	8	4, 5 PCLKB	2, 3 ICLK	Resets	
0008 C291h	SYSTEM	Reset Status Register 1	RSTSR1	8	8	4, 5 PCLKB	2, 3 ICLK		

Table 4.1 List of I/O Registers (Address Order) (29/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0009 1840h	CAN1	Control Register	CTLR	16	8, 16	2, 3 PCLKB	2 ICLK	CAN	Not present in versions with 64 or 48 pins.
0009 1842h	CAN1	Status Register	STR	16	8, 16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0009 1844h	CAN1	Bit Configuration Register	BCR	32	8, 16, 32	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0009 1848h	CAN1	Receive FIFO Control Register	RFCR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0009 1849h	CAN1	Receive FIFO Pointer Control Register	RFPCR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0009 184Ah	CAN1	Transmit FIFO Control Register	TFCR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0009 184Bh	CAN1	Transmit FIFO Pointer Control Register	TFPCR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0009 184Ch	CAN1	Error Interrupt Enable Register	EIER	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0009 184Dh	CAN1	Error Interrupt Factor Judge Register	EIFR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0009 184Eh	CAN1	Receive Error Count Register	RECR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0009 184Fh	CAN1	Transmit Error Count Register	TECR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0009 1850h	CAN1	Error Code Store Register	ECSR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0009 1851h	CAN1	Channel Search Support Register	CSSR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0009 1852h	CAN1	Mailbox Search Status Register	MSSR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0009 1853h	CAN1	Mailbox Search Mode Register	MSMR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0009 1854h	CAN1	Time Stamp Register	TSR	16	8, 16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0009 1856h	CAN1	Acceptance Filter Support Register	AFSR	16	8, 16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0009 1858h	CAN1	Test Control Register	TCR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
000A 0000h	USB0	System Configuration Control Register	SYSCFG	16	16	3, 4 PCLKB	2, 3 ICLK	USBa	Not present in versions with 112, 100, 64, or 48 pins.
000A 0004h	USB0	System Configuration Status Register 0	SYSSTS0	16	16	9 PCLKB or more			Not present in versions with 112, 100, 64, or 48 pins.
000A 0008h	USB0	Device State Control Register 0	DVSTCTR0	16	16	9 PCLKB or more			Not present in versions with 112, 100, 64, or 48 pins.
000A 0014h	USB0	CFIFO Port Register	CFIFO	16	8, 16	3, 4 PCLKB	2, 3 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
000A 0018h	USB0	D0FIFO Port Register	D0FIFO	16	8, 16	3, 4 PCLKB	2, 3 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
000A 001Ch	USB0	D1FIFO Port Register	D1FIFO	16	8, 16	3, 4 PCLKB	2, 3 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
000A 0020h	USB0	CFIFO Port Select Register	CFIFOSEL	16	16	3, 4 PCLKB	2, 3 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
000A 0022h	USB0	CFIFO Port Control Register	CFIFOCTR	16	16	3, 4 PCLKB	2, 3 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
000A 0028h	USB0	D0FIFO Port Select Register	D0FIFOSEL	16	16	3, 4 PCLKB	2, 3 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
000A 002Ah	USB0	D0FIFO Port Control Register	D0FIFOCTR	16	16	3, 4 PCLKB	2, 3 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
000A 002Ch	USB0	D1FIFO Port Select Register	D1FIFOSEL	16	16	3, 4 PCLKB	2, 3 ICLK		Not present in versions with 112, 100, 64, or 48 pins.

Note 4. This is calculated from the formula below, where n is the number of cycles set by the PLLWTCR.PSTS[4:0] bits.

$$t_{PLLWT1} = t_{PLL1} + \frac{n + 131072}{f_{PLL}}$$

$$t_{PLLWT2} = t_{PLL2} + \frac{n + 131072}{f_{PLL}} = t_{MAINOSC} + t_{PLL1} + \frac{n + 131072}{f_{PLL}}$$

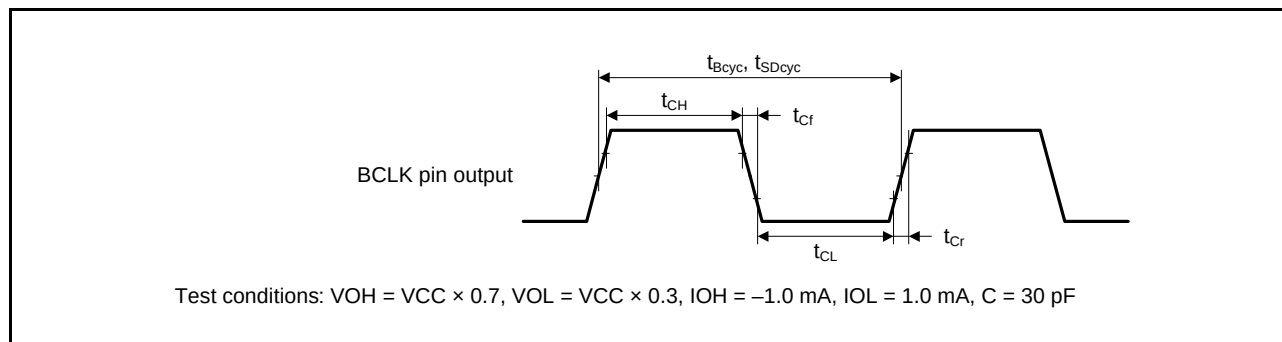


Figure 5.3 BCLK Pin Output Timing

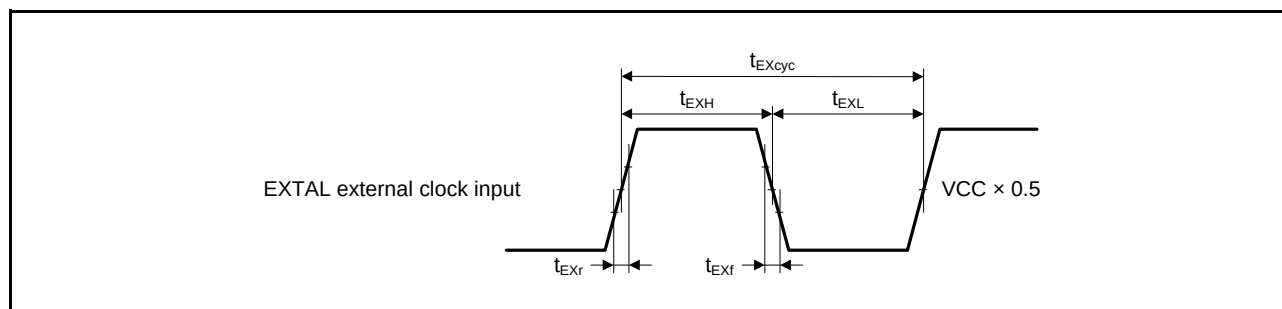


Figure 5.4 EXTAL External Clock Input Timing

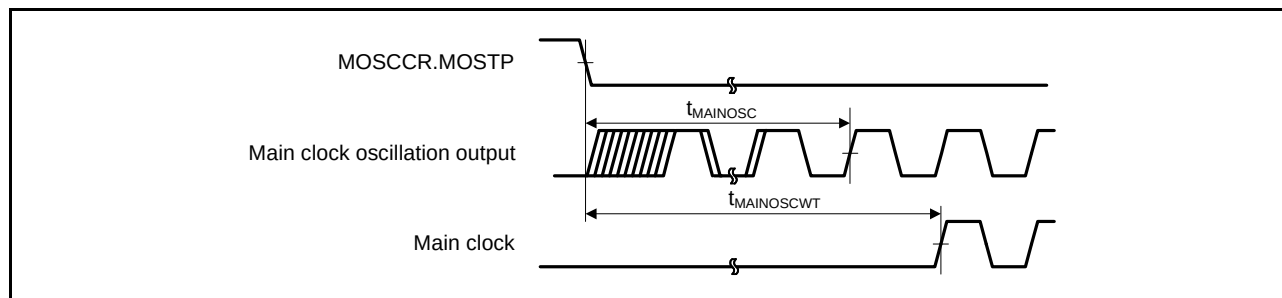


Figure 5.5 Main Clock Oscillation Start Timing

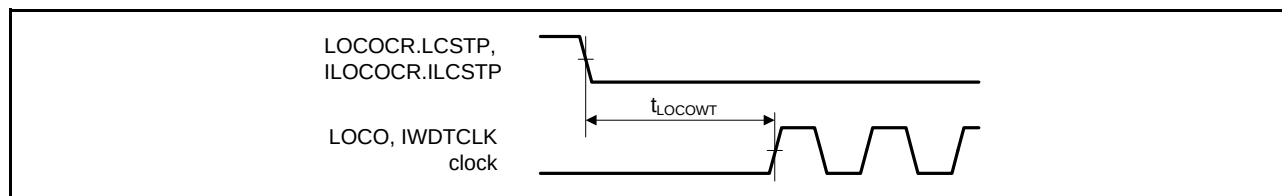


Figure 5.6 LOCO, IWDTCCLK Clock Oscillation Start Timing

Table 5.15 Bus Timing (Multiplexed Bus) (4)Condition: $V_{CC} = PLLVCC = AVCC0 = AVCC = VREF = 4.0$ to 5.5 V, $V_{CC_USB} = 3.0$ to 3.6 V $VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0$ V, $VREFH0 = 4.0$ V to $AVCC0$ $T_a = T_{opr}$ Output load conditions: $V_{OH} = V_{CC} \times 0.5$, $V_{OL} = V_{CC} \times 0.5$, $I_{OH} = -1.0$ mA, $I_{OL} = 1.0$ mA, $C = 30$ pF

Item	Symbol	Min.	Max.	Unit	Test Conditions
Address delay time	t_{AD}	—	15	ns	Figure 5.18, Figure 5.19
Byte control delay time	t_{BCD}	—	15	ns	
CS# delay time	t_{CSD}	—	15	ns	
RD# delay time	t_{RSD}	—	15	ns	
ALE delay time	t_{ALED}	—	15	ns	
Read data setup time	t_{RDS}	15	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	—	15	ns	
Write data delay time	t_{WDD}	—	15	ns	
Write data hold time	t_{WDH}	0	—	ns	
WAIT# setup time	t_{WTS}	15	—	ns	Figure 5.17
WAIT# hold time	t_{WTH}	0.0	—	ns	

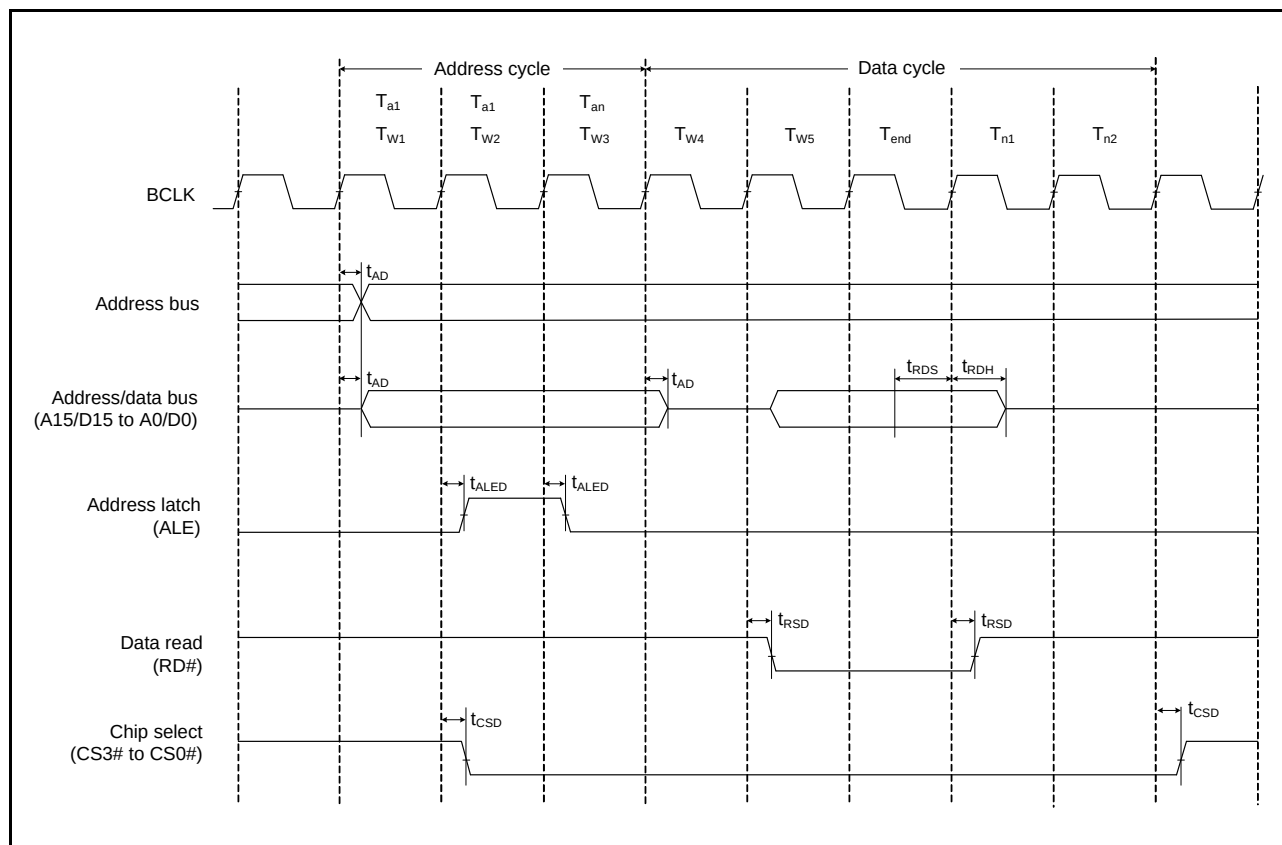
**Figure 5.18 Example of External Bus Timing/Read Access Operation (Multiplexed)**

Table 5.20 10-Bit A/D Conversion Characteristics (2)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: $V_{CC} = PLLVCC = VCC_USB = 2.7$ to 3.6 V, $VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0$ V
 $AVCC0 = AVCC = VREF = 3.0$ to 3.6 V, $VREFH0 = 3.0$ V to $AVCC0$

Condition 2: $V_{CC} = PLLVCC = VCC_USB = 2.7$ to 3.6 V, $VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0$ V
 $AVCC0 = AVCC = VREF = 4.0$ to 5.5 V, $VREFH0 = 4.0$ V to $AVCC0$

Condition 3: $V_{CC} = PLLVCC = 4.0$ to 5.5 V, $VCC_USB = 3.0$ to 3.6 V, $VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0$ V
 $AVCC0 = AVCC = VREF = 4.0$ to 5.5 V, $VREFH0 = 4.0$ V to $AVCC0$

$T_a = T_{opr}$ is common to conditions 1 to 3.

Item			Min.	Typ.	Max.	Unit	Test Conditions
Resolution			10	10	10	Bit	
Conversion time*1 (Operation at ADCLK = 50 MHz)	Without 0.1-μF external capacitor Permissible signal source impedance (max.) = 1 kΩ	AN0 to AN7	0.8	—	—	μs	Sampling in 15 states
		Other channels	1.0	—	—	μs	Sampling in 25 states
Analog input capacitance			—	—	6	pF	
Integral nonlinearity error			—	—	±2.0	LSB	
Offset error			—	—	±2.0	LSB	
Full-scale error			—	—	±3.0	LSB	
Quantization error			—	±0.5	—	LSB	
Absolute accuracy			—	—	±4.0	LSB	

Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

6.2 DC Characteristics

Table 6.2 DC Characteristics (1)

Conditions: $V_{CC} = 2.7$ to 3.6 V, $V_{SS} = AVSS0 = VREFL0 = 0$ V,
 $AVCC0 = 3.0$ to 3.6 V, $VREFH0 = 3.0$ V to $AVCC0$,
 $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	IRQ input pin	V_{IH}	$V_{CC} \times 0.8$	—	$V_{CC} + 0.3$	V
	MTU3 input pin	V_{IL}	-0.3	—	$V_{CC} \times 0.2$	
	POE3 input pin	ΔV_T	$V_{CC} \times 0.06$	—	—	
	SCI input pin					
	A/D trigger input pin					
	GPT input pin					
	RES#, NMI					
	RIIC input pin (IICBus operating)	V_{IH}	$V_{CC} \times 0.7$	—	5.8	
		V_{IL}	-0.3	—	$V_{CC} \times 0.3$	
		ΔV_T	$V_{CC} \times 0.05$	—	—	
	Port 4 (also used as an analog port)	V_{IH}	$AVCC0 \times 0.8$	—	$AVCC0 + 0.3$	
		V_{IL}	-0.3	—	$AVCC0 \times 0.2$	
	Ports for 5 V tolerant*1	V_{IH}	$V_{CC} \times 0.8$	—	5.8	
		V_{IL}	-0.3	—	$V_{CC} \times 0.2$	
Input high voltage (except for Schmitt trigger input pin)	MD pin, EMLE	V_{IH}	$V_{CC} \times 0.9$	—	$V_{CC} + 0.3$	V
	EXTAL, TCK, RSPI input pin		$V_{CC} \times 0.8$	—	$V_{CC} + 0.3$	
	RIIC input pin (SMBus operating)		2.1	—	$V_{CC} + 0.3$	
Input low voltage (except for Schmitt trigger input pin)	MD pin, EMLE	V_{IL}	-0.3	—	$V_{CC} \times 0.1$	
	EXTAL, TCK, RSPI input pin		-0.3	—	$V_{CC} \times 0.2$	
	RIIC input pin (SMBus operating)		-0.3	—	0.8	
Output high voltage	All output pins	V_{OH}	$V_{CC} - 0.5$	—	—	$I_{OH} = -1$ mA
Output low voltage	All output pins (except for RIIC pins)	V_{OL}	—	—	0.5	$I_{OL} = 1.0$ mA
			—	—	0.4	$I_{OL} = 3$ mA
	RIIC pins		—	—	0.6	$I_{OL} = 6$ mA
Input leakage current	RES#, MD pin, EMLE, Ports 4 and PE2	$ I_{in} $	—	—	1.0	μA , $V_{in} = 0V$, $V_{in} = V_{CC}$
Three-state leakage current (off state)	Ports for 5V tolerant	$ I_{TSI} $	—	—	1.0	μA , $V_{in} = 0V$, $V_{in} = 5.5$ V
			—	—	5.0	
Input capacitance	All input pins (except for ports PB1 and PB2)	C_{in}	—	—	15	pF , $V_{in} = 0V$, $f = 1$ MHz, $T_a = 25^\circ C$
	Ports PB1 and PB2		—	—	30	

Note 1. Ports 0, 1, 2, 3, 7, 9, A, B, and D are 5 V tolerant.

Table 6.13 Timing of On-Chip Peripheral Modules (3)

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
 AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
 Ta = T_{opr}

Item		Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI	SCK clock cycle output (master)	t _{SPcyc}	4	65536	t _{Pcyc}	Figure 6.20
	SCK clock cycle input (slave)		8	65536		
	SCK clock high pulse width	t _{SPCKWH}	0.4	0.6	t _{SPcyc}	
	SCK clock low pulse width	t _{SPCKWL}	0.4	0.6	t _{SPcyc}	
	SCK clock rise/fall time	t _{SPCKR} , t _{SPCKF}	—	20	ns	
	Data input setup time	t _{SU}	40	—	ns	Figure 6.21 to Figure 6.24
	Data input hold time	t _H	40	—	ns	
	SS input setup time	t _{LEAD}	6	—	t _{Pcyc}	
	SS input hold time	t _{LAG}	6	—	t _{Pcyc}	
	Data output delay time	t _{OD}	—	40	ns	
	Data output hold time	t _{OH}	−10	—	ns	
	Data rise/fall time	t _{DR} , t _{DF}	—	20	ns	
	SS input rise/fall time	t _{SSLr} , t _{SSLf}	—	20	ns	
	Slave access time	t _{SA}	—	5	t _{Pcyc}	Figure 6.23 and Figure 6.24
	Slave output release time	t _{REL}	—	5	t _{Pcyc}	

Note 1. t_{Pcyc}: PCLK cycle

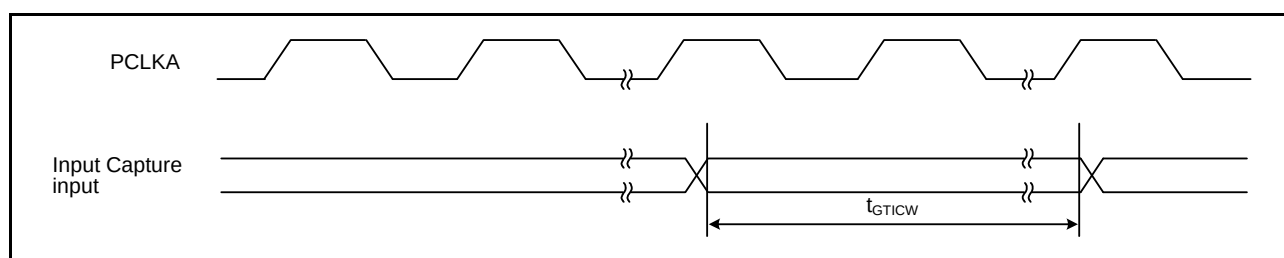


Figure 6.15 GPT Input/Output Timing

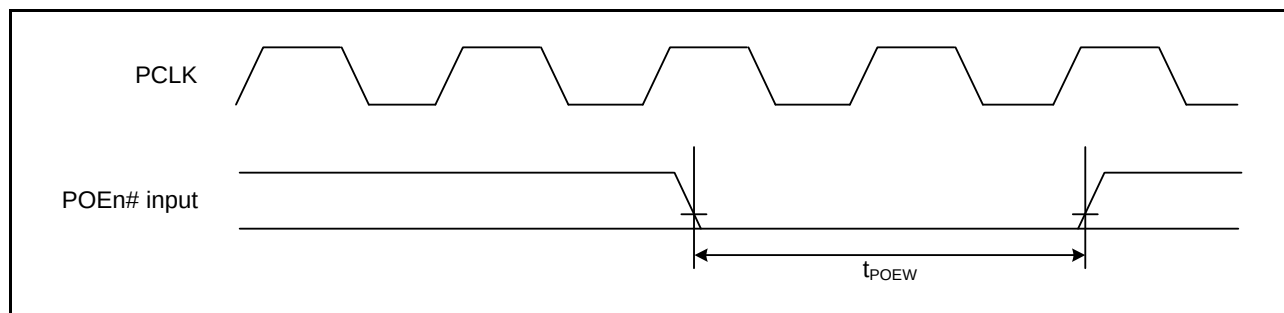


Figure 6.16 POE3# Input Timing

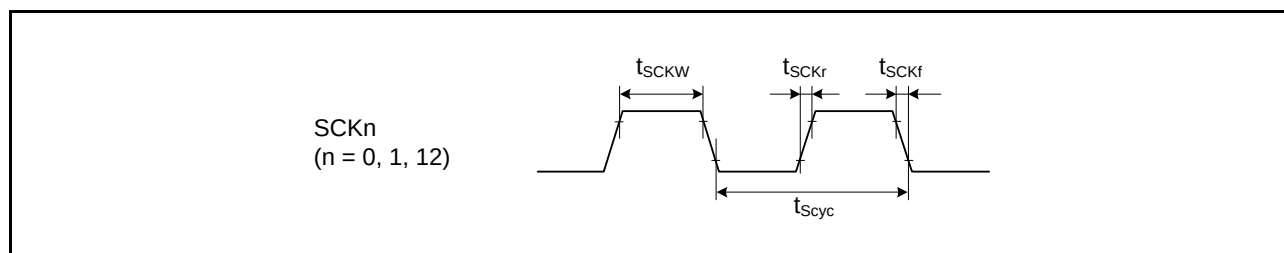


Figure 6.17 SCK Clock Input Timing

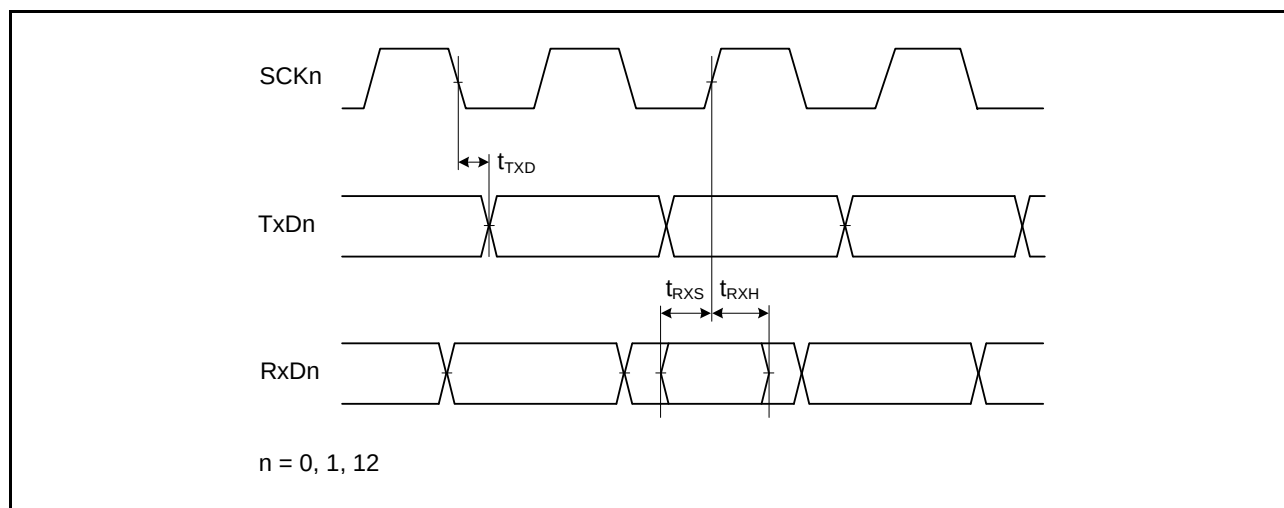
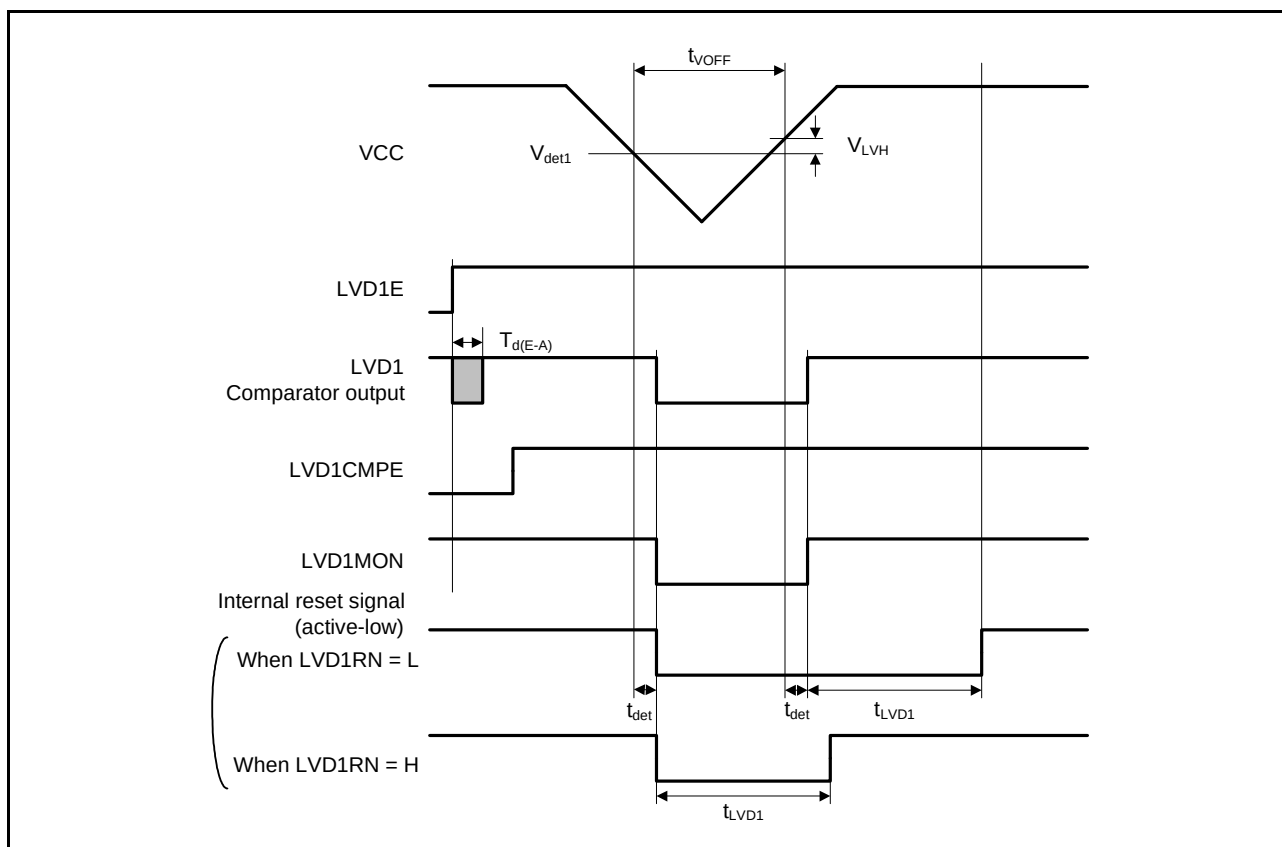
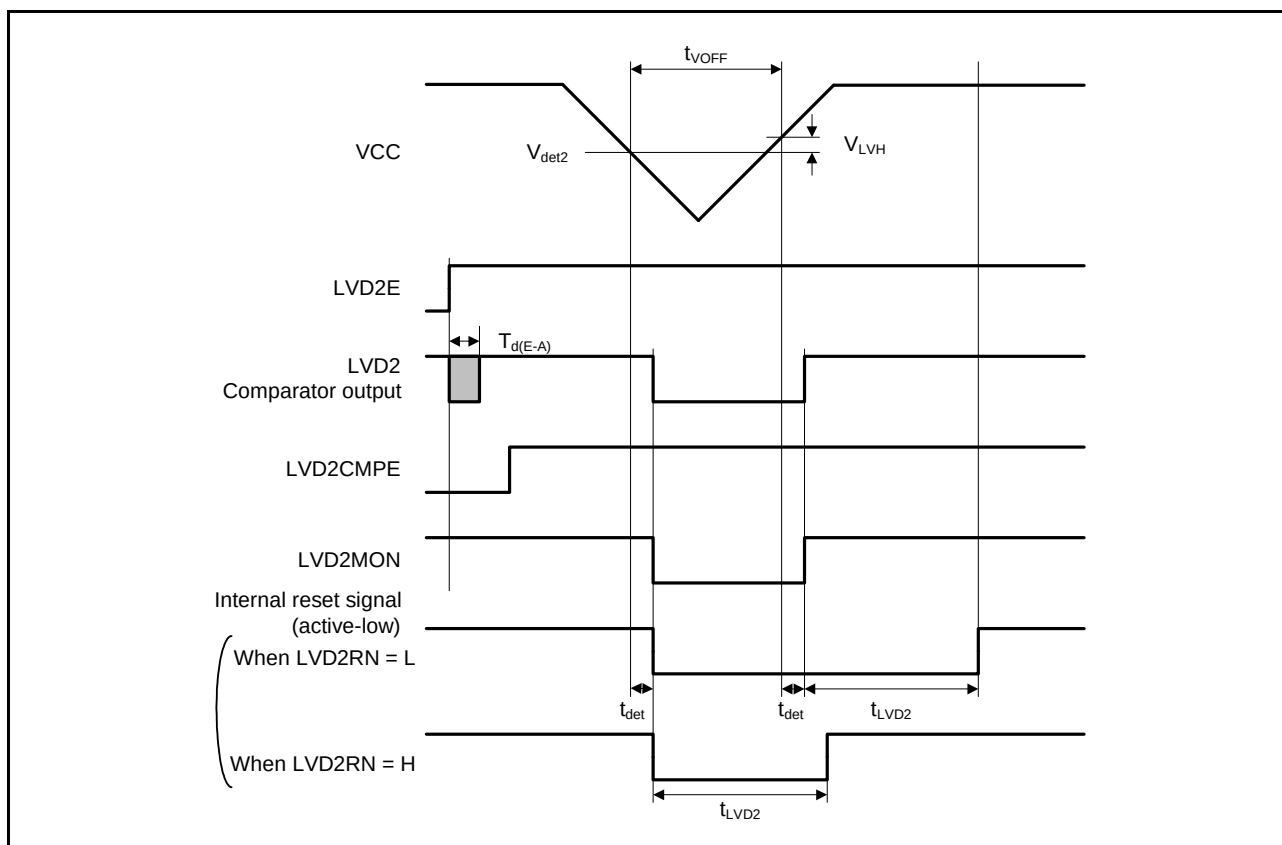


Figure 6.18 SCI Input/Output Timing: Clock Synchronous Mode

Figure 6.28 Voltage Detection Circuit Timing (V_{det1})Figure 6.29 Voltage Detection Circuit Timing (V_{det2})

6.6 Oscillation Stop Detection Circuit Characteristics

Table 6.19 Oscillation Stop Detection Circuit Characteristics

Conditions: $V_{CC} = 2.7$ to 3.6 V, $V_{SS} = AVSS0 = VREFL0 = 0$ V, $AVCC0 = 3.0$ to 3.6 V,
 $VREFH0 = 3.0$ V to $AVCC0$, $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection time	t_{dr}	—	—	1.0	ms	Figure 6.30

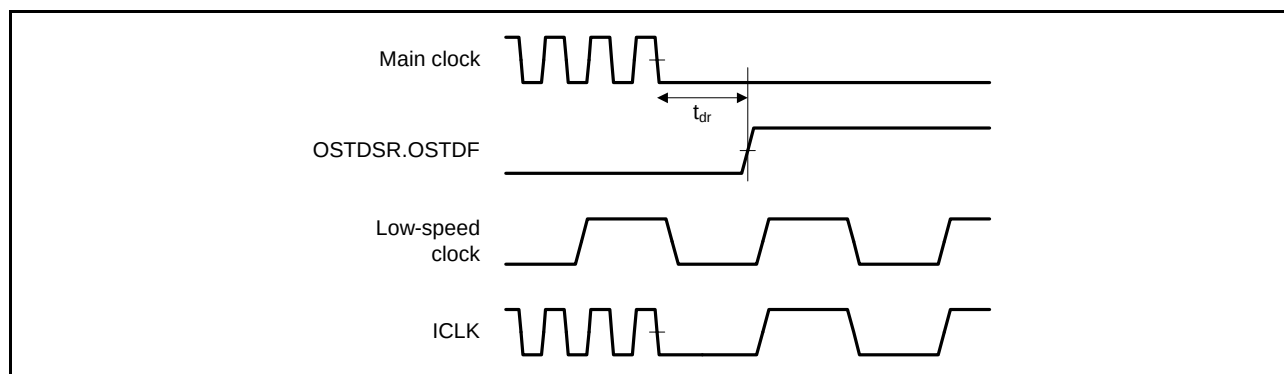


Figure 6.30 Oscillation Stop Detection Timing

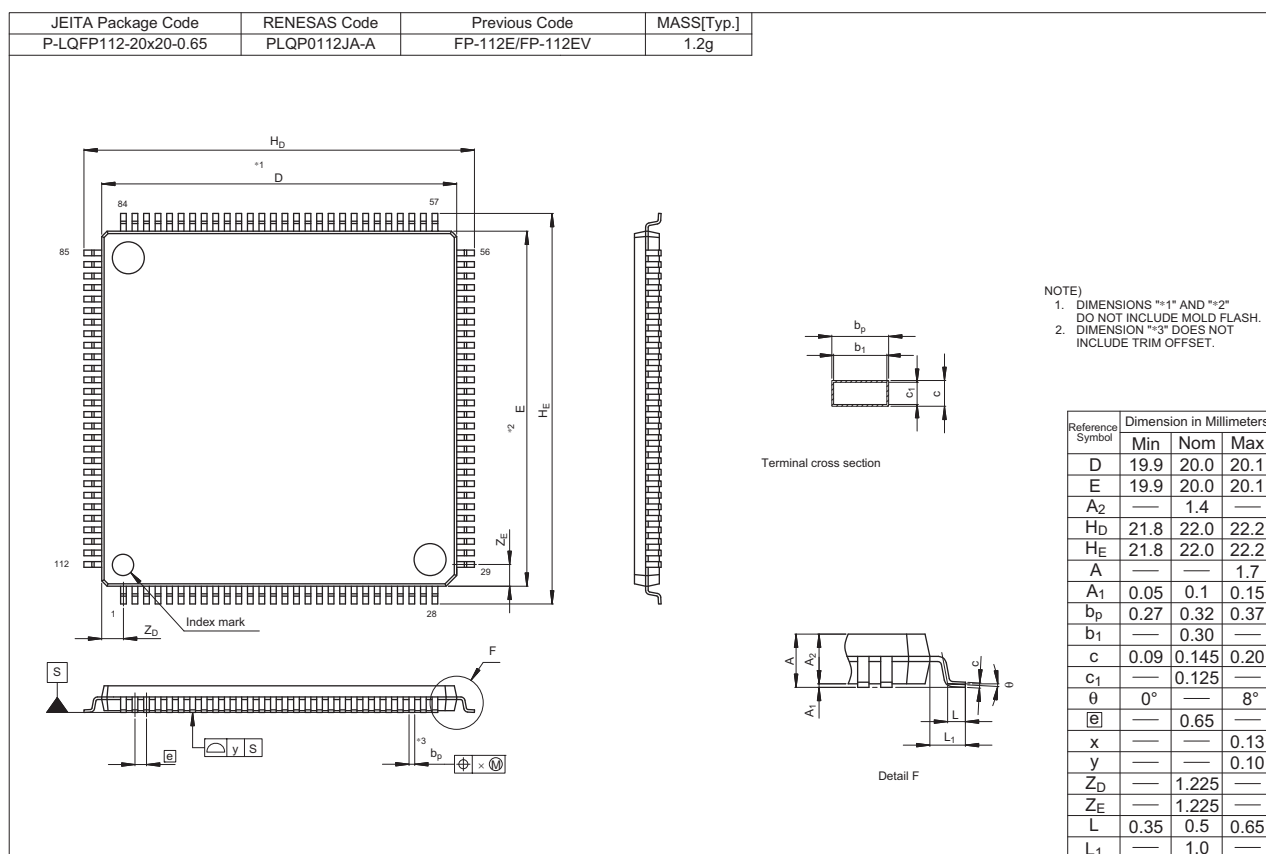


Figure C 112-Pin LQFP (PLQP0112JA-A)

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