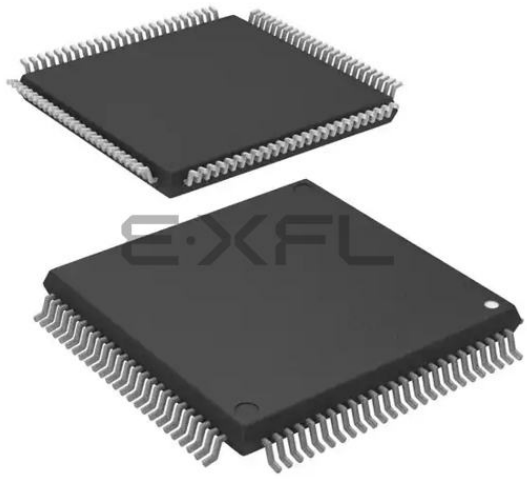
Renesas Electronics America Inc - R5F563TCBDFP#V0 Datasheet



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Applications of "Embedded - Microcontrollers"

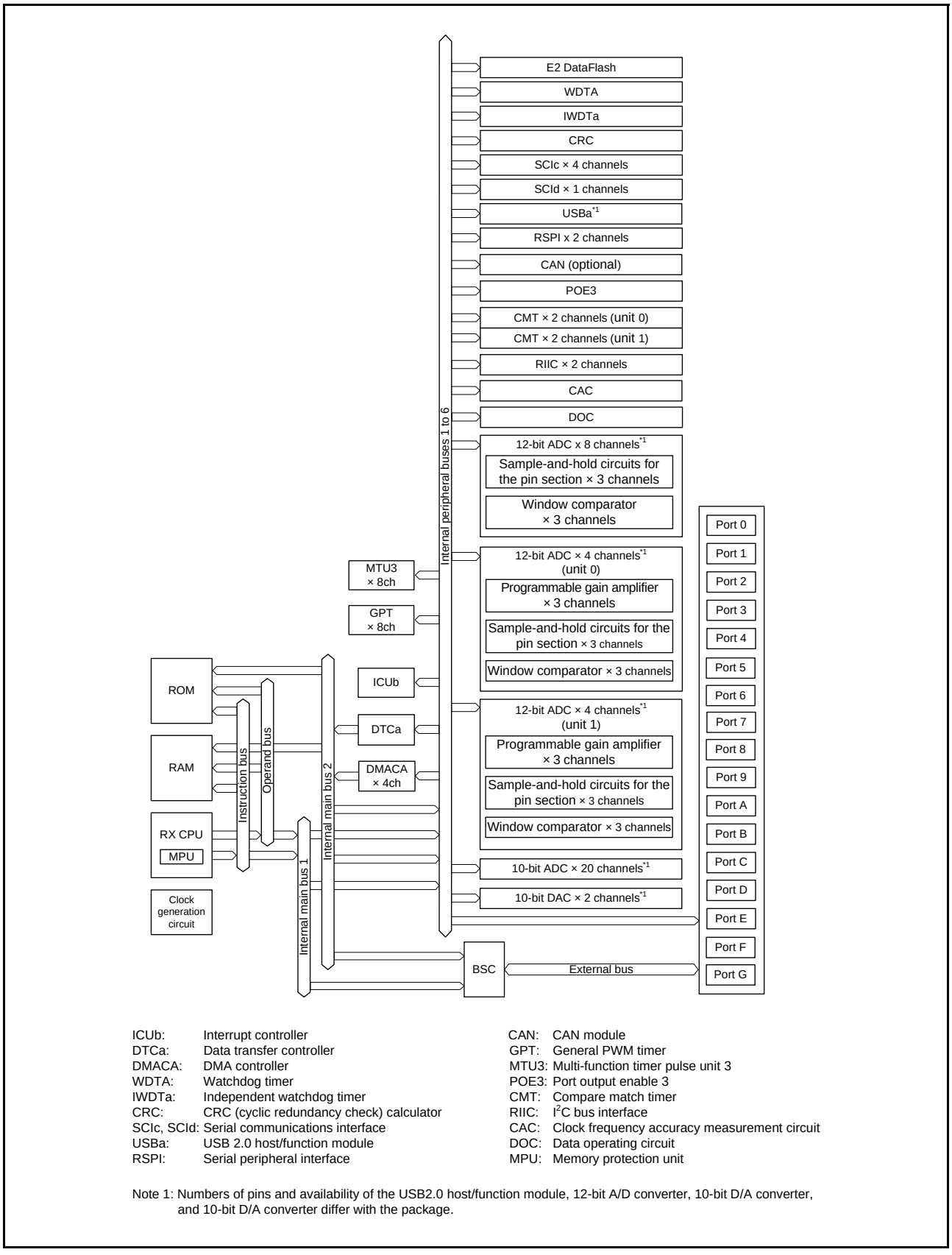
Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	57
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 12x10b, 8x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f563tcbdfp-v0

Table 1.1 Outline of Specifications (6/7)

Classification Module/Function	Description
12-bit A/D converter (S12ADB) [64- and 48-pin versions]	• 12 bits (8 channels x 1 unit) • 12-bit resolution • Conversion time 1.0 µs per channel (S12ADB clock: PCLKD (A/D conversion clock: ADCLK) = 50 MHz • Operating modes Scan mode (single scan mode / continuous scan mode / group scan mode) Group A priority control (group scan mode only) • Sample-and-hold function A common sample-and-hold circuit for units is included Separate sample-and-hold circuits are also included (three channels per unit) • Self-diagnosis function Three analog input voltages (VREFL0, VREFH0 × 1/2, VREFH0) can be generated internally by the self-diagnosis function. • Double trigger mode (double the results of A/D conversion) • Three ways to start A/D conversion Conversion can be started by software, a conversion start trigger from a timer (MTU3 or GPT), or an external trigger signal. • Window comparators (three channels per unit)
10-bit A/D converter (ADA)	10 bits (20 channels × 1 unit) • 10-bit resolution • Conversion time 0.5 µs per channel (A/D conversion clock ADCLK = 100 MHz) • Two operating modes Single mode, scan mode • Scan mode Single-cycle scan mode Continuous scan mode • Sample-and-hold function A common sample-and-hold circuit for units is included • Three ways to start A/D conversion Conversion can be started by software, a conversion start trigger from a timer (MTU3 or GPT), or an external trigger signal. • 8-bit precision output 2-bit right shifting for output of conversion results is selectable. • Self-diagnostic function The self-diagnostic function internally generates three analog input voltages (AVSS, VREF x 1/2, VREF)
D/A converter (DAa)	• 2 channels • 10-bit resolution • Output voltage: 0 V to VREF
CRC calculator (CRC)	• CRC code generation for arbitrary amounts of data in 8-bit units • Select any of three generating polynomials: $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$. • Generation of CRC codes for use with LSB-first or MSB-first communications is selectable
Data operating circuit (DOC)	• Comparison, addition, and subtraction of 16-bit data
Digital power supply controller (DPC)	• Control parameters calculation unit of the digital switch-mode power supply systems. • Adopt robust control algorithm with high control stability • Results of measurement by the 10-bit A/D converter can be used in calculating the control parameters.
Operating frequency	Up to 100 MHz
Power supply voltage [144-, 120-, 112- and 100-pin versions]	• 3-V product VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V AVCC0 = AVCC = VREF = 3.0 to 3.6 V, or 4.0 to 5.5 V VREFH0 = 3.0 to AVCC0, or 4.0 to AVCC0 • 5-V product VCC = PLLVCC = 4.0 to 5.5 V VCC_USB = 3.0 to 3.6 V AVCC0 = AVCC = VREF = 4.0 to 5.5 V VREFH0 = 4.0 to AVCC0
Power supply voltage [64- and 48-pin versions]	VCC = 2.7 to 3.6 V, AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

1.3 Block Diagram

Figure 1.2 shows a block diagram.



ICUb: Interrupt controller
DTCa: Data transfer controller
DMACA: DMA controller
WDTA: Watchdog timer
IWDTa: Independent watchdog timer
CRC: CRC (cyclic redundancy check) calculator
SCIc, SCId: Serial communications interface
USBa: USB 2.0 host/function module
RSPI: Serial peripheral interface
CAN: CAN module
GPT: General PWM timer
MTU3: Multi-function timer pulse unit 3
POE3: Port output enable 3
CMT: Compare match timer
RIIC: I^2C bus interface
CAC: Clock frequency accuracy measurement circuit
DOC: Data operating circuit
MPU: Memory protection unit

Note 1: Numbers of pins and availability of the USB2.0 host/function module, 12-bit A/D converter, 10-bit D/A converter, and 10-bit D/A converter differ with the package.

Figure 1.2 Block Diagram

Table 1.4 Pin Functions (3/5)

Classifications	Pin Name	I/O	Description
Serial communications interface (SCIc)	Asynchronous mode/clock synchronous mode		
	SCK0, SCK1, SCK2, SCK3	I/O	Input/output pins for clock signals.
	RXD0, RXD1, RXD2, RXD3	Input	Input pins for data reception.
	TXD0, TXD1, TXD2, TXD3	Output	Output pins for data transmission.
	CTS0#, CTS1#, CTS2#, CTS3#	Input	Transmit/receive start control input pins
	RTS0#, RTS1#, RTS2#, RTS3#	Output	Transmit/receive start control output pins
	Simple I^2C mode		
	SSCL0, SSCL1, SSCL2, SSCL3	I/O	Input/output pins for the I^2C clock
	SSDA0, SSDA1, SSDA2, SSDA3	I/O	Input/output pins for the I^2C data
	Simple SPI mode		
	SCK0, SCK1, SCK2, SCK3	I/O	Input/output pins for the clock
	SMISO0, SMISO1, SMISO2, SMISO3	I/O	Input/output pins for slave transmit data.
	SMOSI0, SMOSI1, SMOSI2, SMOSI3	I/O	Input/output pins for master transmit data.
	SS0#, SS1#, SS2#, SS3#	Input	Input pins for chip select signals
Serial communications interface (SCId)	Asynchronous mode/clock synchronous mode		
	SCK12	I/O	Input/output pin for clock signals.
	RXD12	Input	Input pin for data reception.
	TXD12	Output	Output pin for data transmission.
	CTS12#	Input	Transmit/receive start control input pins
	RTS12#	Output	Transmit/receive start control output pins
	Simple I^2C mode		
	SSCL12	I/O	Input/output pins for the I^2C clock
	SSDA12	I/O	Input/output pins for the I^2C data
	Simple SPI mode		
	SCK12	I/O	Input/output pins for the clock
	SMISO12	I/O	Input/output pins for slave transmit data.
	SMOSI12	I/O	Input/output pins for master transmit data.
	SS12#	Input	Input pins for chip select signals
	Extended serial mode		
	RXDX12	Input	Input pin for receive data
	TXDX12	Output	Output pin for transmit data
	SIOX12	I/O	Input/output pin for transfer data
I^2C bus interface	SCL, SCL0, SCL1	I/O	Clock input/output pin. N-channel open drain can directly drive buses.
	SDA, SDA0, SDA1	I/O	Data input/output pin. N-channel open drain can directly drive buses.

Table 1.6 List of Pins and Pin Functions (120-Pin LQFP) (1/4)

Pin Number 120-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3, GPT, POE3, CAC)	Communications (SCIc, SCId, RSPI, RIIC, CAN, USB)	Interrupt	S12ADB, AD, DA
1	VCC_USB						
2		PE5	BCLK		USB0_VBUS	IRQ0	
3	EMLE						
4	VSS						
5		P01	RD#		CTS0#/RTS0#/SS0#/ USB0_DRPD		
6	VCL						
7		P00	CS1#	CACREF			
8	MD/FINED						
9		PE4	A10	POE10#/MTCLKC		IRQ1	
10		PE3	A11	POE11#/MTCLKD		IRQ2-DS	
11		P13			CTS2#/RTS2#/SS2#/ USB0_VBUSEN		
12	RES#						
13	XTAL						
14	VSS						
15	EXTAL						
16	VCC						
17		PE2		POE10#		NMI	
18		PE1	WR0#/WR#		CTS12#/RTS12#/ SS12#/SSLA3/SSLB3/ USB0_OVRCURA		
19		PE0	WR1#/BC1#/ WAIT#		SSLA2/SSLB2/CRX1/ USB0_OVRCURB	IRQ7	
20	TRST#	PD7		GTIOC0A	CTS0#/RTS0#/SS0#/ SSLA1/SSLB1/CTX1		
21	TMS	PD6		GTIOC0B	SSLA0/SSLB0		
22	TDI	PD5		GTIOC1A	RXD1/SMISO1/SSCL1	IRQ6	
23	TCK/FINEC	PD4		GTIOC1B	SCK1		
24	TDO	PD3		GTIOC2A	TXD1/SMOSI1/SSDA1		
25		PD2	CS2#	GTIOC2B	MOSIA/MOSIB/ USB0_ID		
26		PD1	CS0#	GTIOC3A	MISOA/MISOB/ USB0_EXICEN		
27		PD0	A12	GTIOC3B	RSPCKA/RSPCKB		
28		PF3			TXD1/SMOSI1/SSDA1		
29		PF2	CS1#		RXD1/SMISO1/SSCL1	IRQ5	
30		PF1					
31		PF0					
32		PB7	A19		SCK12		
33		PB6	A18		RXD12/SMISO12/ SSCL12/RXDX12/ CRX1	IRQ2	
34		PB5	A17		TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/CTX1		
35	PLLVCC						
36		PB4	A16	POE8#/GTETRG0		IRQ3-DS	

Table 1.7 List of Pins and Pin Functions (112-Pin LQFP) (4/4)

Pin Number 112-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3, GPT, POE3, CAC)	Communications (SCIc, SCId, RSPI, RIIC, CAN)	Interrupt	S12ADB, AD, DA
110		P10		MTCLKD		IRQ0-DS	
111	TRST#	P05	WAIT#/CS2#				
112	TMS	P04					

Note 1. Available for use as SCI pin only in boot mode.

Table 1.9 List of Pins and Pin Functions (64-Pin LQFP) (3/3)

Pin Number 64-Pin LQFP	Power Supply Clock System Control	I/O Port	POE3	Timer (MTU3, GPT, CAC)	Communications (SCIc, SCId)	Communications (RSPI, RIIC)	Interrupt	S12ADB
50		P46						AN006
51		P45						AN005
52		P44						AN004
53		P43						AN003 CVREFL
54		P42						AN002
55		P41						AN001
56		P40						AN000
57	AVCC0							
58	VREFH0							
59	VREFL0							
60	AVSS0							
61		P11		MTCLKC			IRQ1-DS	
62		P10		MTCLKD			IRQ0-DS	
63		PA5		MTIOC1A		MISOA		
64		PA4		MTIOC1B		RSPCKA		ADTRG0#

4.1 I/O Register Addresses (Address Order)

Table 4.1 List of I/O Registers (Address Order) (1/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 0000h	SYSTEM	Mode Monitor Register	MDMONR	16	16	3 ICLK		Operating Modes	
0008 0002h	SYSTEM	Mode Status Register	MDSR	16	16	3 ICLK			Not present in versions with 64 or 48 pins.
0008 0006h	SYSTEM	System Control Register 0	SYSCR0	16	16	3 ICLK			
0008 0008h	SYSTEM	System Control Register 1	SYSCR1	16	16	3 ICLK			
0008 000Ch	SYSTEM	Standby Control Register	SBYCR	16	16	3 ICLK		Low Power Consumption	
0008 0010h	SYSTEM	Module Stop Control Register A	MSTPCRA	32	32	3 ICLK			
0008 0014h	SYSTEM	Module Stop Control Register B	MSTPCRB	32	32	3 ICLK			
0008 0018h	SYSTEM	Module Stop Control Register C	MSTPCRC	32	32	3 ICLK			
0008 0020h	SYSTEM	System Clock Control Register	SCKCR	32	32	3 ICLK		Clock Generation Circuit	
0008 0024h	SYSTEM	System Clock Control Register 2	SCKCR2	16	16	3 ICLK			Not present in versions with 64 or 48 pins.
0008 0026h	SYSTEM	System Clock Control Register 3	SCKCR3	16	16	3 ICLK			
0008 0028h	SYSTEM	PLL Control Register	PLLCR	16	16	3 ICLK			
0008 002Ah	SYSTEM	PLL Control Register 2	PLLCR2	8	8	3 ICLK			
0008 0030h	SYSTEM	External Bus Clock Control Register	BCKCR	8	8	3 ICLK			Not present in versions with 64 or 48 pins.
0008 0032h	SYSTEM	Main Clock Oscillator Control Register	MOSCCR	8	8	3 ICLK			
0008 0034h	SYSTEM	Low-Speed On-Chip Oscillator Control Register	LOCOCR	8	8	3 ICLK			
0008 0035h	SYSTEM	IWDT-Dedicated On-Chip Oscillator Control Register	ILOCOCR	8	8	3 ICLK			
0008 0040h	SYSTEM	Oscillation Stop Detection Control Register	OSTDCR	8	8	3 ICLK			
0008 0041h	SYSTEM	Oscillation Stop Detection Status Register	OSTDSR	8	8	3 ICLK			
0008 00A2h	SYSTEM	Main Clock Oscillator Wait Control Register	MOSCWTCR	8	8	3 ICLK		Low Power Consumption	
0008 00A6h	SYSTEM	PLL Wait Control Register	PLLWTCR	8	8	3 ICLK			
0008 00C0h	SYSTEM	Reset Status Register 2	RSTSR2	8	8	3 ICLK		Resets	
0008 00C2h	SYSTEM	Software Reset Register	SWRR	16	16	3 ICLK			
0008 00E0h	SYSTEM	Voltage Monitoring 1 Circuit Control Register 1	LVD1CR1	8	8	3 ICLK		LVDA	
0008 00E1h	SYSTEM	Voltage Monitoring 1 Circuit Status Register	LVD1SR	8	8	3 ICLK			
0008 00E2h	SYSTEM	Voltage Monitoring 2 Circuit Control Register 1	LVD2CR1	8	8	3 ICLK			
0008 00E3h	SYSTEM	Voltage Monitoring 2 Circuit Status Register	LVD2SR	8	8	3 ICLK			
0008 03FEh	SYSTEM	Protect Register	PRCR	16	16	3 ICLK		Register Write Protection Function	
0008 1300h	BSC	Bus Error Status Clear Register	BERCLR	8	8	2 ICLK		Buses	
0008 1304h	BSC	Bus Error Monitoring Enable Register	BEREN	8	8	2 ICLK			
0008 1308h	BSC	Bus Error Status Register 1	BERSR1	8	8	2 ICLK			
0008 130Ah	BSC	Bus Error Status Register 2	BERSR2	16	16	2 ICLK			
0008 1310h	BSC	Bus Priority Control Register	BUSPRI	16	16	2 ICLK			
0008 2000h	DMAC0	DMA Source Address Register	DMSAR	32	32	2 ICLK		DMACA	
0008 2004h	DMAC0	DMA Destination Address Register	DMDAR	32	32	2 ICLK			
0008 2008h	DMAC0	DMA Transfer Count Register	DMCRA	32	32	2 ICLK			
0008 200Ch	DMAC0	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK			
0008 2010h	DMAC0	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK			
0008 2013h	DMAC0	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK			
0008 2014h	DMAC0	DMA Address Mode Register	DMAMD	16	16	2 ICLK			
0008 2018h	DMAC0	DMA Offset Register	DMOFR	32	32	2 ICLK			
0008 201Ch	DMAC0	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK			
0008 201Dh	DMAC0	DMA Software Start Register	DMREQ	8	8	2 ICLK			
0008 201Eh	DMAC0	DMA Status Register	DMSTS	8	8	2 ICLK			

Table 4.1 List of I/O Registers (Address Order) (6/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 7098h	ICU	Interrupt Request Register 152	IR152	8	8	2 ICLK		ICUb	
0008 7099h	ICU	Interrupt Request Register 153	IR153	8	8	2 ICLK			
0008 709Ah	ICU	Interrupt Request Register 154	IR154	8	8	2 ICLK			
0008 709Bh	ICU	Interrupt Request Register 155	IR155	8	8	2 ICLK			
0008 709Ch	ICU	Interrupt Request Register 156	IR156	8	8	2 ICLK			
0008 709Dh	ICU	Interrupt Request Register 157	IR157	8	8	2 ICLK			
0008 709Eh	ICU	Interrupt Request Register 158	IR158	8	8	2 ICLK			
0008 70A1h	ICU	Interrupt Request Register 161	IR161	8	8	2 ICLK			
0008 70A2h	ICU	Interrupt Request Register 162	IR162	8	8	2 ICLK			
0008 70A3h	ICU	Interrupt Request Register 163	IR163	8	8	2 ICLK			
0008 70A4h	ICU	Interrupt Request Register 164	IR164	8	8	2 ICLK			
0008 70A5h	ICU	Interrupt Request Register 165	IR165	8	8	2 ICLK			
0008 70A6h	ICU	Interrupt Request Register 166	IR166	8	8	2 ICLK			
0008 70A7h	ICU	Interrupt Request Register 167	IR167	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70A8h	ICU	Interrupt Request Register 168	IR168	8	8	2 ICLK			
0008 70A9h	ICU	Interrupt Request Register 169	IR169	8	8	2 ICLK			
0008 70AAh	ICU	Interrupt Request Register 170	IR170	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70ABh	ICU	Interrupt Request Register 171	IR171	8	8	2 ICLK			
0008 70ACh	ICU	Interrupt Request Register 172	IR172	8	8	2 ICLK			
0008 70ADh	ICU	Interrupt Request Register 173	IR173	8	8	2 ICLK			
0008 70AEh	ICU	Interrupt Request Register 174	IR174	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70AFh	ICU	Interrupt Request Register 175	IR175	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70B0h	ICU	Interrupt Request Register 176	IR176	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70B1h	ICU	Interrupt Request Register 177	IR177	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70B2h	ICU	Interrupt Request Register 178	IR178	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70B3h	ICU	Interrupt Request Register 179	IR179	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70B4h	ICU	Interrupt Request Register 180	IR180	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70B5h	ICU	Interrupt Request Register 181	IR181	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70B6h	ICU	Interrupt Request Register 182	IR182	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70B7h	ICU	Interrupt Request Register 183	IR183	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70B8h	ICU	Interrupt Request Register 184	IR184	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70B9h	ICU	Interrupt Request Register 185	IR185	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70BAh	ICU	Interrupt Request Register 186	IR186	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70BBh	ICU	Interrupt Request Register 187	IR187	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70BCh	ICU	Interrupt Request Register 188	IR188	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70BDh	ICU	Interrupt Request Register 189	IR189	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70BEh	ICU	Interrupt Request Register 190	IR190	8	8	2 ICLK			Not present in versions with 112, 100, 64 or 48 pins.
0008 70BFh	ICU	Interrupt Request Register 191	IR191	8	8	2 ICLK			Not present in versions with 112, 100, 64 or 48 pins.

Table 4.1 List of I/O Registers (Address Order) (19/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 9804h	AD	A/D Channel Select Register 0	ADANSA0	16	16	2, 3 PCLKB	2 ICLK	AD	Not present in versions with 64 or 48 pins.
0008 9806h	AD	A/D Channel Select Register 1	ADANSA1	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64 or 48 pins.
0008 9808h	AD	A/D-Converted Value Addition Mode Select Register0	ADADS0	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 980Ah	AD	A/D-Converted Value Addition Mode Select Register1	ADADS1	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64 or 48 pins.
0008 980Ch	AD	A/D-Converted Value Addition Count Select Register	ADADC	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 980Eh	AD	A/D Control Extended Register	ADCER	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9810h	AD	A/D Start Trigger Select Register	ADSTRGR	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 981Eh	AD	A/D Self-Diagnosis Data Register	ADRD	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9820h	AD	A/D Data Register A	ADDRA	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9822h	AD	A/D Data Register B	ADDRB	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9824h	AD	A/D Data Register C	ADDRC	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9826h	AD	A/D Data Register D	ADDRD	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9828h	AD	A/D Data Register E	ADDRE	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 982Ah	AD	A/D Data Register F	ADDRF	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 982Ch	AD	A/D Data Register G	ADDRG	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 982Eh	AD	A/D Data Register H	ADDRH	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9830h	AD	A/D Data Register I	ADDRI	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9832h	AD	A/D Data Register J	ADDRJ	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9834h	AD	A/D Data Register K	ADDRK	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9836h	AD	A/D Data Register L	ADDRL	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9838h	AD	A/D Data Register M	ADDRM	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 983Ah	AD	A/D Data Register N	ADDRN	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 983Ch	AD	A/D Data Register O	ADDRO	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 983Eh	AD	A/D Data Register P	ADDRP	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 9840h	AD	A/D Data Register Q	ADDRQ	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 9842h	AD	A/D Data Register R	ADDRR	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 9844h	AD	A/D Data Register S	ADDRS	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 9846h	AD	A/D Data Register T	ADDRT	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 9860h	AD	A/D Sampling State Register 0	ADSSTR0	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9861h	AD	A/D Sampling State Register L	ADSSTRL	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.

Table 4.1 List of I/O Registers (Address Order) (28/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 C293h	SYSTEM	Main Clock Oscillator Forced Oscillation Control Register	MOFCR	8	8	4, 5 PCLKB	2, 3 ICLK	Clock Generation Circuit	
0008 C296h	FLASH	Flash P/E Protection Register	FWEPROR	8	8	4, 5 PCLKB	2, 3 ICLK	ROM	
0008 C297h	SYSTEM	Voltage Monitoring Circuit Control Register	LVCMPCR	8	8	4, 5 PCLKB	2, 3 ICLK	LVDA	
0008 C298h	SYSTEM	Voltage Detection Level Select Register	LVDLVLR	8	8	4, 5 PCLKB	2, 3 ICLK		
0008 C29Ah	SYSTEM	Voltage Monitoring 1 Circuit Control Register 0	LVD1CR0	8	8	4, 5 PCLKB	2, 3 ICLK		
0008 C29Bh	SYSTEM	Voltage Monitoring 2 Circuit Control Register 0	LVD2CR0	8	8	4, 5 PCLKB	2, 3 ICLK		
0008 C2A0h to 0008 C2BFh	SYSTEM	Deep Standby Backup Register 0 to 31	DPSBKR0 to 31	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption	
0008 C300h	ICU	Group 0 Interrupt Source Register	GRP00	32	32	1, 2 PCLKB	2 ICLK	ICUb	Not present in versions with 64 or 48 pins.
0008 C330h	ICU	Group 12 Interrupt Source Register	GRP12	32	32	1, 2 PCLKB	2 ICLK		
0008 C340h	ICU	Group 0 Interrupt Enable Register	GEN00	32	32	1, 2 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C370h	ICU	Group 12 Interrupt Enable Register	GEN12	32	32	1, 2 PCLKB	2 ICLK		
0008 C380h	ICU	Group 0 Interrupt Clear Register	GCR00	32	32	1, 2 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C4C0h	POE	Input Level Control/Status Register 1	ICSR1	16	8, 16	2, 3 PCLKB	2 ICLK	POE3	
0008 C4C2h	POE	Output Level Control/Status Register 1	OCSR1	16	8, 16	2, 3 PCLKB	2 ICLK		
0008 C4C4h	POE	Input Level Control/Status Register 2	ICSR2	16	8, 16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C4C6h	POE	Output Level Control/Status Register 2	OCSR2	16	8, 16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C4C8h	POE	Input Level Control/Status Register 3	ICSR3	16	8, 16	2, 3 PCLKB	2 ICLK		
0008 C4CAh	POE	Software Port Output Enable Register	SPOER	8	8	2, 3 PCLKB	2 ICLK		
0008 C4CBh	POE	Port Output Enable Control Register 1	POECR1	8	8	2, 3 PCLKB	2 ICLK		
0008 C4CCh	POE	Port Output Enable Control Register 2	POECR2	16	16	2, 3 PCLKB	2 ICLK		
0008 C4CEh	POE	Port Output Enable Control Register 3	POECR3	16	16	2, 3 PCLKB	2 ICLK		
0008 C4D0h	POE	Port Output Enable Control Register 4	POECR4	16	16	2, 3 PCLKB	2 ICLK		
0008 C4D2h	POE	Port Output Enable Control Register 5	POECR5	16	16	2, 3 PCLKB	2 ICLK		
0008 C4D4h	POE	Port Output Enable Control Register 6	POECR6	16	16	2, 3 PCLKB	2 ICLK		
0008 C4D6h	POE	Input Level Control/Status Register 4	ICSR4	16	8, 16	2, 3 PCLKB	2 ICLK		
0008 C4D8h	POE	Input Level Control/Status Register 5	ICSR5	16	8, 16	2, 3 PCLKB	2 ICLK		
0008 C4DAh	POE	Active Level Setting Register 1	ALR1	16	8, 16	2, 3 PCLKB	2 ICLK		
0008 C4DCh	POE	Input Level Control/Status Register 6	ICSR6	16	16	2, 3 PCLKB	2 ICLK		
0008 C4DEh	POE	Active Level Setting Register 2	ALR2	16	8, 16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C4E0h	POE	Input Level Control/Status Register 7	ICSR7	16	8, 16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C4E2h	POE	Port Output Enable Control Register 7	POECR7	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C4E4h	POE	Port Output Enable Control Register 8	POECR8	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0009 1200h to 0009 13FFh	CAN1	Mailbox Register 0 to 31	MB0 to 31	128	8, 16, 32	2, 3 PCLKB	2 ICLK	CAN	Not present in versions with 64 or 48 pins.
0009 1400h to 0009 141Ch	CAN1	Mask Register 0 to 7	MKR0 to 7	32	8, 16, 32	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0009 1420h	CAN1	FIFO Received ID Compare Register 0 and 1	FIDCR0	32	8, 16, 32	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0009 1424h	CAN1	FIFO Received ID Compare Register 0 and 1	FIDCR1	32	8, 16, 32	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0009 1428h	CAN1	Mask Invalid Register	MKIVLR	32	8, 16, 32	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0009 142Ch	CAN1	Mailbox Interrupt Enable Register	MIER	32	8, 16, 32	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0009 1820h to 0009 183Fh	CAN1	Message Control Register 0 to 31	MCTL0 to 31	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.

Table 4.1 List of I/O Registers (Address Order) (29/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0009 1840h	CAN1	Control Register	CTLR	16	8, 16	2, 3 PCLKB	2 ICLK	CAN	Not present in versions with 64 or 48 pins.
0009 1842h	CAN1	Status Register	STR	16	8, 16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0009 1844h	CAN1	Bit Configuration Register	BCR	32	8, 16, 32	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0009 1848h	CAN1	Receive FIFO Control Register	RFCR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0009 1849h	CAN1	Receive FIFO Pointer Control Register	RFPCR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0009 184Ah	CAN1	Transmit FIFO Control Register	TFCR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0009 184Bh	CAN1	Transmit FIFO Pointer Control Register	TFPCR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0009 184Ch	CAN1	Error Interrupt Enable Register	EIER	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0009 184Dh	CAN1	Error Interrupt Factor Judge Register	EIFR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0009 184Eh	CAN1	Receive Error Count Register	RECR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0009 184Fh	CAN1	Transmit Error Count Register	TECR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0009 1850h	CAN1	Error Code Store Register	ECSR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0009 1851h	CAN1	Channel Search Support Register	CSSR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0009 1852h	CAN1	Mailbox Search Status Register	MSSR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0009 1853h	CAN1	Mailbox Search Mode Register	MSMR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0009 1854h	CAN1	Time Stamp Register	TSR	16	8, 16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0009 1856h	CAN1	Acceptance Filter Support Register	AFSR	16	8, 16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0009 1858h	CAN1	Test Control Register	TCR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
000A 0000h	USB0	System Configuration Control Register	SYSCFG	16	16	3, 4 PCLKB	2, 3 ICLK	USBa	Not present in versions with 112, 100, 64, or 48 pins.
000A 0004h	USB0	System Configuration Status Register 0	SYSSTS0	16	16	9 PCLKB or more			Not present in versions with 112, 100, 64, or 48 pins.
000A 0008h	USB0	Device State Control Register 0	DVSTCTR0	16	16	9 PCLKB or more			Not present in versions with 112, 100, 64, or 48 pins.
000A 0014h	USB0	CFIFO Port Register	CFIFO	16	8, 16	3, 4 PCLKB	2, 3 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
000A 0018h	USB0	D0FIFO Port Registe	D0FIFO	16	8, 16	3, 4 PCLKB	2, 3 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
000A 001Ch	USB0	D1FIFO Port Register	D1FIFO	16	8, 16	3, 4 PCLKB	2, 3 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
000A 0020h	USB0	CFIFO Port Select Register	CFIFOSEL	16	16	3, 4 PCLKB	2, 3 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
000A 0022h	USB0	CFIFO Port Control Register	CFIFOCTR	16	16	3, 4 PCLKB	2, 3 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
000A 0028h	USB0	D0FIFO Port Select Register	D0FIFOSEL	16	16	3, 4 PCLKB	2, 3 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
000A 002Ah	USB0	D0FIFO Port Control Register	D0FIFOCTR	16	16	3, 4 PCLKB	2, 3 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
000A 002Ch	USB0	D1FIFO Port Select Register	D1FIFOSEL	16	16	3, 4 PCLKB	2, 3 ICLK		Not present in versions with 112, 100, 64, or 48 pins.

Table 4.1 List of I/O Registers (Address Order) (35/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
000C 1308h	MTU0	Timer General Register A	TGRA	16	16, 32	4, 5 PCLKA	2, 3 ICLK	MTU3	
000C 130Ah	MTU0	Timer General Register B	TGRB	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 130Ch	MTU0	Timer General Register C	TGRC	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 130Eh	MTU0	Timer General Register D	TGRD	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1320h	MTU0	Timer General Register E	TGRE	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1322h	MTU0	Timer General Register F	TGRF	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1324h	MTU0	Timer Interrupt Enable Register 2	TIER2	8	8, 16	4, 5 PCLKA	2, 3 ICLK		
000C 1325h	MTU0	Timer Status Register 2	TSR2	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1326h	MTU0	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1380h	MTU1	Timer Control Register	TCR	8	8, 16	4, 5 PCLKA	2, 3 ICLK		
000C 1381h	MTU1	Timer Mode Register 1	TMDR1	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1382h	MTU1	Timer I/O Control Register	TIOR	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1384h	MTU1	Timer Interrupt Enable Register	TIER	8	8, 16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1385h	MTU1	Timer Status Register	TSR	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1386h	MTU1	Timer Counter	TCNT	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1388h	MTU1	Timer General Register A	TGRA	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 138Ah	MTU1	Timer General Register B	TGRB	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1390h	MTU1	Timer Input Capture Control Register	TICCR	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1400h	MTU2	Timer Control Register	TCR	8	8, 16	4, 5 PCLKA	2, 3 ICLK		
000C 1401h	MTU2	Timer Mode Register 1	TMDR1	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1402h	MTU2	Timer I/O Control Register	TIOR	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1404h	MTU2	Timer Interrupt Enable Register	TIER	8	8, 16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1405h	MTU2	Timer Status Register	TSR	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1406h	MTU2	Timer Counter	TCNT	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1408h	MTU2	Timer General Register A	TGRA	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 140Ah	MTU2	Timer General Register B	TGRB	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1A00h	MTU6	Timer Control Register	TCR	8	8, 16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1A01h	MTU7	Timer Control Register	TCR	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1A02h	MTU6	Timer Mode Register 1	TMDR1	8	8, 16	4, 5 PCLKA	2, 3 ICLK		
000C 1A03h	MTU7	Timer Mode Register 1	TMDR1	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1A04h	MTU6	Timer I/O Control Register H	TIORH	8	8, 16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1A05h	MTU6	Timer I/O Control Register L	TIORL	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1A06h	MTU7	Timer I/O Control Register H	TIORH	8	8, 16	4, 5 PCLKA	2, 3 ICLK		
000C 1A07h	MTU7	Timer I/O Control Register L	TIORL	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1A08h	MTU6	Timer Interrupt Enable Register	TIER	8	8, 16	4, 5 PCLKA	2, 3 ICLK		
000C 1A09h	MTU7	Timer Interrupt Enable Register	TIER	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1A0Ah	MTU	Timer Output Master Enable Register B	TOERB	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1A0Eh	MTU	Timer Output Control Register 1B	TOCR1B	8	8, 16	4, 5 PCLKA	2, 3 ICLK		
000C 1A0Fh	MTU	Timer Output Control Register 2B	TOCR2B	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1A10h	MTU6	Timer Counter	TCNT	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1A12h	MTU7	Timer Counter	TCNT	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1A14h	MTU	Timer Cycle Data Register B	TCDRB	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1A16h	MTU	Timer Dead Time Data Register B	TDDRB	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1A18h	MTU6	Timer General Register A	TGRA	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1A1Ah	MTU6	Timer General Register B	TGRB	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1A1Ch	MTU7	Timer General Register A	TGRA	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1A1Eh	MTU7	Timer General Register B	TGRB	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1A20h	MTU	Timer Subcounter B	TCNTSB	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1A22h	MTU	Timer Cycle Buffer Register B	TCBRB	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1A24h	MTU6	Timer General Register C	TGRC	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1A26h	MTU6	Timer General Register D	TGRD	16	16	4, 5 PCLKA	2, 3 ICLK		

Table 4.1 List of I/O Registers (Address Order) (40/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
000C 2230h	GPT2	A/D Converter Start Request Timing Double-Buffer Register B	GTADTDBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK	GPT	
000C 2234h	GPT2	General PWM Timer Output Negate Control Register	GTONCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2236h	GPT2	General PWM Timer Dead Time Control Register	GTDTCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2238h	GPT2	General PWM Timer Dead Time Value Register U	GTDVU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 223Ah	GPT2	General PWM Timer Dead Time Value Register D	GTDVD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 223Ch	GPT2	General PWM Timer Dead Time Buffer Register U	GTDBU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 223Eh	GPT2	General PWM Timer Dead Time Buffer Register D	GTDBD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2240h	GPT2	General PWM Timer Output Protection Function Status Register	GTSOS	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2242h	GPT2	General PWM Timer Output Protection Function Temporary Release Register	GTSOTR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2280h	GPT3	General PWM Timer I/O Control Register	GTIOR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2282h	GPT3	General PWM Timer Interrupt Output Setting Register	GTINTAD	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2284h	GPT3	General PWM Timer Control Register	GTCR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2286h	GPT3	General PWM Timer Buffer Enable Register	GTBER	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2288h	GPT3	General PWM Timer Count Direction Register	GTUDC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 228Ah	GPT3	General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register	GTITC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 228Ch	GPT3	General PWM Timer Status Register	GTST	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 228Eh	GPT3	General PWM Timer Counter	GTCNT	16	16	2 to 5 PCLKA	2, 3 ICLK		
000C 2290h	GPT3	General PWM Timer Compare Capture Register A	GTCCRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2292h	GPT3	General PWM Timer Compare Capture Register B	GTCCRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2294h	GPT3	General PWM Timer Compare Capture Register C	GTCCRC	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2296h	GPT3	General PWM Timer Compare Capture Register D	GTCCRD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2298h	GPT3	General PWM Timer Compare Capture Register E	GTCCRE	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 229Ah	GPT3	General PWM Timer Compare Capture Register F	GTCCRF	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 229Ch	GPT3	General PWM Timer Cycle Setting Register	GTPR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 229Eh	GPT3	General PWM Timer Cycle Setting Buffer Register	GTPBR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 22A0h	GPT3	General PWM Timer Cycle Setting Double-Buffer Register	GTPDBR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 22A4h	GPT3	A/D Converter Start Request Timing Register A	GTADTRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 22A6h	GPT3	A/D Converter Start Request Timing Buffer Register A	GTADTBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 22A8h	GPT3	A/D Converter Start Request Timing Double-Buffer Register A	GTADTDBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 22ACh	GPT3	A/D Converter Start Request Timing Register B	GTADTRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 22AEh	GPT3	A/D Converter Start Request Timing Buffer Register B	GTADTBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 22B0h	GPT3	A/D Converter Start Request Timing Double-Buffer Register B	GTADTDBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 22B4h	GPT3	General PWM Timer Output Negate Control Register	GTONCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 22B6h	GPT3	General PWM Timer Dead Time Control Register	GTDTCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 22B8h	GPT3	General PWM Timer Dead Time Value Register U	GTDVU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		

Table 5.3 DC Characteristics (2)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

The following relation applies when the USB is in use under condition 1 or condition 2: Vcc = PLLVcc = Vcc_USB = 3.0 to 3.6 V.

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output high voltage	All output pins (except for P52, P53, P60 to P65, P71 to P76, P90 to P95, and USB0_DPUPE)	V_{OH}	VCC – 0.5	—	—	V	I_{OH} = –1 mA
	P52, P53, and P60 to P65		AVCC – 0.5	—	—		I_{OH} = –1 mA
	USB0_DPUPE		VCC_USB – 0.5				I_{OH} = –1 mA
	P71 to P76, and P90 to P95		VCC – 1.0	—	—		I_{OH} = –5 mA
Output low voltage	All output pins (except for P71 to P76, P90 to P95, and RIIC pins)	V_{OL}	—	—	0.5	V	I_{OL} = 1.0 mA
	P71 to P76, and P90 to P95		—	—	1.1		I_{OL} = 15 mA
	RIIC pins		—	—	0.4		I_{OL} = 3 mA
			—	—	0.6		I_{OL} = 6 mA
Input leakage current	RES#, MD pin, EMLE, Port 4, Ports P50, P51, P54 to P57, and Port C	$\lvert I_{in} \rvert$	—	—	1.0	µA	V_{in} = 0 V, V_{in} = VCC
Three-state leakage current (off state)	Port 0, Port 1, Ports P20 to P24, Port 3, Ports P52, P53, Ports 6 to A, Ports PB0, PB3 to PB7, and Ports D to G	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	V_{in} = 0 V, V_{in} = VCC
	Ports P25, P26, PB1, and PB2		—	—	5.0		
Input capacitance	All output pins (except for P25, P26, PB1, and PB2)	C_{in}	—	—	15	pF	V_{in} = 0 V, f = 1 MHz, T_a = 25 ºC
	Ports P25, P26, PB1, and PB2		—	—	30		

Table 5.16 Timing of On-Chip Peripheral Modules (4)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item		Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI	SCK clock cycle output (master)	t_{SPcyc}	4	65536	t_{Pcyc}	C = 30 pF, Figure 5.30
	SCK clock cycle input (slave)		8	65536		
	SCK clock high pulse width	t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width	t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise/fall time	t_{SPCKR}, t_{SPCKF}	—	20	ns	
	Data input setup time	t_{SU}	40	—	ns	C = 30 pF, Figure 5.31 to Figure 5.38
	Data input hold time	t_H	40	—	ns	
	SS input setup time	t_{LEAD}	6	—	t_{Pcyc}	
	SS input hold time	t_{LAG}	6	—	t_{Pcyc}	
	Data output delay time	t_{OD}	—	40	ns	
	Data output hold time	t_{OH}	–10	—	ns	
	Data rise/fall time	t_{DR}, t_{DF}	—	20	ns	
	SS input rise/fall time	t_{SSLr}, t_{SSLf}	—	20	ns	
	Slave access time	t_{SA}	—	5	t_{Pcyc}	C = 30 pF, Figure 5.37 and Figure 5.38
	Slave output release time	t_{REL}	—	5	t_{Pcyc}	

Note 1. t_{Pcyc}: PCLK cycle

Table 6.13 Timing of On-Chip Peripheral Modules (3)

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item		Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI	SCK clock cycle output (master)	t_{SPcyc}	4	65536	t_{Pcyc}	Figure 6.20
	SCK clock cycle input (slave)		8	65536		
	SCK clock high pulse width	t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width	t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise/fall time	t_{SPCKR}, t_{SPCKF}	—	20	ns	
	Data input setup time	t_{SU}	40	—	ns	Figure 6.21 to Figure 6.24
	Data input hold time	t_{H}	40	—	ns	
	SS input setup time	t_{LEAD}	6	—	t_{Pcyc}	
	SS input hold time	t_{LAG}	6	—	t_{Pcyc}	
	Data output delay time	t_{OD}	—	40	ns	
	Data output hold time	t_{OH}	–10	—	ns	
	Data rise/fall time	t_{DR}, t_{DF}	—	20	ns	
	SS input rise/fall time	t_{SSLr}, t_{SSLf}	—	20	ns	
	Slave access time	t_{SA}	—	5	t_{Pcyc}	Figure 6.23 and Figure 6.24
	Slave output release time	t_{REL}	—	5	t_{Pcyc}	

Note 1. t_{Pcyc}: PCLK cycle

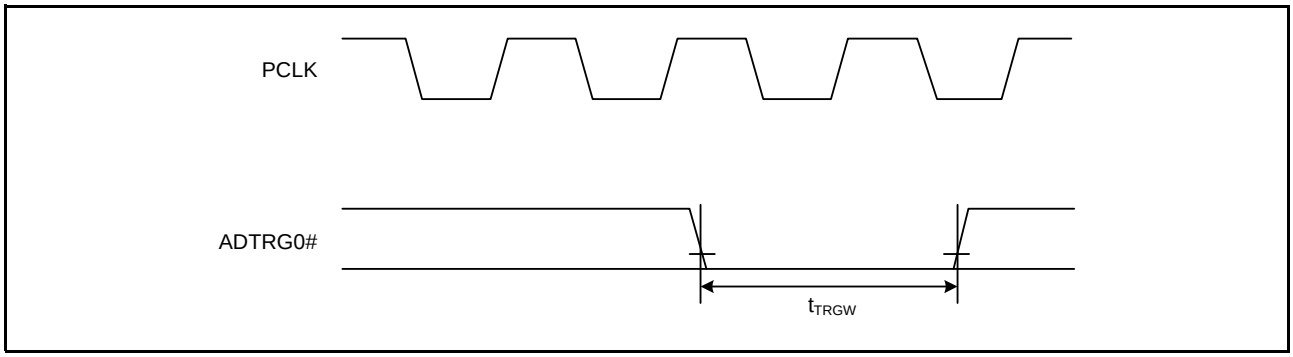


Figure 6.19 AD Converter External Trigger Input Timing

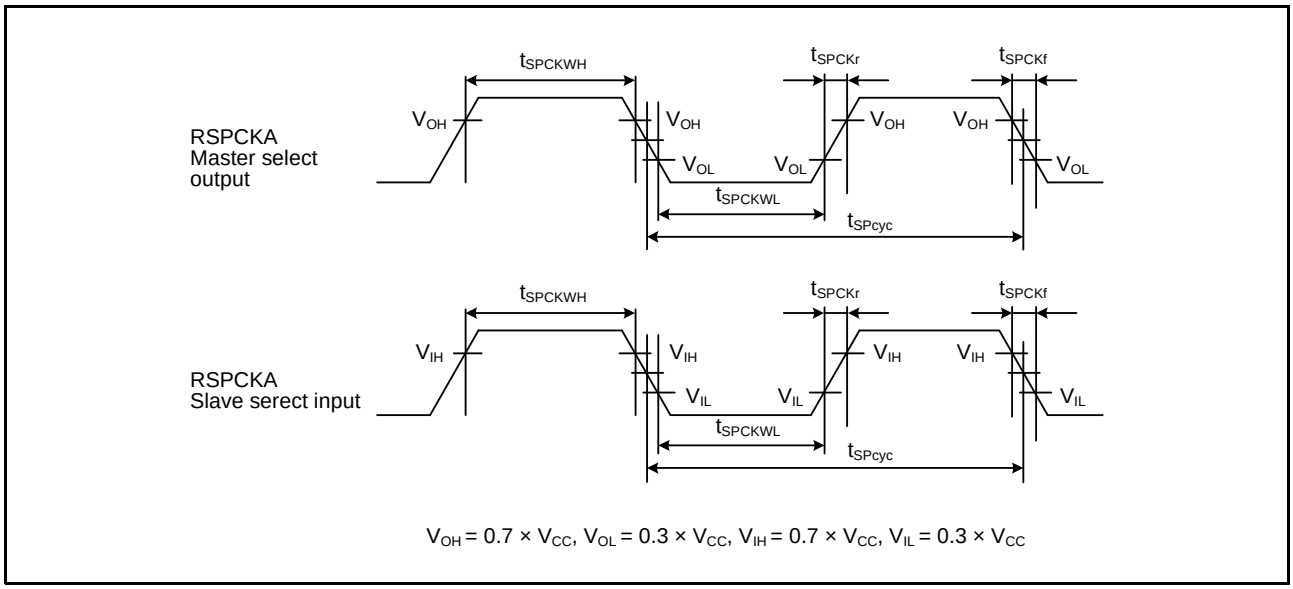


Figure 6.20 RSPI Clock Timing and Simple SPI Clock Timing

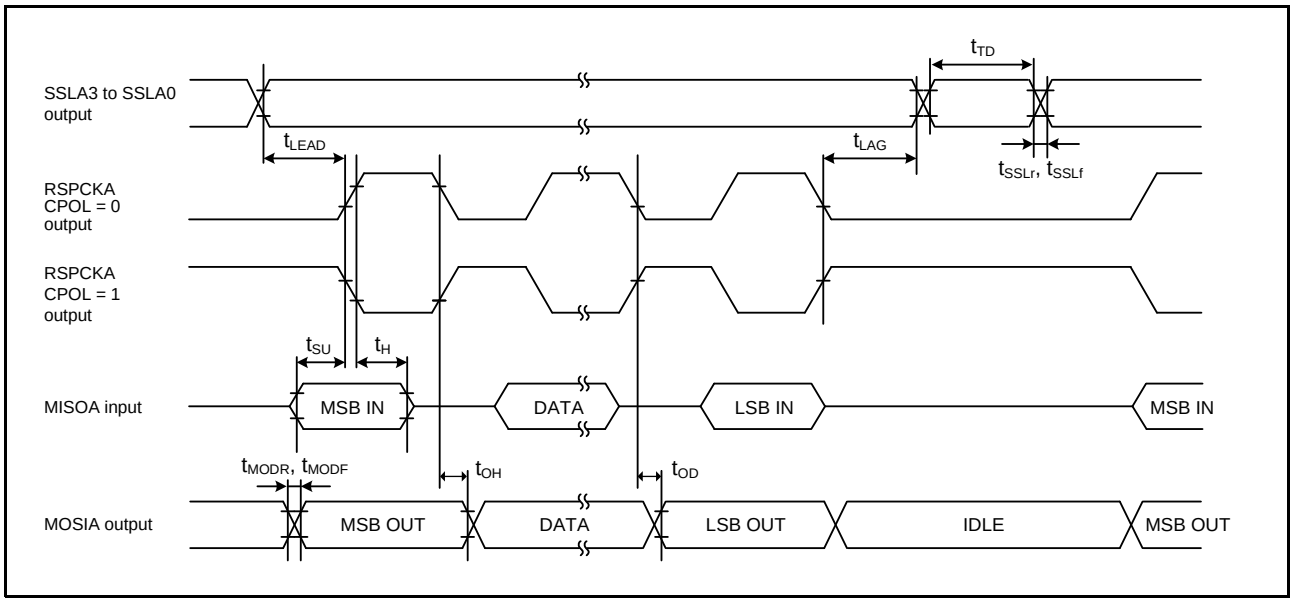
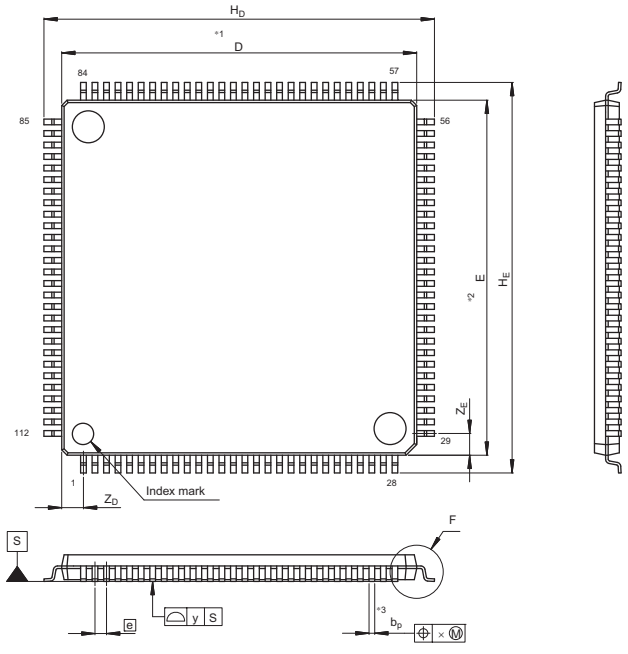
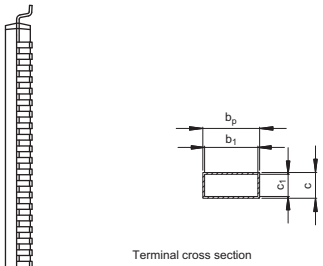
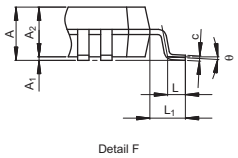


Figure 6.21 RSPI Timing (Master, CPHA = 0) and Simple SPI Timing (Master, CKPH = 1)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP112-20x20-0.65	PLQP0112JA-A	FP-112E/FP-112EV	1.2g





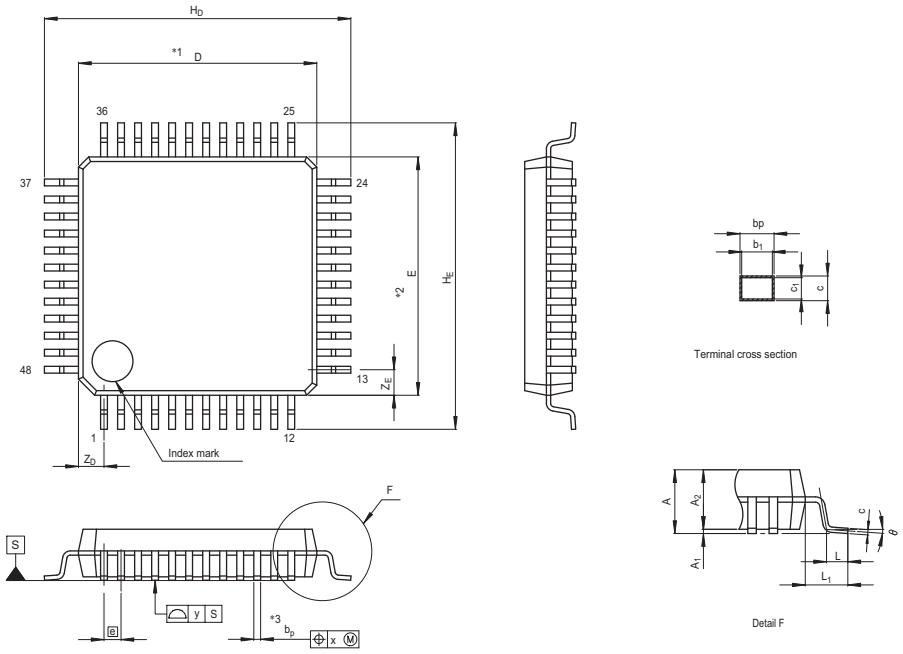


NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	19.9	20.0	20.1
E	19.9	20.0	20.1
A_2	—	1.4	—
H_D	21.8	22.0	22.2
H_E	21.8	22.0	22.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.27	0.32	0.37
b_1	—	0.30	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z_D	—	1.225	—
Z_E	—	1.225	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure C 112-Pin LQFP (PLQP0112JA-A)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP48-7x7-0.50	PLQP0048KB-A	48P6Q-A	0.2g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A_2	—	1.4	—
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.17	0.22	0.27
b_1	—	0.20	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z_D	—	0.75	—
Z_E	—	0.75	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure F 48-Pin LQFP (PLQP0048KB-A)

Rev.	Date	Description	
		Page	Summary
2.10	Sep 26, 2013	36 to 39	Table 1.7 List of Pins and Pin Functions (112-Pin LQFP), changed
		40 to 42	Table 1.8 List of Pins and Pin Functions (100-Pin LQFP), changed
		43 to 45	Table 1.9 List of Pins and Pin Functions (64-Pin LQFP), changed
		46 to 47	Table 1.10 List of Pins and Pin Functions (48-Pin LQFP), changed
		4. I/O Registers	
		56 to 103	Table 4.1 List of I/O Registers (Address Order), changed
		5. Electrical Characteristics [144-, 120-, 112- and 100-Pin Versions]	
		104	Table 5.1 Absolute Maximum Ratings, changed
		107	Table 5.4 DC Characteristics (3), Note 7, deleted
		108	Table 5.6 Permissible Power Consumption, added
		128	5.3.7 Timing of PWM Delay Generation Circuit, added
		128	Table 42.21 Timing of the PWM Delay Generation Circuit, added
		132	Figure 5.32 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKB Division Ratio Set to a Value Other Than 1/2) and Simple SPI Timing (Master, CKPH = 1), changed
		133	Figure 5.34 RSPI Timing (Slave, CPHA = 0) and Simple SPI Timing (Slave, CKPH = 0), changed
		134	Figure 5.35 RSPI Timing (Slave, CPHA = 1) and Simple SPI Timing (Slave, CKPH = 1), changed
		6. Electrical Characteristics [64- and 48-Pin Versions]	
		149	Table 6.1 Absolute Maximum Ratings, changed
		151	Table 6.3 DC Characteristics (2), Note 3, changed
		152	Table 6.5 Permissible Power Consumption, added