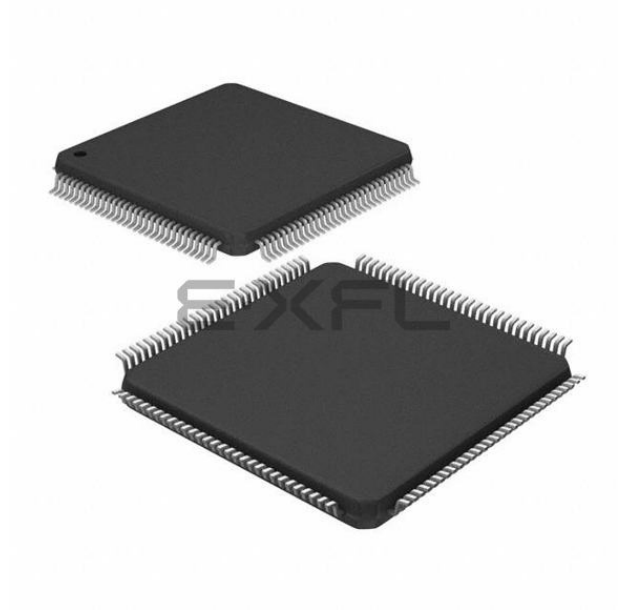
Renesas Electronics America Inc - R5F563TCDDFA#V1 Datasheet



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	EBI/EMI, I²C, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	72
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x10b, 8x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	120-LQFP
Supplier Device Package	120-LQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f563tcddfa-v1

Table 1.1 Outline of Specifications (2/7)

Classification	Module/Function	Description
Clock	Clock generation circuit	• Main clock oscillator, low-speed on-chip oscillator, PLL frequency synthesizer, and dedicated on-chip oscillator for the IWDT • Main-clock oscillation stop detection • Separate frequency-division and multiplication settings for the system clock (ICLK), peripheral module clock (PCLKA), peripheral module clock (PCLKB), AD clock (PCLKC), FlashIF clock (FCLK) and S12AD clock (PCLKD). The CPU and other bus masters run in synchronization with the system clock (ICLK): Up to 100 MHz Multi-function timer pulse unit 3 and general PWM timer run in synchronization with PCLKA: Up to 100 MHz Peripheral modules run in synchronization with the peripheral module clock (PCLKB): Up to 50 MHz Flash IF run in synchronization with the FlashIF clock (FCLK): Up to 50 MHz Devices connected to the external bus run in synchronization with the external bus clock (BCLK): Up to 50 MHz 10-bit A/D converter runs in synchronization with the AD clock (PCLKC): Up to 100 MHz 12-bit A/D converter runs in synchronization with the S12AD clock (PCLKD): Up to 50 MHz
Clock	Clock frequency accuracy measurement circuit (CAC)	The frequency of the following clocks can be measured; the main clock oscillator, PLL circuit, and IWDT-dedicated on-chip oscillator.
Reset		RES# pin reset, power-on reset, voltage-monitoring reset, independent watchdog timer reset, watchdog timer reset, deep software standby reset, and software reset
Voltage detection circuit		When the voltage on VCC passes the voltage detection level (Vdet), an internal reset or internal interrupt is generated.
Low power consumption	Low power consumption facilities	• Module stop function • Four low power consumption modes Sleep mode, all-module clock stop mode, software standby mode, and deep software standby mode
Interrupt	Interrupt controller (ICUb)	• Peripheral function interrupts: Up to 169 sources • External interrupts: Up to 8 (pins IRQ0 to IRQ7) • Software interrupts: One source • Non-maskable interrupts: 6 sources • Sixteen levels specifiable for the order of priority
External bus extension		• The external address space can be divided into four areas (CS0 to CS3), each with independent control of access settings. Capacity of each area: 1 Mbyte (CS0 to CS3) A chip-select signal (CS0# to CS3#) can be output for each area. Each area is specifiable as an 8- or 16-bit bus space The data arrangement in each area is selectable as little or big endian (only for data). • Bus format: Separate bus, multiplex bus • Wait control • Write buffer facility
DMA	DMA controller (DMACA)	• 4 channels • Three transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Software trigger, external interrupts, and interrupt requests from peripheral functions
	Data transfer controller (DTCa)	• Three transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Software interrupt activation register settings, external interrupts, and interrupt requests from peripheral functions

Table 1.1 Outline of Specifications (5/7)

Classification	Module/Function	Description
Communication function	I^2C bus interfaces (RIIC)	• 2 channels Communication formats I^2C bus format/SMBus format Supports the multi-master Max. transfer rate: 400 kbps
	CAN module (CAN)	• 1 channels • Compliance with the ISO11898-1 specification (standard frame and extended frame) • 32 mailboxes per channel
	Serial peripheral interfaces (RSPI)	• 2 channels • RSPI transfer facility Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPCK (RSPI clock) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) Capable of handling serial transfer as a master or slave • Data formats Switching between MSB first and LSB first The number of bits in each transfer can be changed to any number of bits from 8 to 16, or to 20, 24, or 32 bits. 128-bit buffers for transmission and reception Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) • Buffered structure Double buffers for both transmission and reception • Max. transfer rate In master mode: [144-, 120-, 112- and 100-pin versions] 25 Mbps [64- and 48-pin versions] 12.5 Mbps In slave mode: 6.25 Mbps
12-bit A/D converter (S12ADB) [144-, 120-, 112- and 100-pin versions]		• 12 bits (4 channels x 2 unit) • 12-bit resolution • Conversion time 1.0 μs per channel (clock for S12ADB, PCLKD (A/D conversion clock ADCLK) = 50 MHz, AVCC0 = 4.0 to 5.5 V) 2.0 μs per channel (clock for S12ADB, PCLKD (A/D conversion clock ADCLK) = 25 MHz, AVCC0 = 3.0 to 3.6 V) • Operating modes Scan mode (single-cycle scan mode/continuous scan mode/group scan mode) Group A priority control (only for the group scan mode) • Sample-and-hold function A common sample-and-hold circuit for units is included. Additionally, sample-and-hold circuit for each unit is included. (three channels per unit) • Self-diagnostic function The self-diagnostic function internally generates three analog input voltages (VREFL0, VREFH0 x 1/2, VREFH0). • Double trigger mode (duplication of A/D converted data) • Input signal amplification function using programmable gain amplifier (three channels per unit) Amplification factors: 2.0 times, 2.5 times, 3.077 times, 3.636 times, 4.0 times, 4.444 times, 5.0 times, 5.714 times, 6.667 times, 10.0 times, 13.333 times (total of 11 steps) • Three ways to start A/D conversion Conversion can be started by software, a conversion start trigger from a timer (MTU3 or GPT), or an external trigger signal. • Window comparators (three channels per unit)

Table 1.2 Comparison of Functions for Different Packages

Functions			RX63T Group					
Package			**144 Pins**	**120 Pins**	**112 Pins**	**100 Pins**	**64 Pins**	**48 Pins**
External bus			16 bits				—	
External address space			1 Mbyte × 4 areas				—	
DMA	DMA controller (DMACA)		Ch. 0 to 3					
	Data transfer controller (DTCa)		Supported					
Interrupt controller (ICUb)	NMI pin		Supported					
	IRQ pin		Supported (x 8)				Supported (x 6)	
Timers	Multi-function timer pulse unit 3 (MTU3)*1		Ch. 0 to 7					
	General PWM timer (GPT)*1	Generation of delays in PWM, not supported	Ch. 0 to 7				Ch. 0 to 3	
		Generation of delays in PWM, supported	Ch. 0 to 3				—	
	Port output enable 3 (POE3)		Supported (POE pins × 6)			Supported (POE pins × 5)	Supported (POE pins × 4)	
	Compare match timer (CMT)		Ch. 0 to 3					
	Watchdog timer (WDTA)		Supported					
	Independent watchdog timer (IWDTa)		Supported					
Communication function	USB2.0 host/function module (USBa)		Ch. 0		—			
	Serial communications interfaces (SCIc)		Ch. 0 to 3			Ch. 0 to 2	Ch. 0, 1	
	Serial communications interfaces (SCId)		Ch. 12					
	I^2C bus interfaces (RIIC)		Ch. 0, 1		Ch. 0			
	Serial peripheral interfaces (RSPI)		Ch. 0, 1				Ch. 0	
	CAN module (CAN) (as an optional function)*1		Ch. 0				—	
12-bit A/D converter (S12ADB)			4 channels × 2 units				8 channels × 1 unit (AN000 to 007)	8 channels × 1 unit (AN000 to 004, 007)
	Three-channel simultaneous sampling function		2 units				1 unit	
	Programmable gain amplifier		3 channels × 2 units				—	
	Window comparator		3 channels × 2 units				3 channels × 1 unit	
10-bit A/D converter (ADA)			20 channels	12 channels			—	
D/A converter (DAa)			Ch. 0, 1				—	
Clock Frequency Accuracy Measurement Circuit			Supported					
Digital power supply controller (DPC)*2			Supported				Not supported	

Note 1. For the MTU3 and GPT, the number of pins will differ with the package. See the list of pins and pin functions for details. In addition, the CAN module is an optional function. For details, see Table 1.3.

Note 2. Not provided for the product ID code O.

Table 1.5 List of Pins and Pin Functions (144-Pin LQFP) (1/4)

Pin Number 144-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3, GPT, POE3, CAC)	Communications (SCIc, SCId, RSPI, RIIC, CAN, USB)	Interrupt	S12ADB, AD, DA
1	VCC_USB						
2		PE5	BCLK		USB0_VBUS	IRQ0	
3	EMLE						
4	TRSYNC	P03			RXD2/SMISO2/SSCL2	IRQ7	
5	TRDATA3	P02			TXD2/SMOSI2/SSDA2		
6	VSS						
7		P01	RD#		CTS0#/RTS0#/SS0#/ USB0_DRPD		
8	VCL						
9		P00	CS1#	CACREF			
10	MD/FINED						
11		PE4	A10	POE10#/MTCLKC		IRQ1	
12		PE3	A11	POE11#/MTCLKD		IRQ2-DS	
13	TRDATA2	P14			SCK2		
14	VCC						
15		P13			CTS2#/RTS2#/SS2#/ USB0_VBUSEN		
16	RES#						
17	XTAL						
18	VSS						
19	EXTAL						
20	VCC						
21		PE2		POE10#		NMI	
22		PE1	WR0#/WR#		CTS12#/RTS12#/ SS12#/SSLA3/SSLB3/ USB0_OVRCURA		
23		PE0	WR1#/BC1#/ WAIT#		SSLA2/SSLB2/CRX1/ USB0_OVRCURB	IRQ7	
24		PD7		GTIOC0A	CTS0#/RTS0#/SS0#/ SSLA1/SSLB1/CTX1		
25		PD6		GTIOC0B	SSLA0/SSLB0		
26		PD5		GTIOC1A	RXD1/SMISO1/SSCL1	IRQ6	
27	VSS						
28		PD4		GTIOC1B	SCK1		
29		PD3		GTIOC2A	TXD1/SMOSI1/SSDA1		
30		PD2	CS2#	GTIOC2B	MOSIA/MOSIB/ USB0_ID		
31		PD1	CS0#	GTIOC3A	MISOA/MISOB/ USB0_EXICEN		
32		PD0	A12	GTIOC3B	RSPCKA/RSPCKB		
33		PF4	CS3#				
34		PF3			TXD1/SMOSI1/SSDA1		
35		PF2	CS1#		RXD1/SMISO1/SSCL1	IRQ5	
36	TRST#	PF1					
37	TMS	PF0					
38		PB7	A19		SCK12		

Table 1.6 List of Pins and Pin Functions (120-Pin LQFP) (3/4)

Pin Number 120-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3, GPT, POE3, CAC)	Communications (SCIc, SCId, RSPI, RIIC, CAN, USB)	Interrupt	S12ADB, AD, DA
75	VSS						
76		P30	D10/[A10/D10]	MTIOC0B/MTCLKD	SCK0/SSLA0/SSLB0		
77		P26	CS0#		TXD1/SMOSI1/SSDA1/SDA1		
78		P25	CS1#		SCK1/SCL1		
79		P24	D11/[A11/D11]		CTS0#/RTS0#/SS0#/RSPCKA/RSPCKB	IRQ4	
80		P23	D12/[A12/D12]	CACREF	TXD0/SMOSI0/SSDA0/MOSIA/MOSIB/CTX1		
81		P22	D13/[A13/D13]		RXD0/SMISO0/SSCL0/MISOA/MISOB/CRX1		ADTRG#
82		P21	D14/[A14/D14]	MTCLKA		IRQ6-DS	ADTRG1#
83		P20	D15/[A15/D15]	MTCLKB		IRQ7-DS	ADTRG0#
84		P65	A0/BC0#				AN5
85		P64	A1				AN4
86	AVCC						
87	VREF						
88	AVSS						
89		P63	A2				AN3
90		P62	A3				AN2
91		P61	A4				AN1
92		P60	A5				AN0
93		P55					AN11/DA1
94		P54					AN10/DA0
95		P53	A6				AN9
96		P52	A7				AN8
97		P51					AN7
98		P50					AN6
99		P47					AN103/CVREFH
100		P46					AN102
101		P45					AN101
102		P44					AN100
103		P43					AN003/CVREFL
104		P42					AN002
105		P41					AN001
106		P40					AN000
107	AVCC0						
108	VREFH0						
109	VREFL0						
110	AVSS0						

Table 1.7 List of Pins and Pin Functions (112-Pin LQFP) (4/4)

Pin Number 112-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3, GPT, POE3, CAC)	Communications (SCIc, SCId, RSPI, RIIC, CAN)	Interrupt	S12ADB, AD, DA
110		P10		MTCLKD		IRQ0-DS	
111	TRST#	P05	WAIT#/CS2#				
112	TMS	P04					

Note 1. Available for use as SCI pin only in boot mode.

Table 4.1 List of I/O Registers (Address Order) (5/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 703Eh	ICU	Interrupt Request Register 062	IR062	8	8	2 ICLK		ICUb	Not present in versions with 64 or 48 pins.
0008 7040h	ICU	Interrupt Request Register 064	IR064	8	8	2 ICLK			
0008 7041h	ICU	Interrupt Request Register 065	IR065	8	8	2 ICLK			
0008 7042h	ICU	Interrupt Request Register 066	IR066	8	8	2 ICLK			
0008 7043h	ICU	Interrupt Request Register 067	IR067	8	8	2 ICLK			
0008 7044h	ICU	Interrupt Request Register 068	IR068	8	8	2 ICLK			
0008 7045h	ICU	Interrupt Request Register 069	IR069	8	8	2 ICLK			
0008 7046h	ICU	Interrupt Request Register 070	IR070	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7047h	ICU	Interrupt Request Register 071	IR071	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 705Ah	ICU	Interrupt Request Register 090	IR090	8	8	2 ICLK			Not present in versions with 112, 100, 64 or 48 pins.
0008 7062h	ICU	Interrupt Request Register 098	IR098	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7066h	ICU	Interrupt Request Register 102	IR102	8	8	2 ICLK			
0008 7067h	ICU	Interrupt Request Register 103	IR103	8	8	2 ICLK			
0008 7068h	ICU	Interrupt Request Register 104	IR104	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7069h	ICU	Interrupt Request Register 105	IR105	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 706Ah	ICU	Interrupt Request Register 106	IR106	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7072h	ICU	Interrupt Request Register 114	IR114	8	8	2 ICLK			
0008 707Ah	ICU	Interrupt Request Register 122	IR122	8	8	2 ICLK			
0008 707Bh	ICU	Interrupt Request Register 123	IR123	8	8	2 ICLK			
0008 707Ch	ICU	Interrupt Request Register 124	IR124	8	8	2 ICLK			
0008 707Dh	ICU	Interrupt Request Register 125	IR125	8	8	2 ICLK			
0008 707Eh	ICU	Interrupt Request Register 126	IR126	8	8	2 ICLK			
0008 707Fh	ICU	Interrupt Request Register 127	IR127	8	8	2 ICLK			
0008 7080h	ICU	Interrupt Request Register 128	IR128	8	8	2 ICLK			
0008 7081h	ICU	Interrupt Request Register 129	IR129	8	8	2 ICLK			
0008 7082h	ICU	Interrupt Request Register 130	IR130	8	8	2 ICLK			
0008 7083h	ICU	Interrupt Request Register 131	IR131	8	8	2 ICLK			
0008 7084h	ICU	Interrupt Request Register 132	IR132	8	8	2 ICLK			
0008 7085h	ICU	Interrupt Request Register 133	IR133	8	8	2 ICLK			
0008 7086h	ICU	Interrupt Request Register 134	IR134	8	8	2 ICLK			
0008 7087h	ICU	Interrupt Request Register 135	IR135	8	8	2 ICLK			
0008 7088h	ICU	Interrupt Request Register 136	IR136	8	8	2 ICLK			
0008 7089h	ICU	Interrupt Request Register 137	IR137	8	8	2 ICLK			
0008 708Ah	ICU	Interrupt Request Register 138	IR138	8	8	2 ICLK			
0008 708Bh	ICU	Interrupt Request Register 139	IR139	8	8	2 ICLK			
0008 708Ch	ICU	Interrupt Request Register 140	IR140	8	8	2 ICLK			
0008 708Dh	ICU	Interrupt Request Register 141	IR141	8	8	2 ICLK			
0008 708Eh	ICU	Interrupt Request Register 142	IR142	8	8	2 ICLK			
0008 708Fh	ICU	Interrupt Request Register 143	IR143	8	8	2 ICLK			
0008 7090h	ICU	Interrupt Request Register 144	IR144	8	8	2 ICLK			
0008 7091h	ICU	Interrupt Request Register 145	IR145	8	8	2 ICLK			
0008 7092h	ICU	Interrupt Request Register 146	IR146	8	8	2 ICLK			
0008 7093h	ICU	Interrupt Request Register 147	IR147	8	8	2 ICLK			
0008 7094h	ICU	Interrupt Request Register 148	IR148	8	8	2 ICLK			
0008 7095h	ICU	Interrupt Request Register 149	IR149	8	8	2 ICLK			
0008 7096h	ICU	Interrupt Request Register 150	IR150	8	8	2 ICLK			
0008 7097h	ICU	Interrupt Request Register 151	IR151	8	8	2 ICLK			

Table 4.1 List of I/O Registers (Address Order) (27/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 C1A3h	MPC	PC3 Pin Function Control Register	PC3PFS	8	8	2, 3 PCLKB	2 ICLK	MPC	Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 C1A4h	MPC	PC4 Pin Function Control Register	PC4PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 C1A5h	MPC	PC5 Pin Function Control Register	PC5PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 C1A8h	MPC	PD0 Pin Function Control Register	PD0PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C1A9h	MPC	PD1 Pin Function Control Register	PD1PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C1AAh	MPC	PD2 Pin Function Control Register	PD2PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C1ABh	MPC	PD3 Pin Function Control Register	PD3PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C1ACh	MPC	PD4 Pin Function Control Register	PD4PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C1ADh	MPC	PD5 Pin Function Control Register	PD5PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C1AEh	MPC	PD6 Pin Function Control Register	PD6PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C1AFh	MPC	PD7 Pin Function Control Register	PD7PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C1B0h	MPC	PE0 Pin Function Control Register	PE0PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C1B1h	MPC	PE1 Pin Function Control Register	PE1PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C1B2h	MPC	PE2 Pin Function Control Register	PE2PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C1B3h	MPC	PE3 Pin Function Control Register	PE3PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C1B4h	MPC	PE4 Pin Function Control Register	PE4PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C1B5h	MPC	PE5 Pin Function Control Register	PE5PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C1BAh	MPC	PF2 Pin Function Control Register	PF2PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 100, 64, or 48 pins.
0008 C1BBh	MPC	PF3 Pin Function Control Register	PF3PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 100, 64, or 48 pins.
0008 C1C0h	MPC	PG0 Pin Function Control Register	PG0PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 100, 64, or 48 pins.
0008 C1C1h	MPC	PG1 Pin Function Control Register	PG1PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 100, 64, or 48 pins.
0008 C1C2h	MPC	PG2 Pin Function Control Register	PG2PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 100, 64, or 48 pins.
0008 C1C3h	MPC	PG3 Pin Function Control Register	PG3PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 100, 64, or 48 pins.
0008 C1C4h	MPC	PG4 Pin Function Control Register	PG4PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 100, 64, or 48 pins.
0008 C1C5h	MPC	PG5 Pin Function Control Register	PG5PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 100, 64, or 48 pins.
0008 C1C6h	MPC	PG6 Pin Function Control Register	PG6PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
0008 C1D0h	MPC	USB0_DPUPE Pin Function Control Register	UDPUPEPFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
0008 C280h	SYSTEM	Deep Standby Control Register	DPSBYCR	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption	
0008 C282h	SYSTEM	Deep Standby Interrupt Enable Register 0	DPSIER0	8	8	4, 5 PCLKB	2, 3 ICLK		
0008 C284h	SYSTEM	Deep Standby Interrupt Enable Register 2	DPSIER2	8	8	4, 5 PCLKB	2, 3 ICLK		
0008 C286h	SYSTEM	Deep Standby Interrupt Flag Register 0	DPSIFR0	8	8	4, 5 PCLKB	2, 3 ICLK		
0008 C288h	SYSTEM	Deep Standby Interrupt Flag Register 2	DPSIFR2	8	8	4, 5 PCLKB	2, 3 ICLK		
0008 C28Ah	SYSTEM	Deep Standby Interrupt Edge Register 0	DPSIEGR0	8	8	4, 5 PCLKB	2, 3 ICLK		
0008 C28Ch	SYSTEM	Deep Standby Interrupt Edge Register 2	DPSIEGR2	8	8	4, 5 PCLKB	2, 3 ICLK		
0008 C290h	SYSTEM	Reset Status Register 0	RSTSR0	8	8	4, 5 PCLKB	2, 3 ICLK	Resets	
0008 C291h	SYSTEM	Reset Status Register 1	RSTSR1	8	8	4, 5 PCLKB	2, 3 ICLK		

Table 4.1 List of I/O Registers (Address Order) (34/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
000C 120Fh	MTU	Timer Output Control Register 2A	TOCR2A	8	8	4, 5 PCLKA	2, 3 ICLK	MTU3	
000C 1210h	MTU3	Timer Counter	TCNT	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1212h	MTU4	Timer Counter	TCNT	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1214h	MTU	Timer Cycle Data Register A	TCDRA	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1216h	MTU	Timer Dead Time Data Register A	TDDRA	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1218h	MTU3	Timer General Register A	TGRA	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 121Ah	MTU3	Timer General Register B	TGRB	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 121Ch	MTU4	Timer General Register A	TGRA	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 121Eh	MTU4	Timer General Register B	TGRB	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1220h	MTU	Timer Subcounter A	TCNTSA	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1222h	MTU	Timer Cycle Buffer Register A	TCBRA	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1224h	MTU3	Timer General Register C	TGRC	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1226h	MTU3	Timer General Register D	TGRD	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1228h	MTU4	Timer General Register C	TGRC	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 122Ah	MTU4	Timer General Register D	TGRD	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 122Ch	MTU3	Timer Status Register	TSR	8	8, 16	4, 5 PCLKA	2, 3 ICLK		
000C 122Dh	MTU4	Timer Status Register	TSR	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1230h	MTU	Timer Interrupt Skipping Set Register 1A	TITCR1A	8	8, 16	4, 5 PCLKA	2, 3 ICLK		
000C 1231h	MTU	Timer Interrupt Skipping Counters 1A	TITCNT1A	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1232h	MTU	Timer Buffer Transfer Set Register A	TBTERA	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1234h	MTU	Timer dead time enable register A	TDERA	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1236h	MTU	Timer output level buffer register A	TOLBRA	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1238h	MTU3	Timer Buffer Operation Transfer Mode Register	TBTM	8	8, 16	4, 5 PCLKA	2, 3 ICLK		
000C 1239h	MTU4	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 123Ah	MTU	Timer Interrupt Skipping Mode Register A	TITMRA	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 123Bh	MTU	Timer Interrupt Skipping Set Register 2A	TITCR2A	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 123Ch	MTU	Timer Interrupt Skipping Counters 2A	TITCNT2A	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1240h	MTU4	Timer A/D Converter Start Request Control Register	TADCR	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1244h	MTU4	Timer A/D Converter Start Request Cycle Set Register A	TADCORA	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1246h	MTU4	Timer A/D Converter Start Request Cycle Set Register B	TADCORB	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1248h	MTU4	Timer A/D Converter Start Request Cycle Set Buffer Register A	TADCOBRA	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 124Ah	MTU4	Timer A/D Converter Start Request Cycle Set Buffer Register B	TADCOBRB	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1260h	MTU	Timer Waveform Control Register A	TWCRA	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1270h	MTU	Timer Mode Register 2A	TMDR2A	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1272h	MTU3	Timer General Register E	TGRE	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1274h	MTU4	Timer General Register E	TGRE	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1276h	MTU4	Timer General Register F	TGRF	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1280h	MTU	Timer Start Register A	TSTRA	8	8, 16	4, 5 PCLKA	2, 3 ICLK		
000C 1281h	MTU	Timer Synchronous Register A	TSYRA	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1282h	MTU	Timer Counter Synchronous Start Register	TCSYSTR	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1284h	MTU	Timer Read/Write Enable Register A	TRWERA	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1300h	MTU0	Timer Control Register	TCR	8	8, 16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1301h	MTU0	Timer Mode Register 1	TMDR1	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1302h	MTU0	Timer I/O Control Register H	TIORH	8	8, 16	4, 5 PCLKA	2, 3 ICLK		
000C 1303h	MTU0	Timer I/O Control Register L	TIORL	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1304h	MTU0	Timer Interrupt Enable Register	TIER	8	8, 16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1305h	MTU0	Timer Status Register	TSR	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1306h	MTU0	Timer Counter	TCNT	16	16	4, 5 PCLKA	2, 3 ICLK		

Table 5.3 DC Characteristics (2)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

The following relation applies when the USB is in use under condition 1 or condition 2: Vcc = PLLVcc = Vcc_USB = 3.0 to 3.6 V.

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output high voltage	All output pins (except for P52, P53, P60 to P65, P71 to P76, P90 to P95, and USB0_DPUPE)	V_{OH}	VCC – 0.5	—	—	V	I_{OH} = –1 mA
	P52, P53, and P60 to P65		AVCC – 0.5	—	—		I_{OH} = –1 mA
	USB0_DPUPE		VCC_USB – 0.5				I_{OH} = –1 mA
	P71 to P76, and P90 to P95		VCC – 1.0	—	—		I_{OH} = –5 mA
Output low voltage	All output pins (except for P71 to P76, P90 to P95, and RIIC pins)	V_{OL}	—	—	0.5	V	I_{OL} = 1.0 mA
	P71 to P76, and P90 to P95		—	—	1.1		I_{OL} = 15 mA
	RIIC pins		—	—	0.4		I_{OL} = 3 mA
			—	—	0.6		I_{OL} = 6 mA
Input leakage current	RES#, MD pin, EMLE, Port 4, Ports P50, P51, P54 to P57, and Port C	$\lvert I_{in} \rvert$	—	—	1.0	µA	V_{in} = 0 V, V_{in} = VCC
Three-state leakage current (off state)	Port 0, Port 1, Ports P20 to P24, Port 3, Ports P52, P53, Ports 6 to A, Ports PB0, PB3 to PB7, and Ports D to G	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	V_{in} = 0 V, V_{in} = VCC
	Ports P25, P26, PB1, and PB2		—	—	5.0		
Input capacitance	All output pins (except for P25, P26, PB1, and PB2)	C_{in}	—	—	15	pF	V_{in} = 0 V, f = 1 MHz, T_a = 25 ºC
	Ports P25, P26, PB1, and PB2		—	—	30		

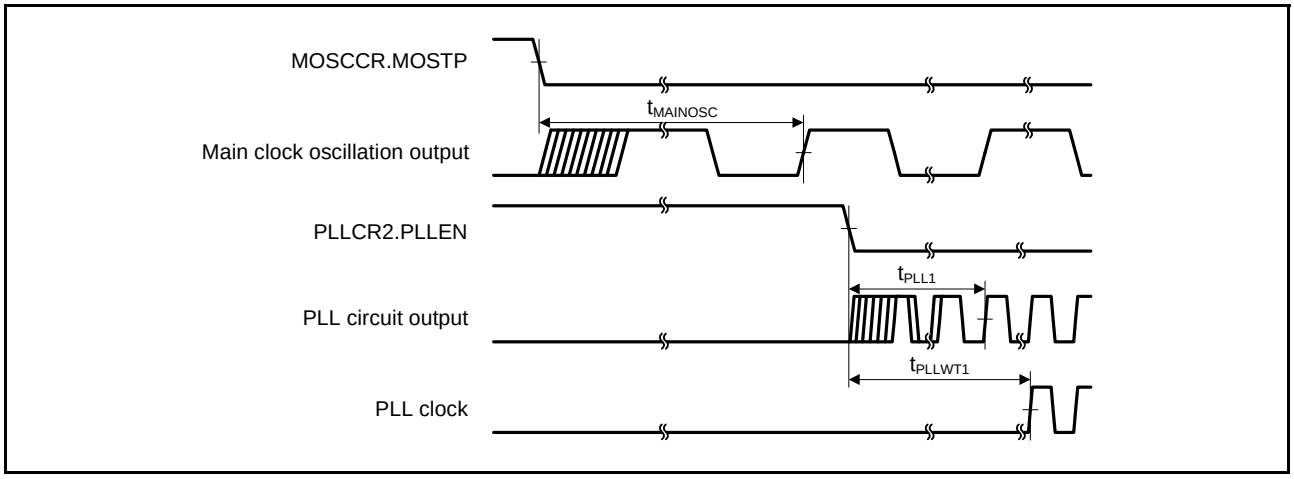


Figure 5.7 PLL Clock Oscillation Start Timing (PLL is Operated after Main Clock Oscillation Has Settled)

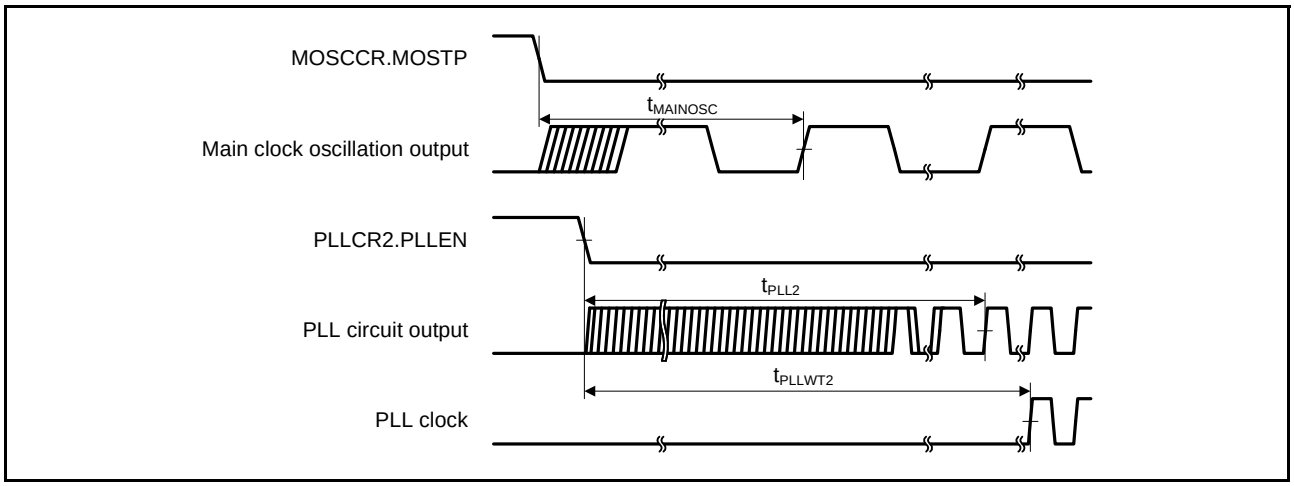


Figure 5.8 PLL Clock Oscillation Start Timing (PLL is Operated before Main Clock Oscillation Has Settled)

Table 5.16 Timing of On-Chip Peripheral Modules (3)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS =PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

High drive output is selected by the drive capacity control register.

Item				Symbol	Min.	Max.	Unit*1	Test Conditions
RSPI	RSPCK clock cycle	Master		t_{SPcyc}	2	4096	t_{Pcyc}	C = 30 pF, Figure 5.32
		Slave			8	4096		
	RSPCK clock high pulse width	Master		t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2 - 3$	—	ns	
		Slave			$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2$	—		
	RSPCK clock low pulse width	Master		t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2 - 3$	—	ns	
		Slave			$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2$	—		
	RSPCK clock rise/fall time	Output		t_{SPCKR}, t_{SPCKF}	—	5	ns	
		Input			—	1	µs	
	RSPCK clock fall time	Input		t_{SPCKF}	—	0.1	µs/V	
	Data input setup time	Master		t_{SU}	4	—	ns	C = 30 pF, Figure 5.33 to Figure 5.40
		Slave			$20 - t_{Pcyc}$	—		
	Data input hold time	Master	PCLKB division ratio set to a value other than 1/2	t_H	t_{Pcyc}	—	ns	
			PCLKB division ratio set to 1/2	t_{HF}	0	—		
		Slave		t_H	$20 + 2 \times t_{Pcyc}$	—		
	SSL setup time	Master		t_{LEAD}	1	8	t_{SPcyc}	
		Slave			4	—	t_{Pcyc}	
	SSL hold time	Master		t_{LAG}	1	8	t_{SPcyc}	
		Slave			4	—	t_{Pcyc}	
	Data output delay time	Master		t_{OD}	—	10	ns	
		Slave			—	$3 \times t_{Pcyc} + 40$		
	Data output hold time	Master		t_{OH}	0	—	ns	
		Slave			0	—		
	Successive transmission delay time	Master		t_{TD}	$t_{SPcyc} + 2 \times t_{Pcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	ns	
		Slave			$4 \times t_{Pcyc}$	—		
	MOSI and MISO rise/fall time	Output		t_{DR}, t_{DF}	—	5	ns	
		Input			—	1	µs	
	SSL rise/fall time	Output		t_{SSLr}, t_{SSLf}	—	15	ns	
		Input			—	1	µs	
	Slave access time			t_{SA}	—	4	t_{Pcyc}	Figure 5.39 and Figure 5.40
	Slave output release time			t_{REL}	—	3	t_{Pcyc}	

Note 1. t_{Pcyc}: PCLK cycle

Table 5.16 Timing of On-Chip Peripheral Modules (5)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item		Symbol	Min.*1,*2	Max.	Unit	Test Conditions
RIIC (Standard-mode)	SCL input cycle time	t_{SCL}	$6(12) \times t_{IICcyc} + 1300$	—	ns	Figure 5.36
	SCL input high pulse width	t_{SCLH}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	SCL input low pulse width	t_{SCLL}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	SCL, SDA input rise time	t_{Sr}	—	1000	ns	
	SCL, SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	$1(4) \times t_{IICcyc}$	ns	
	SDA input bus free time	t_{BUF}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	Start condition input hold time	t_{STAH}	$t_{IICcyc} + 300$	—	ns	
	Restart condition input setup time	t_{STAS}	1000	—	ns	
	Stop condition input setup time	t_{STOS}	1000	—	ns	
	Data input setup time	t_{SDAS}	$t_{IICcyc} + 50$	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
RIIC (Fast-mode)	SCL input cycle time	t_{SCL}	$6(12) \times t_{IICcyc} + 600$	—	ns	
	SCL input high pulse width	t_{SCLH}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	SCL input low pulse width	t_{SCLL}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	SCL, SDA input rise time	t_{Sr}	$20 + 0.1C_b$	300	ns	
	SCL, SDA input fall time	t_{Sf}	$20 + 0.1C_b$	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	$1(4) \times t_{IICcyc}$	ns	
	SDA input bus free time	t_{BUF}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	Start condition input hold time	t_{STAH}	$t_{IICcyc} + 300$	—	ns	
	Restart condition input setup time	t_{STAS}	300	—	ns	
	Stop condition input setup time	t_{STOS}	300	—	ns	
	Data input setup time	t_{SDAS}	$t_{IICcyc} + 50$	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note: • t_{IICcyc}: RIIC internal reference clock (IICϕ) cycle

Note 1. The value within parentheses is applicable when the value of the ICMR3.NF[1:0] bits is 11b while the digital filter is enabled by the setting ICFER.NFE = 1.

Note 2. Cb is the total capacitance of the bus lines.

Table 5.27 Power-on Reset Circuit and Voltage Detection Circuit Characteristics (2)

Condition: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0
$T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	V_{POR}	3.6	3.8	4.0	V	Figure 5.41
	Voltage detection circuit (LVD0)	V_{DET0}	4.0	4.2	4.4		Figure 5.42
	Voltage detection circuit (LVD1)*1	V_{DET1_8}	4.59	4.77	4.95		Figure 5.43
		V_{DET1_9}	4.05	4.23	4.41		
		V_{DET1_A}	4.32	4.50	4.68		
	Voltage detection circuit (LVD2)*2	V_{DET2_8}	4.59	4.77	4.95		Figure 5.44
		V_{DET2_9}	4.05	4.23	4.41		
		V_{DET2_A}	4.32	4.50	4.68		
Internal reset time	Power-on reset (POR)	t_{POR}		9.7		ms	Figure 5.41
	Voltage detection circuit (LVD0)	t_{LVD0}		9.7			Figure 5.42
	Voltage detection circuit (LVD1)	t_{LVD1}		0.9			Figure 5.43
	Voltage detection circuit (LVD2)	t_{LVD2}		0.9			Figure 5.44
Minimum VCC down time*3		t_{VOFF}	200	—	—	µs	Figure 5.41 to Figure 5.44
Response delay time		t_{DET}			200	µs	
LVD operation stabilization time (after LVD is enabled)		$Td_{(E-A)}$			3	µs	Figure 5.41 to Figure 5.44
Hysteresis width (LVD1 and LVD2)		V_{LVH}		80		mV	

Note 1. # in symbol $V_{DET1\_\#}$ indicates the value of the LVDLVLR.LVD1LVL[3:0] bits.
Note 2. # in symbol $V_{DET2\_\#}$ indicates the value of the LVDLVLR.LVD2LVL[3:0] bits.
Note 3. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{DET1}, and V_{DET2} for the POR/ LVD.

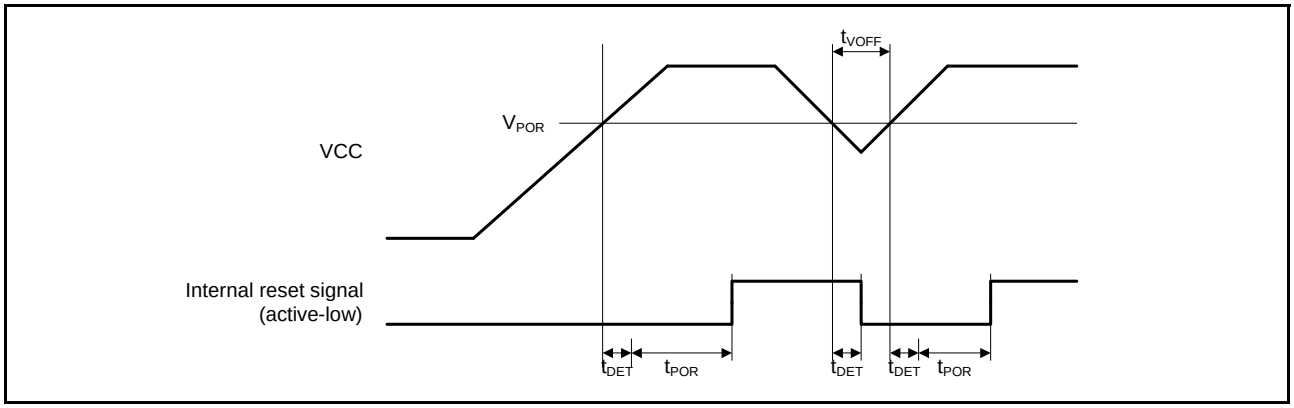


Figure 5.39 Power-on Reset Timing

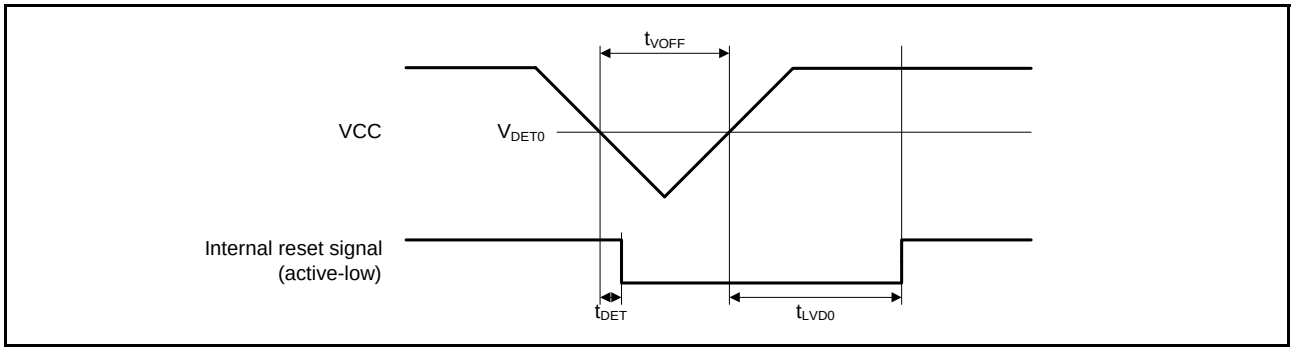


Figure 5.40 Voltage Detection Circuit Timing (V_{DET0})

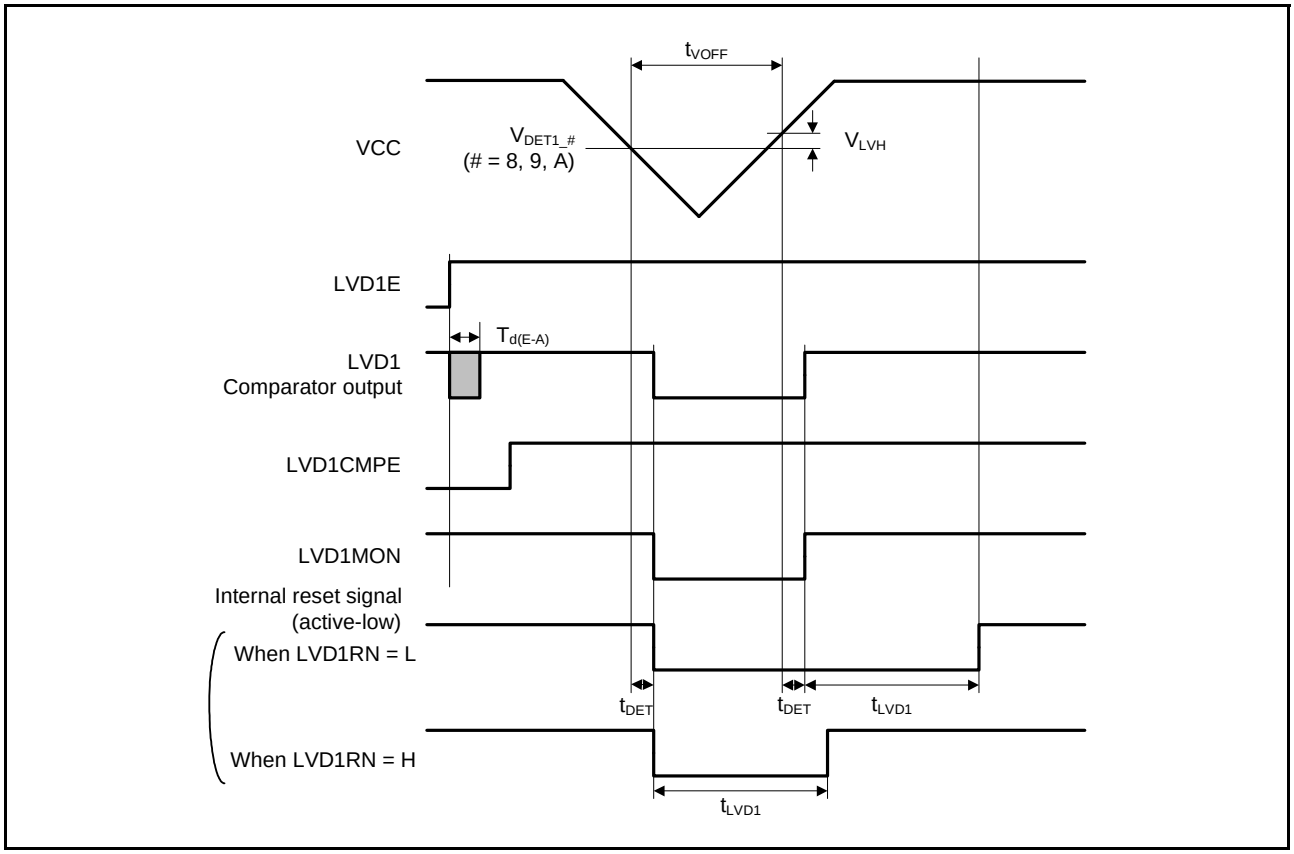


Figure 5.41 Voltage Detection Circuit Timing (V_{DET1})

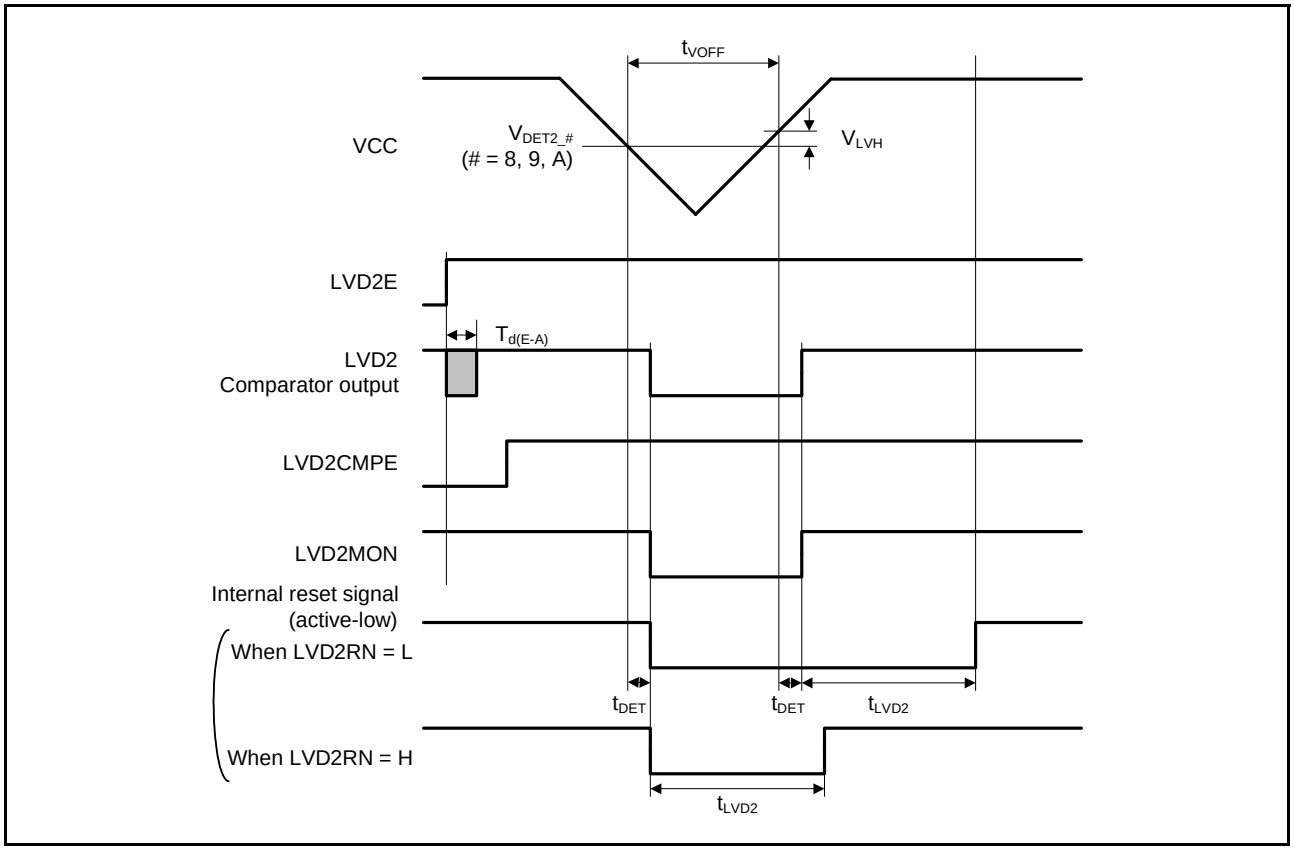


Figure 5.42 Voltage Detection Circuit Timing (V_{DET2})

6.3 AC Characteristics

Table 6.6 Operation Frequency Value

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item		Symbol	Min.	Typ	Max.	Unit
Operation frequency	System clock (ICLK)	f	—	—	100	MHz
	Peripheral module clock PCLK		—	—	50	
	Timer module clock (PCLKA)		—	—	100	
	S12AD clock (PCLKD)		—	—	50	
	Flash clock (FCLK)		—*1	—	50	

Note 1. The FCLK must run at a frequency of at least 4 MHz when changing the ROM or E2 DataFlash memory contents.

6.3.1 Clock Timing

Table 6.7 Clock Timing

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item		Symbol	Min	Typ	Max.	Unit	Test Conditions
EXTAL external clock input cycle time		t_{EXcyc}	50	—	—	ns	Figure 6.1
EXTAL external clock input high pulse width		t_{EXH}	20	—	—	ns	
EXTAL external clock input low pulse width		t_{EXL}	20	—	—	ns	
EXTAL external clock rising time		t_{EXr}	—	—	5	ns	
EXTAL external clock falling time		t_{EXf}	—	—	5	ns	
EXTAL external clock input wait time*1		t_{EXWT}	1	—	—	ms	
Main clock oscillator oscillation frequency		f_{MAIN}	4	—	16	MHz	
Main clock oscillation stabilization time (crystal)		$t_{MAINOSC}$	—	—	—*2	ms	Figure 6.2
Main clock oscillation stabilization wait time (crystal)		$t_{MAINOSCWT}$	—	—	—*3	ms	
LOCO, IWDTCLK clock cycle time		t_{cyc}	6.96	8	9.4	µs	
LOCO, IWDTCLK clock oscillation frequency		f_{LOCO}	106.25	125	143.75	kHz	
LOCO, IWDTCLK clock oscillation stabilization wait time		t_{LOCOWT}	—	—	20	µs	Figure 6.2
PLL clock oscillation stabilization time	PLL operation started after main clock oscillation has settled	t_{PLL1}	—	—	500	µs	Figure 6.4
PLL clock oscillation stabilization wait time		t_{PLLWT1}	—	—	—*4	ms	
PLL clock oscillation stabilization time PLL	PLL operation started before main clock oscillation has settled	t_{PLL2}	—	—	$t_{MAINOSC}$ + t_{PLL1}	ms	Figure 6.5
PLL clock oscillation stabilization wait time		t_{PLLWT2}	—	—	—*4	ms	

Note 1. This is the time until the clock is used after clearing the main clock oscillator stop bit (MOSCCR.MOSTP) to 0 (selecting operation).
Note 2. When using a main clock, ask the manufacturer of the oscillator to evaluate its oscillation. Refer to the results of evaluation provided by the manufacturer for the oscillation stabilization time.
Note 3. This is calculated from the formula below, where n is the number of cycles set by the MOSCWTCR.MSTS[4:0] bits.

$$t_{MAINOSCWT} = t_{MAINOSC} + \frac{n + 16384}{f_{MAIN}}$$

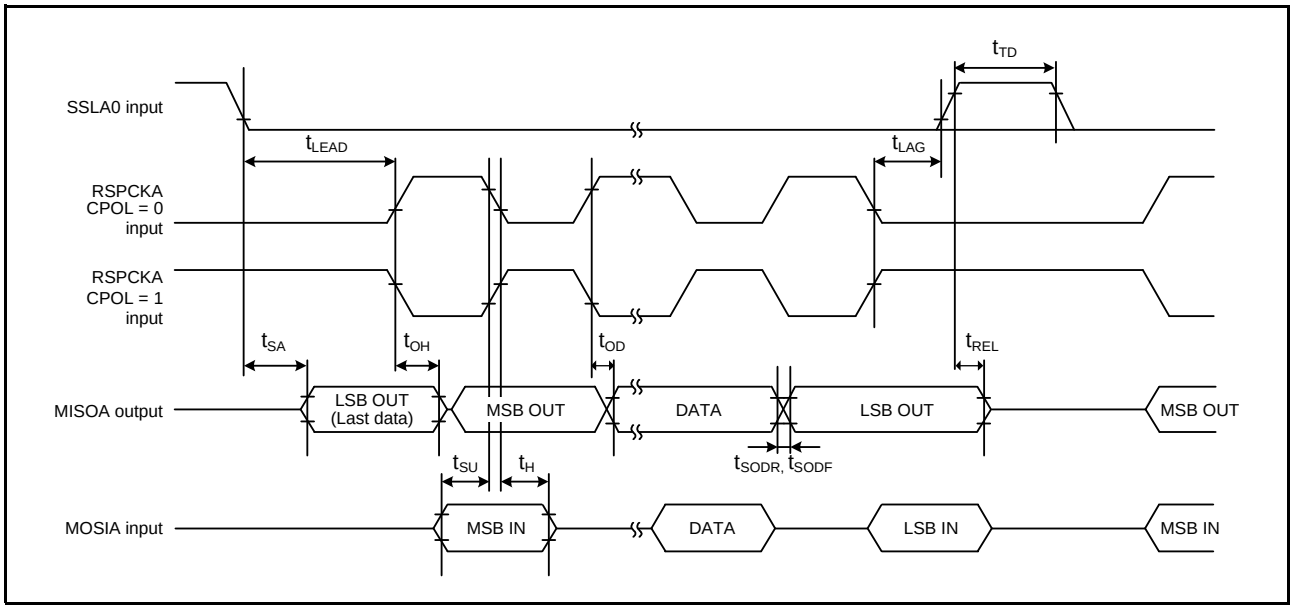
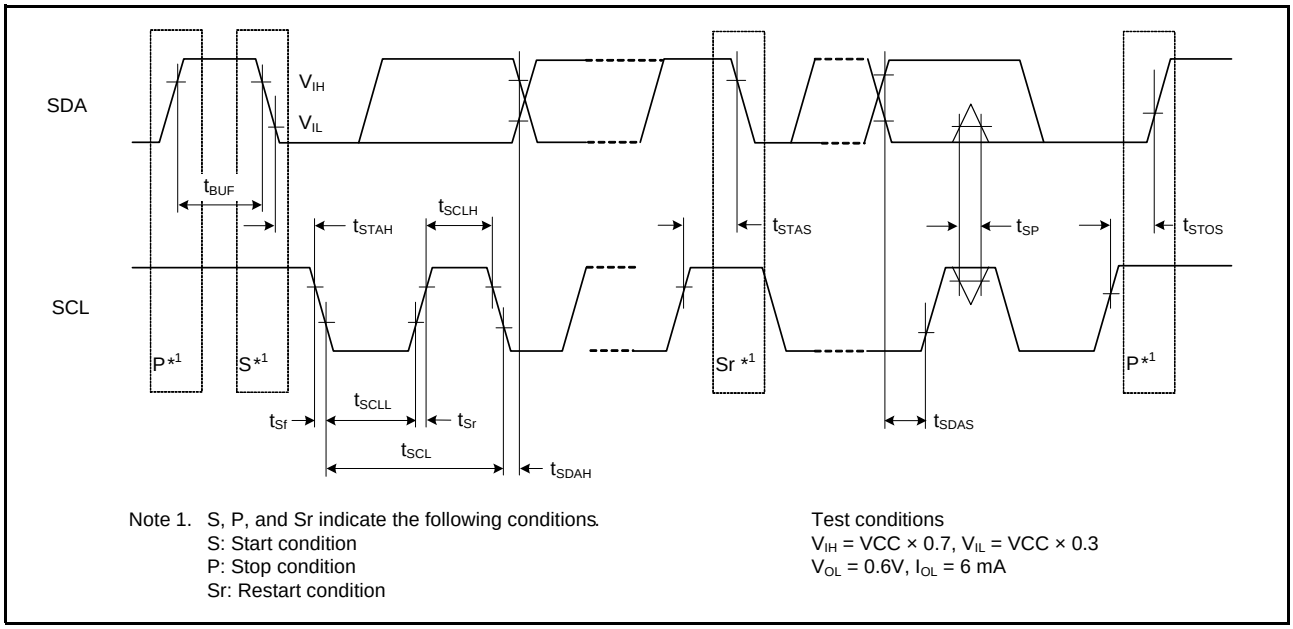


Figure 6.24 RSPI Timing (Slave, CPHA = 1) and Simple SPI Timing (Slave, CKPH = 0)

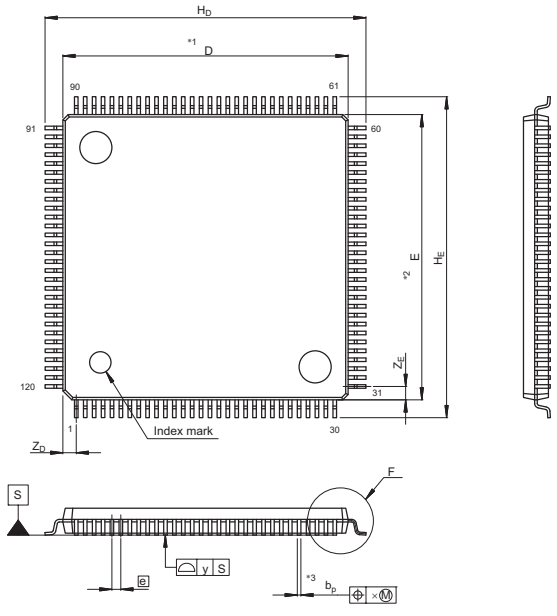


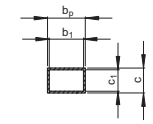
Note 1. S, P, and Sr indicate the following conditions.
S: Start condition
P: Stop condition
Sr: Restart condition

Test conditions
V_{IH} = VCC × 0.7, V_{IL} = VCC × 0.3
V_{OL} = 0.6V, I_{OL} = 6 mA

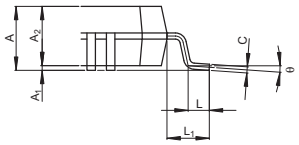
Figure 6.25 RIIC Bus Interface Input/Output Timing and Simple IIC Bus Interface Input/Output Timing

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP120-16x16-0.50	PLQP0120KA-A	—	0.9g





Terminal cross section



Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	15.9	16.0	16.1
E	15.9	16.0	16.1
A_2	—	1.4	—
H_D	17.8	18.0	18.2
H_E	17.8	18.0	18.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.17	0.22	0.27
b_1	—	0.20	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	0.75	—
Z_E	—	0.75	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure B 120-Pin LQFP (PLQP0120KA-A)

REVISION HISTORY — RX63T Group Datasheet

Rev.	Date	Description	
		Page	Summary
1.00	Aug 28, 2012	—	First Edition issued
2.00	Mar 11, 2013	Features	
		1	Changed
		1. Overview	
		2	1.1 Outline of Specifications, description changed
		2 to 8	Table 1.1 Outline of Specifications, changed
		9	Table 1.2 Comparison of Functions for Different Packages, changed
		10 to 12	Table 1.3 List of Products, changed
		12	Figure 1.1 How to Read the Product Part Number, changed
		13	Figure 1.2 Block Diagram, changed
		14 to 18	Table 1.4 Pin Functions, changed
		19	Figure 1.3 Pin Assignment (144-Pin LQFP), added
		20	Figure 1.4 Pin Assignment (120-Pin LQFP), added
		21	Figure 1.5 Pin Assignment (112-Pin LQFP), added
		22	Figure 1.6 Pin Assignment (100-Pin LQFP), added
		23	Figure 1.7 Pin Assignment (64-Pin LQFP), notes changed
		24	Figure 1.8 Pin Assignment (48-Pin LQFP), notes changed
		25 to 28	Table 1.5 List of Pins and Pin Functions (144-Pin LQFP), added
		29 to 32	Table 1.6 List of Pins and Pin Functions (120-Pin LQFP), added
		33 to 36	Table 1.7 List of Pins and Pin Functions (112-Pin LQFP), added
		37 to 39	Table 1.8 List of Pins and Pin Functions (100-Pin LQFP), added
		3. Address Space	
		49	Figure 3.1 Memory Map in Each Operating Mode, changed
		50	3.2 External Address Space, added
		4. I/O Registers	
		52	(3) Number of Access Cycles to I/O Registers, description changed
		53 to 103	Table 4.1 List of I/O Registers (Address Order), changed
		5. Electrical Characteristics [144-, 120-, 112- and 100-Pin Versions]	
		104 to 148	Added
		6. Electrical Characteristics [64- and 48-Pin Versions]	
		149	Title changed
		152	Table 6.6 Clock Timing, changed
		158	Table 6.10 Timing of On-Chip Peripheral Modules (1), changed
		160	Table 6.12 Timing of On-Chip Peripheral Modules (3), changed
		170	6.6 Oscillation Stop Detection Circuit Characteristics, title changed
		170	Table 6.18 Oscillation Stop Detection Circuit Characteristics, title changed
		171	Table 6.19 ROM (Flash Memory for Code Storage) Characteristics (1), added
		171	Table 6.20 ROM (Flash Memory for Code Storage) Characteristics (2), title and description changed
		172	Table 6.21 DataFlash (Flash Memory for Data Storage) Characteristics (1), added
		172	Table 6.22 DataFlash (Flash Memory for Data Storage) Characteristics (2), title and description changed
		Appendix 1. Package Dimensions	
		174 to 177	Figure A 144-Pin LQFP (PLQP0144KA-A) to Figure D 100-Pin LQFP (PLQP0100KB-A), added
2.10	Sep 26, 2013	The RX63T Group and RX63T changed to this MCU	
		Features	
		1	Changed
		1. Overview	
		2 to 8	Table 1.1 Outline of Specifications, changed, Note 1, added.
		9	Table 1.2 Comparison of Functions for Different Packages, changed, Note 2, added.
		10 to 14	Table 1.3 List of Products, changed, Note 1, added
		15	Figure 1.1 How to Read the Product Part Number, changed
		28 to 31	Table 1.5 List of Pins and Pin Functions (144-Pin LQFP), changed
		32 to 35	Table 1.6 List of Pins and Pin Functions (120-Pin LQFP), changed

Rev.	Date	Description	
		Page	Summary
2.10	Sep 26, 2013	36 to 39	Table 1.7 List of Pins and Pin Functions (112-Pin LQFP), changed
		40 to 42	Table 1.8 List of Pins and Pin Functions (100-Pin LQFP), changed
		43 to 45	Table 1.9 List of Pins and Pin Functions (64-Pin LQFP), changed
		46 to 47	Table 1.10 List of Pins and Pin Functions (48-Pin LQFP), changed
		4. I/O Registers	
		56 to 103	Table 4.1 List of I/O Registers (Address Order), changed
		5. Electrical Characteristics [144-, 120-, 112- and 100-Pin Versions]	
		104	Table 5.1 Absolute Maximum Ratings, changed
		107	Table 5.4 DC Characteristics (3), Note 7, deleted
		108	Table 5.6 Permissible Power Consumption, added
		128	5.3.7 Timing of PWM Delay Generation Circuit, added
		128	Table 42.21 Timing of the PWM Delay Generation Circuit, added
		132	Figure 5.32 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKB Division Ratio Set to a Value Other Than 1/2) and Simple SPI Timing (Master, CKPH = 1), changed
		133	Figure 5.34 RSPI Timing (Slave, CPHA = 0) and Simple SPI Timing (Slave, CKPH = 0), changed
		134	Figure 5.35 RSPI Timing (Slave, CPHA = 1) and Simple SPI Timing (Slave, CKPH = 1), changed
		6. Electrical Characteristics [64- and 48-Pin Versions]	
		149	Table 6.1 Absolute Maximum Ratings, changed
		151	Table 6.3 DC Characteristics (2), Note 3, changed
		152	Table 6.5 Permissible Power Consumption, added