Renesas Electronics America Inc - R5F563TCDDFH#V0 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	EBI/EMI, I²C, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	69
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x10b, 8x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f563tcddfh-v0

Table 1.1 Outline of Specifications (7/7)

Classification	Module/Function	Description
Operating temperature		D version: -40 to +85°C, G version: -40 to +105°C *1
Package		144-pin LQFP (PLQP0144KA-A (20 × 20, 0.5-mm pitch)) 120-pin LQFP (PLQP0120KA-A (16 × 16, 0.5-mm pitch)) 112-pin LQFP (PLQP0112JA-A (20 × 20, 0.65-mm pitch)) 100-pin LQFP (PLQP0100KB-A (14 × 14, 0.5-mm pitch)) 64-pin LQFP (PLQP0064KB-A (10 × 10, 0.5-mm pitch)) 48-pin LQFP (PLQP0048KB-A (07 × 07, 0.5-mm pitch))
On-chip debugging system		• E1 emulator (JTAG and FINE interfaces) • E20 emulator (JTAG interface)

Note 1. Please contact Renesas Electronics sales office for derating of operation under Ta = +85°C to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.

Table 1.4 Pin Functions (4/5)

Classifications	Pin Name	I/O	Description
USB 2.0 host/function module	VCC_USB	Input	Power supply pin for USB
	VSS_USB	Input	Ground pin for USB
	USB0_DP	I/O	USB internal transceiver D + input and output pins
	USB0_DM	I/O	USB internal transceiver D - input and output pins
	USB0_EXICEN	Output	Low power control signal for OTG chip
	USB0_VBUSEN	Output	Supply enable signal of VBUS (5 V) to OTG chip
	USB0_ID	Input	Mini AB connector ID input pin for use in OTG operation
	USB0_DPRPD	Output	D+ signal pull-down control pin for use during host operation
	USB0_DRPD	Output	D- signal pull-down control pin for use during host operation
	USB0_DPUPE	Output	D+ signal pull-up control pin for use during function operation
	USB0_VBUS	Input	Pin for monitoring USB cable connection
	USB0_OVRCURA, USB0_OVRCURB	Input	Pin for detecting external over current
CAN module	CRX1	Input	Input pins
	CTX1	Output	Output pins
Serial peripheral interface	RSPCKA, RSPCKB	I/O	Clock input/output pins
	MOSIA, MOSIB	I/O	Inputs or outputs data output from the master
	MISOA, MISOB	I/O	Inputs or outputs data output from the slave
	SSLA0, SSLB0	I/O	Input or output pins for slave selection
	SSLA1 to SSLA3 SSLB1 to SSLB3	Output	Output pins for slave selection
12-bit A/D converter	AN000 to AN007 AN100 to AN103	Input	Input pins for the analog signals to be processed by the A/D converter
	ADTRG0#, ADTRG1#	Input	Input pins for the external trigger signals that start the A/D conversion
	CVREFH	Input	Input pin for the high-level reference voltage to the comparator
	CVREFL	Input	Input pin for the low-level reference voltage to the comparator
10-bit A/D converter	AN0 to AN19	Input	Input pins for the analog signals to be processed by the 10-bit A/D converter
	ADTRG#	Input	Input pins for the external trigger signals that start the A/D conversion
D/A converter	DA0, DA1	Output	Output pins for the analog signals to be processed by the 10-bit A/D converter
Analog power supply	AVCC0	—	Analog voltage supply pin for the 12-bit A/D converter. Connect this pin to VCC if the 12-bit A/D converter is not to be used
	AVSS0	—	Analog ground pin for the 12-bit A/D converter. Connect this pin to VSS if the 12-bit A/D converter is not to be used
	VREFH0	—	Reference voltage supply pin for the 12-bit A/D converter. Connect this pin to VCC if the 12-bit A/D converter is not to be used
	VREFL0	—	Reference ground pin for the 12-bit A/D converter. Connect this pin to VSS if the 12-bit A/D converter is not to be used
	AVCC	—	Analog voltage supply pin for the 10-bit A/D converter and the 10-bit D/A converter. Connect this pin to the power supply of the system if the A/D converter and the D/A converter are not to be used.
	AVSS	—	Ground pin for the 10-bit A/D converter and 10-bit D/A converter. Connect this pin to the power-supply ground for the system (0 V).
	VREF	—	Reference-voltage input pin for the 10-bit A/D converter and the 10-bit D/A converter. Connect this pin to the power supply for the system if the A/D converter and the D/A converter are not to be used.

Table 1.9 List of Pins and Pin Functions (64-Pin LQFP) (1/3)

Pin Number 64-Pin LQFP	Power Supply Clock System Control	I/O Port	POE3	Timer (MTU3, GPT, CAC)	Communications (SCIc, SCId)	Communications (RSPI, RIIC)	Interrupt	S12ADB
1	EMLE							
2		P00		GTIOC3A	CTS0# RTS0# SS0#		IRQ2-DS	
3	VCL							
4		P01		GTIOC3B CACREF			IRQ4-DS	
5	MD FINED							
6	RES#							
7	XTAL							
8	VSS							
9	EXTAL							
10	VCC							
11		PE2	POE10#				NMI	
12	TRST#	PD7		GTIOC0A	CTS0# RTS0# SS0#			
13	TMS	PD6		GTIOC0B				
14	TDI	PD5		GTIOC1A	RXD1 SMISO1 SSCL1			
15	TCK FINEC	PD4		GTIOC1B	SCK1			
16	TDO	PD3		GTIOC2A	TXD1 SMOSI1 SSDA1			
17		PB7		GTIOC2B	SCK12			
18		PB6		GTIOC2B	RXD12 SMISO12 SSCL12 RXDX12			
19		PB5	POE11#		TXD12 SMOSI12 SSDA12 TXDX12 SIOX12		IRQ0	
20	VCC							
21		PB4	POE8#	GTETRG	CTS12# RTS12# SS12#		IRQ3-DS	
22	VSS							
23		PB3		MTIOC0A MTCLKA CACREF	SCK0			
24		PB2		MTIOC0B MTCLKB	TXD0 SMOSI0 SSDA0	SDA		
25		PB1		MTIOC0C	RXD0 SMISO0 SSCL0	SCL		
26		PB0		MTIOC0D		MOSIA		

3. Address Space

3.1 Address Space

This MCU has a 4-Gbyte address space, consisting of the range of addresses from 0000 0000h to FFFF FFFFh. That is, linear access to an address space of up to 4 Gbytes is possible, and this contains both program and data areas.
Figure 3.1 shows the memory maps in the respective operating modes. Accessible areas will differ according to the operating mode and states of control bits.

Table 4.1 List of I/O Registers (Address Order) (13/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 739Ah	ICU	Interrupt Source Priority Register 154	IPR154	8	8	2 ICLK		ICUb	
0008 739Eh	ICU	Interrupt Source Priority Register 158	IPR158	8	8	2 ICLK			
0008 73A1h	ICU	Interrupt Source Priority Register 161	IPR161	8	8	2 ICLK			
0008 73A3h	ICU	Interrupt Source Priority Register 163	IPR163	8	8	2 ICLK			
0008 73A5h	ICU	Interrupt Source Priority Register 165	IPR165	8	8	2 ICLK			
0008 73A6h	ICU	Interrupt Source Priority Register 166	IPR166	8	8	2 ICLK			
0008 73ABh	ICU	Interrupt Source Priority Register 171	IPR171	8	8	2 ICLK			
0008 73ACh	ICU	Interrupt Source Priority Register 172	IPR172	8	8	2 ICLK			
0008 73ADh	ICU	Interrupt Source Priority Register 173	IPR173	8	8	2 ICLK			
0008 73AEh	ICU	Interrupt Source Priority Register 174	IPR174	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 73B1h	ICU	Interrupt Source Priority Register 177	IPR177	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 73B4h	ICU	Interrupt Source Priority Register 180	IPR180	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 73B7h	ICU	Interrupt Source Priority Register 183	IPR183	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 73B9h	ICU	Interrupt Source Priority Register 185	IPR185	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 73BCh	ICU	Interrupt Source Priority Register 188	IPR188	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 73BEh	ICU	Interrupt Source Priority Register 190	IPR190	8	8	2 ICLK			Not present in versions with 112, 100, 64 or 48 pins.
0008 73C2h	ICU	Interrupt Source Priority Register 194	IPR194	8	8	2 ICLK			
0008 73C6h	ICU	Interrupt Source Priority Register 198	IPR198	8	8	2 ICLK			
0008 73C7h	ICU	Interrupt Source Priority Register 199	IPR199	8	8	2 ICLK			
0008 73C8h	ICU	Interrupt Source Priority Register 200	IPR200	8	8	2 ICLK			
0008 73C9h	ICU	Interrupt Source Priority Register 201	IPR201	8	8	2 ICLK			
0008 73D6h	ICU	Interrupt Source Priority Register 214	IPR214	8	8	2 ICLK			
0008 73D9h	ICU	Interrupt Source Priority Register 217	IPR217	8	8	2 ICLK			
0008 73DCh	ICU	Interrupt Source Priority Register 220	IPR220	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 73DFh	ICU	Interrupt Source Priority Register 223	IPR223	8	8	2 ICLK			Not present in versions with 100, 64 or 48 pins.
0008 73E2h	ICU	Interrupt Source Priority Register 226	IPR226	8	8	2 ICLK			
0008 73E5h	ICU	Interrupt Source Priority Register 229	IPR229	8	8	2 ICLK			
0008 73E8h	ICU	Interrupt Source Priority Register 232	IPR232	8	8	2 ICLK			
0008 73EBh	ICU	Interrupt Source Priority Register 235	IPR235	8	8	2 ICLK			
0008 73EEh	ICU	Interrupt Source Priority Register 238	IPR238	8	8	2 ICLK			
0008 73F1h	ICU	Interrupt Source Priority Register 241	IPR241	8	8	2 ICLK			
0008 73F4h	ICU	Interrupt Source Priority Register 244	IPR244	8	8	2 ICLK			
0008 73F7h	ICU	Interrupt Source Priority Register 247	IPR247	8	8	2 ICLK			
0008 73FAh	ICU	Interrupt Source Priority Register 250	IPR250	8	8	2 ICLK			
0008 7400h	ICU	DMAC Activation Request Select Register 0	DMRSR0	8	8	2 ICLK			
0008 7404h	ICU	DMAC Activation Request Select Register 1	DMRSR1	8	8	2 ICLK			
0008 7408h	ICU	DMAC Activation Request Select Register 2	DMRSR2	8	8	2 ICLK			
0008 740Ch	ICU	DMAC Activation Request Select Register 3	DMRSR3	8	8	2 ICLK			
0008 7500h	ICU	IRQ Control Register 0	IRQCR0	8	8	2 ICLK			
0008 7501h	ICU	IRQ Control Register 1	IRQCR1	8	8	2 ICLK			
0008 7502h	ICU	IRQ Control Register 2	IRQCR2	8	8	2 ICLK			
0008 7503h	ICU	IRQ Control Register 3	IRQCR3	8	8	2 ICLK			
0008 7504h	ICU	IRQ Control Register 4	IRQCR4	8	8	2 ICLK			
0008 7505h	ICU	IRQ Control Register 5	IRQCR5	8	8	2 ICLK			
0008 7506h	ICU	IRQ Control Register 6	IRQCR6	8	8	2 ICLK			Not present in versions with 64 or 48 pins.

Table 4.1 List of I/O Registers (Address Order) (27/48)

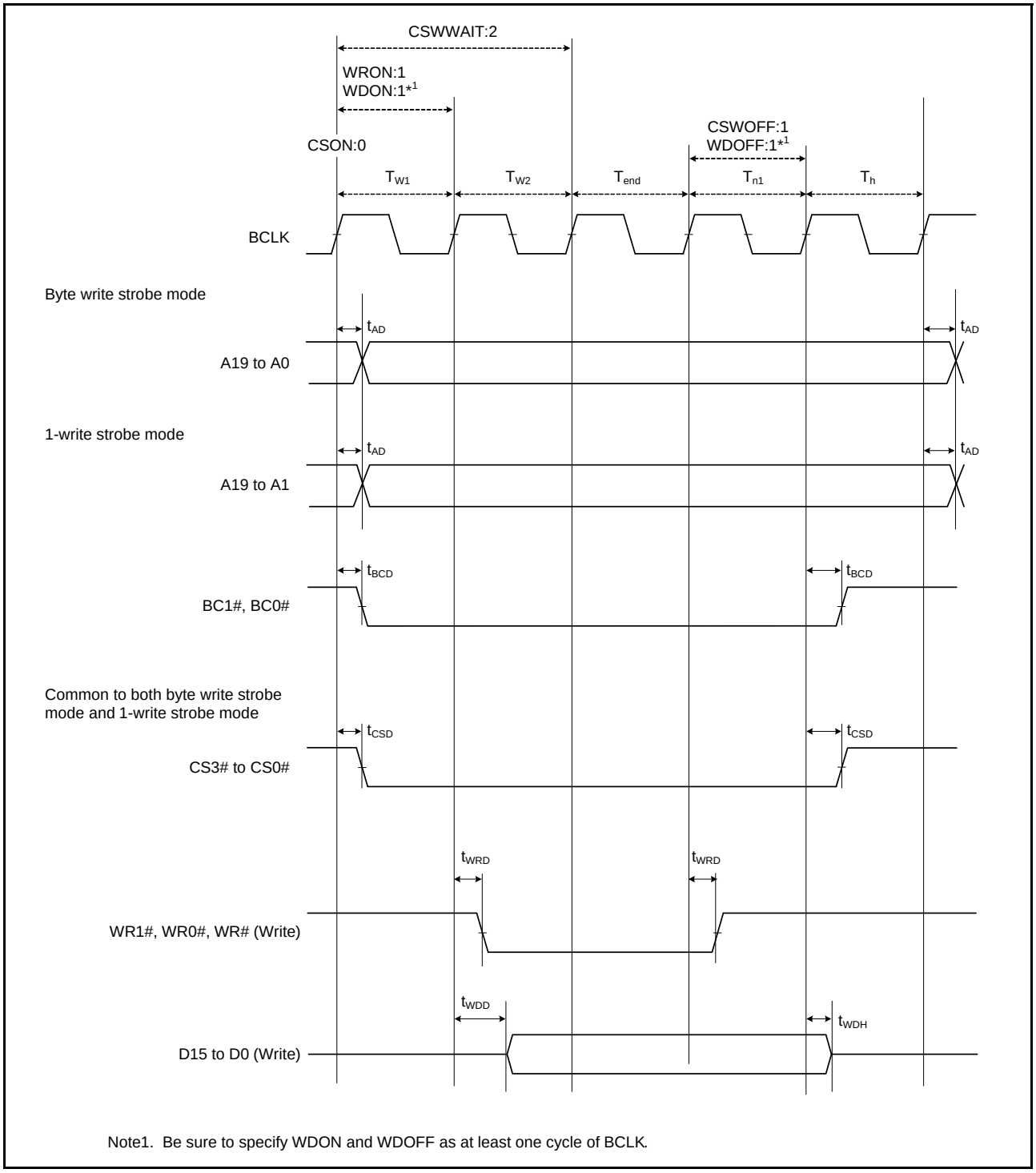
Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 C1A3h	MPC	PC3 Pin Function Control Register	PC3PFS	8	8	2, 3 PCLKB	2 ICLK	MPC	Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 C1A4h	MPC	PC4 Pin Function Control Register	PC4PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 C1A5h	MPC	PC5 Pin Function Control Register	PC5PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 C1A8h	MPC	PD0 Pin Function Control Register	PD0PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C1A9h	MPC	PD1 Pin Function Control Register	PD1PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C1AAh	MPC	PD2 Pin Function Control Register	PD2PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C1ABh	MPC	PD3 Pin Function Control Register	PD3PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C1ACh	MPC	PD4 Pin Function Control Register	PD4PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C1ADh	MPC	PD5 Pin Function Control Register	PD5PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C1AEh	MPC	PD6 Pin Function Control Register	PD6PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C1AFh	MPC	PD7 Pin Function Control Register	PD7PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C1B0h	MPC	PE0 Pin Function Control Register	PE0PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C1B1h	MPC	PE1 Pin Function Control Register	PE1PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C1B2h	MPC	PE2 Pin Function Control Register	PE2PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C1B3h	MPC	PE3 Pin Function Control Register	PE3PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C1B4h	MPC	PE4 Pin Function Control Register	PE4PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C1B5h	MPC	PE5 Pin Function Control Register	PE5PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C1BAh	MPC	PF2 Pin Function Control Register	PF2PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 100, 64, or 48 pins.
0008 C1BBh	MPC	PF3 Pin Function Control Register	PF3PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 100, 64, or 48 pins.
0008 C1C0h	MPC	PG0 Pin Function Control Register	PG0PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 100, 64, or 48 pins.
0008 C1C1h	MPC	PG1 Pin Function Control Register	PG1PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 100, 64, or 48 pins.
0008 C1C2h	MPC	PG2 Pin Function Control Register	PG2PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 100, 64, or 48 pins.
0008 C1C3h	MPC	PG3 Pin Function Control Register	PG3PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 100, 64, or 48 pins.
0008 C1C4h	MPC	PG4 Pin Function Control Register	PG4PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 100, 64, or 48 pins.
0008 C1C5h	MPC	PG5 Pin Function Control Register	PG5PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 100, 64, or 48 pins.
0008 C1C6h	MPC	PG6 Pin Function Control Register	PG6PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
0008 C1D0h	MPC	USB0_DPUPE Pin Function Control Register	UDPUPEPFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
0008 C280h	SYSTEM	Deep Standby Control Register	DPSBYCR	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption	
0008 C282h	SYSTEM	Deep Standby Interrupt Enable Register 0	DPSIER0	8	8	4, 5 PCLKB	2, 3 ICLK		
0008 C284h	SYSTEM	Deep Standby Interrupt Enable Register 2	DPSIER2	8	8	4, 5 PCLKB	2, 3 ICLK		
0008 C286h	SYSTEM	Deep Standby Interrupt Flag Register 0	DPSIFR0	8	8	4, 5 PCLKB	2, 3 ICLK		
0008 C288h	SYSTEM	Deep Standby Interrupt Flag Register 2	DPSIFR2	8	8	4, 5 PCLKB	2, 3 ICLK		
0008 C28Ah	SYSTEM	Deep Standby Interrupt Edge Register 0	DPSIEGR0	8	8	4, 5 PCLKB	2, 3 ICLK		
0008 C28Ch	SYSTEM	Deep Standby Interrupt Edge Register 2	DPSIEGR2	8	8	4, 5 PCLKB	2, 3 ICLK		
0008 C290h	SYSTEM	Reset Status Register 0	RSTSR0	8	8	4, 5 PCLKB	2, 3 ICLK	Resets	
0008 C291h	SYSTEM	Reset Status Register 1	RSTSR1	8	8	4, 5 PCLKB	2, 3 ICLK		

Table 4.1 List of I/O Registers (Address Order) (30/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
000A 002Eh	USB0	D1FIFO Port Control Register	D1FIFOCTR	16	16	3, 4 PCLKB	2, 3 ICLK	USBa	Not present in versions with 112, 100, 64, or 48 pins.
000A 0030h	USB0	Interrupt Enable Register 0	INTENB0	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 0032h	USB0	Interrupt Enable Register 1	INTENB1	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 0036h	USB0	BRDY Interrupt Enable Register	BRDYENB	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 0038h	USB0	NRDY Interrupt Enable Register	NRDYENB	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 003Ah	USB0	BEMP Interrupt Enable Register	BEMPENB	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 003Ch	USB0	SOF Output Configuration Register	SOFCFG	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 0040h	USB0	Interrupt Status Register 0	INTSTS0	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 0042h	USB0	Interrupt Status Register 1	INTSTS1	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 0046h	USB0	BRDY Interrupt Status Register	BRDYSTS	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 0048h	USB0	NRDY Interrupt Status Register	NRDYSTS	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 004Ah	USB0	BEMP Interrupt Status Register	BEMPSTS	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.

Table 4.1 List of I/O Registers (Address Order) (31/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
000A 004Ch	USB0	Frame Number Register	FRMNUM	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1	USBa	Not present in versions with 112, 100, 64, or 48 pins.
000A 004Eh	USB0	Device State Change Register	DVCHGR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 0050h	USB0	USB Address Register	USBADDR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 0054h	USB0	USB Request Type Register	USBREQ	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 0056h	USB0	USB Request Value Register	USBVAL	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 0058h	USB0	USB Request Index Register	USBINDX	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 005Ah	USB0	USB Request Length Register	USBLENG	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 005Ch	USB0	DCP Configuration Register	DCPCFG	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 005Eh	USB0	DCP Maximum Packet Size Register	DCPMAXP	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 0060h	USB0	DCP Control Register	DCPCTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 0064h	USB0	Pipe Window Select Register	PIPESEL	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 0068h	USB0	Pipe Configuration Register	PIPECFG	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.



Note1. Be sure to specify WDON and WDOFF as at least one cycle of BCLK.

Figure 5.14 External Bus Timing/Normal Write Cycle (Bus Clock Synchronized)

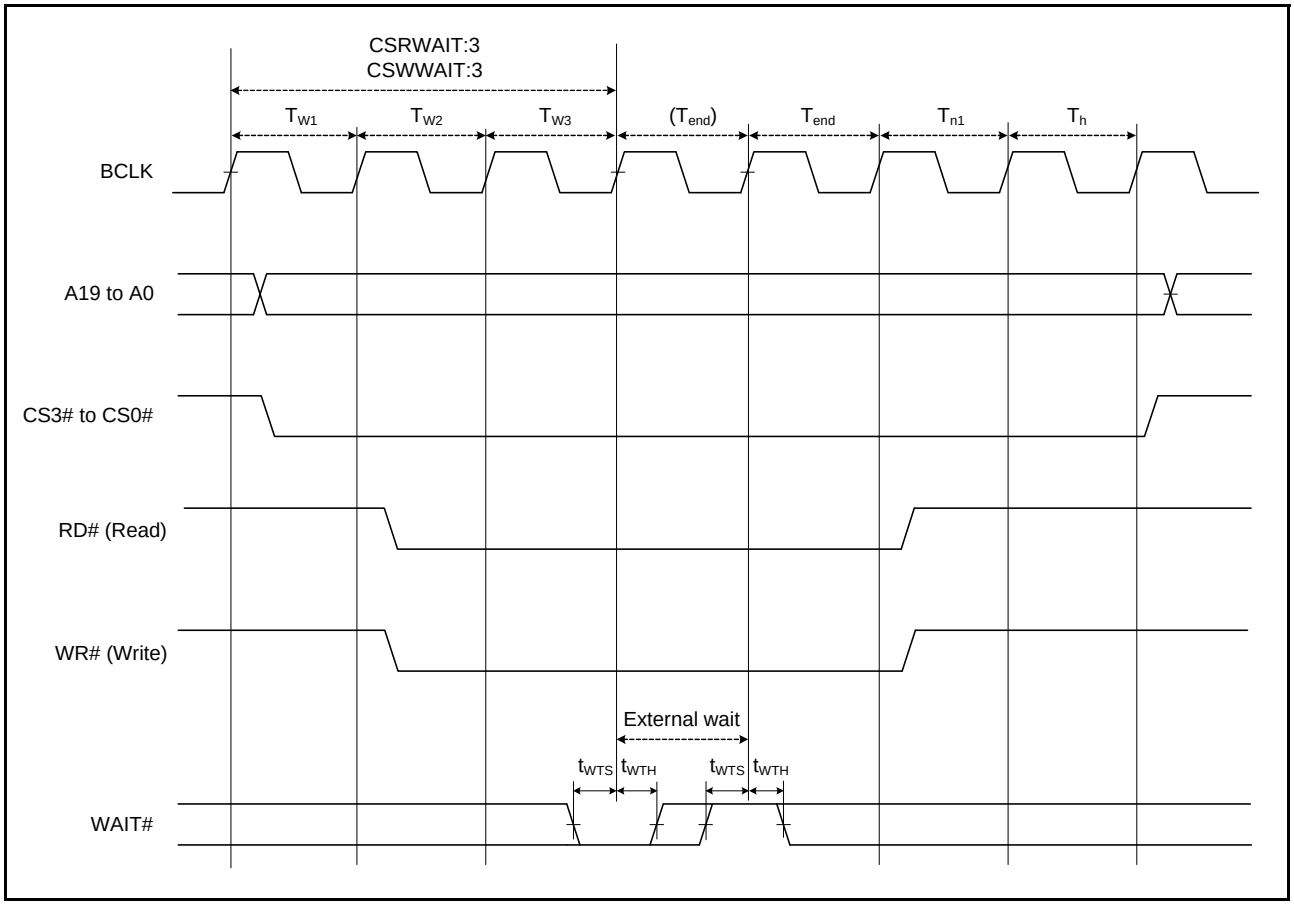


Figure 5.17 External Bus Timing/External Wait Control

Table 5.14 Bus Timing (Multiplexed Bus) (3)

Condition: PLLVCC = VCC_USB = AVCC0 = AVCC = VREF = 3.0 to 3.6 V
VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V, VREFH0 = 3.0 V to AVCC0
$T_a = T_{opr}$
Output load conditions: V_{OH} = VCC x 0.5, V_{OL} = VCC x 0.5, I_{OH} = –1.0 mA, I_{OL} = 1.0 mA, C = 30 pF

Item	Symbol	Min.	Max.	Unit	Test Conditions
Address delay time	t_{AD}	—	35	ns	Figure 5.18, Figure 5.19
Byte control delay time	t_{BCD}	—	30	ns	
CS# delay time	t_{CSD}	—	30	ns	
RD# delay time	t_{RSD}	—	30	ns	
ALE delay time	t_{ALED}	—	30	ns	
Read data setup time	t_{RDS}	20	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	—	30	ns	
Write data delay time	t_{WDD}	—	35	ns	
Write data hold time	t_{WDH}	0	—	ns	
WAIT# setup time	t_{WTS}	20	—	ns	Figure 5.17
WAIT# hold time	t_{WTH}	0.0	—	ns	

5.3.6 Timing of On-Chip Peripheral Modules

Table 5.16 Timing of On-Chip Peripheral Modules (1)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
I/O ports	Input data pulse width		t_{PRW}	1.5	—	t_{Pcyc}	Figure 5.22
MTU3	Input capture input pulse width	Single-edge setting	t_{TICW}	3	—	t_{PAcyc}	Figure 5.23
		Both-edge setting		5	—		
	Input capture input fall time		t_{TICTF}	—	0.1	µs/V	When Input capture at rising edge, or Input capture at both edges is selected.
	Timer clock pulse width	Single-edge setting	t_{TCKWH}, t_{TCKWL}	3	—	t_{PAcyc}	Figure 5.25
		Both-edge setting		5	—		
		Phase counting mode		5	—		
	Timer clock input fall time		t_{TCKTF}	—	0.1	µs/V	
POE3	POE# input pulse width		t_{POEW}	1.5	—	t_{Pcyc}	Figure 5.28
GPT	Input capture input pulse width	Single-edge setting	t_{GTICW}	3	—	t_{PAcyc}	Figure 5.26
		Both-edge setting		5	—		
	Input capture input fall time		t_{GTICTF}	—	0.1	µs/V	When Input capture at rising edge, or Input capture at both edges is selected. When Count operation is started at rising edge, or Count operation is started at both edges is selected. When Count operation is stopped at rising edge, or Count operation is stopped at both edges is selected. When Counter is cleared at rising edge, or Counter is cleared at both edges is selected.
	External trigger input pulse width	Single-edge setting	t_{OTETW}	3	—	t_{PAcyc}	Figure 5.27
		Both-edge setting		5	—		
	External trigger input fall time		$t_{GTETRGTF}$	—	0.1	µs/V	When Count operation is started at rising edge, or Count operation is started at both edges is selected. When Count operation is stopped at rising edge, or Count operation is stopped at both edges is selected. When Counter is cleared at rising edge, or Counter is cleared at both edges is selected.

5.5 A/D Conversion Characteristics

Table 5.19 10-Bit A/D Conversion Characteristics (1)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item			Min.	Typ.	Max.	Unit	Test Conditions
Resolution			10	10	10	Bit	
Conversion time*1 (Operation at ADCLK = 100 MHz)	With 0.1-µF external capacitor	AN0 to AN7	0.5	—	—	µs	Sampling in 25 states
		Other channels	0.75	—	—	µs	Sampling in 50 states
	Without 0.1-µF external capacitor Permissible signal source impedance (max.) = 1 kΩ	AN0 to AN7	0.6	—	—	µs	Sampling in 35 states
		Other channels	0.75	—	—	µs	Sampling in 50 states
Analog input capacitance			—	—	6	pF	
Integral nonlinearity error			—	—	±3.0	LSB	
Offset error			—	—	±2.0	LSB	
Full-scale error			—	—	±3.0	LSB	
Quantization error			—	±0.5	—	LSB	
Absolute accuracy			—	—	±6.0	LSB	

Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Table 5.20 10-Bit A/D Conversion Characteristics (2)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$ is common to conditions 1 to 3.

Item			Min.	Typ.	Max.	Unit	Test Conditions
Resolution			10	10	10	Bit	
Conversion time*1 (Operation at ADCLK = 50 MHz)	Without 0.1-µF external capacitor Permissible signal source impedance (max.) = 1 kΩ	AN0 to AN7	0.8	—	—	µs	Sampling in 15 states
		Other channels	1.0	—	—	µs	Sampling in 25 states
Analog input capacitance			—	—	6	pF	
Integral nonlinearity error			—	—	±2.0	LSB	
Offset error			—	—	±2.0	LSB	
Full-scale error			—	—	±3.0	LSB	
Quantization error			—	±0.5	—	LSB	
Absolute accuracy			—	—	±4.0	LSB	

Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Table 5.23 Characteristics of the Programmable Gain Amplifier

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Analog input capacitance		C_{in}	—	—	8	pF	
Input offset voltage		V_{off}	—	—	8	mV	
Input voltage range (V_{in})	Gain × 2.000	V_{in}	0.050 × AVcc	—	0.450 × AVcc	V	
	Gain × 2.500		0.047 × AVcc		0.360 × AVcc		
	Gain × 3.077		0.045 × AVcc		0.292 × AVcc		
	Gain × 3.636		0.042 × AVcc		0.247 × AVcc		
	Gain × 4.000		0.040 × AVcc		0.212 × AVcc		
	Gain × 4.444		0.036 × AVcc		0.191 × AVcc		
	Gain × 5.000		0.033 × AVcc		0.170 × AVcc		
	Gain × 5.714		0.031 × AVcc		0.148 × AVcc		
	Gain × 6.667		0.029 × AVcc		0.127 × AVcc		
	Gain × 10.000		0.025 × AVcc		0.08 × AVcc		
	Gain × 13.333		0.023 × AVcc	—	0.06 × AVcc		
Slew rate		SR	10	—	—	V/µs	
Gain error	Gain × 2.000	—	—	—	1	%	
	Gain × 2.500		—	—	1		
	Gain × 3.077		—	—	1		
	Gain × 3.636		—	—	1.5		
	Gain × 4.000		—	—	1.5		
	Gain × 4.444		—	—	2		
	Gain × 5.000		—	—	2		
	Gain × 5.714		—	—	2		
	Gain × 6.667		—	—	3		
	Gain × 10.000		—	—	4		
	Gain × 13.333		—	—	4		

5.8 Oscillation Stop Detection Circuit Characteristics

Table 5.28 Oscillation Stop Detection Circuit Characteristics

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection time	t_{dr}	—	—	1.0	ms	Figure 5.43

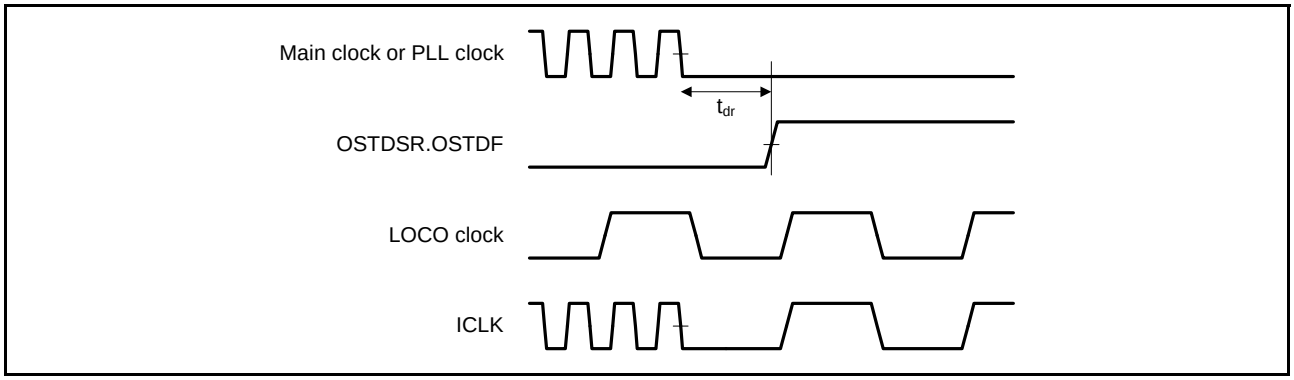


Figure 5.43 Oscillation Stop Detection Timing

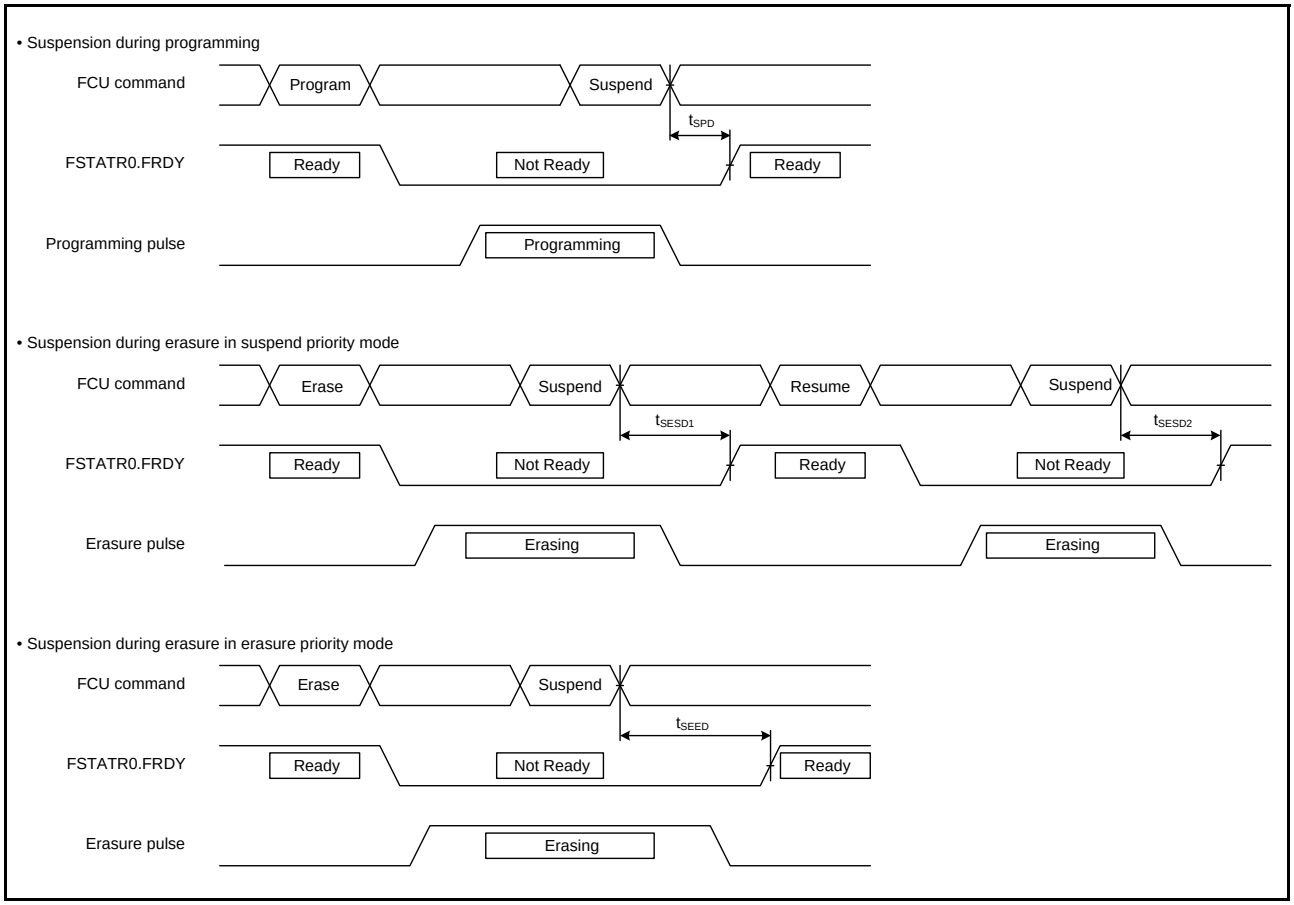


Figure 5.44 Flash Memory Program/Erase Suspend Timing

Table 6.3 DC Characteristics (2)

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Supply current*1	During operation	Max. *2	I_{CC}*3	—	—	60	mA	ICLK = 100MHz PCLKA = 100MHz PCLKB = 50MHz PCLKD = 50MHz FCLK = 50MHz
		Normal *4		—	25	—		
		Increased by BGO operation*5		—	15	—		
	Sleep mode				25	35		
	All-module-clock-stop mode*6				14	25		
	During standby	Software standby mode		—	0.2	6	mA	
		Deep software standby mode		—	16	40	µA	
Analog power supply current	During 12-bit A/D conversion (sample & hold circuit in use)		AI_{CC0}	—	3	4	mA	
	During 12-bit A/D conversion (sample & hold circuit not in use)			—	2	3	mA	
	Window comparator (1-channel operation)				0.4	1	mA	
	Window comparator (3-channel operation)			—	0.5	1	mA	
	Waiting for 12-bit AD conversion			—	25	32	µA	
Reference power supply current	During 12-bit A/D conversion		AI_{REFH0}	—	0.6	0.7	mA	
	Waiting for 12-bit A/D conversion			—	0.6	0.7	mA	
VCC rising gradient			SrVcc	—	—	20000	ms/V	

Note 1. Supply current values are with all output pins unloaded.
Note 2. Measured with clocks supplied to the peripheral functions. This does not include the BGO operation.
Note 3. I_{CC} depends on f (ICLK) as follows. (ICLK: PCLK = 8:4)
ICC max = 0.45 × f + 15 (Max)
ICC typ = 0.18 × f + 7 (Normal)
ICC max = 0.22 × f + 13 (sleep mode)
Note 4. Measured with clocks not supplied to the peripheral functions. This does not include the BGO operation.
Note 5. Incremented if data is written to or erased from the on-chip ROM or on-chip data-flash memory for data storage during the program execution.
Note 6. The values are for reference.

Table 6.4 Permissible Output Currents

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item	Symbol	Min.	Typ.	Max.	Unit
Permissible output low current (average value per pin)	I_{OL}	—	—	2.0*1	mA
Permissible output low current (max. value per pin)	I_{OL}	—	—	4.0*1	mA
Permissible output low current (total)	ΣI_{OL}	—	—	32	mA
Permissible output high current (average value per pin)	$-I_{OH}$	—	—	2.0	mA
Permissible output high current (max. value per pin)	$-I_{OH}$	—	—	4.0	mA
Permissible output high current (total)	$\Sigma-I_{OH}$	—	—	32	mA

Caution: To protect the MCU's reliability, the output current values should not exceed the values in this table.
Note 1. RIIC pin: IOL = 6 mA (max.)

Table 6.15 Timing of On-Chip Peripheral Modules (5)

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item		Symbol	Min.*1, *2	Max.	Unit	Test Conditions
Simple IIC (Standard-mode)	SCL, SDAinput rise time	t_{Sr}	—	1000	ns	Figure 6.25
	SCL, SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	4 × t_{IICcyc}	ns	
	Data input setup time	t_{SDAS}	250	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
Simple IIC (Fast-mode)	SCL, SDA input rise time	t_{Sr}	20 + 0.1C_b	300	ns	
	SCL, SDA input fall time	t_{Sf}	20 + 0.1C_b	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	4 × t_{IICcyc}	ns	
	Data input setup time	t_{SDAS}	100	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note 1. The value in parentheses is used when ICMR3.NF[1:0] are set to 11b while a digital filter is enabled with ICFER.NFE = 1.
Note 2. Cb indicates the total capacity of the bus line.

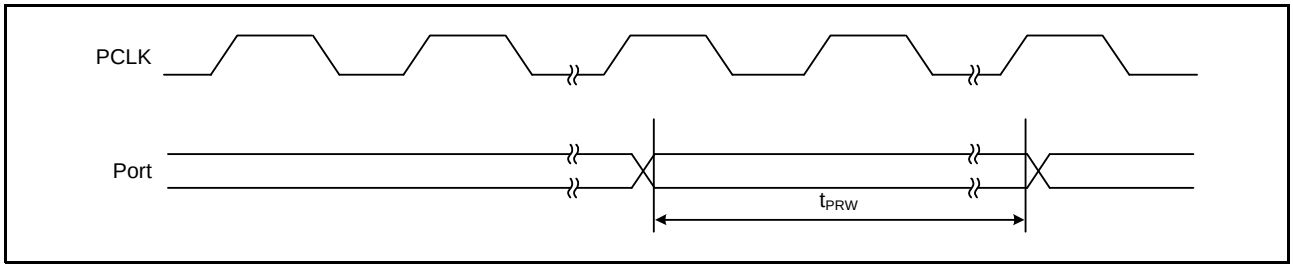


Figure 6.12 I/O port Input Timing

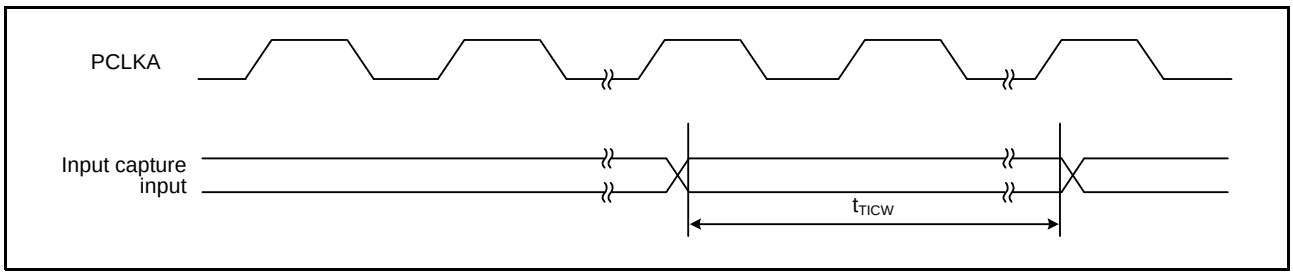


Figure 6.13 MTU3 Input/Output Timing

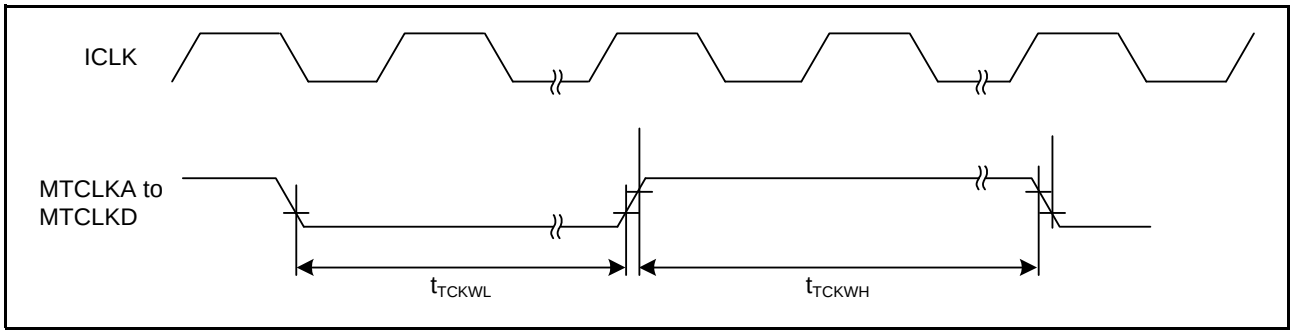
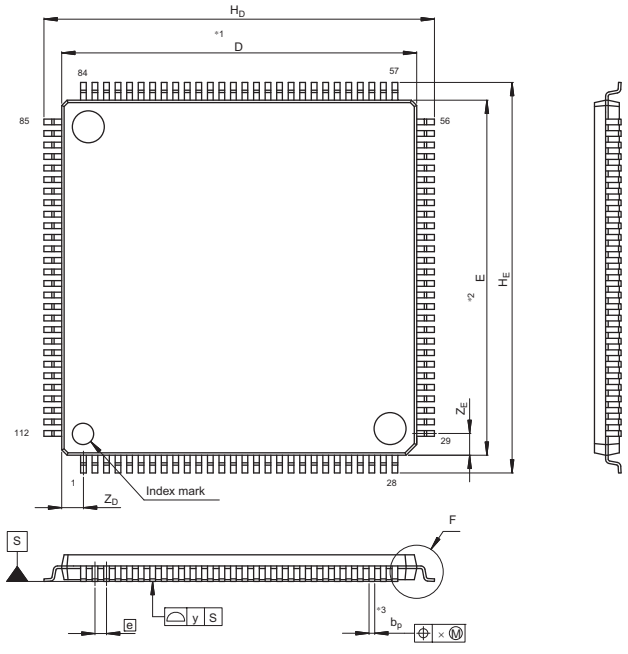
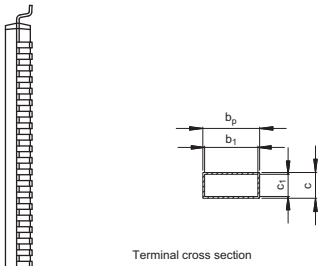
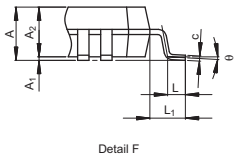


Figure 6.14 MTU3 Clock Input Timing

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP112-20x20-0.65	PLQP0112JA-A	FP-112E/FP-112EV	1.2g







NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	19.9	20.0	20.1
E	19.9	20.0	20.1
A_2	—	1.4	—
H_D	21.8	22.0	22.2
H_E	21.8	22.0	22.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.27	0.32	0.37
b_1	—	0.30	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z_D	—	1.225	—
Z_E	—	1.225	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure C 112-Pin LQFP (PLQP0112JA-A)

Rev.	Date	Description	
		Page	Summary
2.10	Sep 26, 2013	36 to 39	Table 1.7 List of Pins and Pin Functions (112-Pin LQFP), changed
		40 to 42	Table 1.8 List of Pins and Pin Functions (100-Pin LQFP), changed
		43 to 45	Table 1.9 List of Pins and Pin Functions (64-Pin LQFP), changed
		46 to 47	Table 1.10 List of Pins and Pin Functions (48-Pin LQFP), changed
		4. I/O Registers	
		56 to 103	Table 4.1 List of I/O Registers (Address Order), changed
		5. Electrical Characteristics [144-, 120-, 112- and 100-Pin Versions]	
		104	Table 5.1 Absolute Maximum Ratings, changed
		107	Table 5.4 DC Characteristics (3), Note 7, deleted
		108	Table 5.6 Permissible Power Consumption, added
		128	5.3.7 Timing of PWM Delay Generation Circuit, added
		128	Table 42.21 Timing of the PWM Delay Generation Circuit, added
		132	Figure 5.32 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKB Division Ratio Set to a Value Other Than 1/2) and Simple SPI Timing (Master, CKPH = 1), changed
		133	Figure 5.34 RSPI Timing (Slave, CPHA = 0) and Simple SPI Timing (Slave, CKPH = 0), changed
		134	Figure 5.35 RSPI Timing (Slave, CPHA = 1) and Simple SPI Timing (Slave, CKPH = 1), changed
		6. Electrical Characteristics [64- and 48-Pin Versions]	
		149	Table 6.1 Absolute Maximum Ratings, changed
		151	Table 6.3 DC Characteristics (2), Note 3, changed
		152	Table 6.5 Permissible Power Consumption, added