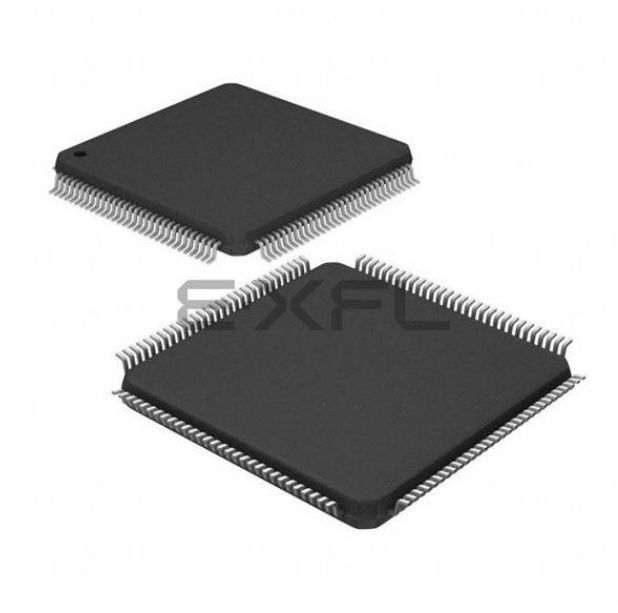
Renesas Electronics America Inc - R5F563TEADFA#V0 Datasheet



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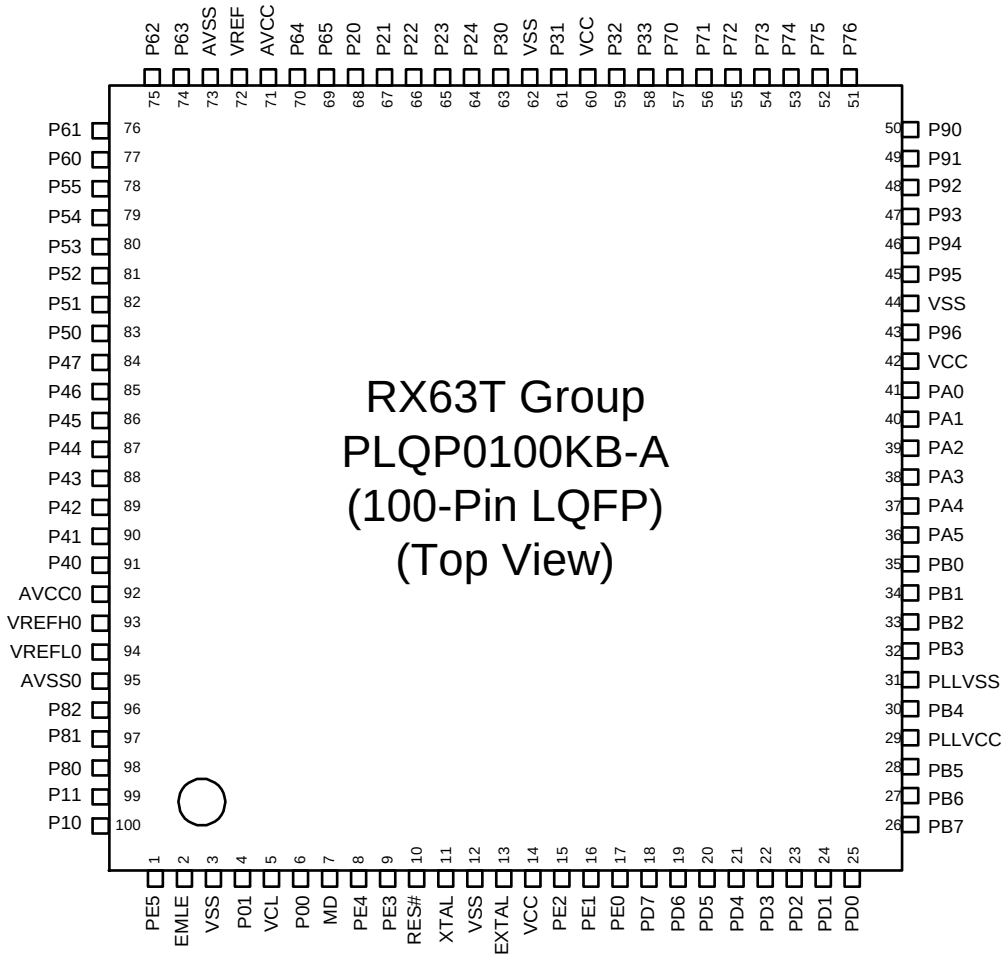
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	72
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x10b, 8x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	120-LQFP
Supplier Device Package	120-LQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f563teadfa-v0

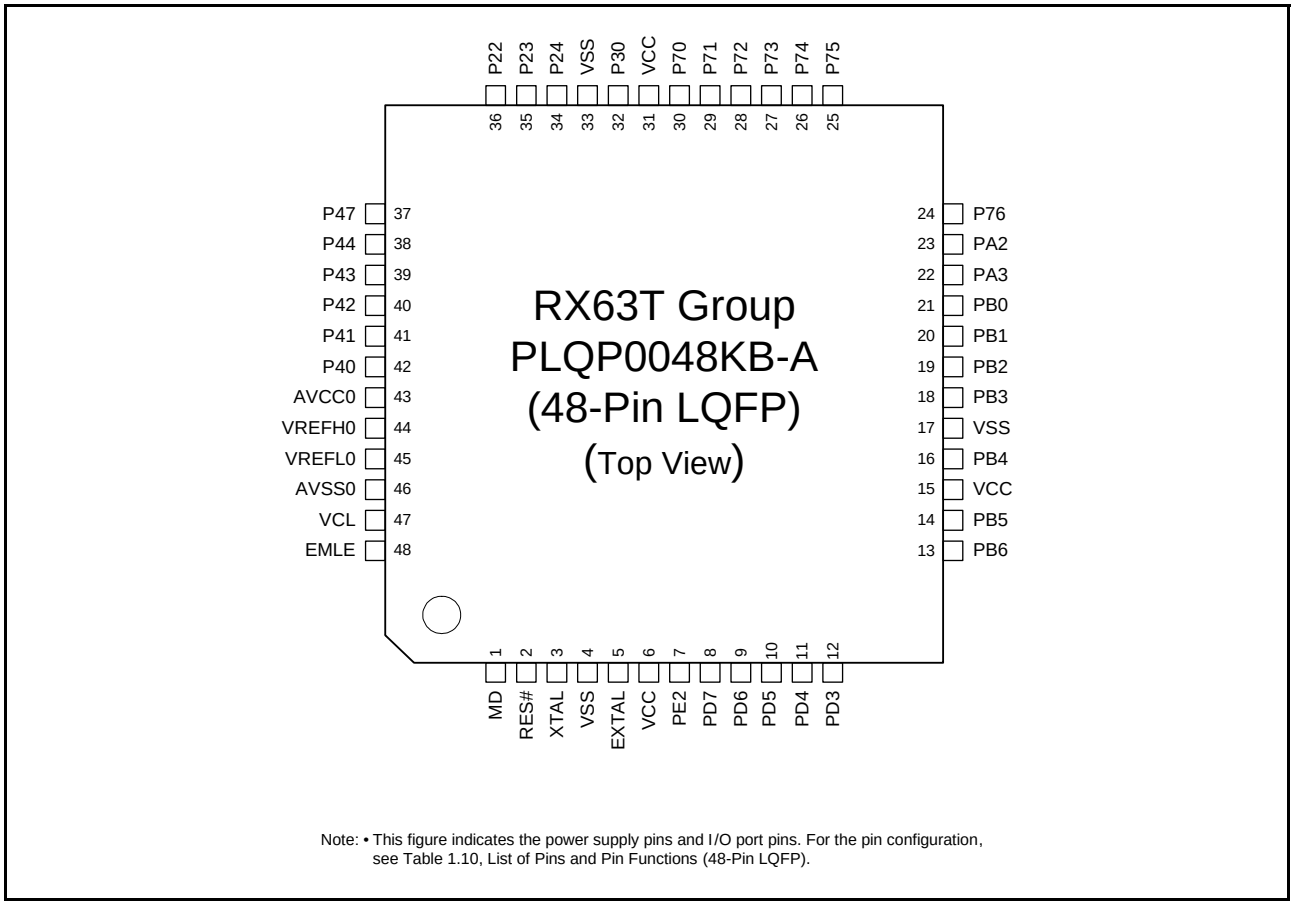
Table 1.4 Pin Functions (5/5)

Classifications	Pin Name	I/O	Description
I/O ports	P00 to P05	I/O	6-bit input/output pins
	P10 to P14	I/O	5-bit input/output pins
	P20 to P26	I/O	7-bit input/output pins
	P30 to P35	I/O	6-bit input/output pins
	P40 to P47	Input	8-bit input pins
	P50 to P57	Input	8-bit input pins
	P60 to P65	Input	6-bit input pins
	P70 to P76	I/O	7-bit input/output pins
	P80 to P82	I/O	3-bit input/output pins
	P90 to P96	I/O	7-bit input/output pins
	PA0 to PA6	I/O	7-bit input/output pins
	PB0 to PB7	I/O	8-bit input/output pins
	PC0 to PC5	Input	6-bit input pins
	PD0 to PD7	I/O	8-bit input/output pins
	PE0, PE1, PE3 to PE5	I/O	6-bit input/output pins
	PE2	Input	1-bit input pin
	PF0 to PF4	I/O	5-bit input/output pins
	PG0 to PG6	I/O	7-bit input/output pins



Note: • This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.8, List of Pins and Pin Functions (100-Pin LQFP).

Figure 1.6 Pin Assignment (100-Pin LQFP)



Note: • This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.10, List of Pins and Pin Functions (48-Pin LQFP).

Figure 1.8 Pin Assignment (48-Pin LQFP)

2.1 General-Purpose Registers (R0 to R15)

This CPU has sixteen general-purpose registers (R0 to R15). R1 to R15 can be used as data registers or address registers. R0, a general-purpose register, also functions as the stack pointer (SP).
The stack pointer is switched to operate as the interrupt stack pointer (ISP) or user stack pointer (USP) by the value of the stack pointer select bit (U) in the processor status word (PSW).

2.2 Control Registers

(1) Interrupt Stack Pointer (ISP)/User Stack Pointer (USP)

The stack pointer (SP) can be either of two types, the interrupt stack pointer (ISP) or the user stack pointer (USP). Whether the stack pointer operates as the ISP or USP depends on the value of the stack pointer select bit (U) in the processor status word (PSW).
Set the ISP or USP to a multiple of four, as this reduces the numbers of cycles required to execute interrupt sequences and instructions entailing stack manipulation.

(2) Interrupt Table Register (INTB)

The interrupt table register (INTB) specifies the address where the relocatable vector table starts.

(3) Program Counter (PC)

The program counter (PC) indicates the address of the instruction being executed.

(4) Processor Status Word (PSW)

The processor status word (PSW) indicates the results of instruction execution or the state of the CPU.

(5) Backup PC (BPC)

The backup PC (BPC) is provided to speed up response to interrupts.
After a fast interrupt has been generated, the contents of the program counter (PC) are saved in the BPC register.

(6) Backup PSW (BPSW)

The backup PSW (BPSW) is provided to speed up response to interrupts.
After a fast interrupt has been generated, the contents of the processor status word (PSW) are saved in the BPSW. The allocation of bits in the BPSW corresponds to that in the PSW.

(7) Fast Interrupt Vector Register (FINTV)

The fast interrupt vector register (FINTV) is provided to speed up response to interrupts.
The FINTV register specifies a branch destination address when a fast interrupt has been generated.

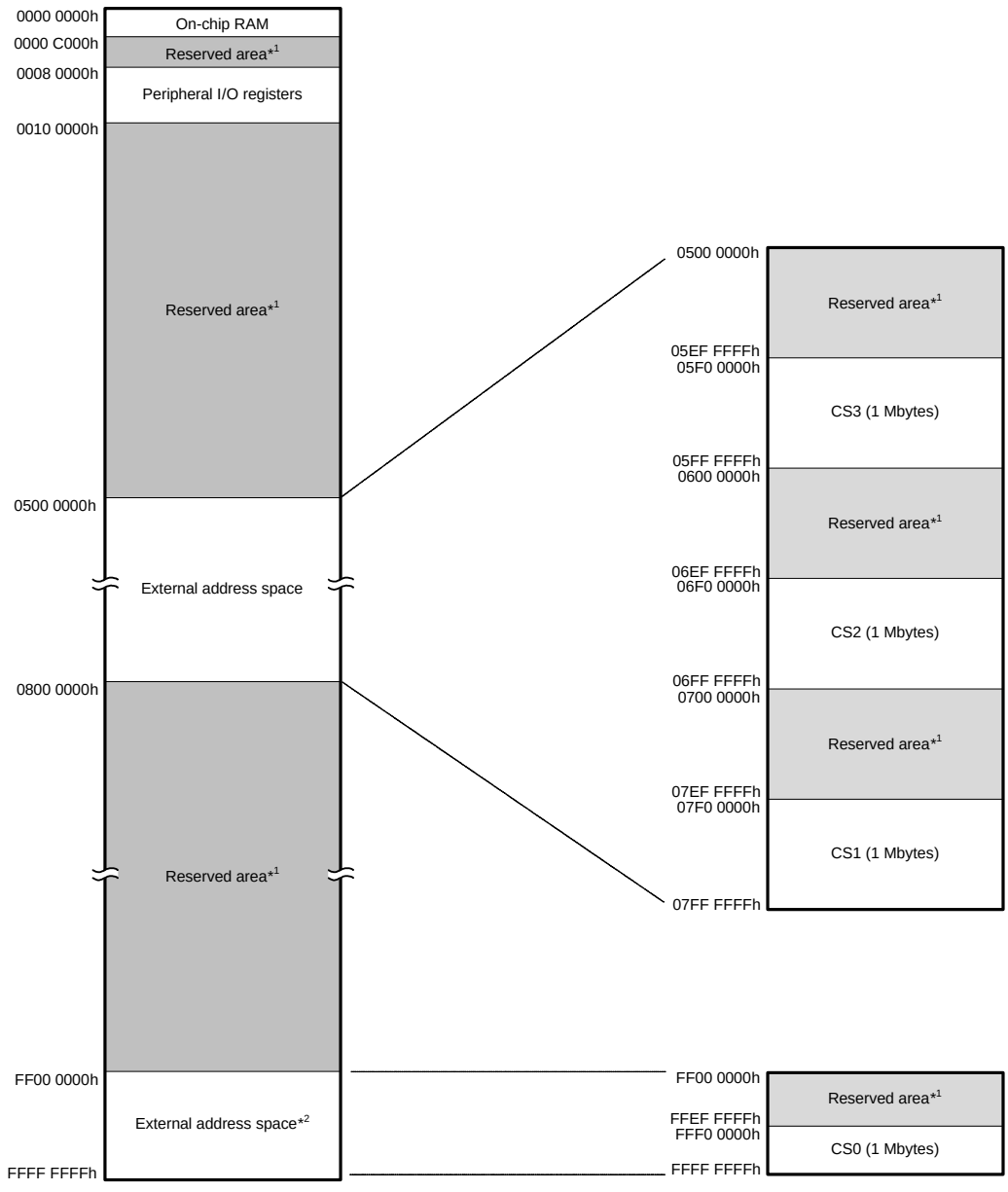
(8) Floating-Point Status Word (FPSW)

The floating-point status word (FPSW) indicates the results of floating-point operations.
When an exception handling enable bit (Ej) enables the exception handling (Ej = 1), the exception cause can be identified by checking the corresponding Cj flag in the exception handling routine. If the exception handling is masked (Ej = 0), the occurrence of exception can be checked by reading the Fj flag at the end of a series of processing. Once the Fj flag has been set to 1, this value is retained until it is cleared to 0 by software (j = X, U, Z, O, or V).

3.2 External Address Space

The external address space is divided into up to four CS areas (CS0 to CS3), each corresponding to the CSn# signal output from a CSn# (n = 0 to 3) pin.

Figure 3.2 shows the address ranges corresponding to the individual CS areas (CS0 to CS3) in on-chip ROM disabled extended mode.



Note 1. Reserved areas should not be accessed.
Note 2. The CS0 area is disabled in on-chip ROM enabled extended mode.
In this mode, the address space for addresses above 0800 0000h is as shown in Figure 3.1, Memory Map in Each Operating Mode.

Figure 3.2 Correspondence between External Address Spaces and CS Areas (In On-Chip ROM Disabled Extended Mode)

Table 4.1 List of I/O Registers (Address Order) (14/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 7507h	ICU	IRQ Control Register 7	IRQCR7	8	8	2 ICLK		ICUb	Not present in versions with 64 or 48 pins.
0008 7510h	ICU	IRQ Pin Digital Filter Enable Register 0	IRQFLTE0	8	8	2 ICLK			
0008 7514h	ICU	IRQ Pin Digital Filter Setting Register 0	IRQFLTC0	16	16	2 ICLK			
0008 7580h	ICU	Non-Maskable Interrupt Status Register	NMISR	8	8	2 ICLK			
0008 7581h	ICU	Non-Maskable Interrupt Enable Register	NMIER	8	8	2 ICLK			
0008 7582h	ICU	Non-Maskable Interrupt Status Clear Register	NMICLR	8	8	2 ICLK			
0008 7583h	ICU	NMI Pin Interrupt Control Register	NMICR	8	8	2 ICLK			
0008 7590h	ICU	NMI Pin Digital Filter Enable Register	NMIFLTE	8	8	2 ICLK			
0008 7594h	ICU	NMI Pin Digital Filter Setting Register	NMIFLTC	8	8	2 ICLK			
0008 8000h	CMT	Compare Match Timer Start Register 0	CMSTR0	16	16	2, 3 PCLKB	2 ICLK	CMT	
0008 8002h	CMT0	Compare Match Timer Control Register	CMCR	16	16	2, 3 PCLKB	2 ICLK		
0008 8004h	CMT0	Compare Match Timer Counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK		
0008 8006h	CMT0	Compare Match Timer Constant Register	CMCOR	16	16	2, 3 PCLKB	2 ICLK		
0008 8008h	CMT1	Compare Match Timer Control Register	CMCR	16	16	2, 3 PCLKB	2 ICLK		
0008 800Ah	CMT1	Compare Match Timer Counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK		
0008 800Ch	CMT1	Compare Match Timer Constant Register	CMCOR	16	16	2, 3 PCLKB	2 ICLK		
0008 8010h	CMT	Compare Match Timer Start Register 1	CMSTR1	16	16	2, 3 PCLKB	2 ICLK		
0008 8012h	CMT2	Compare Match Timer Control Register	CMCR	16	16	2, 3 PCLKB	2 ICLK		
0008 8014h	CMT2	Compare Match Timer Counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK		
0008 8016h	CMT2	Compare Match Timer Constant Register	CMCOR	16	16	2, 3 PCLKB	2 ICLK		
0008 8018h	CMT3	Compare Match Timer Control Register	CMCR	16	16	2, 3 PCLKB	2 ICLK		
0008 801Ah	CMT3	Compare Match Timer Counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK		
0008 801Ch	CMT3	Compare Match Timer Constant Register	CMCOR	16	16	2, 3 PCLKB	2 ICLK		
0008 8020h	WDT	WDT Refresh Register	WDTRR	8	8	2, 3 PCLKB	2 ICLK	WDTA	
0008 8022h	WDT	WDT Control Register	WDTCR	16	16	2, 3 PCLKB	2 ICLK		
0008 8024h	WDT	WDT Status Register	WDTSR	16	16	2, 3 PCLKB	2 ICLK		
0008 8026h	WDT	WDT Reset Control Register	WDTRCR	8	8	2, 3 PCLKB	2 ICLK		
0008 8030h	IWDT	IWDT Refresh Register	IWDTRR	8	8	2, 3 PCLKB	2 ICLK	IWDTa	
0008 8032h	IWDT	IWDT Control Register	IWDTCR	16	16	2, 3 PCLKB	2 ICLK		
0008 8034h	IWDT	IWDT Status Register	IWDTSR	16	16	2, 3 PCLKB	2 ICLK		
0008 8036h	IWDT	IWDT Reset Control Register	IWDTRCR	8	8	2, 3 PCLKB	2 ICLK		
0008 8038h	IWDT	IWDT Count Stop Control Register	IWDTCSTPR	8	8	2, 3 PCLKB	2 ICLK		
0008 80C0h	DA	D/A Data Register 0	DADR0	16	16	2, 3 PCLKB	2 ICLK	DAa	Not present in versions with 64 or 48 pins.
0008 80C2h	DA	D/A Data Register 1	DADR1	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 80C4h	DA	D/A Control Register	DACR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 80C5h	DA	DADRm Format Select Register	DADPR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 80C6h	DA	D/A A/D Synchronous Start Control Register	DAADSCR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 8280h	CRC	CRC Control Register	CRCCR	8	8	2, 3 PCLKB	2 ICLK	CRC	
0008 8281h	CRC	CRC Data Input Register	CRCDIR	8	8	2, 3 PCLKB	2 ICLK		
0008 8282h	CRC	CRC Data Output Register	CRCDOR	16	16	2, 3 PCLKB	2 ICLK		
0008 8300h	RIIC0	I^2C Bus Control Register 1	ICCR1	8	8	2, 3 PCLKB	2 ICLK	RIIC	
0008 8301h	RIIC0	I^2C Bus Control Register 2	ICCR2	8	8	2, 3 PCLKB	2 ICLK		
0008 8302h	RIIC0	I^2C Bus Mode Register 1	ICMR1	8	8	2, 3 PCLKB	2 ICLK		
0008 8303h	RIIC0	I^2C Bus Mode Register 2	ICMR2	8	8	2, 3 PCLKB	2 ICLK		
0008 8304h	RIIC0	I^2C Bus Mode Register 3	ICMR3	8	8	2, 3 PCLKB	2 ICLK		
0008 8305h	RIIC0	I^2C Bus Function Enable Register	ICFER	8	8	2, 3 PCLKB	2 ICLK		
0008 8306h	RIIC0	I^2C Bus Status Enable Register	ICSER	8	8	2, 3 PCLKB	2 ICLK		
0008 8307h	RIIC0	I^2C Bus Interrupt Enable Register	ICIER	8	8	2, 3 PCLKB	2 ICLK		

Table 4.1 List of I/O Registers (Address Order) (19/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 9804h	AD	A/D Channel Select Register 0	ADANSA0	16	16	2, 3 PCLKB	2 ICLK	AD	Not present in versions with 64 or 48 pins.
0008 9806h	AD	A/D Channel Select Register 1	ADANSA1	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64 or 48 pins.
0008 9808h	AD	A/D-Converted Value Addition Mode Select Register0	ADADS0	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 980Ah	AD	A/D-Converted Value Addition Mode Select Register1	ADADS1	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64 or 48 pins.
0008 980Ch	AD	A/D-Converted Value Addition Count Select Register	ADADC	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 980Eh	AD	A/D Control Extended Register	ADCER	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9810h	AD	A/D Start Trigger Select Register	ADSTRGR	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 981Eh	AD	A/D Self-Diagnosis Data Register	ADRD	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9820h	AD	A/D Data Register A	ADDRA	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9822h	AD	A/D Data Register B	ADDRB	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9824h	AD	A/D Data Register C	ADDRC	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9826h	AD	A/D Data Register D	ADDRD	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9828h	AD	A/D Data Register E	ADDRE	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 982Ah	AD	A/D Data Register F	ADDRF	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 982Ch	AD	A/D Data Register G	ADDRG	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 982Eh	AD	A/D Data Register H	ADDRH	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9830h	AD	A/D Data Register I	ADDRI	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9832h	AD	A/D Data Register J	ADDRJ	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9834h	AD	A/D Data Register K	ADDRK	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9836h	AD	A/D Data Register L	ADDRL	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9838h	AD	A/D Data Register M	ADDRM	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 983Ah	AD	A/D Data Register N	ADDRN	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 983Ch	AD	A/D Data Register O	ADDRO	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 983Eh	AD	A/D Data Register P	ADDRP	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 9840h	AD	A/D Data Register Q	ADDRQ	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 9842h	AD	A/D Data Register R	ADDRR	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 9844h	AD	A/D Data Register S	ADDRS	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 9846h	AD	A/D Data Register T	ADDRT	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 9860h	AD	A/D Sampling State Register 0	ADSSTR0	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9861h	AD	A/D Sampling State Register L	ADSSTRL	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.

Table 4.1 List of I/O Registers (Address Order) (31/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
000A 004Ch	USB0	Frame Number Register	FRMNUM	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1	USBa	Not present in versions with 112, 100, 64, or 48 pins.
000A 004Eh	USB0	Device State Change Register	DVCHGR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 0050h	USB0	USB Address Register	USBADDR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 0054h	USB0	USB Request Type Register	USBREQ	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 0056h	USB0	USB Request Value Register	USBVAL	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 0058h	USB0	USB Request Index Register	USBINDX	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 005Ah	USB0	USB Request Length Register	USBLENG	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 005Ch	USB0	DCP Configuration Register	DCPCFG	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 005Eh	USB0	DCP Maximum Packet Size Register	DCPMAXP	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 0060h	USB0	DCP Control Register	DCPCTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 0064h	USB0	Pipe Window Select Register	PIPESEL	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.
000A 0068h	USB0	Pipe Configuration Register	PIPECFG	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*1		Not present in versions with 112, 100, 64, or 48 pins.

Table 4.1 List of I/O Registers (Address Order) (38/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
000C 211Ah	GPT0	General PWM Timer Compare Capture Register F	GTCCRF	16	16, 32	2 to 5 PCLKA	2, 3 ICLK	GPT	
000C 211Ch	GPT0	General PWM Timer Cycle Setting Register	GTPR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 211Eh	GPT0	General PWM Timer Cycle Setting Buffer Register	GTPBR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2120h	GPT0	General PWM Timer Cycle Setting Double-Buffer Register	GTPDBR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2124h	GPT0	A/D Converter Start Request Timing Register A	GTADTRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2126h	GPT0	A/D Converter Start Request Timing Buffer Register A	GTADTBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2128h	GPT0	A/D Converter Start Request Timing Double-Buffer Register A	GTADTDBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 212Ch	GPT0	A/D Converter Start Request Timing Register B	GTADTRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 212Eh	GPT0	A/D Converter Start Request Timing Buffer Register B	GTADTBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2130h	GPT0	A/D Converter Start Request Timing Double-Buffer Register B	GTADTDBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2134h	GPT0	General PWM Timer Output Negate Control Register	GTONCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2136h	GPT0	General PWM Timer Dead Time Control Register	GTDTCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2138h	GPT0	General PWM Timer Dead Time Value Register U	GTDVU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 213Ah	GPT0	General PWM Timer Dead Time Value Register D	GTDVD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 213Ch	GPT0	General PWM Timer Dead Time Buffer Register U	GTDBU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 213Eh	GPT0	General PWM Timer Dead Time Buffer Register D	GTDBD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2140h	GPT0	General PWM Timer Output Protection Function Status Register	GTSOS	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2142h	GPT0	General PWM Timer Output Protection Function Temporary Release Register	GTSOTR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2180h	GPT1	General PWM Timer I/O Control Register	GTIOR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2182h	GPT1	General PWM Timer Interrupt Output Setting Register	GTINTAD	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2184h	GPT1	General PWM Timer Control Register	GTCR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2186h	GPT1	General PWM Timer Buffer Enable Register	GTBER	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2188h	GPT1	General PWM Timer Count Direction Register	GTUDC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 218Ah	GPT1	General PWM Timer Interrupt, A/D Converter Start Request Skipping Setting Register	GTITC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 218Ch	GPT1	General PWM Timer Status Register	GTST	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 218Eh	GPT1	General PWM Timer Counter	GTCNT	16	16	2 to 5 PCLKA	2, 3 ICLK		
000C 2190h	GPT1	General PWM Timer Compare Capture Register A	GTCCRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2192h	GPT1	General PWM Timer Compare Capture Register B	GTCCRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2194h	GPT1	General PWM Timer Compare Capture Register C	GTCCRC	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2196h	GPT1	General PWM Timer Compare Capture Register D	GTCCRD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2198h	GPT1	General PWM Timer Compare Capture Register E	GTCCRE	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 219Ah	GPT1	General PWM Timer Compare Capture Register F	GTCCRF	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 219Ch	GPT1	General PWM Timer Cycle Setting Register	GTPR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 219Eh	GPT1	General PWM Timer Cycle Setting Buffer Register	GTPBR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 21A0h	GPT1	General PWM Timer Cycle Setting Double-Buffer Register	GTPDBR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 21A4h	GPT1	A/D Converter Start Request Timing Register A	GTADTRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		

Table 4.1 List of I/O Registers (Address Order) (39/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
000C 21A6h	GPT1	A/D Converter Start Request Timing Buffer Register A	GTADTBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK	GPT	
000C 21A8h	GPT1	A/D Converter Start Request Timing Double-Buffer Register A	GTADTDBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 21ACh	GPT1	A/D Converter Start Request Timing Register B	GTADTRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 21AEh	GPT1	A/D Converter Start Request Timing Buffer Register B	GTADTBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 21B0h	GPT1	A/D Converter Start Request Timing Double-Buffer Register B	GTADTDBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 21B4h	GPT1	General PWM Timer Output Negate Control Register	GTONCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 21B6h	GPT1	General PWM Timer Dead Time Control Register	GTDTCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 21B8h	GPT1	General PWM Timer Dead Time Value Register U	GTDVU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 21BAh	GPT1	General PWM Timer Dead Time Value Register D	GTDVD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 21BCh	GPT1	General PWM Timer Dead Time Buffer Register U	GTDBU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 21BEh	GPT1	General PWM Timer Dead Time Buffer Register D	GTDBD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 21C0h	GPT1	General PWM Timer Output Protection Function Status Register	GTSOS	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 21C2h	GPT1	General PWM Timer Output Protection Function Temporary Release Register	GTSOTR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2200h	GPT2	General PWM Timer I/O Control Register	GTIOR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2202h	GPT2	General PWM Timer Interrupt Output Setting Register	GTINTAD	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2204h	GPT2	General PWM Timer Control Register	GTCR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2206h	GPT2	General PWM Timer Buffer Enable Register	GTBER	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2208h	GPT2	General PWM Timer Count Direction Register	GTUDC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 220Ah	GPT2	General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register	GTITC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 220Ch	GPT2	General PWM Timer Status Register	GTST	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 220Eh	GPT2	General PWM Timer Counter	GTCNT	16	16	2 to 5 PCLKA	2, 3 ICLK		
000C 2210h	GPT2	General PWM Timer Compare Capture Register A	GTCCRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2212h	GPT2	General PWM Timer Compare Capture Register B	GTCCRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2214h	GPT2	General PWM Timer Compare Capture Register C	GTCCRC	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2216h	GPT2	General PWM Timer Compare Capture Register D	GTCCRD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2218h	GPT2	General PWM Timer Compare Capture Register E	GTCCRE	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 221Ah	GPT2	General PWM Timer Compare Capture Register F	GTCCRF	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 221Ch	GPT2	General PWM Timer Cycle Setting Register	GTPR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 221Eh	GPT2	General PWM Timer Cycle Setting Buffer Register	GTPBR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2220h	GPT2	General PWM Timer Cycle Setting Double-Buffer Register	GTPDBR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2224h	GPT2	A/D Converter Start Request Timing Register A	GTADTRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2226h	GPT2	A/D Converter Start Request Timing Buffer Register A	GTADTBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2228h	GPT2	A/D Converter Start Request Timing Double-Buffer Register A	GTADTDBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 222Ch	GPT2	A/D Converter Start Request Timing Register B	GTADTRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 222Eh	GPT2	A/D Converter Start Request Timing Buffer Register B	GTADTBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		

Table 5.3 DC Characteristics (2)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

The following relation applies when the USB is in use under condition 1 or condition 2: Vcc = PLLVcc = Vcc_USB = 3.0 to 3.6 V.

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output high voltage	All output pins (except for P52, P53, P60 to P65, P71 to P76, P90 to P95, and USB0_DPUPE)	V_{OH}	VCC – 0.5	—	—	V	I_{OH} = –1 mA
	P52, P53, and P60 to P65		AVCC – 0.5	—	—		I_{OH} = –1 mA
	USB0_DPUPE		VCC_USB – 0.5				I_{OH} = –1 mA
	P71 to P76, and P90 to P95		VCC – 1.0	—	—		I_{OH} = –5 mA
Output low voltage	All output pins (except for P71 to P76, P90 to P95, and RIIC pins)	V_{OL}	—	—	0.5	V	I_{OL} = 1.0 mA
	P71 to P76, and P90 to P95		—	—	1.1		I_{OL} = 15 mA
	RIIC pins		—	—	0.4		I_{OL} = 3 mA
			—	—	0.6		I_{OL} = 6 mA
Input leakage current	RES#, MD pin, EMLE, Port 4, Ports P50, P51, P54 to P57, and Port C	$\lvert I_{in} \rvert$	—	—	1.0	µA	V_{in} = 0 V, V_{in} = VCC
Three-state leakage current (off state)	Port 0, Port 1, Ports P20 to P24, Port 3, Ports P52, P53, Ports 6 to A, Ports PB0, PB3 to PB7, and Ports D to G	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	V_{in} = 0 V, V_{in} = VCC
	Ports P25, P26, PB1, and PB2		—	—	5.0		
Input capacitance	All output pins (except for P25, P26, PB1, and PB2)	C_{in}	—	—	15	pF	V_{in} = 0 V, f = 1 MHz, T_a = 25 ºC
	Ports P25, P26, PB1, and PB2		—	—	30		

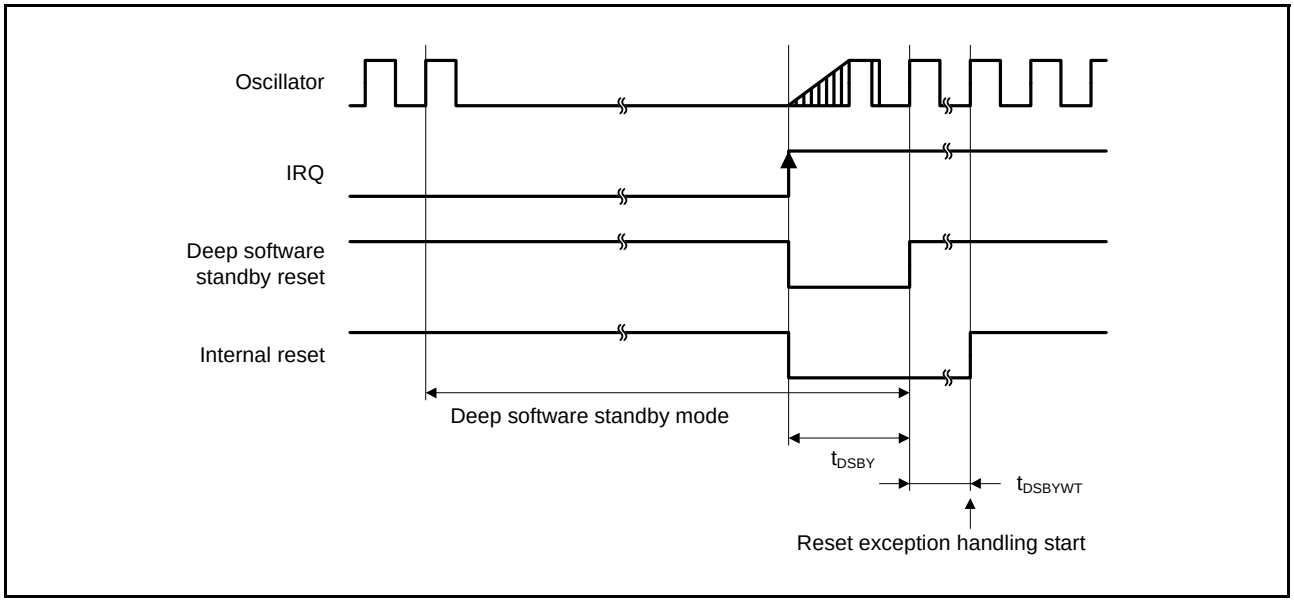


Figure 5.10 Deep Software Standby Mode Cancellation Timing

5.3.4 Control Signal Timing

Table 5.11 Control Signal Timing

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
NMI pulse width	t_{NMIW}	200	—	—	ns	t_c(PCLK) × 2 ≤ 200 ns, Figure 5.11
		t_c(PCLK) × 2	—	—	ns	t_c(PCLK) > 200 ns, Figure 5.11
IRQ pulse width	t_{IRQW}	200	—	—	ns	t_c(PCLK) ≤ 200 ns, Figure 5.12
		t_c(PCLK) × 2	—	—	ns	t_c(PCLK) > 200 ns, Figure 5.12

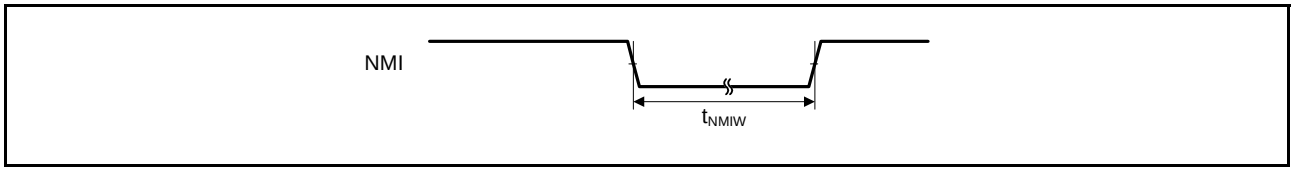


Figure 5.11 NMI Interrupt Input Timing

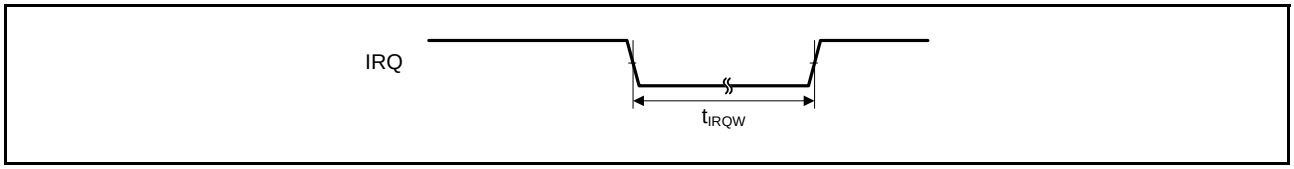


Figure 5.12 IRQ Interrupt Input Timing

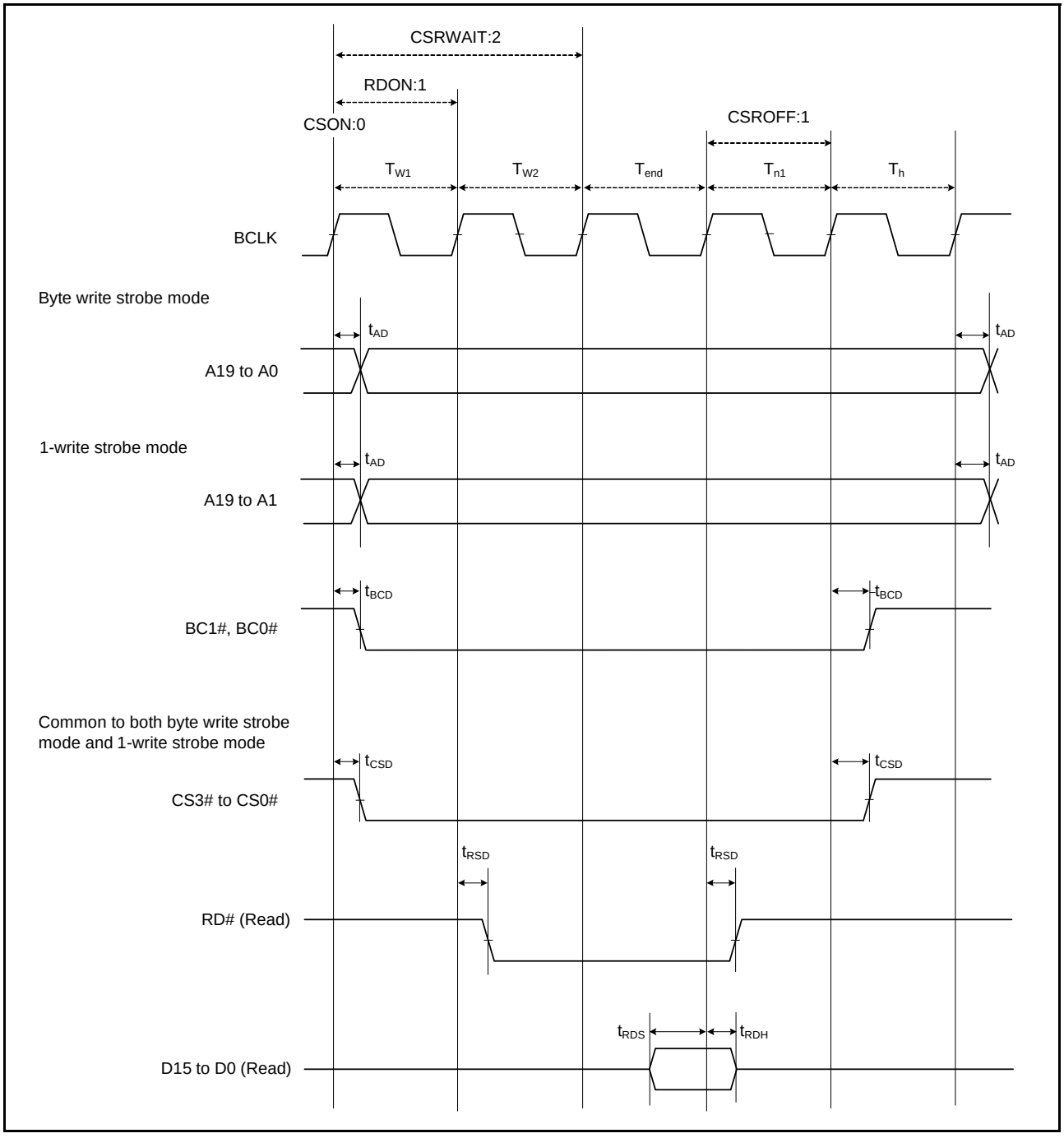


Figure 5.13 External Bus Timing/Normal Read Cycle (Bus Clock Synchronized)

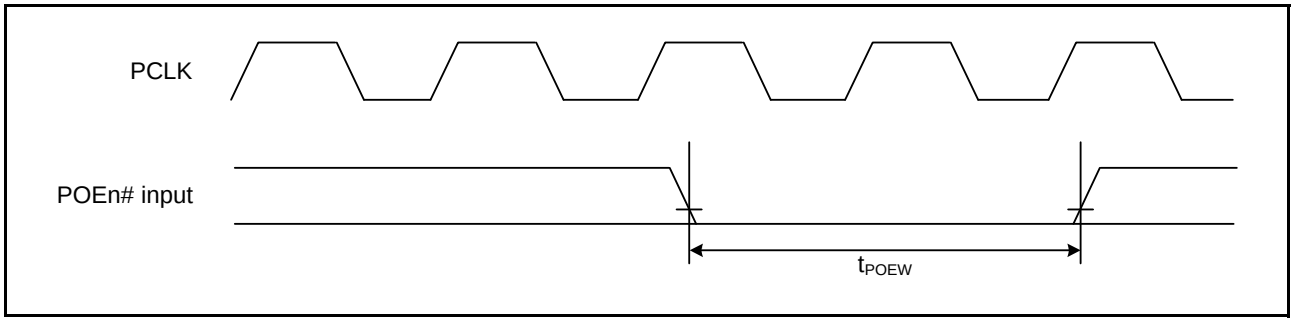


Figure 5.25 POE3# Input Timing

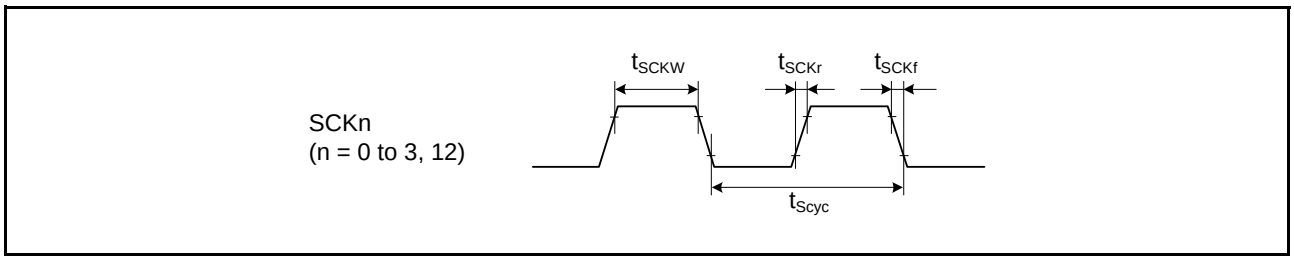


Figure 5.26 SCK Clock Input Timing

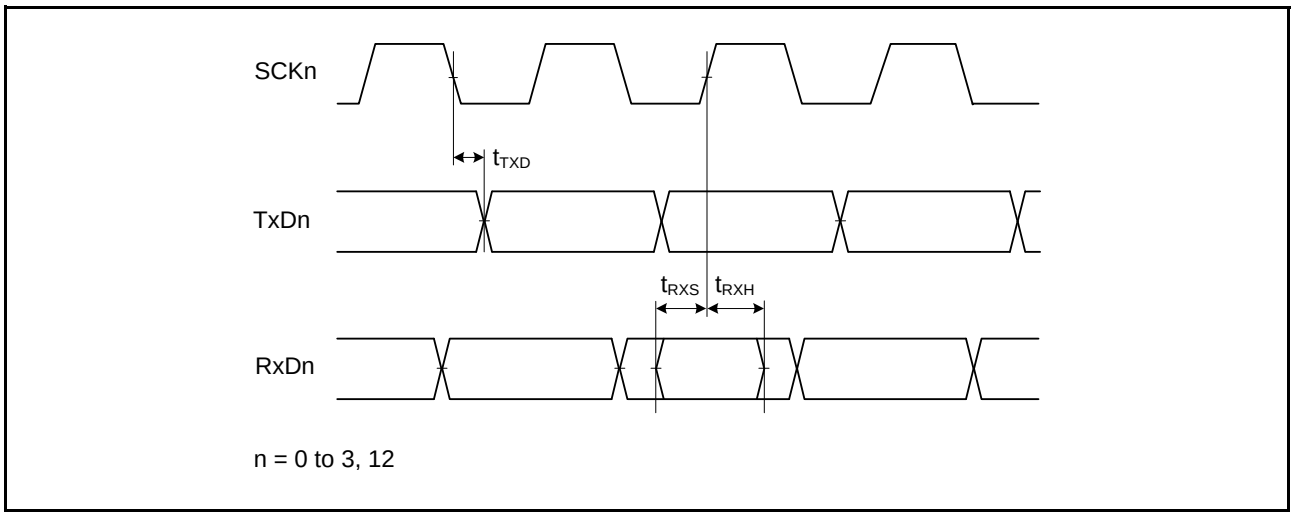


Figure 5.27 SCI Input/Output Timing: Clock Synchronous Mode

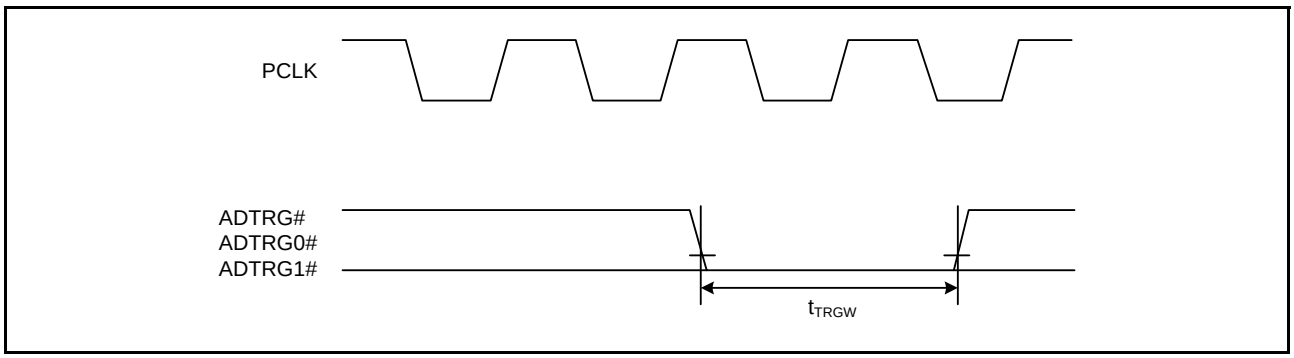


Figure 5.28 AD Converter External Trigger Input Timing

5.7 Power-on Reset Circuit and Voltage Detection Circuit Characteristics

Table 5.26 Power-on Reset Circuit and Voltage Detection Circuit Characteristics (1)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” and “Condition 2” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. T_a is common to conditions 1 and 2.

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	V_{POR}	2.46	2.58	2.7	V	Figure 5.41
	Voltage detection circuit (LVD0)	V_{DET0}	2.7	2.82	2.94		Figure 5.42
	Voltage detection circuit (LVD1)*1	V_{DET1_8}	2.75	2.90	3.05		Figure 5.43
		V_{DET1_9}	2.70	2.85	3.00		
		V_{DET1_A}	2.73	2.88	3.03		
	Voltage detection circuit (LVD2)*2	V_{DET2_8}	2.75	2.9	3.05		Figure 5.44
		V_{DET2_9}	2.70	2.85	3.00		
		V_{DET2_A}	2.73	2.88	3.03		
Internal reset time	Power-on reset (POR)	t_{POR}		9.7		ms	Figure 5.41
	Voltage detection circuit (LVD0)	t_{LVD0}		9.7			Figure 5.42
	Voltage detection circuit (LVD1)	t_{LVD1}		0.9			Figure 5.43
	Voltage detection circuit (LVD2)	t_{LVD2}		0.9			Figure 5.44
Minimum VCC down time*3		t_{VOFF}	200	—	—	µs	Figure 5.41 and Figure 5.42
Response delay time		t_{DET}			200	µs	
LVD operation stabilization time (after LVD is enabled)		$Td_{(E-A)}$			3	µs	Figure 5.41 to Figure 5.44
Hysteresis width (LVD1 and LVD2)		V_{LVH}		80		mV	

Note 1. # in symbol $V_{DET1\_\#}$ indicates the value of the LVDLVLR.LVD1LVL[3:0] bits.
Note 2. # in symbol $V_{DET2\_\#}$ indicates the value of the LVDLVLR.LVD2LVL[3:0] bits.
Note 3. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{DET1}, and V_{DET2} for the POR/ LVD.

Table 6.15 Timing of On-Chip Peripheral Modules (5)

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item		Symbol	Min.*1, *2	Max.	Unit	Test Conditions
Simple IIC (Standard-mode)	SCL, SDAinput rise time	t_{Sr}	—	1000	ns	Figure 6.25
	SCL, SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	4 × t_{IICcyc}	ns	
	Data input setup time	t_{SDAS}	250	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
Simple IIC (Fast-mode)	SCL, SDA input rise time	t_{Sr}	20 + 0.1C_b	300	ns	
	SCL, SDA input fall time	t_{Sf}	20 + 0.1C_b	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	4 × t_{IICcyc}	ns	
	Data input setup time	t_{SDAS}	100	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note 1. The value in parentheses is used when ICMR3.NF[1:0] are set to 11b while a digital filter is enabled with ICFER.NFE = 1.
Note 2. Cb indicates the total capacity of the bus line.

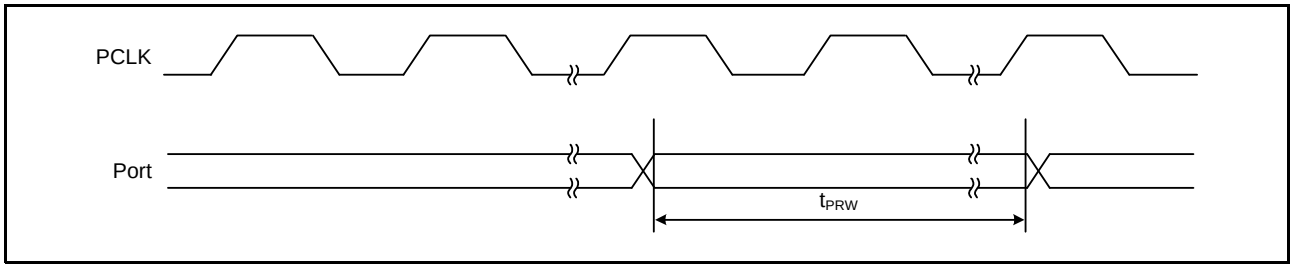


Figure 6.12 I/O port Input Timing

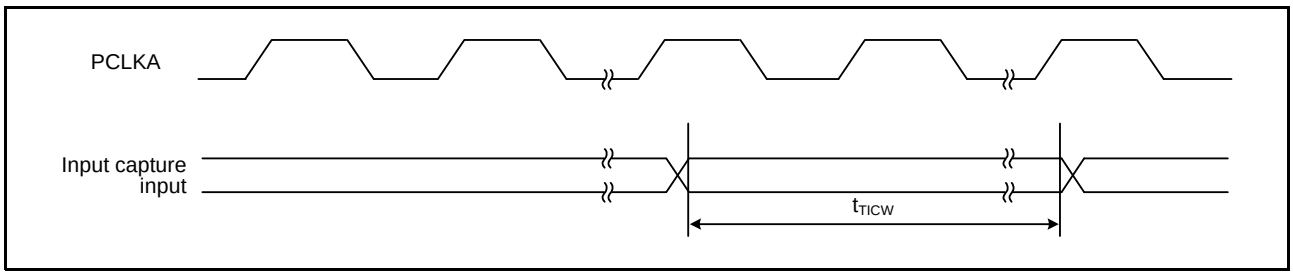


Figure 6.13 MTU3 Input/Output Timing

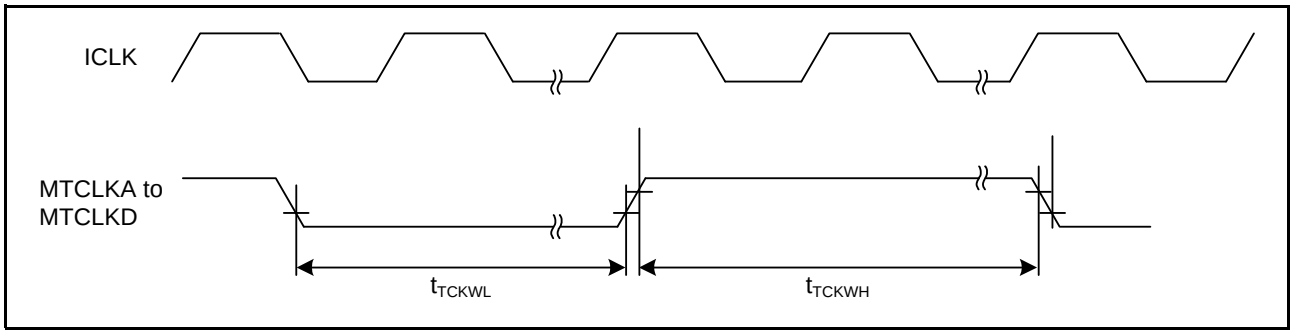


Figure 6.14 MTU3 Clock Input Timing

6.6 Oscillation Stop Detection Circuit Characteristics

Table 6.19 Oscillation Stop Detection Circuit Characteristics

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V, AVCC0 = 3.0 to 3.6 V,
VREFH0 = 3.0 V to AVCC0, Ta = T_{opr}

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection time	t_{dr}	—	—	1.0	ms	Figure 6.30

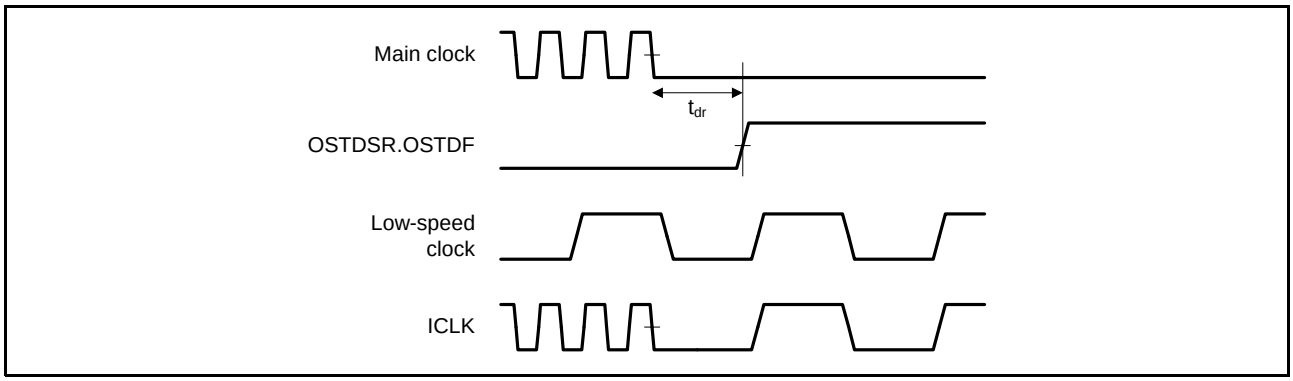


Figure 6.30 Oscillation Stop Detection Timing

6.8 E^2 DataFlash Characteristic

Table 6.22 E^2 DataFlash (Flash Memory for Data Storage) Characteristics (1)

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0
Temperature range for the programming/erasure operation: $T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Reprogram/erase cycle*1	N_{DPEC}	100000	—	—	Times	
Data hold time	t_{DDRP}	30*2	—	—	Year	Ta = +85°C

Note 1. Definition of reprogram/erase cycle:
The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 128-byte programming is performed 16 times for different addresses in 2-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).
Note 2. The value is obtained from the reliability test.

Table 6.23 E^2 DataFlash (Flash Memory for Data Storage) Characteristics (2)

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item		Symbol	min	typ	max	Unit	Test Condition
Programming time	2 bytes	t_{DP2}	—	0.25	2	ms	FCLK = 50 MHz
Erasure time	32 bytes	t_{DE32}	—	2	20	ms	FCLK = 50 MHz $N_{DPEC} \leq 100$
	32 bytes	t_{DE32}	—	4	20	ms	FCLK = 50 MHz $N_{DPEC} > 100$
Blank check time	2 bytes	t_{DBC2}	—	—	30	µs	FCLK = 50 MHz
Suspend delay time during programming		t_{DSPD}	—	—	120	µs	Figure 6.31 PCLKB = 50 MHz
First suspend delay time during erasing (in suspend priority mode)		t_{DSESD1}	—	—	120	µs	
Second suspend delay time during erasing (in suspend priority mode)		t_{DSESD2}	—	—	300	µs	
Suspend delay time during erasing (in erasure priority mode)		t_{DSEED}	—	—	300	µs	

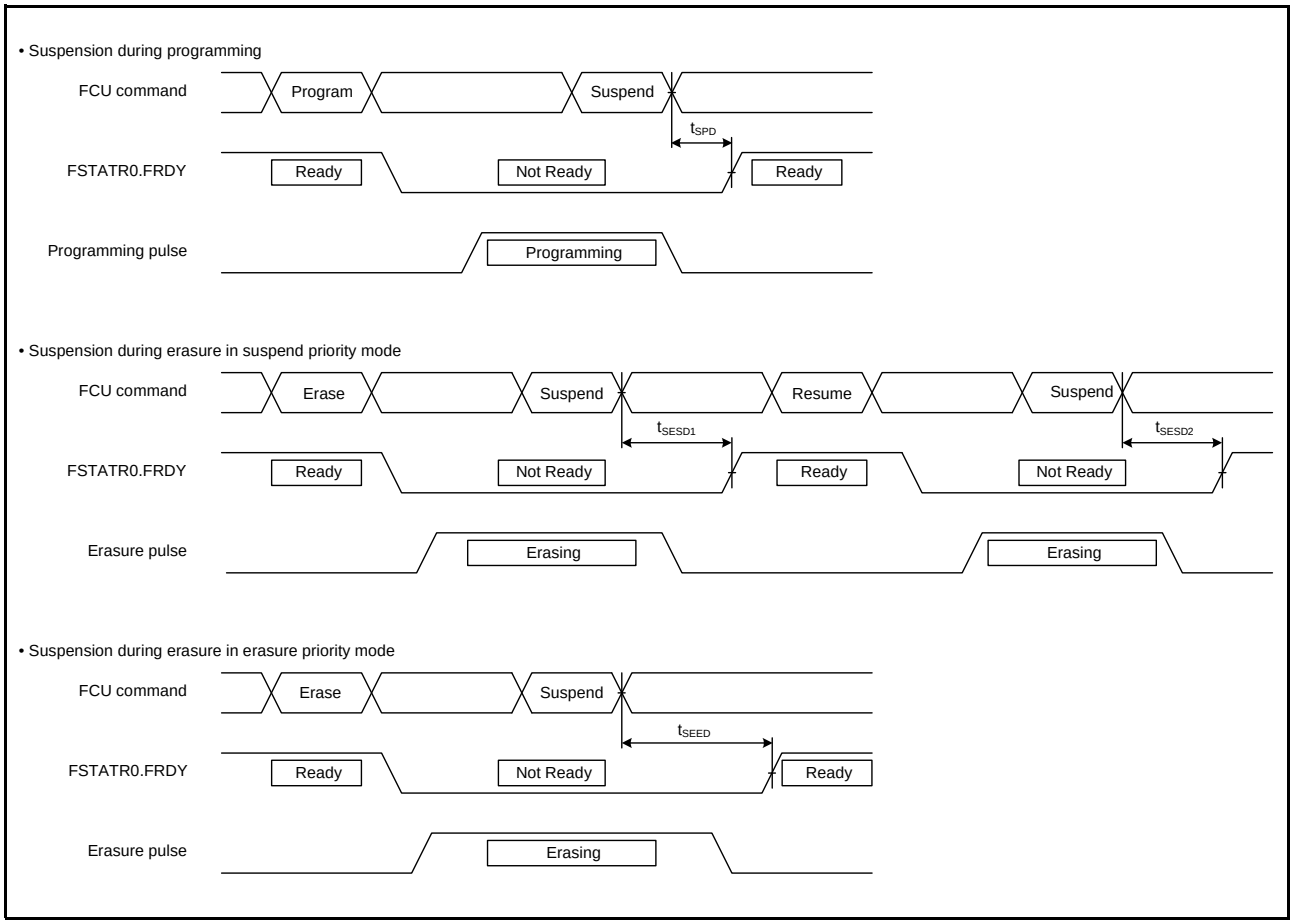


Figure 6.31 Flash Memory Program/Erase Suspend Timing