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Details

Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	72
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x10b, 8x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	120-LQFP
Supplier Device Package	120-LQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f563teadfa-v1

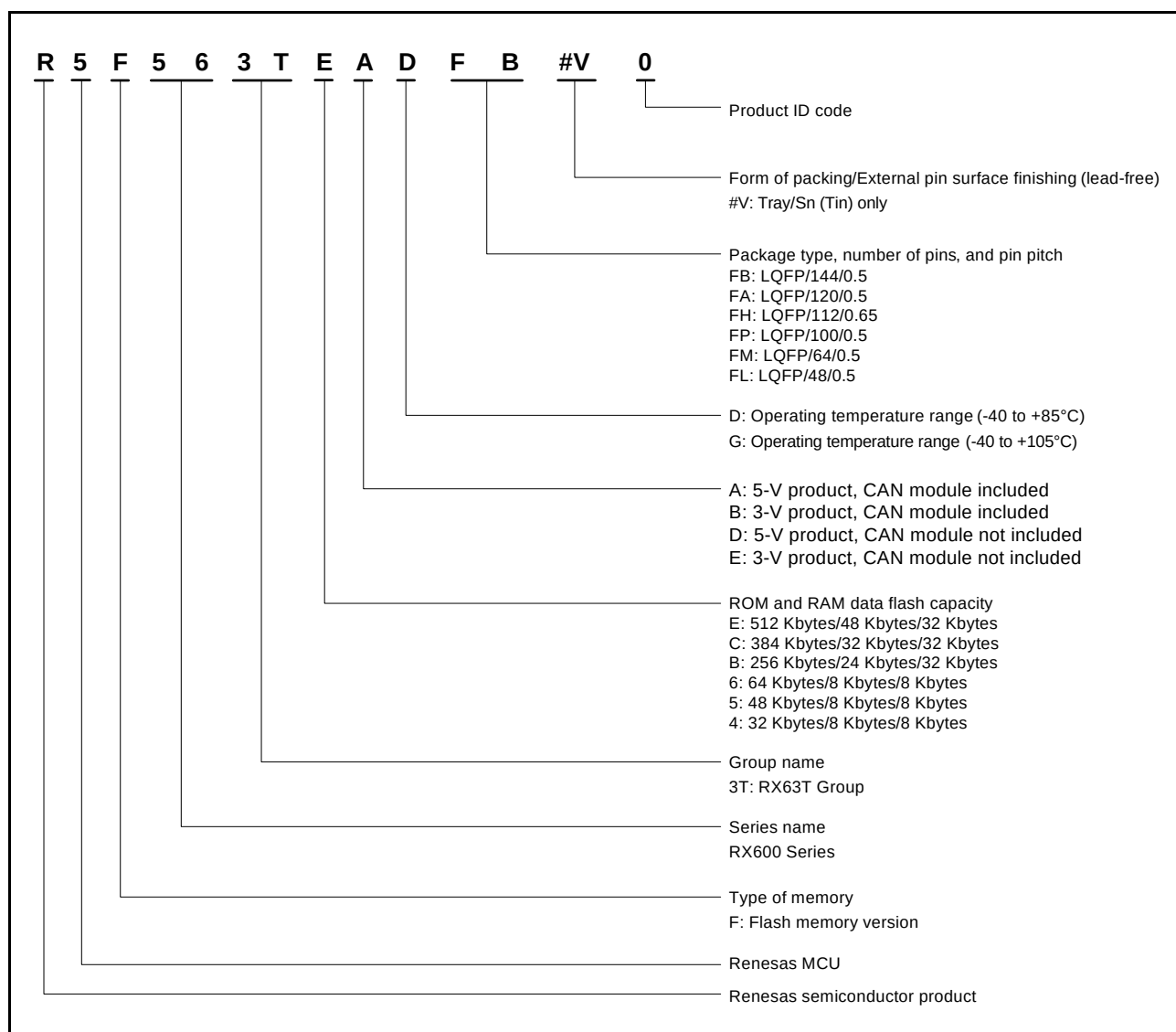


Figure 1.1 How to Read the Product Part Number

Table 1.8 List of Pins and Pin Functions (100-Pin LQFP) (2/3)

Pin Number 100-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3, GPT, POE3, CAC)	Communications (SCIC, SCID, RSPI, RIIC, CAN)	Interrupt	S12ADB, AD, DA
37		PA4		MTIOC1B	TXD0/SMOSI0/ SSDA0/ RSPCKA/RSPCKB		ADTRG0#
38		PA3		MTIOC2A	SCK0/SSLA0/SSLB0		
39		PA2		MTIOC2B	RXD2/SMISO2/ SSCL2/ SSLA1/SSLB1		
40		PA1		MTIOC6A	TXD2/SMOSI2/ SSDA2/ SSLA2/SSLB2		
41		PA0		MTIOC6C	SCK2/SSLA3/SSLB3		
42	VCC						
43		P96	A13	POE4#	RXD1/SMISO1/SSCL1	IRQ4-DS	
44	VSS						
45		P95		MTIOC6B/GTIOC4A	TXD1/SMOSI1/SSDA1		
46		P94		MTIOC7A/GTIOC5A	CTS1#/RTS1#/SS1#		
47		P93		MTIOC7B/GTIOC6A	CTS2#/RTS2#/SS2#		
48		P92		MTIOC6D/GTIOC4B			
49		P91		MTIOC7C/GTIOC5B			
50		P90		MTIOC7D/GTIOC6B			
51		P76	D0/[A0/D0]	MTIOC4D/GTIOC2B			
52		P75	D1/[A1/D1]	MTIOC4C/GTIOC1B			
53		P74	D2/[A2/D2]	MTIOC3D/GTIOC0B			
54		P73	D3/[A3/D3]	MTIOC4B/GTIOC2A			
55		P72	D4/[A4/D4]	MTIOC4A/GTIOC1A			
56		P71	D5/[A5/D5]	MTIOC3B/GTIOC0A			
57		P70	D6/[A6/D6]	POE0#	CTS1#/RTS1#/SS1#	IRQ5-DS	
58		P33	D7/[A7/D7]	MTIOC3A/MTCLKA	SSLA3/SSLB3		
59		P32	D8/[A8/D8]	MTIOC3C/MTCLKB	SSLA2/SSLB2		
60	VCC						
61		P31	D9/[A9/D9]	MTIOC0A/MTCLKC	SSLA1/SSLB1		
62	VSS						
63		P30	D10/[A10/ D10]	MTIOC0B/MTCLKD	SCK0/SSLA0/SSLB0		
64		P24	D11/[A11/D11]		CTS0#/RTS0#/SS0#/ RSPCKA/RSPCKB	IRQ4	
65		P23	D12/[A12/ D12]	CACREF	TXD0/SMOSI0/ SSDA0/MOSIA/ MOSIB/CTX1		
66		P22	D13/[A13/ D13]		RXD0/SMISO0/ SSCL0/MISOA/ MISOB/CRX1		ADTRG#
67		P21	D14/[A14/ D14]	MTCLKA		IRQ6-DS	ADTRG1#
68		P20	D15/[A15/ D15]	MTCLKB		IRQ7-DS	ADTRG0#
69		P65	A0/BC0#				AN5
70		P64	A1				AN4

4. I/O Registers

This section gives information on the on-chip I/O register addresses. The information is given as shown below. Notes on writing to registers are also given at the end.

(1) I/O register addresses (address order)

- Registers are listed from the lower allocation addresses.
- Registers are classified according to module symbols.
- The number of access cycles indicates the number of cycles based on the specified reference clock.
- Among the internal I/O register area, addresses not listed in the list of registers are reserved. Reserved addresses must not be accessed. Do not access these addresses; otherwise, the operation when accessing these bits and subsequent operations cannot be guaranteed.

(2) Notes on writing to I/O registers

When writing to an I/O register, the CPU starts executing the subsequent instruction before completing I/O register write. This may cause the subsequent instruction to be executed before the post-update I/O register value is reflected on the operation.

As described in the following examples, special care is required for the cases in which the subsequent instruction must be executed after the post-update I/O register value is actually reflected.

[Examples of cases requiring special care]

- The subsequent instruction must be executed while an interrupt request is disabled with the IENj bit in IERN of the ICU (interrupt request enable bit) cleared to 0.
- A WAIT instruction is executed immediately after the preprocessing for causing a transition to the low power consumption state.

In the above cases, after writing to an I/O register, wait until the write operation is completed using the following procedure and then execute the subsequent instruction.

- Write to an I/O register.
- Read the value from the I/O register to a general register.
- Execute the operation using the value read.
- Execute the subsequent instruction.

[Instruction examples]

- Byte-size I/O registers

```
MOV.L #SFR_ADDR, R1
MOV.B #SFR_DATA, [R1]
CMP [R1].UB, R1
;; Next process
```

- Word-size I/O registers

```
MOV.L #SFR_ADDR, R1
MOV.W #SFR_DATA, [R1]
CMP [R1].W, R1
;; Next process
```

Table 4.1 List of I/O Registers (Address Order) (5/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 703Eh	ICU	Interrupt Request Register 062	IR062	8	8	2 ICLK		ICUB	Not present in versions with 64 or 48 pins.
0008 7040h	ICU	Interrupt Request Register 064	IR064	8	8	2 ICLK			
0008 7041h	ICU	Interrupt Request Register 065	IR065	8	8	2 ICLK			
0008 7042h	ICU	Interrupt Request Register 066	IR066	8	8	2 ICLK			
0008 7043h	ICU	Interrupt Request Register 067	IR067	8	8	2 ICLK			
0008 7044h	ICU	Interrupt Request Register 068	IR068	8	8	2 ICLK			
0008 7045h	ICU	Interrupt Request Register 069	IR069	8	8	2 ICLK			
0008 7046h	ICU	Interrupt Request Register 070	IR070	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7047h	ICU	Interrupt Request Register 071	IR071	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 705Ah	ICU	Interrupt Request Register 090	IR090	8	8	2 ICLK			Not present in versions with 112, 100, 64 or 48 pins.
0008 7062h	ICU	Interrupt Request Register 098	IR098	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7066h	ICU	Interrupt Request Register 102	IR102	8	8	2 ICLK			
0008 7067h	ICU	Interrupt Request Register 103	IR103	8	8	2 ICLK			
0008 7068h	ICU	Interrupt Request Register 104	IR104	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7069h	ICU	Interrupt Request Register 105	IR105	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 706Ah	ICU	Interrupt Request Register 106	IR106	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7072h	ICU	Interrupt Request Register 114	IR114	8	8	2 ICLK			
0008 707Ah	ICU	Interrupt Request Register 122	IR122	8	8	2 ICLK			
0008 707Bh	ICU	Interrupt Request Register 123	IR123	8	8	2 ICLK			
0008 707Ch	ICU	Interrupt Request Register 124	IR124	8	8	2 ICLK			
0008 707Dh	ICU	Interrupt Request Register 125	IR125	8	8	2 ICLK			
0008 707Eh	ICU	Interrupt Request Register 126	IR126	8	8	2 ICLK			
0008 707Fh	ICU	Interrupt Request Register 127	IR127	8	8	2 ICLK			
0008 7080h	ICU	Interrupt Request Register 128	IR128	8	8	2 ICLK			
0008 7081h	ICU	Interrupt Request Register 129	IR129	8	8	2 ICLK			
0008 7082h	ICU	Interrupt Request Register 130	IR130	8	8	2 ICLK			
0008 7083h	ICU	Interrupt Request Register 131	IR131	8	8	2 ICLK			
0008 7084h	ICU	Interrupt Request Register 132	IR132	8	8	2 ICLK			
0008 7085h	ICU	Interrupt Request Register 133	IR133	8	8	2 ICLK			
0008 7086h	ICU	Interrupt Request Register 134	IR134	8	8	2 ICLK			
0008 7087h	ICU	Interrupt Request Register 135	IR135	8	8	2 ICLK			
0008 7088h	ICU	Interrupt Request Register 136	IR136	8	8	2 ICLK			
0008 7089h	ICU	Interrupt Request Register 137	IR137	8	8	2 ICLK			
0008 708Ah	ICU	Interrupt Request Register 138	IR138	8	8	2 ICLK			
0008 708Bh	ICU	Interrupt Request Register 139	IR139	8	8	2 ICLK			
0008 708Ch	ICU	Interrupt Request Register 140	IR140	8	8	2 ICLK			
0008 708Dh	ICU	Interrupt Request Register 141	IR141	8	8	2 ICLK			
0008 708Eh	ICU	Interrupt Request Register 142	IR142	8	8	2 ICLK			
0008 708Fh	ICU	Interrupt Request Register 143	IR143	8	8	2 ICLK			
0008 7090h	ICU	Interrupt Request Register 144	IR144	8	8	2 ICLK			
0008 7091h	ICU	Interrupt Request Register 145	IR145	8	8	2 ICLK			
0008 7092h	ICU	Interrupt Request Register 146	IR146	8	8	2 ICLK			
0008 7093h	ICU	Interrupt Request Register 147	IR147	8	8	2 ICLK			
0008 7094h	ICU	Interrupt Request Register 148	IR148	8	8	2 ICLK			
0008 7095h	ICU	Interrupt Request Register 149	IR149	8	8	2 ICLK			
0008 7096h	ICU	Interrupt Request Register 150	IR150	8	8	2 ICLK			
0008 7097h	ICU	Interrupt Request Register 151	IR151	8	8	2 ICLK			

Table 4.1 List of I/O Registers (Address Order) (6/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK $\geq$ PCLK	ICLK $<$ PCLK		
0008 7098h	ICU	Interrupt Request Register 152	IR152	8	8	2 ICLK		ICUb	
0008 7099h	ICU	Interrupt Request Register 153	IR153	8	8	2 ICLK			
0008 709Ah	ICU	Interrupt Request Register 154	IR154	8	8	2 ICLK			
0008 709Bh	ICU	Interrupt Request Register 155	IR155	8	8	2 ICLK			
0008 709Ch	ICU	Interrupt Request Register 156	IR156	8	8	2 ICLK			
0008 709Dh	ICU	Interrupt Request Register 157	IR157	8	8	2 ICLK			
0008 709Eh	ICU	Interrupt Request Register 158	IR158	8	8	2 ICLK			
0008 70A1h	ICU	Interrupt Request Register 161	IR161	8	8	2 ICLK			
0008 70A2h	ICU	Interrupt Request Register 162	IR162	8	8	2 ICLK			
0008 70A3h	ICU	Interrupt Request Register 163	IR163	8	8	2 ICLK			
0008 70A4h	ICU	Interrupt Request Register 164	IR164	8	8	2 ICLK			
0008 70A5h	ICU	Interrupt Request Register 165	IR165	8	8	2 ICLK			
0008 70A6h	ICU	Interrupt Request Register 166	IR166	8	8	2 ICLK			
0008 70A7h	ICU	Interrupt Request Register 167	IR167	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70A8h	ICU	Interrupt Request Register 168	IR168	8	8	2 ICLK			
0008 70A9h	ICU	Interrupt Request Register 169	IR169	8	8	2 ICLK			
0008 70AAh	ICU	Interrupt Request Register 170	IR170	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70ABh	ICU	Interrupt Request Register 171	IR171	8	8	2 ICLK			
0008 70ACh	ICU	Interrupt Request Register 172	IR172	8	8	2 ICLK			
0008 70ADh	ICU	Interrupt Request Register 173	IR173	8	8	2 ICLK			
0008 70AEh	ICU	Interrupt Request Register 174	IR174	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70AFh	ICU	Interrupt Request Register 175	IR175	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70B0h	ICU	Interrupt Request Register 176	IR176	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70B1h	ICU	Interrupt Request Register 177	IR177	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70B2h	ICU	Interrupt Request Register 178	IR178	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70B3h	ICU	Interrupt Request Register 179	IR179	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70B4h	ICU	Interrupt Request Register 180	IR180	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70B5h	ICU	Interrupt Request Register 181	IR181	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70B6h	ICU	Interrupt Request Register 182	IR182	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70B7h	ICU	Interrupt Request Register 183	IR183	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70B8h	ICU	Interrupt Request Register 184	IR184	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70B9h	ICU	Interrupt Request Register 185	IR185	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70BAh	ICU	Interrupt Request Register 186	IR186	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70BBh	ICU	Interrupt Request Register 187	IR187	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70BCh	ICU	Interrupt Request Register 188	IR188	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70BDh	ICU	Interrupt Request Register 189	IR189	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70BEh	ICU	Interrupt Request Register 190	IR190	8	8	2 ICLK			Not present in versions with 112, 100, 64 or 48 pins.
0008 70BFh	ICU	Interrupt Request Register 191	IR191	8	8	2 ICLK			Not present in versions with 112, 100, 64 or 48 pins.

Table 4.1 List of I/O Registers (Address Order) (8/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK $\geq$ PCLK	ICLK $<$ PCLK		
0008 711Bh	ICU	DTC Activation Enable Register 027	DTCER027	8	8	2 ICLK		ICUb	
0008 711Ch	ICU	DTC Activation Enable Register 028	DTCER028	8	8	2 ICLK			
0008 711Dh	ICU	DTC Activation Enable Register 029	DTCER029	8	8	2 ICLK			
0008 711Eh	ICU	DTC Activation Enable Register 030	DTCER030	8	8	2 ICLK			
0008 711Fh	ICU	DTC Activation Enable Register 031	DTCER031	8	8	2 ICLK			
0008 7121h	ICU	DTC Activation Enable Register 033	DTCER033	8	8	2 ICLK			Not present in versions with 112, 100, 64 or 48 pins.
0008 7122h	ICU	DTC Activation Enable Register 034	DTCER034	8	8	2 ICLK			Not present in versions with 112, 100, 64 or 48 pins.
0008 7127h	ICU	DTC Activation Enable Register 039	DTCER039	8	8	2 ICLK			
0008 7128h	ICU	DTC Activation Enable Register 040	DTCER040	8	8	2 ICLK			
0008 712Ah	ICU	DTC Activation Enable Register 042	DTCER042	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 712Bh	ICU	DTC Activation Enable Register 043	DTCER043	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7131h	ICU	DTC Activation Enable Register 049	DTCER049	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7132h	ICU	DTC Activation Enable Register 050	DTCER050	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7133h	ICU	DTC Activation Enable Register 051	DTCER051	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7134h	ICU	DTC Activation Enable Register 052	DTCER052	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7135h	ICU	DTC Activation Enable Register 053	DTCER053	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7136h	ICU	DTC Activation Enable Register 054	DTCER054	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7137h	ICU	DTC Activation Enable Register 055	DTCER055	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7138h	ICU	DTC Activation Enable Register 056	DTCER056	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 713Ah	ICU	DTC Activation Enable Register 058	DTCER058	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 713Bh	ICU	DTC Activation Enable Register 059	DTCER059	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 713Ch	ICU	DTC Activation Enable Register 060	DTCER060	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 713Dh	ICU	DTC Activation Enable Register 061	DTCER061	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 713Eh	ICU	DTC Activation Enable Register 062	DTCER062	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7140h	ICU	DTC Activation Enable Register 064	DTCER064	8	8	2 ICLK			
0008 7141h	ICU	DTC Activation Enable Register 065	DTCER065	8	8	2 ICLK			
0008 7142h	ICU	DTC Activation Enable Register 066	DTCER066	8	8	2 ICLK			
0008 7143h	ICU	DTC Activation Enable Register 067	DTCER067	8	8	2 ICLK			
0008 7144h	ICU	DTC Activation Enable Register 068	DTCER068	8	8	2 ICLK			
0008 7145h	ICU	DTC Activation Enable Register 069	DTCER069	8	8	2 ICLK			
0008 7146h	ICU	DTC Activation Enable Register 070	DTCER070	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7147h	ICU	DTC Activation Enable Register 071	DTCER071	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7162h	ICU	DTC Activation Enable Register 098	DTCER098	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7166h	ICU	DTC Activation Enable Register 102	DTCER102	8	8	2 ICLK			
0008 7167h	ICU	DTC Activation Enable Register 103	DTCER103	8	8	2 ICLK			
0008 7168h	ICU	DTC Activation Enable Register 104	DTCER104	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7169h	ICU	DTC Activation Enable Register 105	DTCER105	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 717Eh	ICU	DTC Activation Enable Register 126	DTCER126	8	8	2 ICLK			

Table 4.1 List of I/O Registers (Address Order) (16/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 8330h	RIIC1	I ² C Bus Bit Rate Low-Level Register	ICBRL	8	8	2, 3 PCLKB	2 ICLK	RIIC	Not present in versions with 112, 100, 64, or 48 pins.
0008 8331h	RIIC1	I ² C Bus Bit Rate High-Level Register	ICBRH	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
0008 8332h	RIIC1	I ² C Bus Transmit Data Register	ICDRT	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
0008 8333h	RIIC1	I ² C Bus Receive Data Register	ICDRR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
0008 8380h	RSPI0	RSPI Control Register	SPCR	8	8	2, 3 PCLKB	2 ICLK	RSPI	
0008 8381h	RSPI0	RSPI Slave Select Polarity Register	SSLP	8	8	2, 3 PCLKB	2 ICLK		
0008 8382h	RSPI0	RSPI Pin Control Register	SPPCR	8	8	2, 3 PCLKB	2 ICLK		
0008 8383h	RSPI0	RSPI Status Register	SPSR	8	8	2, 3 PCLKB	2 ICLK		
0008 8384h	RSPI0	RSPI Data Register	SPDR	32	16, 32	2, 3 PCLKB	2 ICLK		
0008 8388h	RSPI0	RSPI Sequence Control Register	SPSCR	8	8	2, 3 PCLKB	2 ICLK		
0008 8389h	RSPI0	RSPI Sequence Status Register	SPSSR	8	8	2, 3 PCLKB	2 ICLK		
0008 838Ah	RSPI0	RSPI Bit Rate Register	SPBR	8	8	2, 3 PCLKB	2 ICLK		
0008 838Bh	RSPI0	RSPI Data Control Register	SPDCR	8	8	2, 3 PCLKB	2 ICLK		
0008 838Ch	RSPI0	RSPI Clock Delay Register	SPCKD	8	8	2, 3 PCLKB	2 ICLK		
0008 838Dh	RSPI0	RSPI Slave Select Negation Delay Register	SSLND	8	8	2, 3 PCLKB	2 ICLK		
0008 838Eh	RSPI0	RSPI Next-Access Delay Register	SPND	8	8	2, 3 PCLKB	2 ICLK		
0008 838Fh	RSPI0	RSPI Control Register 2	SPCR2	8	8	2, 3 PCLKB	2 ICLK		
0008 8390h	RSPI0	RSPI Command Register 0	SPCMD0	16	16	2, 3 PCLKB	2 ICLK		
0008 8392h	RSPI0	RSPI Command Register 1	SPCMD1	16	16	2, 3 PCLKB	2 ICLK		
0008 8394h	RSPI0	RSPI Command Register 2	SPCMD2	16	16	2, 3 PCLKB	2 ICLK		
0008 8396h	RSPI0	RSPI Command Register 3	SPCMD3	16	16	2, 3 PCLKB	2 ICLK		
0008 8398h	RSPI0	RSPI Command Register 4	SPCMD4	16	16	2, 3 PCLKB	2 ICLK		
0008 839Ah	RSPI0	RSPI Command Register 5	SPCMD5	16	16	2, 3 PCLKB	2 ICLK		
0008 839Ch	RSPI0	RSPI Command Register 6	SPCMD6	16	16	2, 3 PCLKB	2 ICLK		
0008 839Eh	RSPI0	RSPI Command Register 7	SPCMD7	16	16	2, 3 PCLKB	2 ICLK		
0008 83A0h	RSPI1	RSPI Control Register	SPCR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 83A1h	RSPI1	RSPI Slave Select Polarity Register	SSLP	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 83A2h	RSPI1	RSPI Pin Control Register	SPPCR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 83A3h	RSPI1	RSPI Status Register	SPSR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 83A4h	RSPI1	RSPI Data Register	SPDR	32	16, 32	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 83A8h	RSPI1	RSPI Sequence Control Register	SPSCR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 83A9h	RSPI1	RSPI Sequence Status Register	SPSSR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 83AAh	RSPI1	RSPI Bit Rate Register	SPBR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 83ABh	RSPI1	RSPI Data Control Register	SPDCR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 83ACh	RSPI1	RSPI Clock Delay Register	SPCKD	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 83ADh	RSPI1	RSPI Slave Select Negation Delay Register	SSLND	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 83AEh	RSPI1	RSPI Next-Access Delay Register	SPND	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 83AFh	RSPI1	RSPI Control Register 2	SPCR2	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 83B0h	RSPI1	RSPI Command Register 0	SPCMD0	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.

Table 4.1 List of I/O Registers (Address Order) (24/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 C086h	PORT3	Open Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK	I/O Ports	Not present in versions with 144, 120, 112, or 100 pins.
0008 C087h	PORT3	Open Drain Control Register 1	ODR1	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64 or 48 pins.
0008 C090h	PORT8	Open Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C092h	PORT9	Open Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 144, 120, 112, 100 or 48 pins.
0008 C093h	PORT9	Open Drain Control Register 1	ODR1	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 48 pins.
0008 C094h	PORTA	Open Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C095h	PORTA	Open Drain Control Register 1	ODR1	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C096h	PORTB	Open Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK		
0008 C097h	PORTB	Open Drain Control Register 1	ODR1	8	8	2, 3 PCLKB	2 ICLK		
0008 C09Ah	PORTD	Open Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK		
0008 C09Bh	PORTD	Open Drain Control Register 1	ODR1	8	8	2, 3 PCLKB	2 ICLK		
0008 C09Eh	PORTF	Open Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 100, 64, or 48 pins.
0008 C0A0h	PORTG	Open Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 100, 64, or 48 pins.
0008 C0A1h	PORTG	Open Drain Control Register 1	ODR1	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 100, 64, or 48 pins.
0008 C0F2h	PORT	Driving Ability Control Register 1	DSCR1	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C0F3h	PORT	Driving Ability Control Register 2	DSCR2	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C100h	MPC	CS Output Enable Register	PFCSE	8	8	2, 3 PCLKB	2 ICLK	MPC	Not present in versions with 64 or 48 pins.
0008 C102h	MPC	CS Output Pin Select Register 0	PFCSS0	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C104h	MPC	Address Output Enable Register 0	PFAOE0	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C105h	MPC	Address Output Enable Register 1	PFAOE1	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C106h	MPC	External Bus Control Register 0	PFBCR0	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C107h	MPC	External Bus Control Register 1	PFBCR1	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C114h	MPC	USB0 Control Register	PFUSB0	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
0008 C11Fh	MPC	Write-Protect Register	PWPR	8	8	2, 3 PCLKB	2 ICLK		
0008 C140h	MPC	P00 Pin Function Control Register	P00PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 48 pins.
0008 C141h	MPC	P01 Pin Function Control Register	P01PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 48 pins.
0008 C142h	MPC	P02 Pin Function Control Register	P02PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 C143h	MPC	P03 Pin Function Control Register	P03PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 C148h	MPC	P10 Pin Function Control Register	P10PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 48 pins.
0008 C149h	MPC	P11 Pin Function Control Register	P11PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 48 pins.
0008 C14Ah	MPC	P12 Pin Function Control Register	P12PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 100, 64, or 48 pins.
0008 C14Bh	MPC	P13 Pin Function Control Register	P13PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 112, 100, 64, or 48 pins.

Table 4.1 List of I/O Registers (Address Order) (40/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK $\geq$ PCLK	ICLK $<$ PCLK		
000C 2230h	GPT2	A/D Converter Start Request Timing Double-Buffer Register B	GTADTDBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK	GPT	
000C 2234h	GPT2	General PWM Timer Output Negate Control Register	GTONCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2236h	GPT2	General PWM Timer Dead Time Control Register	GTDTCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2238h	GPT2	General PWM Timer Dead Time Value Register U	GTDVU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 223Ah	GPT2	General PWM Timer Dead Time Value Register D	GTDVD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 223Ch	GPT2	General PWM Timer Dead Time Buffer Register U	GTDBU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 223Eh	GPT2	General PWM Timer Dead Time Buffer Register D	GTDBD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2240h	GPT2	General PWM Timer Output Protection Function Status Register	GTSOS	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2242h	GPT2	General PWM Timer Output Protection Function Temporary Release Register	GTSOTR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2280h	GPT3	General PWM Timer I/O Control Register	GTIOR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2282h	GPT3	General PWM Timer Interrupt Output Setting Register	GTINTAD	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2284h	GPT3	General PWM Timer Control Register	GTCR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2286h	GPT3	General PWM Timer Buffer Enable Register	GTBER	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2288h	GPT3	General PWM Timer Count Direction Register	GTUDC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 228Ah	GPT3	General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register	GTITC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 228Ch	GPT3	General PWM Timer Status Register	GTST	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 228Eh	GPT3	General PWM Timer Counter	GTCNT	16	16	2 to 5 PCLKA	2, 3 ICLK		
000C 2290h	GPT3	General PWM Timer Compare Capture Register A	GTCCRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2292h	GPT3	General PWM Timer Compare Capture Register B	GTCCRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2294h	GPT3	General PWM Timer Compare Capture Register C	GTCCRC	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2296h	GPT3	General PWM Timer Compare Capture Register D	GTCCRD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2298h	GPT3	General PWM Timer Compare Capture Register E	GTCCRE	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 229Ah	GPT3	General PWM Timer Compare Capture Register F	GTCCRF	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 229Ch	GPT3	General PWM Timer Cycle Setting Register	GTPR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 229Eh	GPT3	General PWM Timer Cycle Setting Buffer Register	GTPBR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 22A0h	GPT3	General PWM Timer Cycle Setting Double-Buffer Register	GTPDBR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 22A4h	GPT3	A/D Converter Start Request Timing Register A	GTADTRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 22A6h	GPT3	A/D Converter Start Request Timing Buffer Register A	GTADTBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 22A8h	GPT3	A/D Converter Start Request Timing Double-Buffer Register A	GTADTDBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 22ACh	GPT3	A/D Converter Start Request Timing Register B	GTADTRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 22AEh	GPT3	A/D Converter Start Request Timing Buffer Register B	GTADTBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 22B0h	GPT3	A/D Converter Start Request Timing Double-Buffer Register B	GTADTDBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 22B4h	GPT3	General PWM Timer Output Negate Control Register	GTONCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 22B6h	GPT3	General PWM Timer Dead Time Control Register	GTDTCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 22B8h	GPT3	General PWM Timer Dead Time Value Register U	GTDVU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		

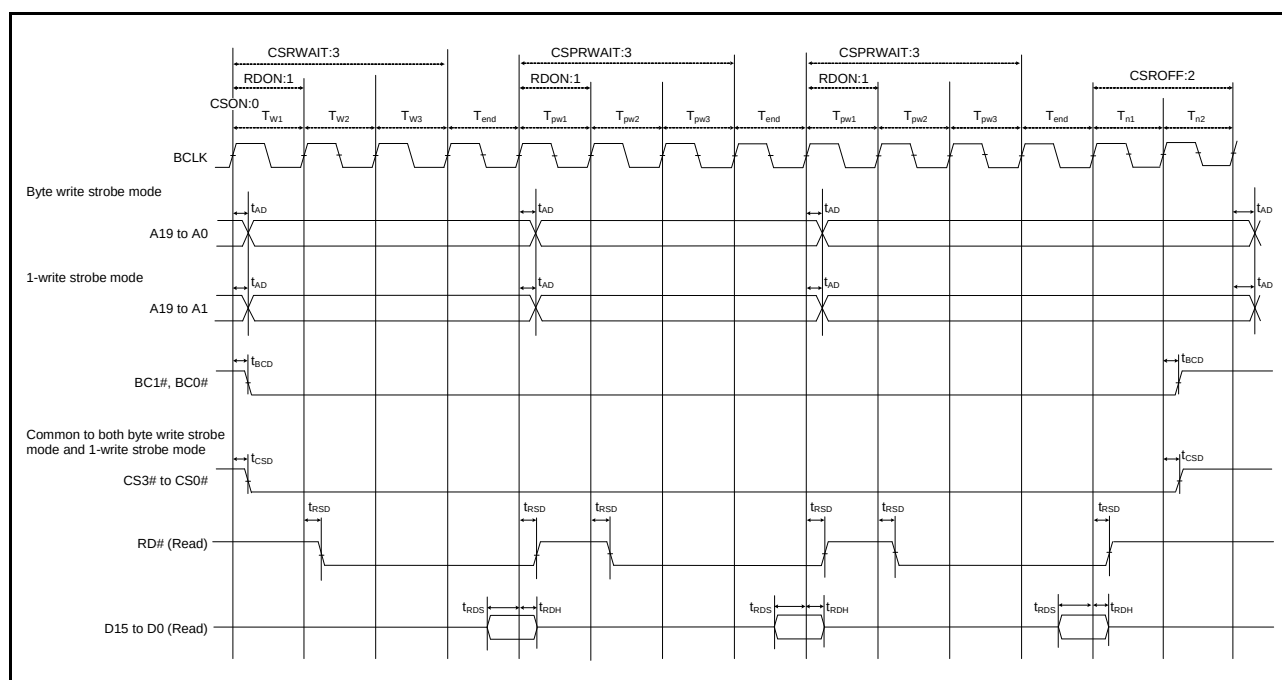


Figure 5.15 External Bus Timing/Page Read Cycle (Bus Clock Synchronized)

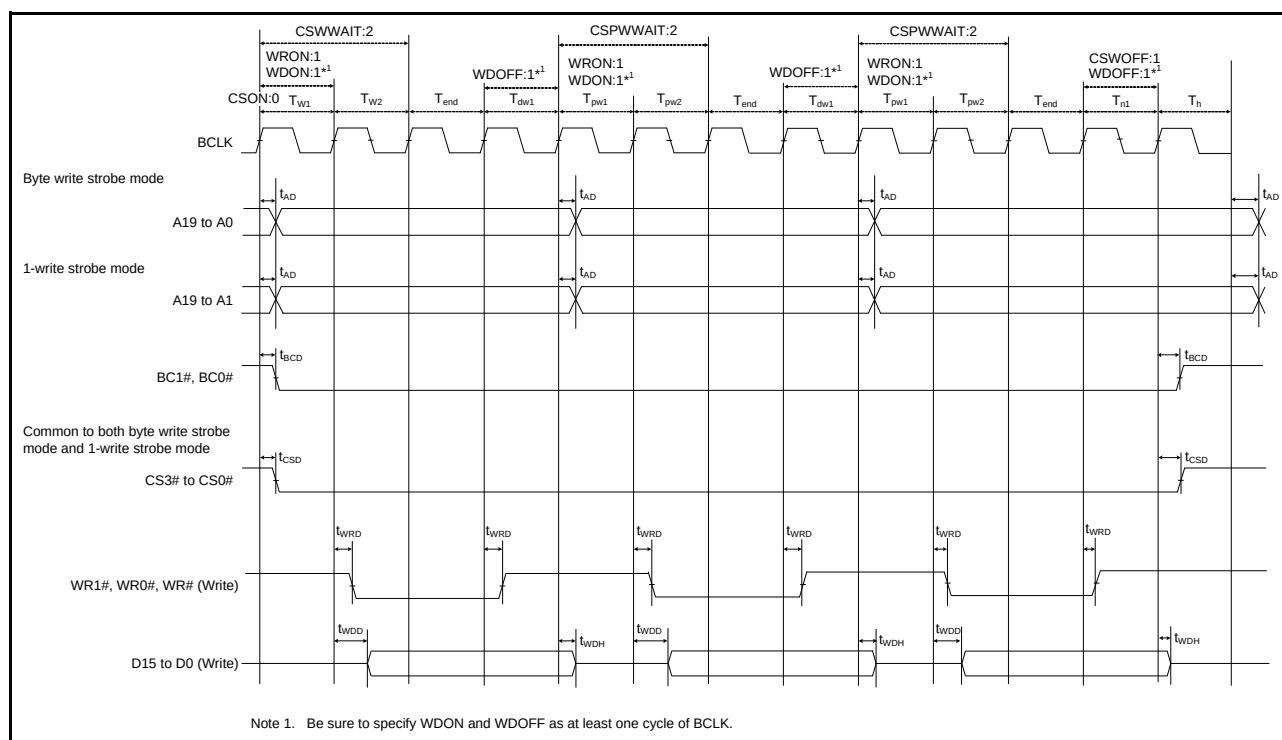


Figure 5.16 External Bus Timing/Page Write Cycle (Bus Clock Synchronized)

5.3.6 Timing of On-Chip Peripheral Modules

Table 5.16 Timing of On-Chip Peripheral Modules (1)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

T_a = T_{opr}. T_a is common to conditions 1 to 3.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
I/O ports	Input data pulse width		t _{PRW}	1.5	—	t _{PCyc}	Figure 5.22
MTU3	Input capture input pulse width	Single-edge setting	t _{TICW}	3	—	t _{PAcyc}	Figure 5.23
		Both-edge setting		5	—		
	Input capture input fall time		t _{TICTF}	—	0.1	μs/V	When Input capture at rising edge, or Input capture at both edges is selected.
	Timer clock pulse width	Single-edge setting	t _{TCKWH} , t _{TCKWL}	3	—	t _{PAcyc}	Figure 5.25
		Both-edge setting		5	—		
		Phase counting mode		5	—		
	Timer clock input fall time		t _{TCKTF}	—	0.1	μs/V	
POE3	POE# input pulse width		t _{POEW}	1.5	—	t _{PCyc}	Figure 5.28
GPT	Input capture input pulse width	Single-edge setting	t _{GTICW}	3	—	t _{PAcyc}	Figure 5.26
		Both-edge setting		5	—		
	Input capture input fall time		t _{GTICTF}	—	0.1	μs/V	When Input capture at rising edge, or Input capture at both edges is selected. When Count operation is started at rising edge, or Count operation is started at both edges is selected. When Count operation is stopped at rising edge, or Count operation is stopped at both edges is selected. When Counter is cleared at rising edge, or Counter is cleared at both edges is selected.
	External trigger input pulse width	Single-edge setting	t _{OTETW}	3	—	t _{PAcyc}	Figure 5.27
		Both-edge setting		5	—		
	External trigger input fall time		t _{GTETRGTF}	—	0.1	μs/V	When Count operation is started at rising edge, or Count operation is started at both edges is selected. When Count operation is stopped at rising edge, or Count operation is stopped at both edges is selected. When Counter is cleared at rising edge, or Counter is cleared at both edges is selected.

Table 5.16 Timing of On-Chip Peripheral Modules (2)

Note: Common standard values for conditions not given in the table are listed as "Condition 1" to "Condition 3" below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$ T_a is common to conditions 1 to 3.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
SCI	Input clock cycle	Asynchronous	t_{Scyc}	4	—	t_{Pcyc}	C = 30 pF Figure 5.29
		Clock synchronous		6	—		
	Input clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time		t_{SCKr}	—	20	ns	
	Input clock fall time		t_{SCKf}	—	20	ns	
	Output clock cycle	Asynchronous	t_{Scyc}	16	—	t_{Pcyc}	
		Clock synchronous		4	—		
	Output clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time		t_{SCKr}	—	20	ns	
	Output clock fall time		t_{SCKf}	—	20	ns	
	Transmit data delay time	Clock synchronous	t_{TXD}	—	40	ns	Figure 5.30
	Receive data setup time	Clock synchronous	t_{RXS}	40	—	ns	
	Receive data hold time	Clock synchronous	t_{RXH}	40	—	ns	
		Receive data fall time		t_{TICTF}	—	0.1	μs/V
A/D converter	10-bit A/D converter trigger input pulse width		t_{TRGW}	1.5	—	t_{Pcyc}	Figure 5.31
	12-bit A/D converter trigger input pulse width			1.5	—		
CAC	CACREF input pulse width	$t_{Pcyc} \leq t_{cac}^{*2}$	t_{CACREF}	$4.5 t_{cac} + 3 t_{Pcyc}$	—	ns	
		$t_{Pcyc} > t_{cac}^{*2}$		$5 t_{cac} + 6.5 t_{Pcyc}$	—	ns	
	CACREF input fall time		$t_{CACREFTF}$	—	0.1	μs/V	

Note 1. t_{Pcyc} : PCLK cycle, t_{PAcyc} : PCLKA cycle

Note 2. t_{cac} : CAC count clock source cycle.

5.7 Power-on Reset Circuit and Voltage Detection Circuit Characteristics

Table 5.26 Power-on Reset Circuit and Voltage Detection Circuit Characteristics (1)

Note: Common standard values for conditions not given in the table are listed as "Condition 1" and "Condition 2" below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$, T_a is common to conditions 1 and 2.

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	V_{POR}	2.46	2.58	2.7	V	Figure 5.41
	Voltage detection circuit (LVD0)	V_{DET0}	2.7	2.82	2.94		Figure 5.42
	Voltage detection circuit (LVD1)*1	V_{DET1_8}	2.75	2.90	3.05		Figure 5.43
		V_{DET1_9}	2.70	2.85	3.00		
		V_{DET1_A}	2.73	2.88	3.03		
	Voltage detection circuit (LVD2)*2	V_{DET2_8}	2.75	2.9	3.05		Figure 5.44
		V_{DET2_9}	2.70	2.85	3.00		
		V_{DET2_A}	2.73	2.88	3.03		
Internal reset time	Power-on reset (POR)	t_{POR}		9.7		ms	Figure 5.41
	Voltage detection circuit (LVD0)	t_{LVD0}		9.7			Figure 5.42
	Voltage detection circuit (LVD1)	t_{LVD1}		0.9			Figure 5.43
	Voltage detection circuit (LVD2)	t_{LVD2}		0.9			Figure 5.44
Minimum VCC down time*3		t_{VOFF}	200	—	—	μs	Figure 5.41 and Figure 5.42
Response delay time		t_{DET}			200	μs	
LVD operation stabilization time (after LVD is enabled)		$T_{d(E-A)}$			3	μs	Figure 5.41 to Figure 5.44
Hysteresis width (LVD1 and LVD2)		V_{LVH}		80		mV	

Note 1. # in symbol $V_{DET1_#}$ indicates the value of the LVDLVLR.LVD1LVL[3:0] bits.

Note 2. # in symbol $V_{DET2_#}$ indicates the value of the LVDLVLR.LVD2LVL[3:0] bits.

Note 3. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR} , V_{DET1} , and V_{DET2} for the POR/ LVD.

6.3.3 Timing of Recovery from Low Power Consumption Modes

Table 6.9 Timing of Recovery from Low Power Consumption Modes

Conditions: $V_{CC} = 2.7$ to 3.6 V, $V_{SS} = AV_{SS0} = V_{REFL0} = 0$ V,
 $AV_{CC0} = 3.0$ to 3.6 V, $V_{REFH0} = 3.0$ V to AV_{CC0} ,
 $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time after cancellation of software standby mode	Crystal resonator connected to main clock oscillator operating	t_{SBYMC}	10	—	—	ms
	Main clock oscillator and PLL circuit operating	t_{SBYPC}	10	—	—	ms
	External clock input to main clock oscillator operating	t_{SBYEX}	1	—	—	ms
	Main clock oscillator and PLL circuit operating	t_{SBYPE}	1	—	—	ms
	Low-speed clock oscillator or IWDG-specific low-speed clock oscillator operating	t_{SBYLO}	—	—	800	μ s
Recovery time after cancellation of deep software standby mode	t_{DSBY}	—	—	1	ms	Figure 6.9
Wait time after cancellation of deep software standby mode	t_{DSBYWT}	45	—	46	t_{cyc}	

Note: • The wait time varies depending on the state in which each oscillator was when the WAIT instruction was executed. The recovery time when multiple oscillators are operating is the same period as that when the oscillator, which takes the longest time for recovery among the operating oscillators, is operating alone.

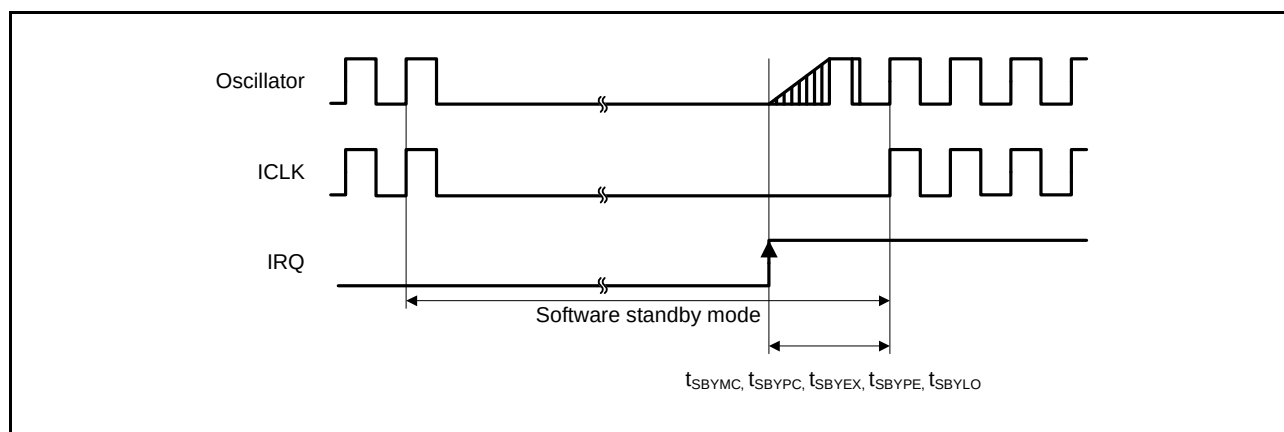


Figure 6.8 Software Standby Mode Cancellation Timing

Table 6.12 Timing of On-Chip Peripheral Modules (2)

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
 AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
 Ta = T_{opr}

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
RSPI	RSPCK clock cycle	Master	t _{SPcyc}	2	4096	t _{Pcyc}	Figure 6.20
		Slave		8	4096		
	RSPCK clock high pulse width	Master	t _{SPCKWH}	(t _{SPcyc} – t _{SPCKR} – t _{SPCKF}) / 2 – 3	—	ns	
		Slave		(t _{SPcyc} – t _{SPCKR} – t _{SPCKF}) / 2	—		
	RSPCK clock low pulse width	Master	t _{SPCKWL}	(t _{SPcyc} – t _{SPCKR} – t _{SPCKF}) / 2 – 3	—	ns	
		Slave		(t _{SPcyc} – t _{SPCKR} – t _{SPCKF}) / 2	—		
	RSPCK clock rise/fall time	Output	t _{SPCKR} , t _{SPCKF}	—	5	ns	
		Input		—	1	μs	
	Data input setup time	Master	t _{SU}	15	—	ns	Figure 6.21 to Figure 6.24
				20	—		
		Slave		20 – t _{Pcyc}	—		
	Data input hold time	Master	t _H	0	—	ns	
		Slave		20 + 2 × t _{Pcyc}	—		
	SSL setup time	Master	t _{LEAD}	1	8	t _{SPcyc}	
		Slave		4	—	t _{Pcyc}	
	SSL hold time	Master	t _{LAG}	1	8	t _{SPcyc}	
		Slave		4	—	t _{Pcyc}	
	Data output delay time	Master	t _{OD}	—	18	ns	
		Slave		—	3 × t _{Pcyc} + 40		
	Data output hold time	Master	t _{OH}	0	—	ns	
		Slave		0	—		
Successive transmission delay time	Master	t _{TD}	t _{SPcyc} + 2 × t _{Pcyc}	8 × t _{SPcyc} + 2 × t _{Pcyc}	ns		
	Slave		4 × t _{Pcyc}	—			
MOSI rise/fall time	Output	t _{MODR} , t _{MODF}	—	5	ns		
	Input		—	1	μs		
MISO rise/fall time	Output	t _{MODR} , t _{MODF}	—	5	ns		
	Input		—	1	μs		
SSL rise/fall time	Output	t _{SSLr} , t _{SSLf}	—	15	ns		
	Input		—	1	μs		
Slave access time			t _{SA}	—	4	t _{Pcyc}	Figure 6.23 and Figure 6.24
Slave output release time			t _{REL}	—	3	t _{Pcyc}	

Note 1. t_{PCyc}: PCLK cycle

Table 6.14 Timing of On-Chip Peripheral Modules (4)

Conditions: $V_{CC} = 2.7$ to 3.6 V, $V_{SS} = AVSS0 = VREFL0 = 0$ V,
 $AVCC0 = 3.0$ to 3.6 V, $VREFH0 = 3.0$ V to $AVCC0$,
 $T_a = T_{opr}$

Item		Sym- bol	Min.	Max.	Unit	Test Conditions
RIIC (Standard-mode)	SCL input cycle time	t_{SCL}	$6(12) \times t_{IICcyc} + 1300$	—	ns	Figure 6.25
	SCL input high pulse width	t_{SCLH}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	SCL input low pulse width	t_{SCLL}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	SCL, SDA input rise time	t_{Sr}	—	1000	ns	
	SCL, SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	$1(4) \times t_{IICcyc}$	ns	
	SDA input bus free time	t_{BUF}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	Start condition input hold time	t_{STAH}	$t_{IICcyc} + 300$	—	ns	
	Restart condition input setup time	t_{STAS}	1000	—	ns	
	Stop condition input setup time	t_{STOS}	1000	—	ns	
	Data input setup time	t_{SDAS}	$t_{IICcyc} + 50$	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
RIIC (Fast-mode)	SCL input cycle time	t_{SCL}	$6(12) \times t_{IICcyc} + 600$	—	ns	
	SCL input high pulse width	t_{SCLH}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	SCL input low pulse width	t_{SCLL}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	SCL, SDA input rise time	t_{Sr}	$20 + 0.1C_b$	300	ns	
	SCL, SDA input fall time	t_{Sf}	$20 + 0.1C_b$	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	$1(4) \times t_{IICcyc}$	ns	
	SDA input bus free time	t_{BUF}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	Start condition input hold time	t_{STAH}	$t_{IICcyc} + 300$	—	ns	
	Restart condition input setup time	t_{STAS}	300	—	ns	
	Stop condition input setup time	t_{STOS}	300	—	ns	
	Data input setup time	t_{SDAS}	$t_{IICcyc} + 50$	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note 1. t_{IICcyc} : RIIC internal reference clock (IIC ϕ) Cycle

Note 2. The value within parentheses is applicable when the value of the ICMR3.NF[1:0] bits is 11b while the digital filter is enabled by the setting ICFER.NFE = 1.

Note 3. C_b is the total capacitance of the bus lines.

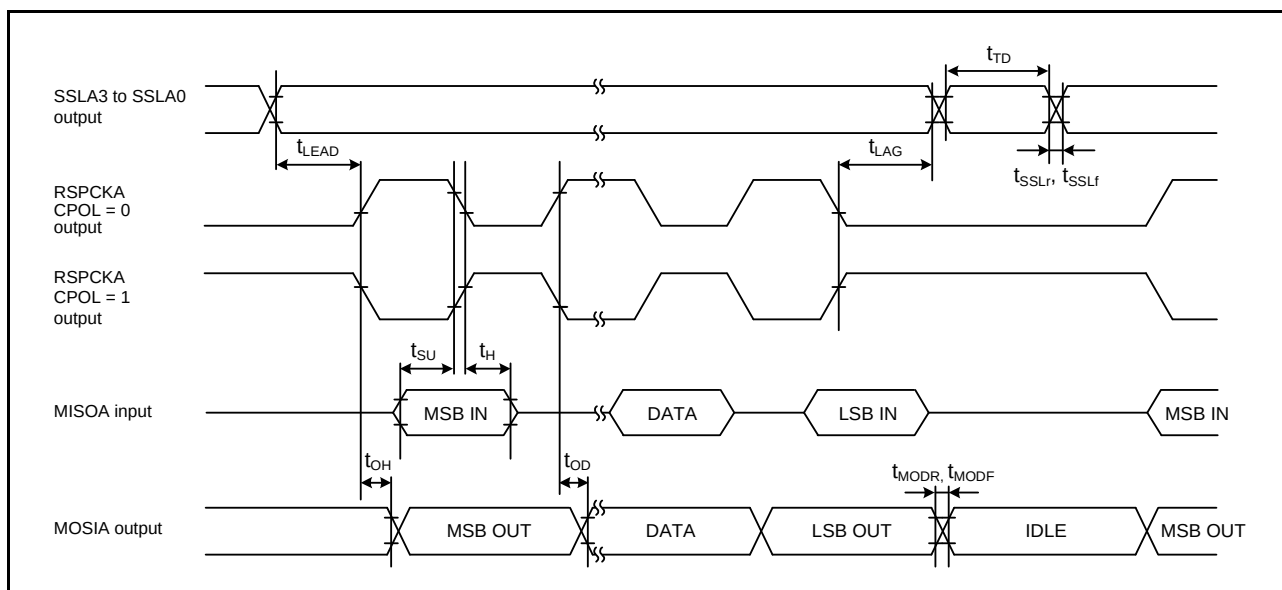


Figure 6.22 RSPI Timing (Master, CPHA = 1) and Simple SPI Timing (Master, CKPH = 0)

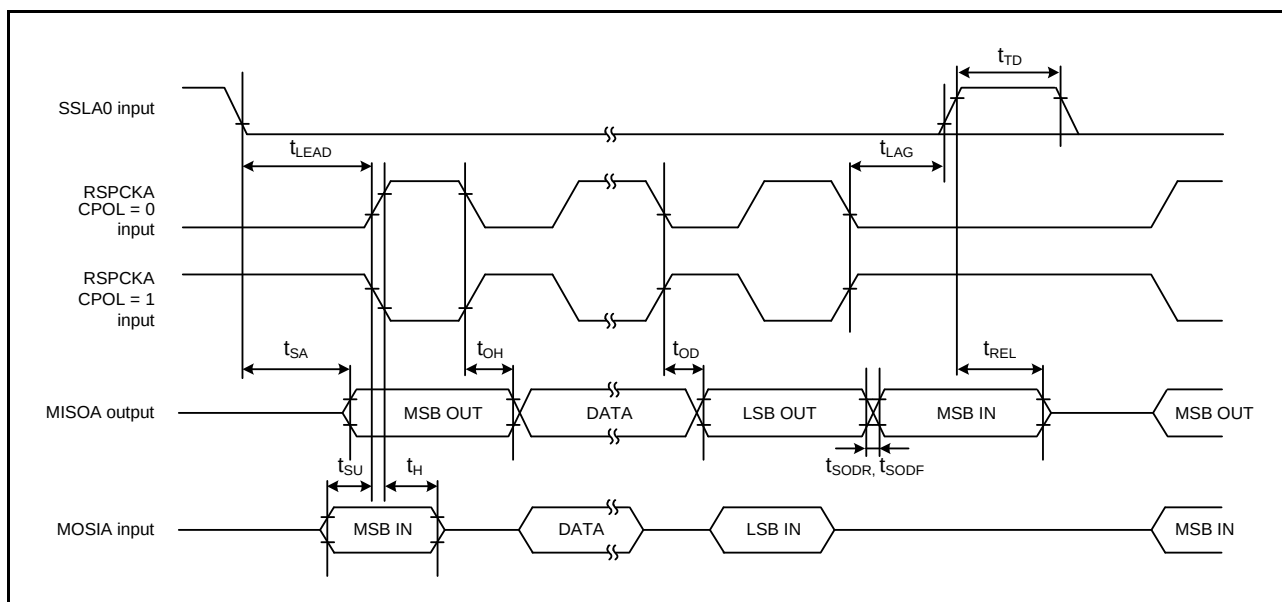


Figure 6.23 RSPI Timing (Slave, CPHA = 0) and Simple SPI Timing (Slave, CKPH = 1)

6.7 ROM (Flash Memory for Code Storage) Characteristics

Table 6.20 ROM (Flash Memory for Code Storage) Characteristics (1)

Condition: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V

AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,

Temperature range for the programming/erasure operation: $T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Reprogram/erase cycle*1	N_{pec}	1000	—	—	Times	
Data hold time	t_{DRP}	30*2	—	—	Year	$T_a = +85^{\circ}\text{C}$

Note 1. Definition of reprogram/erase cycle:

The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times ($n = 1000$), erasing can be performed n times for each block. For instance, when 128-byte programming is performed 16 times for different addresses in 2-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. The value is obtained from the reliability test.

Table 6.21 ROM (Flash Memory for Code Storage) Characteristics (2)

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,

AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,

Temperature range for the programming/erasure operation: $T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item		Symbol	min	typ	max	Unit	Test Conditions
Programming time	128 bytes	t_{P128}	—	1	10	ms	FCLK = 50MHz $N_{PEC} \leq 100$
	4 Kbytes	t_{P4K}	—	23	50	ms	
	16 Kbytes	t_{P16K}	—	90	200	ms	
	128 bytes	t_{P128}	—	1.2	12	ms	FCLK=50MHz $N_{PEC} > 100$
	4 Kbytes	t_{P4K}	—	27.6	60	ms	
	16 Kbytes	t_{P16K}	—	108	240	ms	
Erasure time	4 Kbytes	t_{E4K}	—	25	60	ms	FCLK=50MHz $N_{PEC} \leq 100$
	16 Kbytes	t_{E16K}	—	100	240	ms	
	4 Kbytes	t_{E4K}	—	30	72	ms	FCLK=50MHz $N_{PEC} > 100$
	16 Kbytes	t_{E16K}	—	120	288	ms	
Suspend delay time during programming		t_{SPD}	—	—	120	μs	Figure 6.31 FCLK = 50MHz
First suspend delay time during erasing (in suspend priority mode)		t_{SESD1}	—	—	120	μs	
Second suspend delay time during erasing (in suspend priority mode)		t_{SESD2}	—	—	1.7	ms	
Suspend delay time during erasing (in erasure priority mode)		t_{SEED}	—	—	1.7	ms	
FCU reset time		t_{FCUR}	35	—	—	μs	

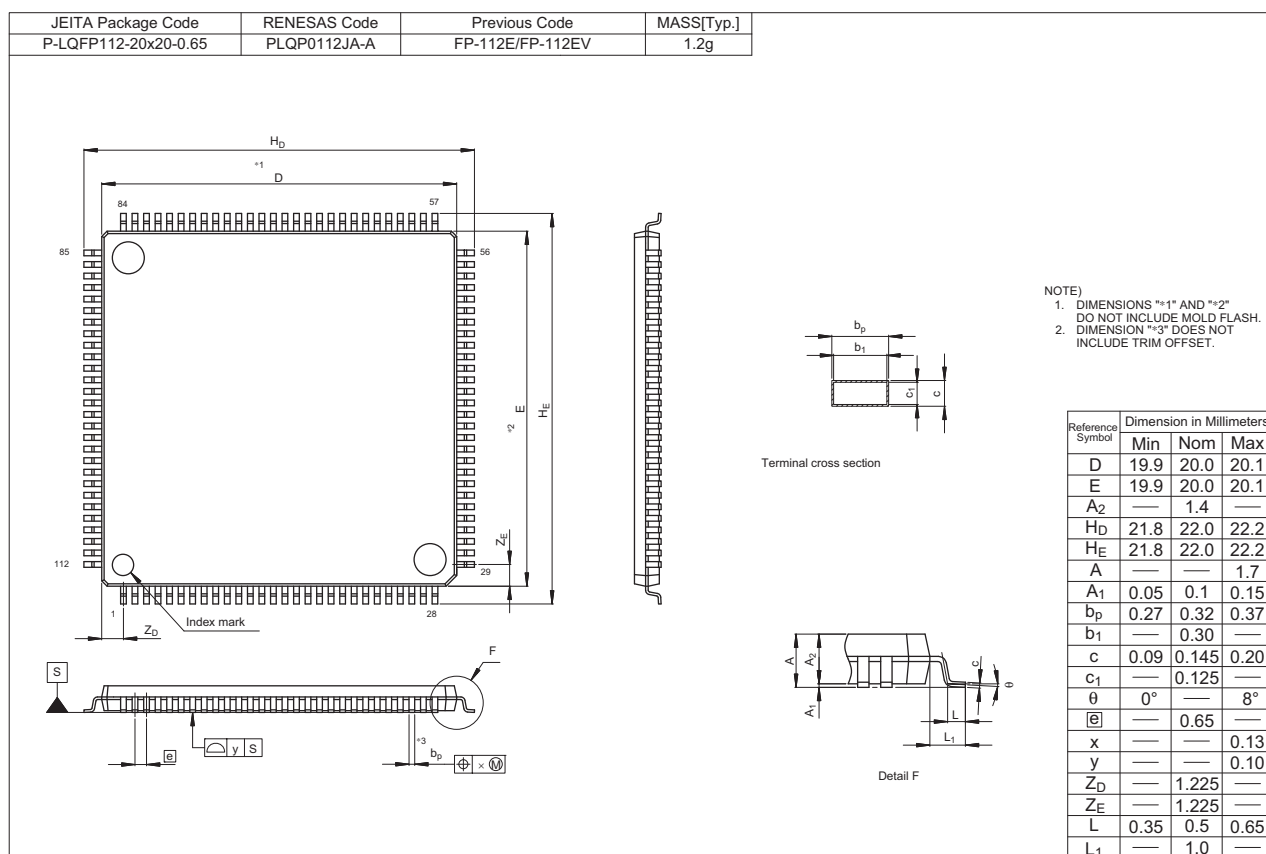


Figure C 112-Pin LQFP (PLQP0112JA-A)

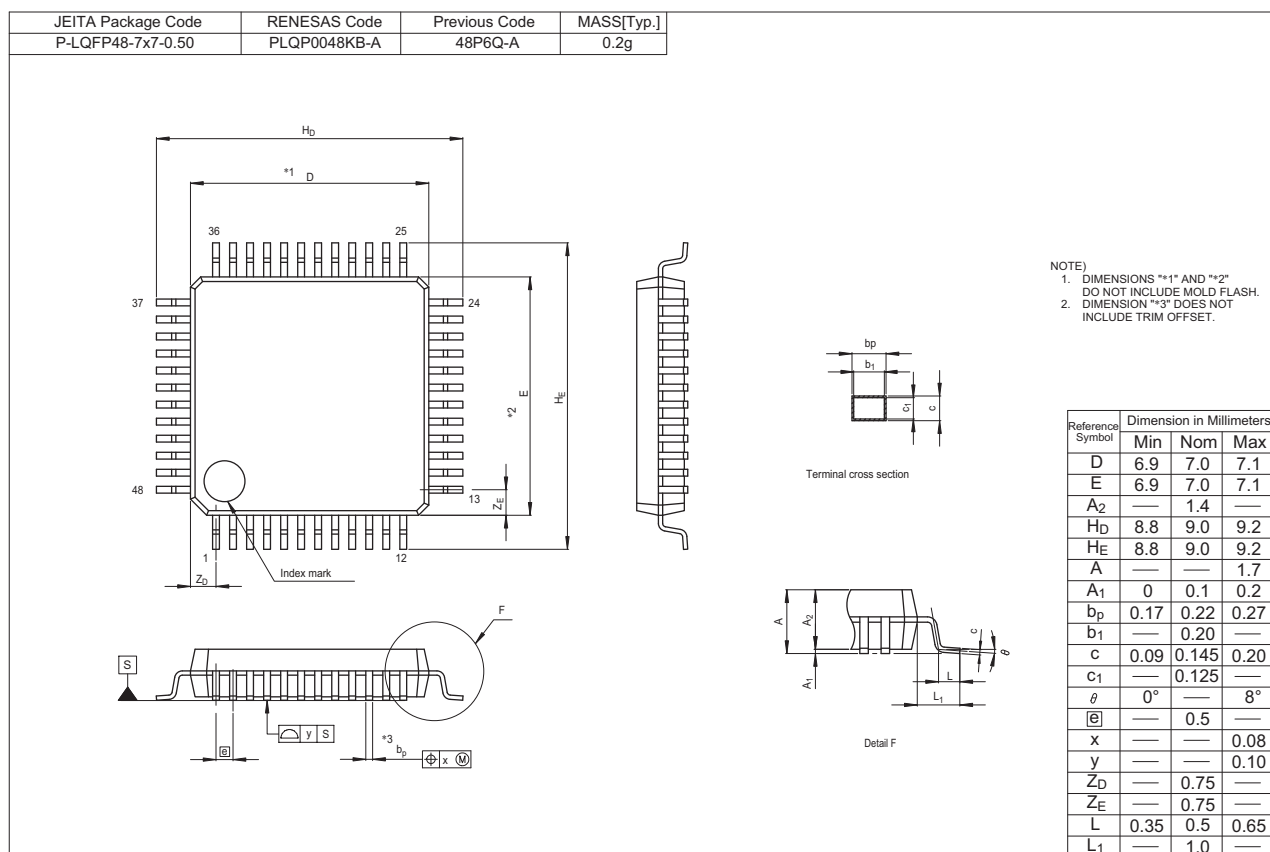


Figure F 48-Pin LQFP (PLQP0048KB-A)