Renesas Electronics America Inc - R5F563TEADFB#V0 Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	81
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 20x10b, 8x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f563teadfb-v0

Table 1.2 Comparison of Functions for Different Packages

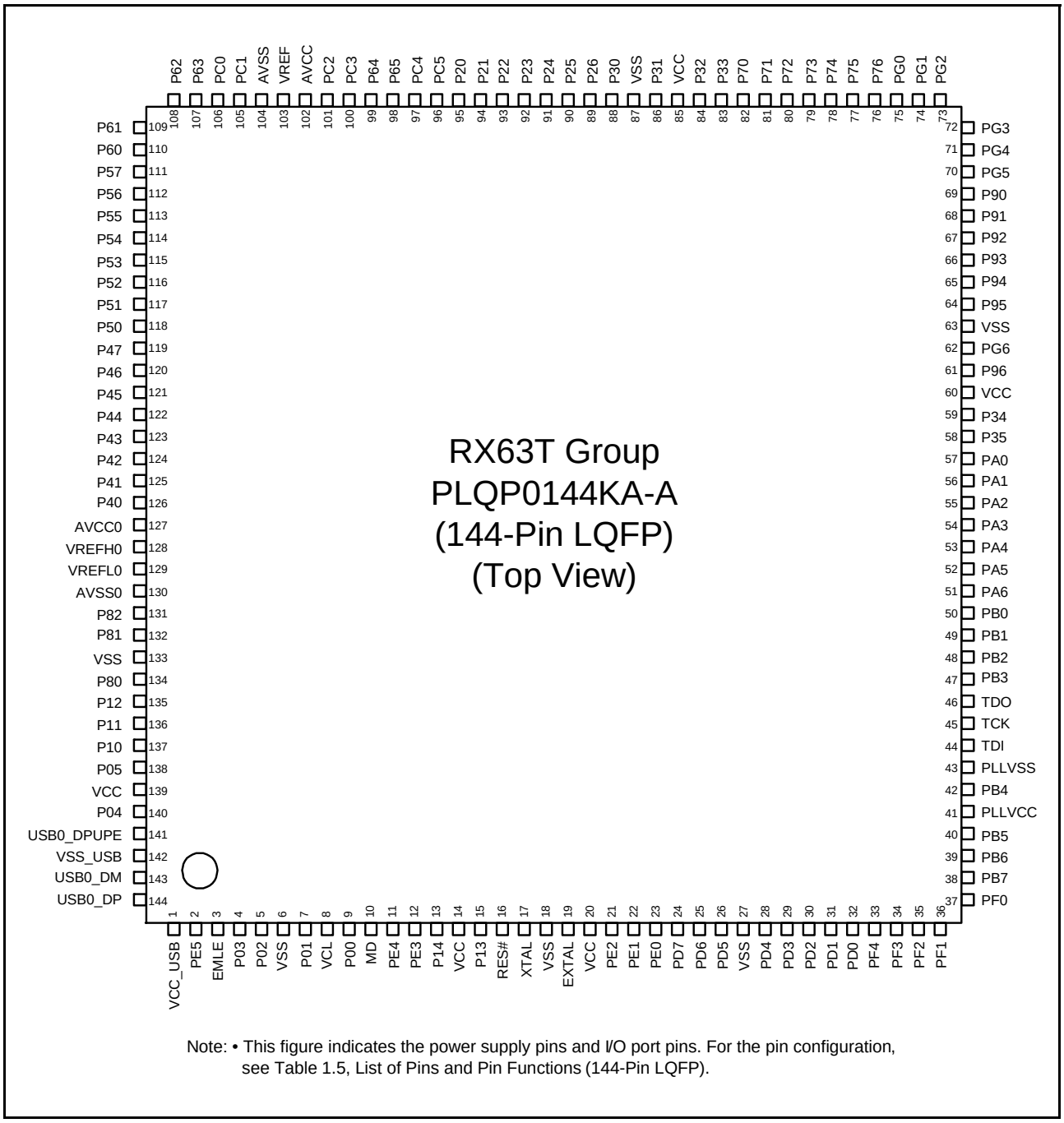
Functions			RX63T Group					
Package			**144 Pins**	**120 Pins**	**112 Pins**	**100 Pins**	**64 Pins**	**48 Pins**
External bus			16 bits				—	
External address space			1 Mbyte × 4 areas				—	
DMA	DMA controller (DMACA)		Ch. 0 to 3					
	Data transfer controller (DTCa)		Supported					
Interrupt controller (ICUb)	NMI pin		Supported					
	IRQ pin		Supported (x 8)				Supported (x 6)	
Timers	Multi-function timer pulse unit 3 (MTU3)*1		Ch. 0 to 7					
	General PWM timer (GPT)*1	Generation of delays in PWM, not supported	Ch. 0 to 7				Ch. 0 to 3	
		Generation of delays in PWM, supported	Ch. 0 to 3				—	
	Port output enable 3 (POE3)		Supported (POE pins × 6)			Supported (POE pins × 5)	Supported (POE pins × 4)	
	Compare match timer (CMT)		Ch. 0 to 3					
	Watchdog timer (WDTA)		Supported					
	Independent watchdog timer (IWDTa)		Supported					
Communication function	USB2.0 host/function module (USBa)		Ch. 0		—			
	Serial communications interfaces (SCIc)		Ch. 0 to 3			Ch. 0 to 2	Ch. 0, 1	
	Serial communications interfaces (SCId)		Ch. 12					
	I^2C bus interfaces (RIIC)		Ch. 0, 1		Ch. 0			
	Serial peripheral interfaces (RSPI)		Ch. 0, 1				Ch. 0	
	CAN module (CAN) (as an optional function)*1		Ch. 0				—	
12-bit A/D converter (S12ADB)			4 channels × 2 units				8 channels × 1 unit (AN000 to 007)	8 channels × 1 unit (AN000 to 004, 007)
	Three-channel simultaneous sampling function		2 units				1 unit	
	Programmable gain amplifier		3 channels × 2 units				—	
	Window comparator		3 channels × 2 units				3 channels × 1 unit	
10-bit A/D converter (ADA)			20 channels	12 channels			—	
D/A converter (DAa)			Ch. 0, 1				—	
Clock Frequency Accuracy Measurement Circuit			Supported					
Digital power supply controller (DPC)*2			Supported				Not supported	

Note 1. For the MTU3 and GPT, the number of pins will differ with the package. See the list of pins and pin functions for details. In addition, the CAN module is an optional function. For details, see Table 1.3.

Note 2. Not provided for the product ID code O.

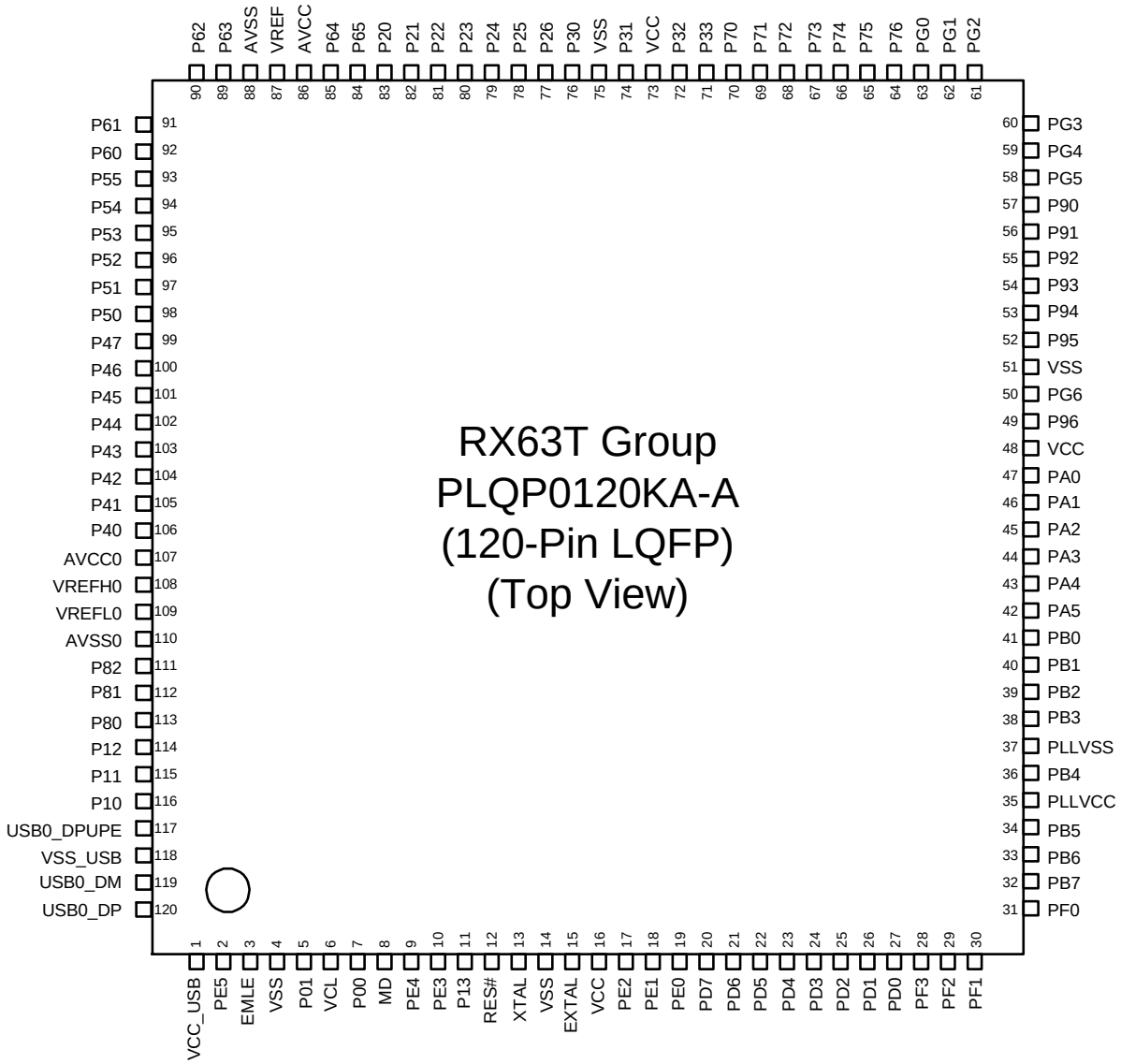
1.5 Pin Assignments

Figure 1.3 to Figure 1.8 show the pin assignments. Table 1.5 to Table 1.10 show the lists of pins and pin functions.



Note: • This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.5, List of Pins and Pin Functions (144-Pin LQFP).

Figure 1.3 Pin Assignment (144-Pin LQFP)



Note: • This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.6, List of Pins and Pin Functions (120-Pin LQFP).

Figure 1.4 Pin Assignment (120-Pin LQFP)

Table 1.5 List of Pins and Pin Functions (144-Pin LQFP) (2/4)

Pin Number 144-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3, GPT, POE3, CAC)	Communications (SCIc, SCId, RSPI, RIIC, CAN, USB)	Interrupt	S12ADB, AD, DA
39		PB6	A18		RXD12/SMISO12/ SSCL12/RXDX12/ CRX1	IRQ2	
40		PB5	A17		TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/ CTX1		
41	PLLVCC						
42		PB4	A16	POE8#/ GTETRG0		IRQ3-DS	
43	PLLVSS						
44	TDI				RXD1*1		
45	TCK/FINEC						
46	TDO				TXD1*1		
47		PB3	A15	MTIOC0A/CACREF	SCK0		
48		PB2		MTIOC0B	TXD0/SMOSI0/ SSDA0/SDA0		
49		PB1		MTIOC0C	RXD0/SMISO0/ SSCL0/SCL0	IRQ4	
50		PB0	A14	MTIOC0D	MOSIA/MOSIB		
51	TRDATA1	PA6	CS3#		CTS3#/RTS3#/SS3#		
52		PA5		MTIOC1A	RXD0/SMISO0/ SSCL0/ MISOA/MISOB		ADTRG1#
53		PA4		MTIOC1B	TXD0/SMOSI0/ SSDA0/SMOSI0/ RSPCKA/RSPCKB		ADTRG0#
54		PA3		MTIOC2A	SCK0/SSLA0/SSLB0		
55		PA2		MTIOC2B	RXD2/SMISO2/ SSCL2/ SSLA1/SSLB1		
56		PA1		MTIOC6A	TXD2/SMOSI2/ SSDA2/SMOSI2/ SSLA2/SSLB2		
57		PA0		MTIOC6C	SCK2/SSLA3/SSLB3		
58	TRDATA0	P35			TXD3/SMOSI3/SSDA3		
59	TRCLK	P34		GTETRG1	RXD3/SMISO3/SSCL3	IRQ3	
60	VCC						
61		P96	A13	POE4#	RXD1/SMISO1/SSCL1	IRQ4-DS	
62		PG6	CS2#		SCK1		
63	VSS						
64		P95		MTIOC6B/GTIOC4A	TXD1/SMOSI1/SSDA1		
65		P94		MTIOC7A/GTIOC5A	CTS1#/RTS1#/SS1#		
66		P93		MTIOC7B/GTIOC6A	CTS2#/RTS2#/SS2#		
67		P92		MTIOC6D/GTIOC4B			
68		P91		MTIOC7C/GTIOC5B			
69		P90		MTIOC7D/GTIOC6B			
70		PG5		POE12#	SCK3		ADTRG#
71		PG4		GTIOC6B	RXD3/SMISO3/SSCL3	IRQ6	

Table 1.7 List of Pins and Pin Functions (112-Pin LQFP) (1/4)

Pin Number 112-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3, GPT, POE3, CAC)	Communications (SCIc, SCId, RSPI, RIIC, CAN)	Interrupt	S12ADB, AD, DA
1		PE5	BCLK			IRQ0	
2	EMLE						
3	VSS						
4		P01	RD#		CTS0#/RTS0#/SS0#		
5	VCL						
6		P00	CS1#	CACREF			
7	MD/FINED						
8		PE4	A10	POE10#/MTCLKC		IRQ1	
9		PE3	A11	POE11#/MTCLKD		IRQ2-DS	
10	RES#						
11	XTAL						
12	VSS						
13	EXTAL						
14	VCC						
15		PE2		POE10#		NMI	
16		PE1	WR0#/WR#		CTS12#/RTS12#/ SS12#/SSLA3/SSLB3		
17		PE0	WR1#/BC1#/ WAIT#		SSLA2/SSLB2/CRX1	IRQ7	
18		PD7		GTIOC0A	CTS0#/RTS0#/SS0#/ SSLA1/SSLB1/CTX1		
19		PD6		GTIOC0B	SSLA0/SSLB0		
20		PD5		GTIOC1A	RXD1/SMISO1/SSCL1	IRQ6	
21		PD4		GTIOC1B	SCK1		
22		PD3		GTIOC2A	TXD1/SMOSI1/SSDA1		
23		PD2	CS2#	GTIOC2B	MOSIA/MOSIB		
24		PD1	CS0#	GTIOC3A	MISOA/MISOB		
25		PD0	A12	GTIOC3B	RSPCKA/RSPCKB		
26	TDI	PF4	CS3#		RXD1*1		
27	TCK/FINEC	PF3			TXD1/SMOSI1/SSDA1		
28	TDO	PF2	CS1#		RXD1/SMISO1/ SSCL1/TXD1*1	IRQ5	
29		PB7	A19		SCK12		
30		PB6	A18		RXD12/SMISO12/ SSCL12/RXDX12/ CRX1	IRQ2	
31		PB5	A17		TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/CTX1		
32	PLLVCC						
33		PB4	A16	POE8#/GTETRG0		IRQ3-DS	
34	PLLVSS						
35		PB3	A15	MTIOC0A/CACREF	SCK0		
36		PB2		MTIOC0B	TXD0/SMOSI0/ SSDA0/SDA0		
37		PB1		MTIOC0C	RXD0/SMISO0/ SSCL0/SCL0	IRQ4	

Table 1.7 List of Pins and Pin Functions (112-Pin LQFP) (4/4)

Pin Number 112-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3, GPT, POE3, CAC)	Communications (SCIc, SCId, RSPI, RIIC, CAN)	Interrupt	S12ADB, AD, DA
110		P10		MTCLKD		IRQ0-DS	
111	TRST#	P05	WAIT#/CS2#				
112	TMS	P04					

Note 1. Available for use as SCI pin only in boot mode.

Table 1.10 List of Pins and Pin Functions (48-Pin LQFP) (2/2)

Pin Number 64-Pin LQFP	Power Supply Clock System Control	I/O Port	POE3	Timer (MTU3, GPT, CAC)	Communications		Interrupt	S12ADB
					(SCIc, SCId)	(RSPI, RIIC)		
26		P74		MTIOC3D GTIOC0B MTIOC6D				
27		P73		MTIOC4B GTIOC2A MTIOC7B				
28		P72		MTIOC4A GTIOC1A MTIOC7A				
29		P71		MTIOC3B GTIOC0A MTIOC6B				
30		P70	POE0#		CTS1# RTS1# SS1#		IRQ5-DS	
31	VCC							
32		P30		MTIOC0B MTCLKD	TXD0 SMOSI0 SSDA0	SSLA0		
33	VSS							
34		P24		MTIC5U MTCLKC	RXD0 SMISO0 SSCL0	RSPCKA		
35		P23		MTIC5V MTCLKB CACREF	SCK0	MOSIA		
36		P22		MTIC5W MTCLKA	CTS0# RTS0# SS0#	MISOA		
37		P47						AN007 CVREFH
38		P44						AN004
39		P43						AN003 CVREFL
40		P42						AN002
41		P41						AN001
42		P40						AN000
43	AVCC0							
44	VREFH0							
45	VREFL0							
46	AVSS0							
47	VCL							
48	EMLE							

Table 4.1 List of I/O Registers (Address Order) (6/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 7098h	ICU	Interrupt Request Register 152	IR152	8	8	2 ICLK		ICUb	
0008 7099h	ICU	Interrupt Request Register 153	IR153	8	8	2 ICLK			
0008 709Ah	ICU	Interrupt Request Register 154	IR154	8	8	2 ICLK			
0008 709Bh	ICU	Interrupt Request Register 155	IR155	8	8	2 ICLK			
0008 709Ch	ICU	Interrupt Request Register 156	IR156	8	8	2 ICLK			
0008 709Dh	ICU	Interrupt Request Register 157	IR157	8	8	2 ICLK			
0008 709Eh	ICU	Interrupt Request Register 158	IR158	8	8	2 ICLK			
0008 70A1h	ICU	Interrupt Request Register 161	IR161	8	8	2 ICLK			
0008 70A2h	ICU	Interrupt Request Register 162	IR162	8	8	2 ICLK			
0008 70A3h	ICU	Interrupt Request Register 163	IR163	8	8	2 ICLK			
0008 70A4h	ICU	Interrupt Request Register 164	IR164	8	8	2 ICLK			
0008 70A5h	ICU	Interrupt Request Register 165	IR165	8	8	2 ICLK			
0008 70A6h	ICU	Interrupt Request Register 166	IR166	8	8	2 ICLK			
0008 70A7h	ICU	Interrupt Request Register 167	IR167	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70A8h	ICU	Interrupt Request Register 168	IR168	8	8	2 ICLK			
0008 70A9h	ICU	Interrupt Request Register 169	IR169	8	8	2 ICLK			
0008 70AAh	ICU	Interrupt Request Register 170	IR170	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70ABh	ICU	Interrupt Request Register 171	IR171	8	8	2 ICLK			
0008 70ACh	ICU	Interrupt Request Register 172	IR172	8	8	2 ICLK			
0008 70ADh	ICU	Interrupt Request Register 173	IR173	8	8	2 ICLK			
0008 70AEh	ICU	Interrupt Request Register 174	IR174	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70AFh	ICU	Interrupt Request Register 175	IR175	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70B0h	ICU	Interrupt Request Register 176	IR176	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70B1h	ICU	Interrupt Request Register 177	IR177	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70B2h	ICU	Interrupt Request Register 178	IR178	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70B3h	ICU	Interrupt Request Register 179	IR179	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70B4h	ICU	Interrupt Request Register 180	IR180	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70B5h	ICU	Interrupt Request Register 181	IR181	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70B6h	ICU	Interrupt Request Register 182	IR182	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70B7h	ICU	Interrupt Request Register 183	IR183	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70B8h	ICU	Interrupt Request Register 184	IR184	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70B9h	ICU	Interrupt Request Register 185	IR185	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70BAh	ICU	Interrupt Request Register 186	IR186	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70BBh	ICU	Interrupt Request Register 187	IR187	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70BCh	ICU	Interrupt Request Register 188	IR188	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70BDh	ICU	Interrupt Request Register 189	IR189	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70BEh	ICU	Interrupt Request Register 190	IR190	8	8	2 ICLK			Not present in versions with 112, 100, 64 or 48 pins.
0008 70BFh	ICU	Interrupt Request Register 191	IR191	8	8	2 ICLK			Not present in versions with 112, 100, 64 or 48 pins.

Table 4.1 List of I/O Registers (Address Order) (14/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 7507h	ICU	IRQ Control Register 7	IRQCR7	8	8	2 ICLK		ICUb	Not present in versions with 64 or 48 pins.
0008 7510h	ICU	IRQ Pin Digital Filter Enable Register 0	IRQFLTE0	8	8	2 ICLK			
0008 7514h	ICU	IRQ Pin Digital Filter Setting Register 0	IRQFLTC0	16	16	2 ICLK			
0008 7580h	ICU	Non-Maskable Interrupt Status Register	NMISR	8	8	2 ICLK			
0008 7581h	ICU	Non-Maskable Interrupt Enable Register	NMIER	8	8	2 ICLK			
0008 7582h	ICU	Non-Maskable Interrupt Status Clear Register	NMICLR	8	8	2 ICLK			
0008 7583h	ICU	NMI Pin Interrupt Control Register	NMICR	8	8	2 ICLK			
0008 7590h	ICU	NMI Pin Digital Filter Enable Register	NMIFLTE	8	8	2 ICLK			
0008 7594h	ICU	NMI Pin Digital Filter Setting Register	NMIFLTC	8	8	2 ICLK			
0008 8000h	CMT	Compare Match Timer Start Register 0	CMSTR0	16	16	2, 3 PCLKB	2 ICLK	CMT	
0008 8002h	CMT0	Compare Match Timer Control Register	CMCR	16	16	2, 3 PCLKB	2 ICLK		
0008 8004h	CMT0	Compare Match Timer Counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK		
0008 8006h	CMT0	Compare Match Timer Constant Register	CMCOR	16	16	2, 3 PCLKB	2 ICLK		
0008 8008h	CMT1	Compare Match Timer Control Register	CMCR	16	16	2, 3 PCLKB	2 ICLK		
0008 800Ah	CMT1	Compare Match Timer Counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK		
0008 800Ch	CMT1	Compare Match Timer Constant Register	CMCOR	16	16	2, 3 PCLKB	2 ICLK		
0008 8010h	CMT	Compare Match Timer Start Register 1	CMSTR1	16	16	2, 3 PCLKB	2 ICLK		
0008 8012h	CMT2	Compare Match Timer Control Register	CMCR	16	16	2, 3 PCLKB	2 ICLK		
0008 8014h	CMT2	Compare Match Timer Counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK		
0008 8016h	CMT2	Compare Match Timer Constant Register	CMCOR	16	16	2, 3 PCLKB	2 ICLK		
0008 8018h	CMT3	Compare Match Timer Control Register	CMCR	16	16	2, 3 PCLKB	2 ICLK		
0008 801Ah	CMT3	Compare Match Timer Counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK		
0008 801Ch	CMT3	Compare Match Timer Constant Register	CMCOR	16	16	2, 3 PCLKB	2 ICLK		
0008 8020h	WDT	WDT Refresh Register	WDTRR	8	8	2, 3 PCLKB	2 ICLK	WDTA	
0008 8022h	WDT	WDT Control Register	WDTCR	16	16	2, 3 PCLKB	2 ICLK		
0008 8024h	WDT	WDT Status Register	WDTSR	16	16	2, 3 PCLKB	2 ICLK		
0008 8026h	WDT	WDT Reset Control Register	WDTRCR	8	8	2, 3 PCLKB	2 ICLK		
0008 8030h	IWDT	IWDT Refresh Register	IWDTRR	8	8	2, 3 PCLKB	2 ICLK	IWDTa	
0008 8032h	IWDT	IWDT Control Register	IWDTCR	16	16	2, 3 PCLKB	2 ICLK		
0008 8034h	IWDT	IWDT Status Register	IWDTSR	16	16	2, 3 PCLKB	2 ICLK		
0008 8036h	IWDT	IWDT Reset Control Register	IWDTRCR	8	8	2, 3 PCLKB	2 ICLK		
0008 8038h	IWDT	IWDT Count Stop Control Register	IWDTCSTPR	8	8	2, 3 PCLKB	2 ICLK		
0008 80C0h	DA	D/A Data Register 0	DADR0	16	16	2, 3 PCLKB	2 ICLK	DAa	Not present in versions with 64 or 48 pins.
0008 80C2h	DA	D/A Data Register 1	DADR1	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 80C4h	DA	D/A Control Register	DACR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 80C5h	DA	DADRm Format Select Register	DADPR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 80C6h	DA	D/A A/D Synchronous Start Control Register	DAADSCR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 8280h	CRC	CRC Control Register	CRCCR	8	8	2, 3 PCLKB	2 ICLK	CRC	
0008 8281h	CRC	CRC Data Input Register	CRCDIR	8	8	2, 3 PCLKB	2 ICLK		
0008 8282h	CRC	CRC Data Output Register	CRCDOR	16	16	2, 3 PCLKB	2 ICLK		
0008 8300h	RIIC0	I^2C Bus Control Register 1	ICCR1	8	8	2, 3 PCLKB	2 ICLK	RIIC	
0008 8301h	RIIC0	I^2C Bus Control Register 2	ICCR2	8	8	2, 3 PCLKB	2 ICLK		
0008 8302h	RIIC0	I^2C Bus Mode Register 1	ICMR1	8	8	2, 3 PCLKB	2 ICLK		
0008 8303h	RIIC0	I^2C Bus Mode Register 2	ICMR2	8	8	2, 3 PCLKB	2 ICLK		
0008 8304h	RIIC0	I^2C Bus Mode Register 3	ICMR3	8	8	2, 3 PCLKB	2 ICLK		
0008 8305h	RIIC0	I^2C Bus Function Enable Register	ICFER	8	8	2, 3 PCLKB	2 ICLK		
0008 8306h	RIIC0	I^2C Bus Status Enable Register	ICSER	8	8	2, 3 PCLKB	2 ICLK		
0008 8307h	RIIC0	I^2C Bus Interrupt Enable Register	ICIER	8	8	2, 3 PCLKB	2 ICLK		

Table 4.1 List of I/O Registers (Address Order) (19/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 9804h	AD	A/D Channel Select Register 0	ADANSA0	16	16	2, 3 PCLKB	2 ICLK	AD	Not present in versions with 64 or 48 pins.
0008 9806h	AD	A/D Channel Select Register 1	ADANSA1	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64 or 48 pins.
0008 9808h	AD	A/D-Converted Value Addition Mode Select Register0	ADADS0	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 980Ah	AD	A/D-Converted Value Addition Mode Select Register1	ADADS1	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64 or 48 pins.
0008 980Ch	AD	A/D-Converted Value Addition Count Select Register	ADADC	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 980Eh	AD	A/D Control Extended Register	ADCER	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9810h	AD	A/D Start Trigger Select Register	ADSTRGR	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 981Eh	AD	A/D Self-Diagnosis Data Register	ADRD	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9820h	AD	A/D Data Register A	ADDRA	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9822h	AD	A/D Data Register B	ADDRB	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9824h	AD	A/D Data Register C	ADDRC	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9826h	AD	A/D Data Register D	ADDRD	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9828h	AD	A/D Data Register E	ADDRE	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 982Ah	AD	A/D Data Register F	ADDRF	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 982Ch	AD	A/D Data Register G	ADDRG	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 982Eh	AD	A/D Data Register H	ADDRH	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9830h	AD	A/D Data Register I	ADDRI	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9832h	AD	A/D Data Register J	ADDRJ	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9834h	AD	A/D Data Register K	ADDRK	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9836h	AD	A/D Data Register L	ADDRL	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9838h	AD	A/D Data Register M	ADDRM	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 983Ah	AD	A/D Data Register N	ADDRN	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 983Ch	AD	A/D Data Register O	ADDRO	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 983Eh	AD	A/D Data Register P	ADDRP	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 9840h	AD	A/D Data Register Q	ADDRQ	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 9842h	AD	A/D Data Register R	ADDRR	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 9844h	AD	A/D Data Register S	ADDRS	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 9846h	AD	A/D Data Register T	ADDRT	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 9860h	AD	A/D Sampling State Register 0	ADSSTR0	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9861h	AD	A/D Sampling State Register L	ADSSTRL	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.

Table 4.1 List of I/O Registers (Address Order) (36/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
000C 1A28h	MTU7	Timer General Register C	TGRC	16	16, 32	4, 5 PCLKA	2, 3 ICLK	MTU3	
000C 1A2Ah	MTU7	Timer General Register D	TGRD	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1A2Ch	MTU6	Timer Status Register	TSR	8	8, 16	4, 5 PCLKA	2, 3 ICLK		
000C 1A2Dh	MTU7	Timer Status Register	TSR	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1A30h	MTU	Timer Interrupt Skipping Set Register 1B	TITCR1B	8	8, 16	4, 5 PCLKA	2, 3 ICLK		
000C 1A31h	MTU	Timer Interrupt Skipping Counters 1B	TITCNT1B	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1A32h	MTU	Timer Buffer Transfer Set Register B	TBTERB	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1A34h	MTU	Timer Dead Time Enable Register B	TDERB	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1A36h	MTU	Timer Output Level Buffer Register B	TOLBRB	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1A38h	MTU6	Timer Buffer Operation Transfer Mode Register	TBTM	8	8, 16	4, 5 PCLKA	2, 3 ICLK		
000C 1A39h	MTU7	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1A3Ah	MTU	Timer Interrupt Skipping Mode Register B	TITMRB	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1A3Bh	MTU	Timer Interrupt Skipping Set Register 2B	TITCR2B	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1A3Ch	MTU	Timer Interrupt Skipping Counters 2B	TITCNT2B	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1A40h	MTU7	Timer A/D Converter Start Request Control Register	TADCR	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1A44h	MTU7	Timer A/D Converter Start Request Cycle Set Register A	TADCORA	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1A46h	MTU7	Timer A/D Converter Start Request Cycle Set Register B	TADCORB	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1A48h	MTU7	Timer A/D Converter Start Request Cycle Set Buffer Register A	TADCOBRA	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1A4Ah	MTU7	Timer A/D Converter Start Request Cycle Set Buffer Register B	TADCOBRB	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1A50h	MTU	Timer Synchronous Clear Register	TSYCR	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1A60h	MTU	Timer Waveform Control Register B	TWCRB	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1A70h	MTU	Timer Mode Register 2B	TMDR2B	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1A72h	MTU6	Timer General Register E	TGRE	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1A74h	MTU7	Timer General Register E	TGRE	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1A76h	MTU7	Timer General Register F	TGRF	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1A80h	MTU	Timer Start Register B	TSTRB	8	8, 16	4, 5 PCLKA	2, 3 ICLK		
000C 1A81h	MTU	Timer Synchronous Register B	TSYRB	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1A84h	MTU	Timer Read/Write Enable Register B	TRWERB	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1C80h	MTU5	Timer Counter U	TCNTU	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1C82h	MTU5	Timer General Register U	TGRU	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1C84h	MTU5	Timer Control Register U	TCRU	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1C86h	MTU5	Timer I/O Control Register U	TIORU	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1C90h	MTU5	Timer Counter V	TCNTV	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1C92h	MTU5	Timer General Register V	TGRV	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1C94h	MTU5	Timer Control Register V	TCRV	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1C96h	MTU5	Timer I/O Control Register V	TIORV	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1CA0h	MTU5	Timer Counter W	TCNTW	16	16, 32	4, 5 PCLKA	2, 3 ICLK		
000C 1CA2h	MTU5	Timer General Register W	TGRW	16	16	4, 5 PCLKA	2, 3 ICLK		
000C 1CA4h	MTU5	Timer Control Register W	TCRW	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1CA6h	MTU5	Timer I/O Control Register W	TIORW	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1CB0h	MTU5	Timer Status Register	TSR	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1CB2h	MTU5	Timer Interrupt Enable Register	TIER	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1CB4h	MTU5	Timer Start Register	TSTR	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 1CB6h	MTU5	Timer Compare Match Clear Register	TCNTCMPCLR	8	8	4, 5 PCLKA	2, 3 ICLK		
000C 2000h	GPT	General PWM Timer Software Start Register	GTSTR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK	GPT	
000C 2004h	GPT	General PWM Timer Hardware Source Start Control Register	GTHSCR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		

Table 4.1 List of I/O Registers (Address Order) (48/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
007F FFB0h	FLASH	Flash Status Register 0	FSTATR0	8	8	2, 3 FCLK	2, 3 ICLK	ROM	
007F FFB1h	FLASH	Flash Status Register 1	FSTATR1	8	8	2, 3 FCLK	2, 3 ICLK		
007F FFB2h	FLASH	Flash P/E Mode Entry Register	FENTRYR	16	16	2, 3 FCLK	2, 3 ICLK	ROM/ E2 DataFlash Memory	
007F FFB4h	FLASH	Flash Protection Register	FPROTR	16	16	2, 3 FCLK	2, 3 ICLK	ROM	
007F FFB6h	FLASH	Flash Reset Register	FRESETR	16	16	2, 3 FCLK	2, 3 ICLK		
007F FFBAh	FLASH	FCU Command Register	FCMDR	16	16	2, 3 FCLK	2, 3 ICLK		
007F FFC8h	FLASH	FCU Processing Switching Register	FCPSR	16	16	2, 3 FCLK	2, 3 ICLK		
007F FFCAh	FLASH	E2 DataFlash Blank Check Control Register	DFLBCCNT	16	16	2, 3 FCLK	2, 3 ICLK	E2 DataFlash Memory	
007F FFCCh	FLASH	Flash P/E Status Register	FPESTAT	16	16	2, 3 FCLK	2, 3 ICLK	ROM	
007F FFCEh	FLASH	E2 DataFlash Blank Check Status Register	DFLBCSTAT	16	16	2, 3 FCLK	2, 3 ICLK	E2 DataFlash Memory	
007F FFE8h	FLASH	Peripheral Clock Notification Register	PCKAR	16	16	2, 3 FCLK	2, 3 ICLK	ROM	

Note: • This table shows the maximum specifications of I/O registers. The I/O registers of individual products correspond to the list of functions given as Table 1.2. For details, refer to Table 1.2, Comparison of Functions for Different Packages.
Note 1. When the register is accessed while the USB is operating, a delay may be generated in accessing.
Note 2. Odd addresses are not accessible in 16-bit units. Obtain 16-bit access to the two registers by access to the address of TMOCNTL.
Note 3. Pins USB0 and RIIC1 are not present in 112-pin products.
Note 4. Pins USB0, RIIC1, and SCI3 are not present in 100-pin products.
Note 5. Pins GPT4 to GPT7, USB0, RSPI1, RIIC1, SCI2, SCI3, CAN1, AD, and S12AD1 are not present in 64- and 48-pin products.

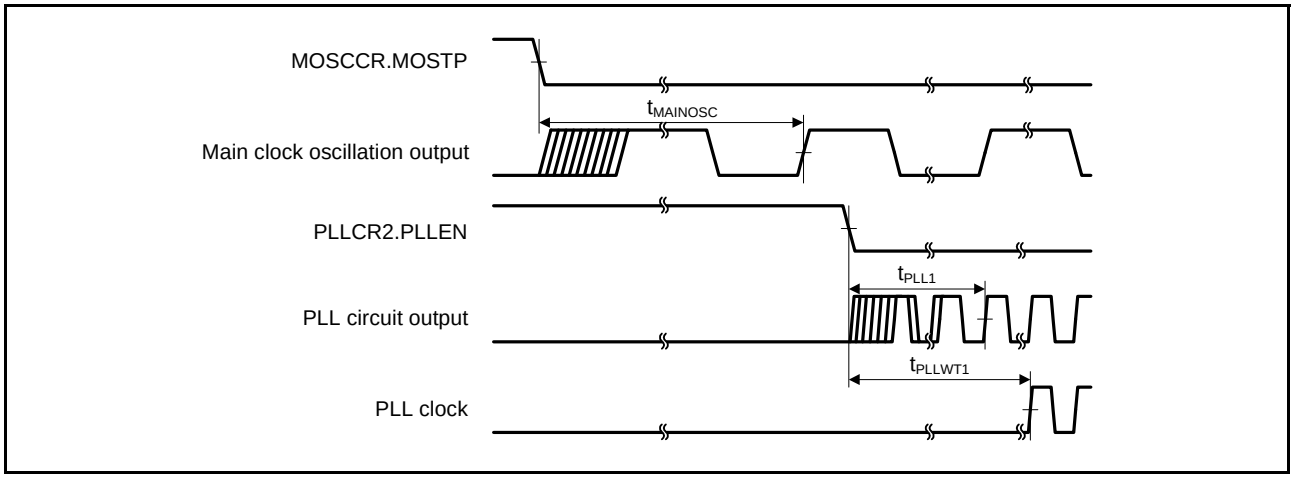


Figure 5.7 PLL Clock Oscillation Start Timing (PLL is Operated after Main Clock Oscillation Has Settled)

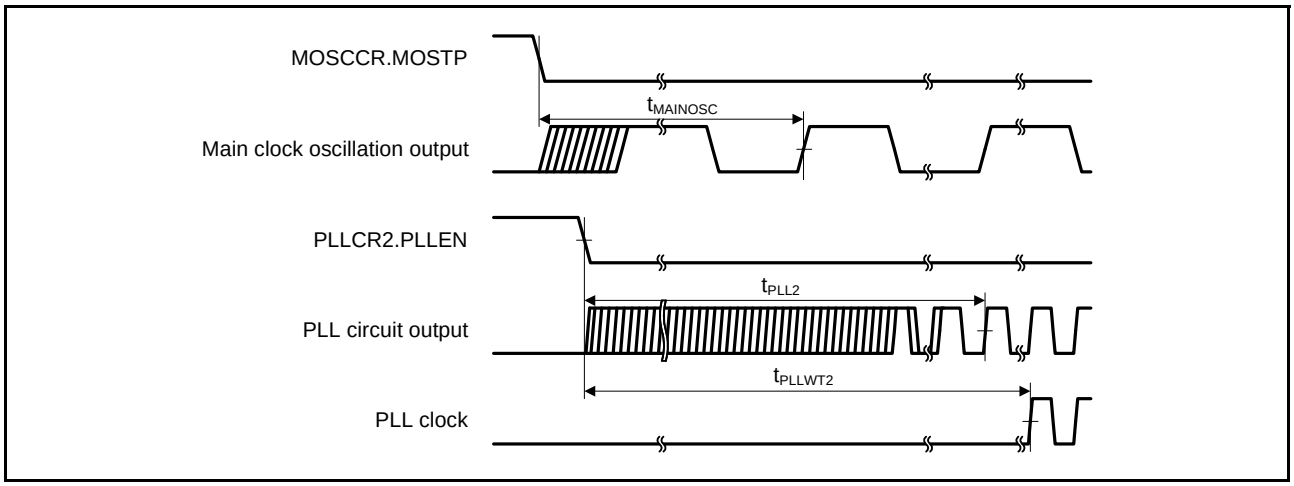


Figure 5.8 PLL Clock Oscillation Start Timing (PLL is Operated before Main Clock Oscillation Has Settled)

Table 5.16 Timing of On-Chip Peripheral Modules (4)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item		Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI	SCK clock cycle output (master)	t_{SPcyc}	4	65536	t_{Pcyc}	C = 30 pF, Figure 5.30
	SCK clock cycle input (slave)		8	65536		
	SCK clock high pulse width	t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width	t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise/fall time	t_{SPCKR}, t_{SPCKF}	—	20	ns	
	Data input setup time	t_{SU}	40	—	ns	C = 30 pF, Figure 5.31 to Figure 5.38
	Data input hold time	t_H	40	—	ns	
	SS input setup time	t_{LEAD}	6	—	t_{Pcyc}	
	SS input hold time	t_{LAG}	6	—	t_{Pcyc}	
	Data output delay time	t_{OD}	—	40	ns	
	Data output hold time	t_{OH}	–10	—	ns	
	Data rise/fall time	t_{DR}, t_{DF}	—	20	ns	
	SS input rise/fall time	t_{SSLr}, t_{SSLf}	—	20	ns	
	Slave access time	t_{SA}	—	5	t_{Pcyc}	C = 30 pF, Figure 5.37 and Figure 5.38
	Slave output release time	t_{REL}	—	5	t_{Pcyc}	

Note 1. t_{Pcyc}: PCLK cycle

5.5 A/D Conversion Characteristics

Table 5.19 10-Bit A/D Conversion Characteristics (1)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item			Min.	Typ.	Max.	Unit	Test Conditions
Resolution			10	10	10	Bit	
Conversion time*1 (Operation at ADCLK = 100 MHz)	With 0.1-µF external capacitor	AN0 to AN7	0.5	—	—	µs	Sampling in 25 states
		Other channels	0.75	—	—	µs	Sampling in 50 states
	Without 0.1-µF external capacitor Permissible signal source impedance (max.) = 1 kΩ	AN0 to AN7	0.6	—	—	µs	Sampling in 35 states
		Other channels	0.75	—	—	µs	Sampling in 50 states
Analog input capacitance			—	—	6	pF	
Integral nonlinearity error			—	—	±3.0	LSB	
Offset error			—	—	±2.0	LSB	
Full-scale error			—	—	±3.0	LSB	
Quantization error			—	±0.5	—	LSB	
Absolute accuracy			—	—	±6.0	LSB	

Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

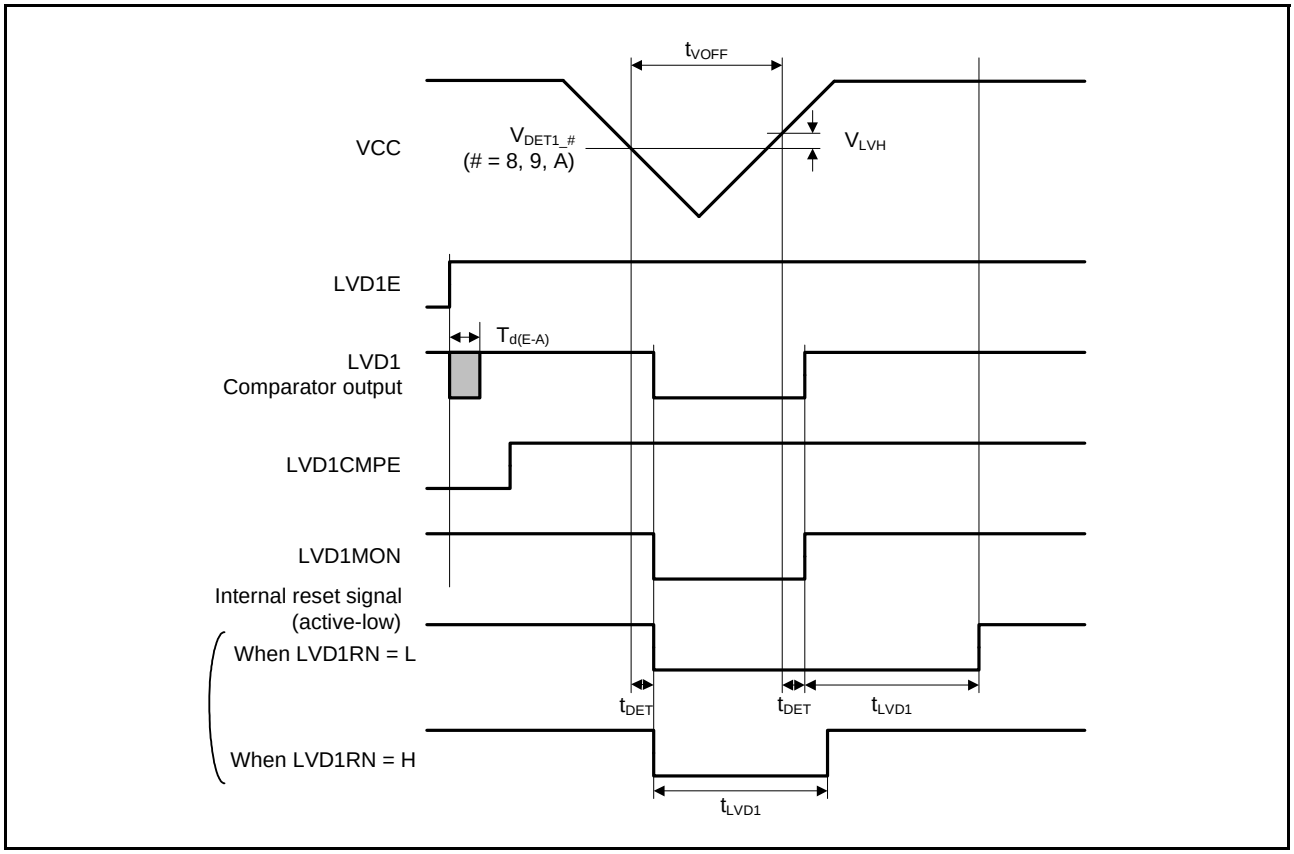


Figure 5.41 Voltage Detection Circuit Timing (V_{DET1})

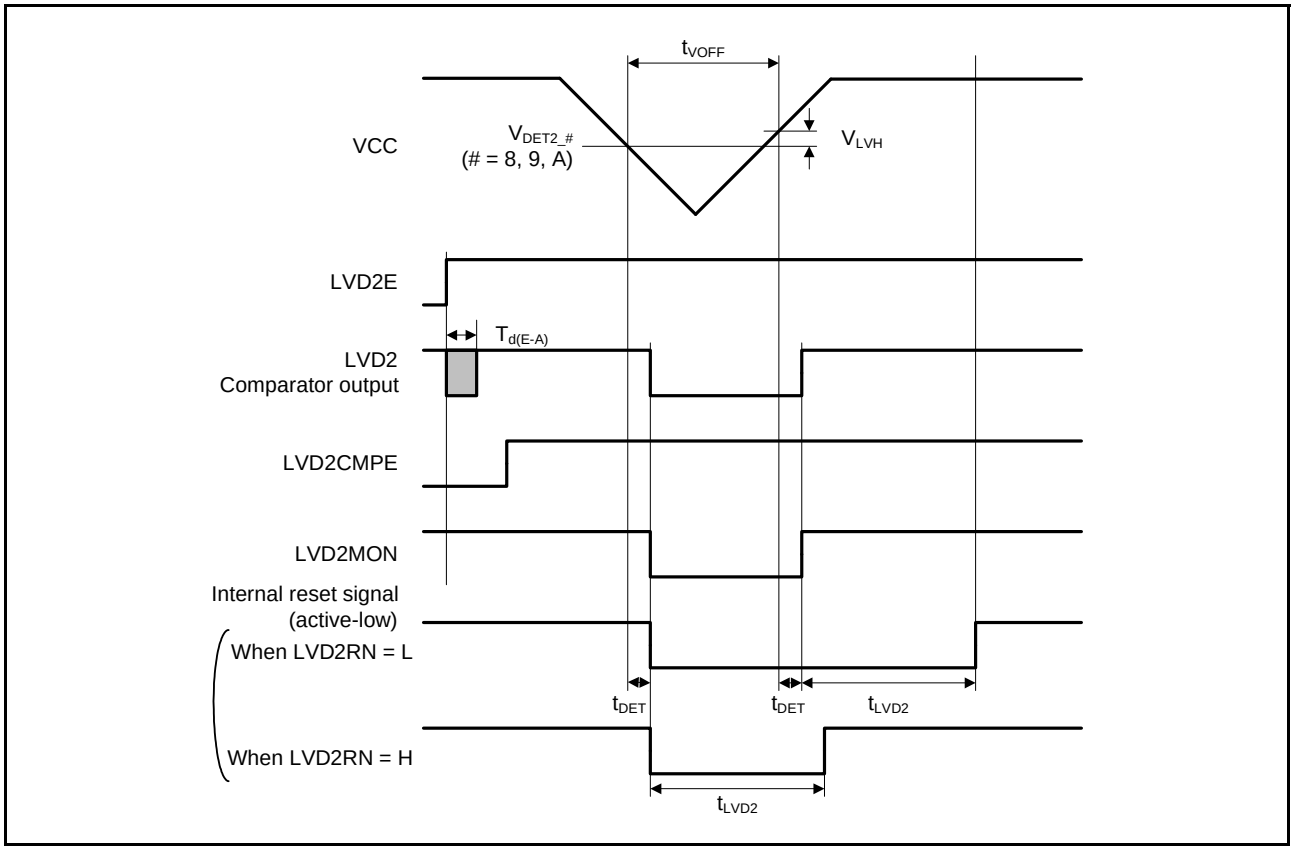


Figure 5.42 Voltage Detection Circuit Timing (V_{DET2})

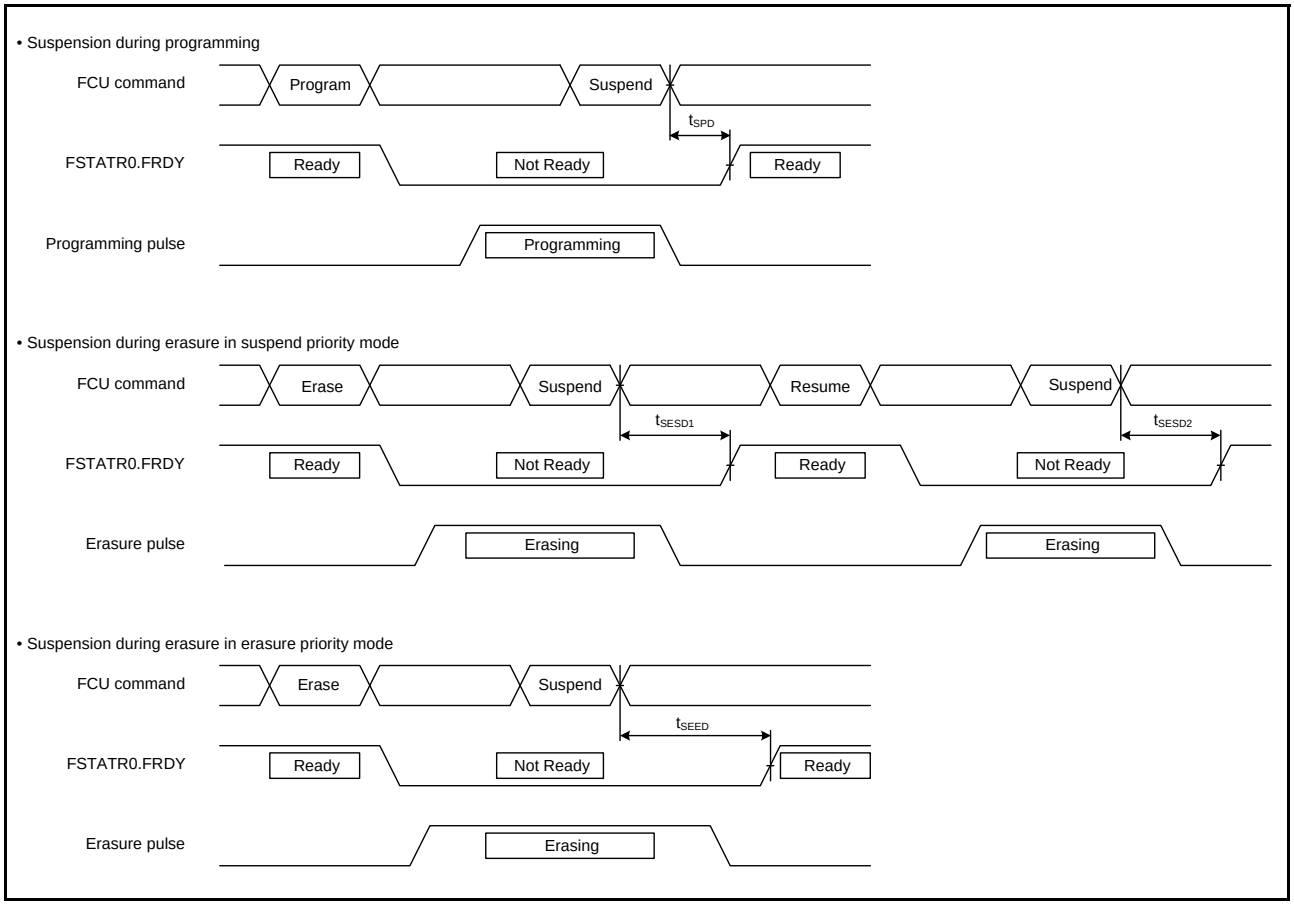


Figure 5.44 Flash Memory Program/Erase Suspend Timing

Table 6.5 Permissible Power Consumption (G version product only)

Condition: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0
$T_a = T_{opr}$

Item	Symbol	Typ.	Max.	Unit	Test Conditions
Total permissible power consumption*1	Pd	—	150	mW	85°C < Ta ≤ 105°C 64-pin version
	Pd	—	120	mW	85°C < Ta ≤ 105 °C 48-pin version

Note: • Please contact Renesas Electronics sales office for derating of operation under Ta = +85°C to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.
Note 1. The total power consumption of the whole chip including output current.

6.4 A/D Conversion Characteristics

Table 6.16 12-Bit A/D Conversion Characteristics

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item		min	typ	max	Unit	Test Conditions
Resolution		12	12	12	Bit	
Conversion time *1 (ADCLK = 50 MHz)	When the sample-and-hold circuit is in use per pin	1.6	—	—	µs	Sampling by the sample-and-hold circuit in 30 states. Sampling by the A/D converter in 20 states.
	When the sample-and-hold circuit is not in use per pin	1.0	—	—	µs	Sampling by the A/D converter in 20 states.
Analog input capacitance		—	—	6	pF	
Integral nonlinearity error		—	—	±4.0	LSB	
Offset error		—	—	±7.5	LSB	
Full-scale error		—	—	±7.5	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy	Sample and hold circuit in use	—	—	±8.0	LSB	AVin = 0.25 to AV_{REFH}–0.25
	Sample and hold circuit not in use	—	—	±8.0	LSB	AVin = AV_{REFL} to AV_{REFH}
Permissible signal source impedance		—	—	3.0	kΩ	

Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Table 6.17 Comparator Characteristics

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item	Symbol	Min	Typ	Max.	Unit	Test Conditions
Analog input capacitance	Cin	—	—	6	pF	
REFH pin offset voltage	Voff	—	—	5	mV	
REFL pin offset voltage		—	—	5	mV	
REFH input voltage range	Vin	1.7	—	AVcc – 0.3	V	
REFL input voltage range		0.3	—	AVcc – 1.7	V	
REFH reply time	tCR	—	—	0.5	µs	
REFL reply time	tCF	—	—	0.5	µs	

6.7 ROM (Flash Memory for Code Storage) Characteristics

Table 6.20 ROM (Flash Memory for Code Storage) Characteristics (1)

Condition: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Temperature range for the programming/erasure operation: $T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Reprogram/erase cycle*1	N_{pec}	1000	—	—	Times	
Data hold time	t_{DRP}	30*2	—	—	Year	Ta = +85°C

Note 1. Definition of reprogram/erase cycle:
The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 128-byte programming is performed 16 times for different addresses in 2-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).
Note 2. The value is obtained from the reliability test.

Table 6.21 ROM (Flash Memory for Code Storage) Characteristics (2)

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Temperature range for the programming/erasure operation: $T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item		Symbol	min	typ	max	Unit	Test Conditions
Programming time	128 bytes	t_{P128}	—	1	10	ms	FCLK = 50MHz $N_{PEC} \leq 100$
	4 Kbytes	t_{P4K}	—	23	50	ms	
	16 Kbytes	t_{P16K}	—	90	200	ms	
	128 bytes	t_{P128}	—	1.2	12	ms	FCLK=50MHz $N_{PEC} > 100$
	4 Kbytes	t_{P4K}	—	27.6	60	ms	
	16 Kbytes	t_{P16K}	—	108	240	ms	
Erasure time	4 Kbytes	t_{E4K}	—	25	60	ms	FCLK=50MHz $N_{PEC} \leq 100$
	16 Kbytes	t_{E16K}	—	100	240	ms	
	4 Kbytes	t_{E4K}	—	30	72	ms	FCLK=50MHz $N_{PEC} > 100$
	16 Kbytes	t_{E16K}	—	120	288	ms	
Suspend delay time during programming		t_{SPD}	—	—	120	µs	Figure 6.31 FCLK = 50MHz
First suspend delay time during erasing (in suspend priority mode)		t_{SESD1}	—	—	120	µs	
Second suspend delay time during erasing (in suspend priority mode)		t_{SESD2}	—	—	1.7	ms	
Suspend delay time during erasing (in erasure priority mode)		t_{SEED}	—	—	1.7	ms	
FCU reset time		t_{FCUR}	35	—	—	µs	