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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	81
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 20x10b, 8x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f563teadfb-v1

Table 1.3 List of Products (4/4)

Group	Part No.	Order Part No.	Package	On-chip ROM Capacity	On-chip RAM Capacity	Option	Operating Voltage	Operating Temperature
RX63T	R5F563TBAGFA	R5F563TBAGFA#V1	PLQP0120KA-A	256 Kbytes	24 Kbytes	CAN module included	VCC/ PLL/VCC 4.0 to 5.5V VCC_USB 3.0 to 3.6V AVCC/ AVCC0 4.0 to 5.5V	-40 to +105°C (G Version)*1
	R5F563TBAGFH	R5F563TBAGFH#V1	PLQP0112JA-A	256 Kbytes	24 Kbytes	CAN module included		
	R5F563TBAGFP	R5F563TBAGFP#V1	PLQP0100KB-A	256 Kbytes	24 Kbytes	CAN module included		
	R5F563TEBGF	R5F563TEBGF#V1	PLQP0144KA-A	512 Kbytes	48 Kbytes	CAN module included	VCC/ PLL/VCC/ VCC_USB 2.7 to 3.6V AVCC/ AVCC0 3.0 to 3.6V or 4.0 to 5.5V	
	R5F563TEBGFA	R5F563TEBGFA#V1	PLQP0120KA-A	512 Kbytes	48 Kbytes	CAN module included		
	R5F563TEBGFH	R5F563TEBGFH#V1	PLQP0112JA-A	512 Kbytes	48 Kbytes	CAN module included		
	R5F563TEBGFP	R5F563TEBGFP#V1	PLQP0100KB-A	512 Kbytes	48 Kbytes	CAN module included		
	R5F563TCBGF	R5F563TCBGF#V1	PLQP0144KA-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TCBGFA	R5F563TCBGFA#V1	PLQP0120KA-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TCBGFH	R5F563TCBGFH#V1	PLQP0112JA-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TCBGFP	R5F563TCBGFP#V1	PLQP0100KB-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TBBGF	R5F563TBBGF#V1	PLQP0144KA-A	256 Kbytes	24 Kbytes	CAN module included		
	R5F563TBBGFA	R5F563TBBGFA#V1	PLQP0120KA-A	256 Kbytes	24 Kbytes	CAN module included		
	R5F563TBBGFH	R5F563TBBGFH#V1	PLQP0112JA-A	256 Kbytes	24 Kbytes	CAN module included		
	R5F563TBBGFP	R5F563TBBGFP#V1	PLQP0100KB-A	256 Kbytes	24 Kbytes	CAN module included		
	R5F563T6EGFM	R5F563T6EGFM#V0	PLQP0064KB-A	64 Kbytes	8 Kbytes	CAN module not included	VCC/ PLL/VCC 2.7 to 3.6V AVCC0 3.0 to 3.6V	
	R5F563T5EGFM	R5F563T5EGFM#V0	PLQP0064KB-A	48 Kbytes	8 Kbytes	CAN module not included		
	R5F563T4EGFM	R5F563T4EGFM#V0	PLQP0064KB-A	32 Kbytes	8 Kbytes	CAN module not included		
	R5F563T6EGFL	R5F563T6EGFL#V0	PLQP0048KB-A	64 Kbytes	8 Kbytes	CAN module not included		
	R5F563T5EGFL	R5F563T5EGFL#V0	PLQP0048KB-A	48 Kbytes	8 Kbytes	CAN module not included		
	R5F563T4EGFL	R5F563T4EGFL#V0	PLQP0048KB-A	32 Kbytes	8 Kbytes	CAN module not included		

Note: • Orderable part numbers are current as of when this manual was published. Please make sure to refer to the relevant product page on the Renesas website for the latest part numbers.

Note: • The products with the product ID code 1 (ex. R5F563TEADFB#V1) are the revised version to the specification constraints of technical update TX-RX*-A84A / E described.

Note 1. Please contact Renesas Electronics sales office for derating of operation under Ta = +85°C to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.

1.5 Pin Assignments

Figure 1.3 to Figure 1.8 show the pin assignments. Table 1.5 to Table 1.10 show the lists of pins and pin functions.

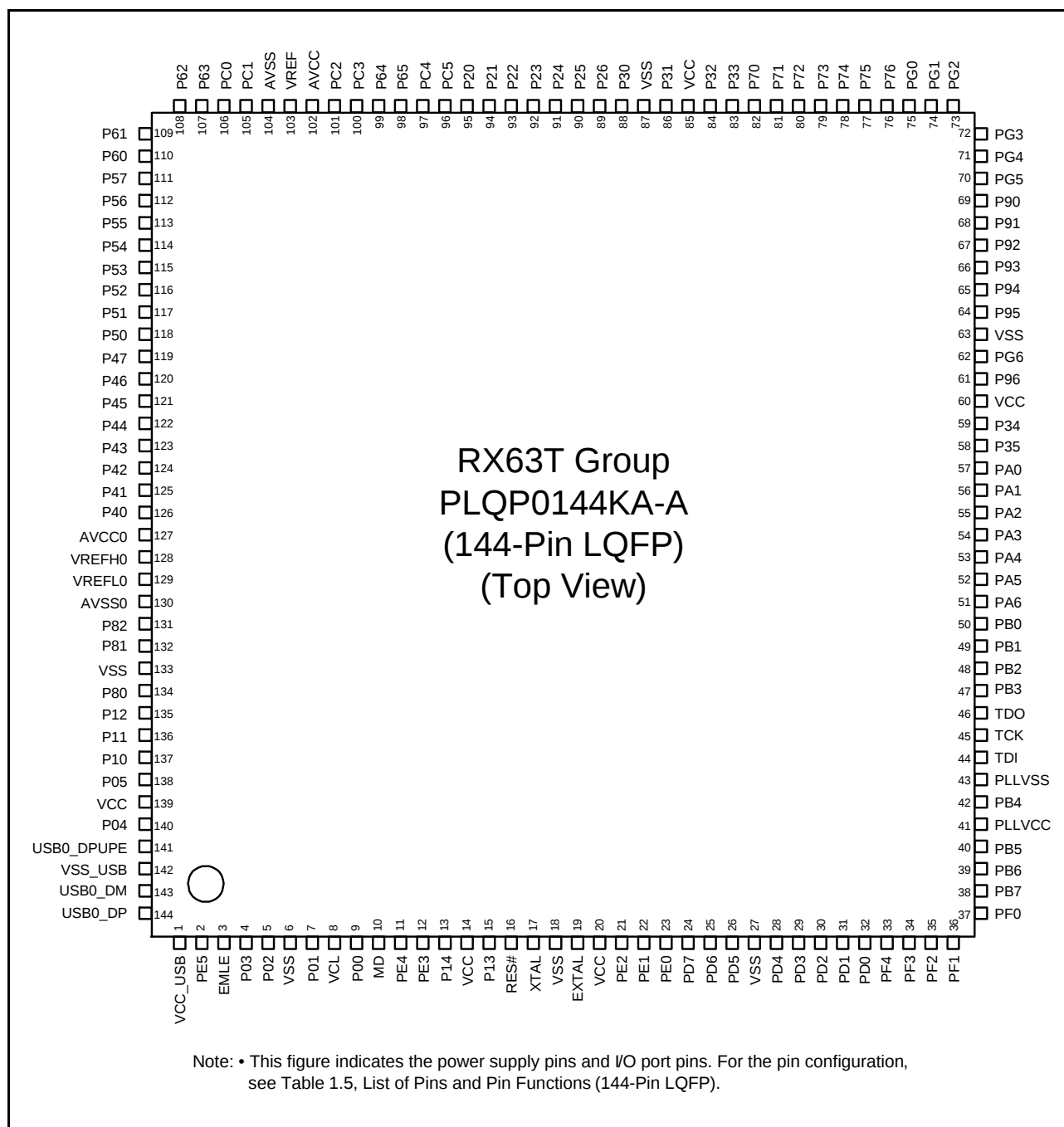


Figure 1.3 Pin Assignment (144-Pin LQFP)

Table 1.7 List of Pins and Pin Functions (112-Pin LQFP) (4/4)

Pin Number 112-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3, GPT, POE3, CAC)	Communications (SCIc, SCId, RSPI, RIIC, CAN)	Interrupt	S12ADB, AD, DA
110		P10		MTCLKD		IRQ0-DS	
111	TRST#	P05	WAIT#/CS2#				
112	TMS	P04					

Note 1. Available for use as SCI pin only in boot mode.

- Longword-size I/O registers

```
MOV.L #SFR_ADDR, R1
MOV.L #SFR_DATA, [R1]
CMP [R1].L, R1
;; Next process
```

If multiple registers are written to and a subsequent instruction should be executed after the write operations are entirely completed, only read the I/O register that was last written to and execute the operation using the value; it is not necessary to read or execute operation for all the registers that were written to.

(3) Number of Access Cycles to I/O Registers

For the number of I/O register access cycles, refer to Table 4.1, List of I/O Registers (Address Order).
The number of access cycles to I/O registers is obtained by following equation.*1

$$\begin{aligned} \text{Number of access cycles to I/O registers} = & \text{Number of bus cycles for internal main bus 1} + \\ & \text{Number of divided clock synchronization cycles} + \\ & \text{Number of bus cycles for internal peripheral bus 1 to 6} \end{aligned}$$

The number of bus cycles of internal peripheral bus 1 to 6 differs according to the register to be accessed.

When peripheral functions connected to internal peripheral bus 2 to 6 are accessed, the number of divided clock synchronization cycles is added.

The number of divided clock synchronization cycles differs depending on the frequency ratio between ICLK and PCLK (or FCLK, BCLK) or bus access timing.

In the peripheral function unit, when the frequency ratio of ICLK is equal to or greater than that of PCLK (or FCLK), the sum of the number of bus cycles for internal main bus 1 and the number of the divided clock synchronization cycles will be one cycle of PCLK (or FCLK) at a maximum. Therefore, one PCLK (or FCLK) has been added to the number of access states shown in Table 4.1.

When the frequency ratio of ICLK is lower than that of PCLK (or FCLK), the subsequent bus access is started from the ICLK cycle following the completion of the access to the peripheral functions. Therefore, the access cycles are described on an ICLK basis.

In the external bus control unit, the sum of the number of bus cycles for internal main bus 1 and the number of divided clock synchronization cycles will be one cycle of BCLK at a maximum. Therefore, one BCLK is added to the number of access cycles shown in Table 4.1.

Note 1. This applies to the number of cycles when the access from the CPU does not conflict with the instruction fetching to the external memory or bus access from the different bus master (DMAC or DTC).

(4) Note on Sleep Mode and Mode Transition

During sleep mode or a mode transition, do not write to the system control related registers (indicated by 'SYSTEM' in the Module Symbol column in Table 4.1, List of I/O Registers (Address Order)).

Table 4.1 List of I/O Registers (Address Order) (11/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 7206h	ICU	Interrupt Request Enable Register 06	IER06	8	8	2 ICLK		ICUb	Not present in versions with 64 or 48 pins.
0008 7207h	ICU	Interrupt Request Enable Register 07	IER07	8	8	2 ICLK			
0008 7208h	ICU	Interrupt Request Enable Register 08	IER08	8	8	2 ICLK			
0008 720Bh	ICU	Interrupt Request Enable Register 0B	IER0B	8	8	2 ICLK			Not present in versions with 112, 100, 64 or 48 pins.
0008 720Ch	ICU	Interrupt Request Enable Register 0C	IER0C	8	8	2 ICLK			
0008 720Dh	ICU	Interrupt Request Enable Register 0D	IER0D	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 720Eh	ICU	Interrupt Request Enable Register 0E	IER0E	8	8	2 ICLK			
0008 720Fh	ICU	Interrupt Request Enable Register 0F	IER0F	8	8	2 ICLK			
0008 7210h	ICU	Interrupt Request Enable Register 10	IER10	8	8	2 ICLK			
0008 7211h	ICU	Interrupt Request Enable Register 11	IER11	8	8	2 ICLK			
0008 7212h	ICU	Interrupt Request Enable Register 12	IER12	8	8	2 ICLK			
0008 7213h	ICU	Interrupt Request Enable Register 13	IER13	8	8	2 ICLK			
0008 7214h	ICU	Interrupt Request Enable Register 14	IER14	8	8	2 ICLK			
0008 7215h	ICU	Interrupt Request Enable Register 15	IER15	8	8	2 ICLK			
0008 7216h	ICU	Interrupt Request Enable Register 16	IER16	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7217h	ICU	Interrupt Request Enable Register 17	IER17	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7218h	ICU	Interrupt Request Enable Register 18	IER18	8	8	2 ICLK			
0008 7219h	ICU	Interrupt Request Enable Register 19	IER19	8	8	2 ICLK			
0008 721Ah	ICU	Interrupt Request Enable Register 1A	IER1A	8	8	2 ICLK			
0008 721Bh	ICU	Interrupt Request Enable Register 1B	IER1B	8	8	2 ICLK			
0008 721Ch	ICU	Interrupt Request Enable Register 1C	IER1C	8	8	2 ICLK			
0008 721Dh	ICU	Interrupt Request Enable Register 1D	IER1D	8	8	2 ICLK			
0008 721Eh	ICU	Interrupt Request Enable Register 1E	IER1E	8	8	2 ICLK			
0008 721Fh	ICU	Interrupt Request Enable Register 1F	IER1F	8	8	2 ICLK			
0008 72E0h	ICU	Software Interrupt Activation Register	SWINTR	8	8	2 ICLK			
0008 72F0h	ICU	Fast Interrupt Set Register	FIR	16	16	2 ICLK			
0008 7300h	ICU	Interrupt Source Priority Register 000	IPR000	8	8	2 ICLK			
0008 7301h	ICU	Interrupt Source Priority Register 001	IPR001	8	8	2 ICLK			
0008 7302h	ICU	Interrupt Source Priority Register 002	IPR002	8	8	2 ICLK			
0008 7303h	ICU	Interrupt Source Priority Register 003	IPR003	8	8	2 ICLK			
0008 7304h	ICU	Interrupt Source Priority Register 004	IPR004	8	8	2 ICLK			
0008 7305h	ICU	Interrupt Source Priority Register 005	IPR005	8	8	2 ICLK			
0008 7306h	ICU	Interrupt Source Priority Register 006	IPR006	8	8	2 ICLK			
0008 7307h	ICU	Interrupt Source Priority Register 007	IPR007	8	8	2 ICLK			
0008 7321h	ICU	Interrupt Source Priority Register 033	IPR033	8	8	2 ICLK			Not present in versions with 112, 100, 64 or 48 pins.
0008 7322h	ICU	Interrupt Source Priority Register 034	IPR034	8	8	2 ICLK			Not present in versions with 112, 100, 64 or 48 pins.
0008 7323h	ICU	Interrupt Source Priority Register 035	IPR035	8	8	2 ICLK			Not present in versions with 112, 100, 64 or 48 pins.
0008 7324h	ICU	Interrupt Source Priority Register 036	IPR036	8	8	2 ICLK			
0008 7327h	ICU	Interrupt Source Priority Register 039	IPR039	8	8	2 ICLK			
0008 7328h	ICU	Interrupt Source Priority Register 040	IPR040	8	8	2 ICLK			
0008 7329h	ICU	Interrupt Source Priority Register 041	IPR041	8	8	2 ICLK			
0008 732Ah	ICU	Interrupt Source Priority Register 042	IPR042	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 732B	ICU	Interrupt Source Priority Register 043	IPR043	8	8	2 ICLK			Not present in versions with 64 or 48 pins.

Table 4.1 List of I/O Registers (Address Order) (13/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK $\geq$ PCLK	ICLK $<$ PCLK		
0008 739Ah	ICU	Interrupt Source Priority Register 154	IPR154	8	8	2 ICLK		ICUB	
0008 739Eh	ICU	Interrupt Source Priority Register 158	IPR158	8	8	2 ICLK			
0008 73A1h	ICU	Interrupt Source Priority Register 161	IPR161	8	8	2 ICLK			
0008 73A3h	ICU	Interrupt Source Priority Register 163	IPR163	8	8	2 ICLK			
0008 73A5h	ICU	Interrupt Source Priority Register 165	IPR165	8	8	2 ICLK			
0008 73A6h	ICU	Interrupt Source Priority Register 166	IPR166	8	8	2 ICLK			
0008 73ABh	ICU	Interrupt Source Priority Register 171	IPR171	8	8	2 ICLK			
0008 73ACh	ICU	Interrupt Source Priority Register 172	IPR172	8	8	2 ICLK			
0008 73ADh	ICU	Interrupt Source Priority Register 173	IPR173	8	8	2 ICLK			
0008 73AEh	ICU	Interrupt Source Priority Register 174	IPR174	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 73B1h	ICU	Interrupt Source Priority Register 177	IPR177	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 73B4h	ICU	Interrupt Source Priority Register 180	IPR180	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 73B7h	ICU	Interrupt Source Priority Register 183	IPR183	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 73B9h	ICU	Interrupt Source Priority Register 185	IPR185	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 73BCh	ICU	Interrupt Source Priority Register 188	IPR188	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 73BEh	ICU	Interrupt Source Priority Register 190	IPR190	8	8	2 ICLK			Not present in versions with 112, 100, 64 or 48 pins.
0008 73C2h	ICU	Interrupt Source Priority Register 194	IPR194	8	8	2 ICLK			
0008 73C6h	ICU	Interrupt Source Priority Register 198	IPR198	8	8	2 ICLK			
0008 73C7h	ICU	Interrupt Source Priority Register 199	IPR199	8	8	2 ICLK			
0008 73C8h	ICU	Interrupt Source Priority Register 200	IPR200	8	8	2 ICLK			
0008 73C9h	ICU	Interrupt Source Priority Register 201	IPR201	8	8	2 ICLK			
0008 73D6h	ICU	Interrupt Source Priority Register 214	IPR214	8	8	2 ICLK			
0008 73D9h	ICU	Interrupt Source Priority Register 217	IPR217	8	8	2 ICLK			
0008 73DCh	ICU	Interrupt Source Priority Register 220	IPR220	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 73DFh	ICU	Interrupt Source Priority Register 223	IPR223	8	8	2 ICLK			Not present in versions with 100, 64 or 48 pins.
0008 73E2h	ICU	Interrupt Source Priority Register 226	IPR226	8	8	2 ICLK			
0008 73E5h	ICU	Interrupt Source Priority Register 229	IPR229	8	8	2 ICLK			
0008 73E8h	ICU	Interrupt Source Priority Register 232	IPR232	8	8	2 ICLK			
0008 73EBh	ICU	Interrupt Source Priority Register 235	IPR235	8	8	2 ICLK			
0008 73EEh	ICU	Interrupt Source Priority Register 238	IPR238	8	8	2 ICLK			
0008 73F1h	ICU	Interrupt Source Priority Register 241	IPR241	8	8	2 ICLK			
0008 73F4h	ICU	Interrupt Source Priority Register 244	IPR244	8	8	2 ICLK			
0008 73F7h	ICU	Interrupt Source Priority Register 247	IPR247	8	8	2 ICLK			
0008 73FAh	ICU	Interrupt Source Priority Register 250	IPR250	8	8	2 ICLK			
0008 7400h	ICU	DMAC Activation Request Select Register 0	DMRSR0	8	8	2 ICLK			
0008 7404h	ICU	DMAC Activation Request Select Register 1	DMRSR1	8	8	2 ICLK			
0008 7408h	ICU	DMAC Activation Request Select Register 2	DMRSR2	8	8	2 ICLK			
0008 740Ch	ICU	DMAC Activation Request Select Register 3	DMRSR3	8	8	2 ICLK			
0008 7500h	ICU	IRQ Control Register 0	IRQCR0	8	8	2 ICLK			
0008 7501h	ICU	IRQ Control Register 1	IRQCR1	8	8	2 ICLK			
0008 7502h	ICU	IRQ Control Register 2	IRQCR2	8	8	2 ICLK			
0008 7503h	ICU	IRQ Control Register 3	IRQCR3	8	8	2 ICLK			
0008 7504h	ICU	IRQ Control Register 4	IRQCR4	8	8	2 ICLK			
0008 7505h	ICU	IRQ Control Register 5	IRQCR5	8	8	2 ICLK			
0008 7506h	ICU	IRQ Control Register 6	IRQCR6	8	8	2 ICLK			Not present in versions with 64 or 48 pins.

Table 4.1 List of I/O Registers (Address Order) (28/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 C293h	SYSTEM	Main Clock Oscillator Forced Oscillation Control Register	MOFCR	8	8	4, 5 PCLKB	2, 3 ICLK	Clock Generation Circuit	
0008 C296h	FLASH	Flash P/E Protection Register	FWEPROR	8	8	4, 5 PCLKB	2, 3 ICLK	ROM	
0008 C297h	SYSTEM	Voltage Monitoring Circuit Control Register	LVMPCR	8	8	4, 5 PCLKB	2, 3 ICLK	LVDA	
0008 C298h	SYSTEM	Voltage Detection Level Select Register	LVDLVLR	8	8	4, 5 PCLKB	2, 3 ICLK		
0008 C29Ah	SYSTEM	Voltage Monitoring 1 Circuit Control Register 0	LVD1CR0	8	8	4, 5 PCLKB	2, 3 ICLK		
0008 C29Bh	SYSTEM	Voltage Monitoring 2 Circuit Control Register 0	LVD2CR0	8	8	4, 5 PCLKB	2, 3 ICLK		
0008 C2A0h to 0008 C2BFh	SYSTEM	Deep Standby Backup Register 0 to 31	DPSBKR0 to 31	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption	
0008 C300h	ICU	Group 0 Interrupt Source Register	GRP00	32	32	1, 2 PCLKB	2 ICLK	ICUb	Not present in versions with 64 or 48 pins.
0008 C330h	ICU	Group 12 Interrupt Source Register	GRP12	32	32	1, 2 PCLKB	2 ICLK		
0008 C340h	ICU	Group 0 Interrupt Enable Register	GEN00	32	32	1, 2 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C370h	ICU	Group 12 Interrupt Enable Register	GEN12	32	32	1, 2 PCLKB	2 ICLK		
0008 C380h	ICU	Group 0 Interrupt Clear Register	GCR00	32	32	1, 2 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C4C0h	POE	Input Level Control/Status Register 1	ICSR1	16	8, 16	2, 3 PCLKB	2 ICLK	POE3	
0008 C4C2h	POE	Output Level Control/Status Register 1	OCSR1	16	8, 16	2, 3 PCLKB	2 ICLK		
0008 C4C4h	POE	Input Level Control/Status Register 2	ICSR2	16	8, 16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C4C6h	POE	Output Level Control/Status Register 2	OCSR2	16	8, 16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C4C8h	POE	Input Level Control/Status Register 3	ICSR3	16	8, 16	2, 3 PCLKB	2 ICLK		
0008 C4CAh	POE	Software Port Output Enable Register	SPOER	8	8	2, 3 PCLKB	2 ICLK		
0008 C4CBh	POE	Port Output Enable Control Register 1	POECR1	8	8	2, 3 PCLKB	2 ICLK		
0008 C4CCh	POE	Port Output Enable Control Register 2	POECR2	16	16	2, 3 PCLKB	2 ICLK		
0008 C4CEh	POE	Port Output Enable Control Register 3	POECR3	16	16	2, 3 PCLKB	2 ICLK		
0008 C4D0h	POE	Port Output Enable Control Register 4	POECR4	16	16	2, 3 PCLKB	2 ICLK		
0008 C4D2h	POE	Port Output Enable Control Register 5	POECR5	16	16	2, 3 PCLKB	2 ICLK		
0008 C4D4h	POE	Port Output Enable Control Register 6	POECR6	16	16	2, 3 PCLKB	2 ICLK		
0008 C4D6h	POE	Input Level Control/Status Register 4	ICSR4	16	8, 16	2, 3 PCLKB	2 ICLK		
0008 C4D8h	POE	Input Level Control/Status Register 5	ICSR5	16	8, 16	2, 3 PCLKB	2 ICLK		
0008 C4DAh	POE	Active Level Setting Register 1	ALR1	16	8, 16	2, 3 PCLKB	2 ICLK		
0008 C4DCh	POE	Input Level Control/Status Register 6	ICSR6	16	16	2, 3 PCLKB	2 ICLK		
0008 C4DEh	POE	Active Level Setting Register 2	ALR2	16	8, 16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C4E0h	POE	Input Level Control/Status Register 7	ICSR7	16	8, 16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C4E2h	POE	Port Output Enable Control Register 7	POECR7	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C4E4h	POE	Port Output Enable Control Register 8	POECR8	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0009 1200h to 0009 13FFh	CAN1	Mailbox Register 0 to 31	MB0 to 31	128	8, 16, 32	2, 3 PCLKB	2 ICLK	CAN	Not present in versions with 64 or 48 pins.
0009 1400h to 0009 141Ch	CAN1	Mask Register 0 to 7	MKR0 to 7	32	8, 16, 32	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0009 1420h	CAN1	FIFO Received ID Compare Register 0 and 1	FIDCR0	32	8, 16, 32	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0009 1424h	CAN1	FIFO Received ID Compare Register 0 and 1	FIDCR1	32	8, 16, 32	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0009 1428h	CAN1	Mask Invalid Register	MKIVLR	32	8, 16, 32	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0009 142Ch	CAN1	Mailbox Interrupt Enable Register	MIER	32	8, 16, 32	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0009 1820h to 0009 183Fh	CAN1	Message Control Register 0 to 31	MCTL0 to 31	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.

Table 4.1 List of I/O Registers (Address Order) (39/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK $\geq$ PCLK	ICLK $<$ PCLK		
000C 21A6h	GPT1	A/D Converter Start Request Timing Buffer Register A	GTADTBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK	GPT	
000C 21A8h	GPT1	A/D Converter Start Request Timing Double-Buffer Register A	GTADTDBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 21ACh	GPT1	A/D Converter Start Request Timing Register B	GTADTRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 21AEh	GPT1	A/D Converter Start Request Timing Buffer Register B	GTADTBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 21B0h	GPT1	A/D Converter Start Request Timing Double-Buffer Register B	GTADTDBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 21B4h	GPT1	General PWM Timer Output Negate Control Register	GTONCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 21B6h	GPT1	General PWM Timer Dead Time Control Register	GTDTCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 21B8h	GPT1	General PWM Timer Dead Time Value Register U	GTDVU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 21BAh	GPT1	General PWM Timer Dead Time Value Register D	GTDVD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 21BCh	GPT1	General PWM Timer Dead Time Buffer Register U	GTDBU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 21BEh	GPT1	General PWM Timer Dead Time Buffer Register D	GTDBD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 21C0h	GPT1	General PWM Timer Output Protection Function Status Register	GTSOS	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 21C2h	GPT1	General PWM Timer Output Protection Function Temporary Release Register	GTSOTR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2200h	GPT2	General PWM Timer I/O Control Register	GTIOR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2202h	GPT2	General PWM Timer Interrupt Output Setting Register	GTINTAD	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2204h	GPT2	General PWM Timer Control Register	GTCR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2206h	GPT2	General PWM Timer Buffer Enable Register	GTBER	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2208h	GPT2	General PWM Timer Count Direction Register	GTUDC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 220Ah	GPT2	General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register	GTITC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 220Ch	GPT2	General PWM Timer Status Register	GTST	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 220Eh	GPT2	General PWM Timer Counter	GTCNT	16	16	2 to 5 PCLKA	2, 3 ICLK		
000C 2210h	GPT2	General PWM Timer Compare Capture Register A	GTCCRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2212h	GPT2	General PWM Timer Compare Capture Register B	GTCCRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2214h	GPT2	General PWM Timer Compare Capture Register C	GTCCRC	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2216h	GPT2	General PWM Timer Compare Capture Register D	GTCCRD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2218h	GPT2	General PWM Timer Compare Capture Register E	GTCCRE	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 221Ah	GPT2	General PWM Timer Compare Capture Register F	GTCCRF	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 221Ch	GPT2	General PWM Timer Cycle Setting Register	GTPR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 221Eh	GPT2	General PWM Timer Cycle Setting Buffer Register	GTPBR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2220h	GPT2	General PWM Timer Cycle Setting Double-Buffer Register	GTPDBR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2224h	GPT2	A/D Converter Start Request Timing Register A	GTADTRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2226h	GPT2	A/D Converter Start Request Timing Buffer Register A	GTADTBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2228h	GPT2	A/D Converter Start Request Timing Double-Buffer Register A	GTADTDBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 222Ch	GPT2	A/D Converter Start Request Timing Register B	GTADTRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 222Eh	GPT2	A/D Converter Start Request Timing Buffer Register B	GTADTBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		

Table 4.1 List of I/O Registers (Address Order) (47/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK $\geq$ PCLK	ICLK $<$ PCLK		
000C3056h	DPC	Control Calculation Parameter Setting Register KQ2	PARAMKQ2	16	16	3 to 5 PCLKA	2, 3 ICLK	DPC	Not present in versions with 64 or 48 pins.
000C305Ah	DPC	Control Calculation Parameter Setting Register KF2	PARAMKF2	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C305Eh	DPC	Control Calculation Parameter Setting Register KP3	PARAMKP3	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3062h	DPC	Control Calculation Parameter Setting Register KI3	PARAMKI3	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3066h	DPC	Control Calculation Parameter Setting Register KQ3	PARAMKQ3	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C306Ah	DPC	Control Calculation Parameter Setting Register KF3	PARAMKF3	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C306Ch	DPC	Control Calculation Result Higher-Order Bits Store Register 0	RESULTU0	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C306Eh	DPC	Control Calculation Result Lower-Order Bits Store Register 0	RESULTL0	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3070h	DPC	Control Calculation Result Higher-Order Bits Store Register 1	RESULTU1	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3072h	DPC	Control Calculation Result Lower-Order Bits Store Register 1	RESULTL1	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3074h	DPC	Control Calculation Result Higher-Order Bits Store Register 2	RESULTU2	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3076h	DPC	Control Calculation Result Lower-Order Bits Store Register 2	RESULTL2	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3078h	DPC	Control Calculation Result Higher-Order Bits Store Register 3	RESULTU3	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C307Ah	DPC	Control Calculation Result Lower-Order Bits Store Register 3	RESULTL3	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C307Eh	DPC	Input Code Monitor Enable Register	TMONEN	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3082h	DPC	Maximum Input Code Monitor Register 0	TMONMAX0	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3086h	DPC	Minimum Input Code Monitor Register 0	TMONMIN0	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C308Ah	DPC	Maximum Input Code Monitor Register 1	TMONMAX1	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C308Eh	DPC	Minimum Input Code Monitor Register 1	TMONMIN1	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3092h	DPC	Maximum Input Code Monitor Register 2	TMONMAX2	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3096h	DPC	Minimum Input Code Monitor Register 2	TMONMIN2	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C309Ah	DPC	Maximum Input Code Monitor Register 3	TMONMAX3	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C309Eh	DPC	Minimum Input Code Monitor Register 3	TMONMIN3	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C30A2h	DPC	Overvoltage Output Error Judgment Threshold Setting Register 0	ERRVTH0	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C30A6h	DPC	Overvoltage Output Error Judgment Threshold Setting Register 1	ERRVTH1	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C30AAh	DPC	Overvoltage Output Error Judgment Threshold Setting Register 2	ERRVTH2	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C30AEh	DPC	Overvoltage Output Error Judgment Threshold Setting Register 3	ERRVTH3	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C30B2h	DPC	PWM Shut-Down at Overvoltage Output Error Setting Register	ERRDWN	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
007F C402h	FLASH	Flash Mode Register	FMODR	8	8	2, 3 FCLK	2, 3 ICLK	ROM/ E2 DataFlash Memory	
007F C410h	FLASH	Flash Access Status Register	FASTAT	8	8	2, 3 FCLK	2, 3 ICLK		
007F C411h	FLASH	Flash Access Error Interrupt Enable Register	FAEINT	8	8	2, 3 FCLK	2, 3 ICLK		
007F C412h	FLASH	Flash Ready Interrupt Enable Register	FRDYIE	8	8	2, 3 FCLK	2, 3 ICLK	ROM	
007F C440h	FLASH	E2 DataFlash Read Enable Register 0	DFLRE0	16	16	2, 3 FCLK	2, 3 ICLK	E2 DataFlash Memory	
007F C442h	FLASH	E2 DataFlash Read Enable Register 1	DFLRE1	16	16	2, 3 FCLK	2, 3 ICLK		
007F C450h	FLASH	E2 DataFlash P/E Enable Register 0	DFLWE0	16	16	2, 3 FCLK	2, 3 ICLK		
007F C452h	FLASH	E2 DataFlash P/E Enable Register 1	DFLWE1	16	16	2, 3 FCLK	2, 3 ICLK		

Table 5.4 DC Characteristics (3)

Note: Common standard values for conditions not given in the table are listed as "Condition 1" to "Condition 3" below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

The following relation applies when the USB is in use under condition 1 or condition 2: Vcc = PLLVcc = Vcc_USB = 3.0 to 3.6 V.

T_a = T_{opr}, T_a is common to conditions 1 to 3.

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Supply current *1	During operation	Max. *2	I _{CC} *3	—	—	70	mA	ICLK = 100 MHz PCLKA = 100 MHz PCLKB = 50 MHz PCLKC = 100 MHz PCLKD = 50 MHz FCLK = 50 MHz
		Normal *4		—	40	—		
		Increased by BGO operation *5		—	15	—		
	Sleep mode				40	55		
	All-module-clock-stop mode *6				20	30		
	During standby	Software standby mode		—	0.10	3	mA	
		Deep software standby mode		—	20	60	μA	
	Analog power supply current	During 12-bit A/D conversion (per unit)		AI _{CC0}	—	1.5	4.2	mA
Programmable gain amplifier (per channel)		—	1		1.5	mA		
Window comparator (per channel)		—	0.5		0.7	mA		
Waiting for 12-bit A/D conversion (all units)		—	0.1		8	μA		
During 10-bit A/D conversion (per channel)		AI _{CC}	—	0.9	1.4	mA		
During D/A conversion (per unit)				0.1	4	μA		
Waiting for 10-bit A/D, D/A conversion (all units)			—	0.1	4	μA		
Reference power supply current	During 12-bit A/D conversion (per unit)		AI _{REFH0}	—	1.6	2.5	mA	
	Waiting for 12-bit A/D conversion (all units)			—	0.1	1.5	μA	
	During 10-bit A/D conversion (per channel)		AI _{REF}	—	0.2	0.3	mA	
	During D/A conversion (per unit)				1	1.5	mA	
	Waiting for 10-bit A/D, D/A conversion (all units)			—	0.1	1.2	μA	
VCC rising gradient			SV _{CC}	—	—	20	ms/ V	

Note 1. Supply current values are with all output pins unloaded.

Note 2. Measured with clocks supplied to the peripheral functions. This does not include the BGO operation.

Note 3. I_{CC} depends on f (ICLK) as follows. (ICLK: PCLK = 8:4)

I_{CC} max = 0.6 × f + 10 (max)

I_{CC} typ = 0.3 × f + 10 (normal)

I_{CC} max = 0.45 × f + 10 (sleep mode)

Note 4. Measured with clocks not supplied to the peripheral functions. This does not include the BGO operation.

Note 5. Incremented if data is written to or erased from the on-chip ROM or on-chip data-flash memory for data storage during the program execution.

Note 6. The values are for reference.

5.3.5 Bus Timing

Table 5.12 Bus Timing (1)

Condition: VCC = PLLVCC = VCC_USB = AVCC0 = AVCC = 3.0 to 3.6 V,

VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V

VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

 $T_a = T_{opr}$ Output load conditions: $V_{OH} = VCC \times 0.5$, $V_{OL} = VCC \times 0.5$, $I_{OH} = -1.0$ mA, $I_{OL} = 1.0$ mA, $C = 30$ pF

Item	Symbol	Min.	Max.	Unit	Test Conditions
Address delay time	t_{AD}	—	30	ns	Figure 5.13 to Figure 5.16
Byte control delay time	t_{BCD}	—	30	ns	
CS# delay time	t_{CSD}	—	30	ns	
RD# delay time	t_{RSD}	—	30	ns	
Read data setup time	t_{RDS}	20	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	—	30	ns	
Write data delay time	t_{WDD}	—	35	ns	
Write data hold time	t_{WDH}	0	—	ns	
WAIT# setup time	t_{WTS}	20	—	ns	Figure 5.17
WAIT# hold time	t_{WTH}	0	—	ns	

Table 5.13 Bus Timing (2)

Condition: VCC = PLLVCC = AVCC0 = AVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V,

VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V

VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

 $T_a = T_{opr}$ Output load conditions: $V_{OH} = VCC \times 0.5$, $V_{OL} = VCC \times 0.5$, $I_{OH} = -1.0$ mA, $I_{OL} = 1.0$ mA, $C = 30$ pF

Item	Symbol	Min.	Max.	Unit	Test Conditions
Address delay time	t_{AD}	—	15	ns	Figure 5.13 to Figure 5.16
Byte control delay time	t_{BCD}	—	15	ns	
CS# delay time	t_{CSD}	—	15	ns	
RD# delay time	t_{RSD}	—	15	ns	
Read data setup time	t_{RDS}	15	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	—	15	ns	
Write data delay time	t_{WDD}	—	15	ns	
Write data hold time	t_{WDH}	0	—	ns	
WAIT# setup time	t_{WTS}	15	—	ns	Figure 5.17
WAIT# hold time	t_{WTH}	0	—	ns	

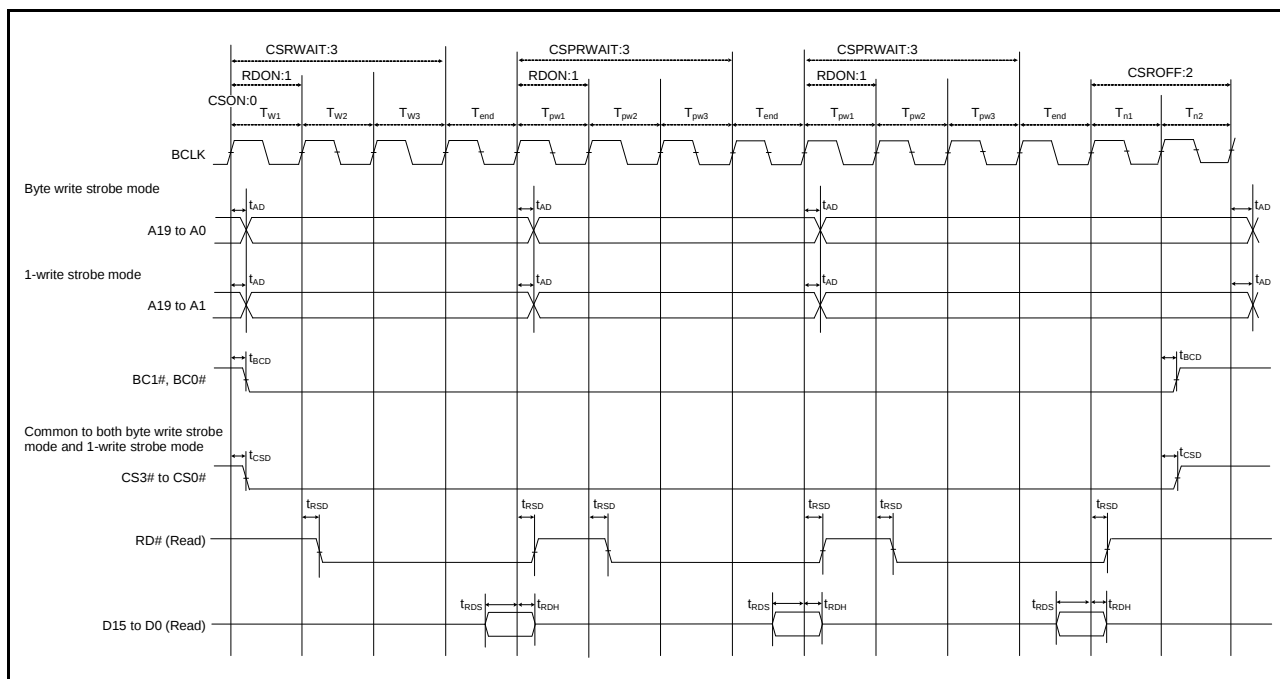


Figure 5.15 External Bus Timing/Page Read Cycle (Bus Clock Synchronized)

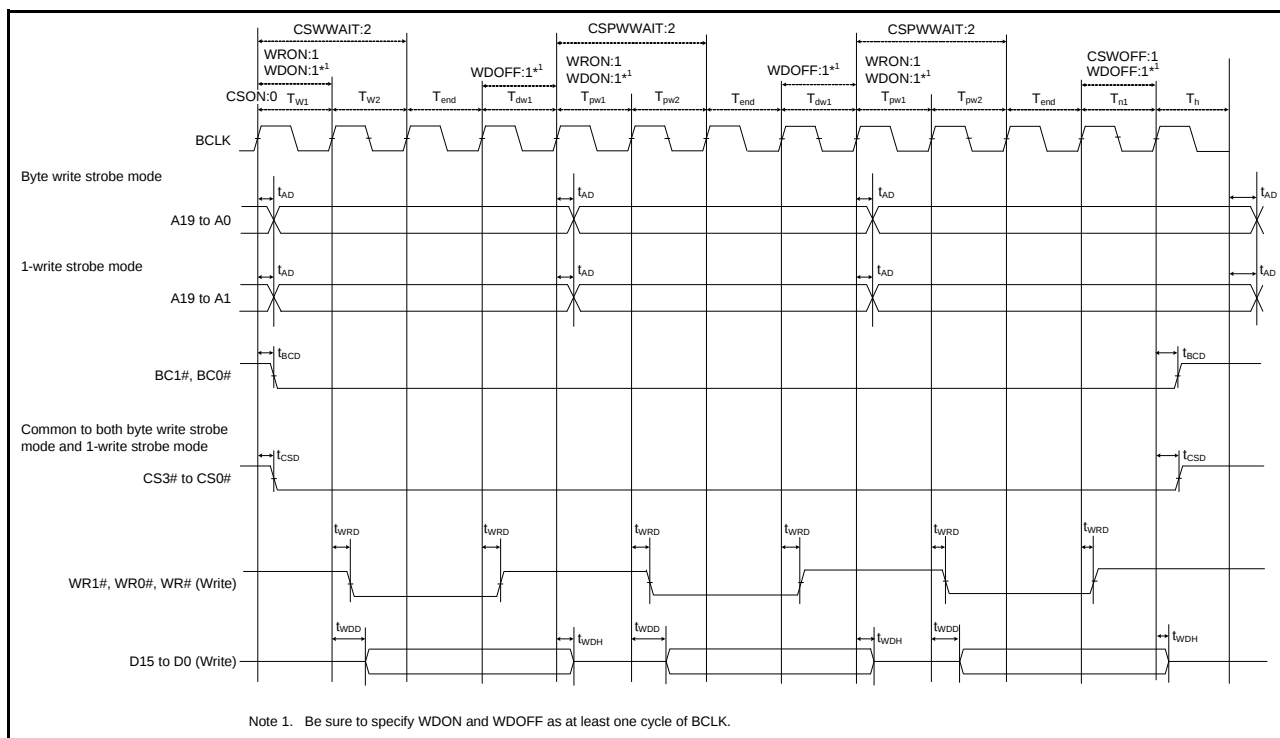


Figure 5.16 External Bus Timing/Page Write Cycle (Bus Clock Synchronized)

5.3.6 Timing of On-Chip Peripheral Modules

Table 5.16 Timing of On-Chip Peripheral Modules (1)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

T_a = T_{opr}. T_a is common to conditions 1 to 3.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
I/O ports	Input data pulse width		t _{PRW}	1.5	—	t _{PCyc}	Figure 5.22
MTU3	Input capture input pulse width	Single-edge setting	t _{TICW}	3	—	t _{PAcyc}	Figure 5.23
		Both-edge setting		5	—		
	Input capture input fall time		t _{TICTF}	—	0.1	μs/V	When Input capture at rising edge, or Input capture at both edges is selected.
	Timer clock pulse width	Single-edge setting	t _{TCKWH} , t _{TCKWL}	3	—	t _{PAcyc}	Figure 5.25
		Both-edge setting		5	—		
		Phase counting mode		5	—		
	Timer clock input fall time		t _{TCKTF}	—	0.1	μs/V	
POE3	POE# input pulse width		t _{POEW}	1.5	—	t _{PCyc}	Figure 5.28
GPT	Input capture input pulse width	Single-edge setting	t _{GTICW}	3	—	t _{PAcyc}	Figure 5.26
		Both-edge setting		5	—		
	Input capture input fall time		t _{GTICTF}	—	0.1	μs/V	When Input capture at rising edge, or Input capture at both edges is selected. When Count operation is started at rising edge, or Count operation is started at both edges is selected. When Count operation is stopped at rising edge, or Count operation is stopped at both edges is selected. When Counter is cleared at rising edge, or Counter is cleared at both edges is selected.
	External trigger input pulse width	Single-edge setting	t _{OTETW}	3	—	t _{PAcyc}	Figure 5.27
		Both-edge setting		5	—		
	External trigger input fall time		t _{GTETRGTF}	—	0.1	μs/V	When Count operation is started at rising edge, or Count operation is started at both edges is selected. When Count operation is stopped at rising edge, or Count operation is stopped at both edges is selected. When Counter is cleared at rising edge, or Counter is cleared at both edges is selected.

Table 5.16 Timing of On-Chip Peripheral Modules (6)

Note: Common standard values for conditions not given in the table are listed as "Condition 1" to "Condition 3" below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

T_a = T_{opr}. T_a is common to conditions 1 to 3.

Item		Symbol	Min.*1, *2	Max.	Unit	Test Conditions
Simple IIC (Standard-mode)	SCL, SDA input rise time	t _{Sr}	—	1000	ns	Figure 5.36
	SCL, SDA input fall time	t _{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t _{SP}	0	4 × t _{Pcyc}	ns	
	Data input setup time	t _{SDAS}	250	—	ns	
	Data input hold time	t _{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C _b	—	400	pF	
Simple IIC (Fast-mode)	SCL, SDA input rise time	t _{Sr}	20 + 0.1C _b	300	ns	
	SCL, SDA input fall time	t _{Sf}	20 + 0.1C _b	300	ns	
	SCL, SDA input spike pulse removal time	t _{SP}	0	4 × t _{Pcyc}	ns	
	Data input setup time	t _{SDAS}	100	—	ns	
	Data input hold time	t _{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C _b	—	400	pF	

Note 1. The value in parentheses is used when ICMR3.NF[1:0] are set to 11b while a digital filter is enabled with ICFER.NFE = 1.

Note 2. C_b indicates the total capacity of the bus line.

Note 3. t_{Pcyc}: PCLK cycle

5.3.7 Timing of PWM Delay Generation Circuit

Table 5.17 Timing of the PWM Delay Generation Circuit

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

T_a = T_{opr}. T_a is common to conditions 1 to 3.

Item	Symbol	Typ.	Max.	Unit	Test Conditions
Resolution	—	312.5	—	ps	PCLKA = 100 MHz
DNL*1	—	±2.0	—	LSB	

Note 1. This value is correct when the difference between each code and the next is a resolution of one bit (1 LSB).

Table 6.5 Permissible Power Consumption (G version product only)

Condition: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V

AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

 $T_a = T_{opr}$

Item	Symbol	Typ.	Max.	Unit	Test Conditions
Total permissible power consumption*1	Pd	—	150	mW	85°C < Ta ≤ 105°C 64-pin version
	Pd	—	120	mW	85°C < Ta ≤ 105 °C 48-pin version

Note: • Please contact Renesas Electronics sales office for derating of operation under Ta = +85°C to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.

Note 1. The total power consumption of the whole chip including output current.

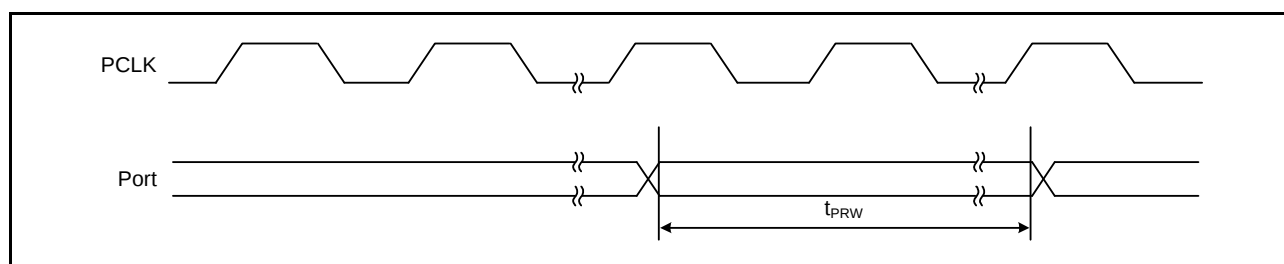
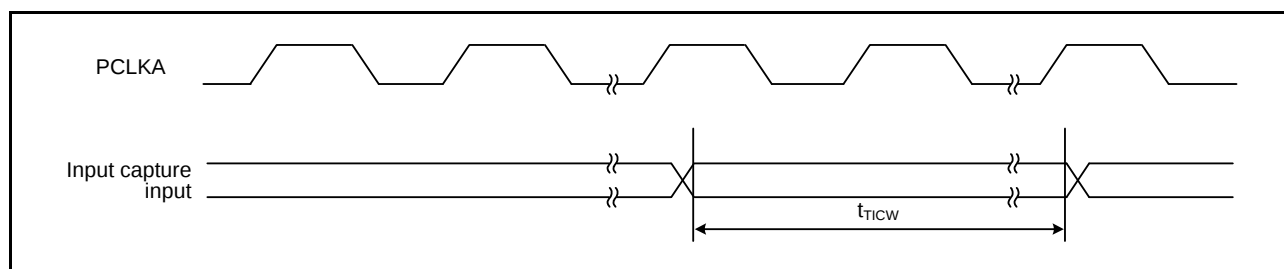
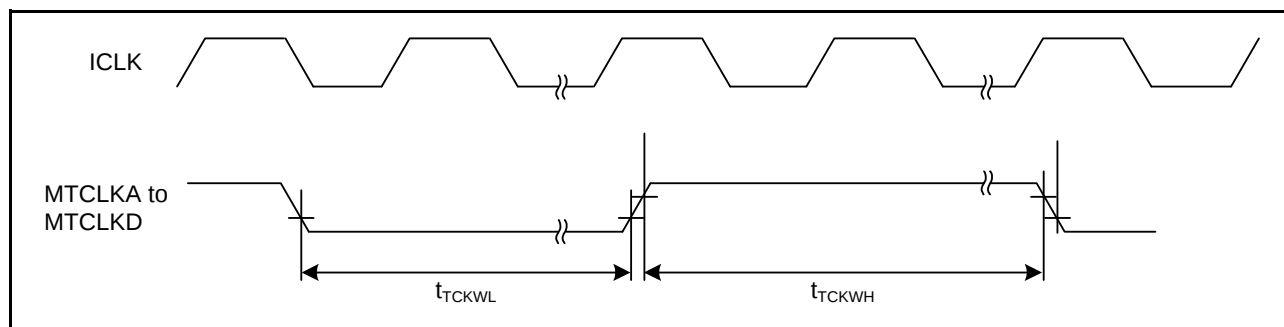
Table 6.15 Timing of On-Chip Peripheral Modules (5)

Conditions: $V_{CC} = 2.7$ to 3.6 V, $V_{SS} = AVSS0 = VREFL0 = 0$ V,
 $AVCC0 = 3.0$ to 3.6 V, $VREFH0 = 3.0$ V to $AVCC0$,
 $T_a = T_{opr}$

	Item	Symbol	Min.*1, *2	Max.	Unit	Test Conditions
Simple IIC (Standard-mode)	SCL, SDA input rise time	t_{Sr}	—	1000	ns	Figure 6.25
	SCL, SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	$4 \times t_{IICcyc}$	ns	
	Data input setup time	t_{SDAS}	250	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
Simple IIC (Fast-mode)	SCL, SDA input rise time	t_{Sr}	$20 + 0.1C_b$	300	ns	
	SCL, SDA input fall time	t_{Sf}	$20 + 0.1C_b$	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	$4 \times t_{IICcyc}$	ns	
	Data input setup time	t_{SDAS}	100	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note 1. The value in parentheses is used when ICMR3.NF[1:0] are set to 11b while a digital filter is enabled with ICFER.NFE = 1.

Note 2. C_b indicates the total capacity of the bus line.

**Figure 6.12 I/O port Input Timing****Figure 6.13 MTU3 Input/Output Timing****Figure 6.14 MTU3 Clock Input Timing**

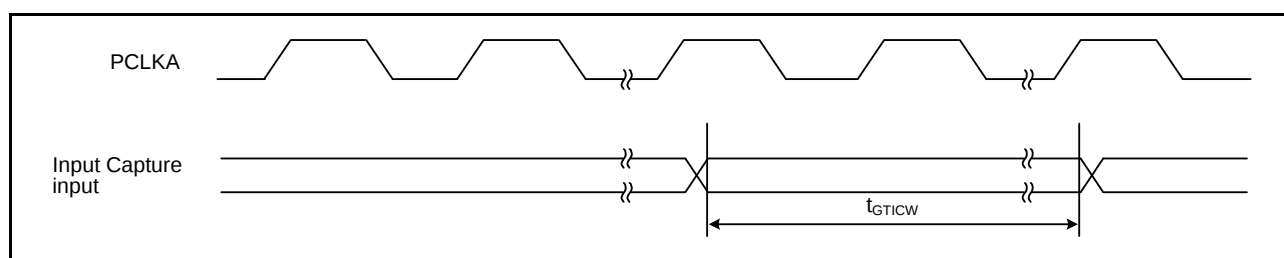


Figure 6.15 GPT Input/Output Timing

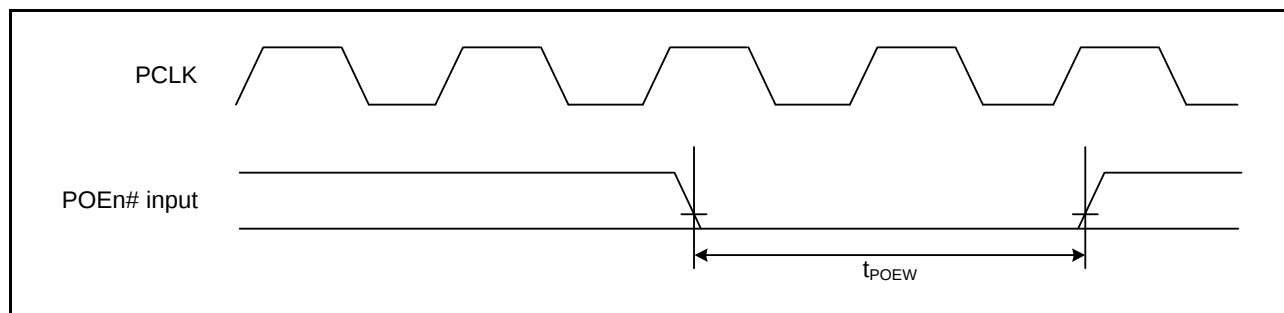


Figure 6.16 POE3# Input Timing

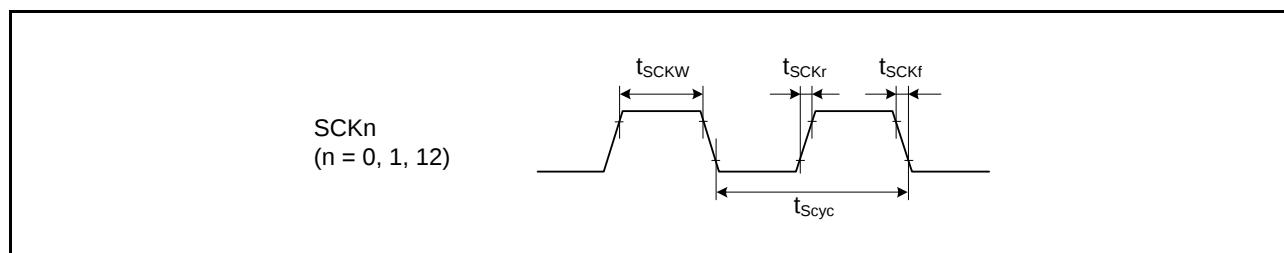


Figure 6.17 SCK Clock Input Timing

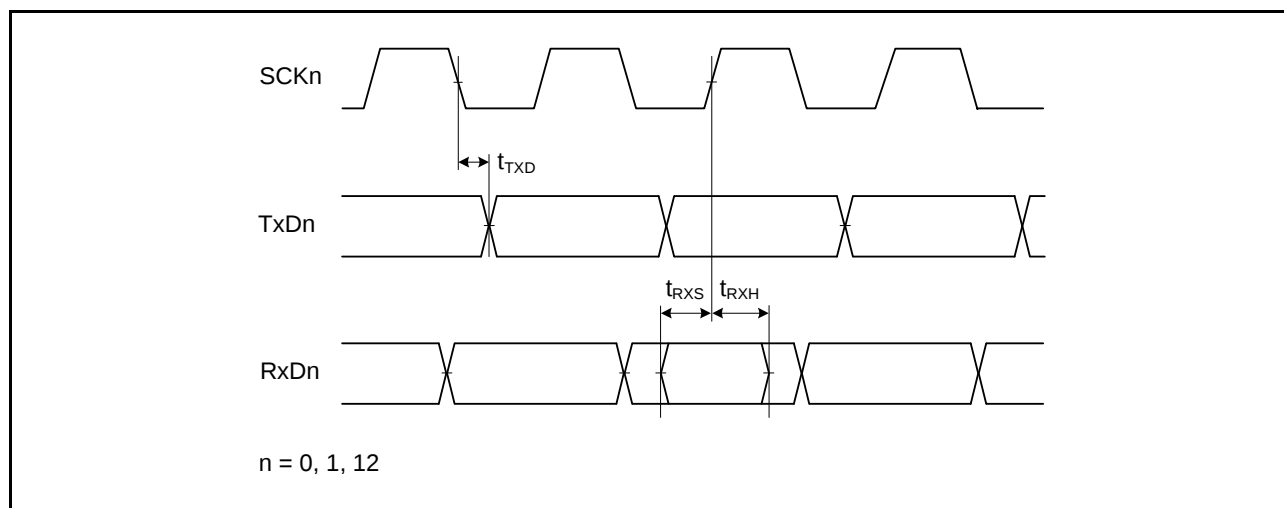


Figure 6.18 SCI Input/Output Timing: Clock Synchronous Mode

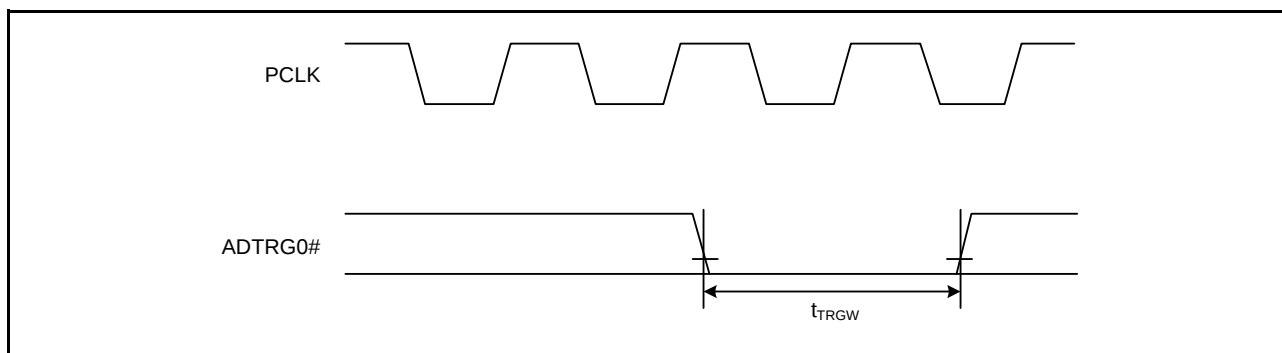


Figure 6.19 AD Converter External Trigger Input Timing

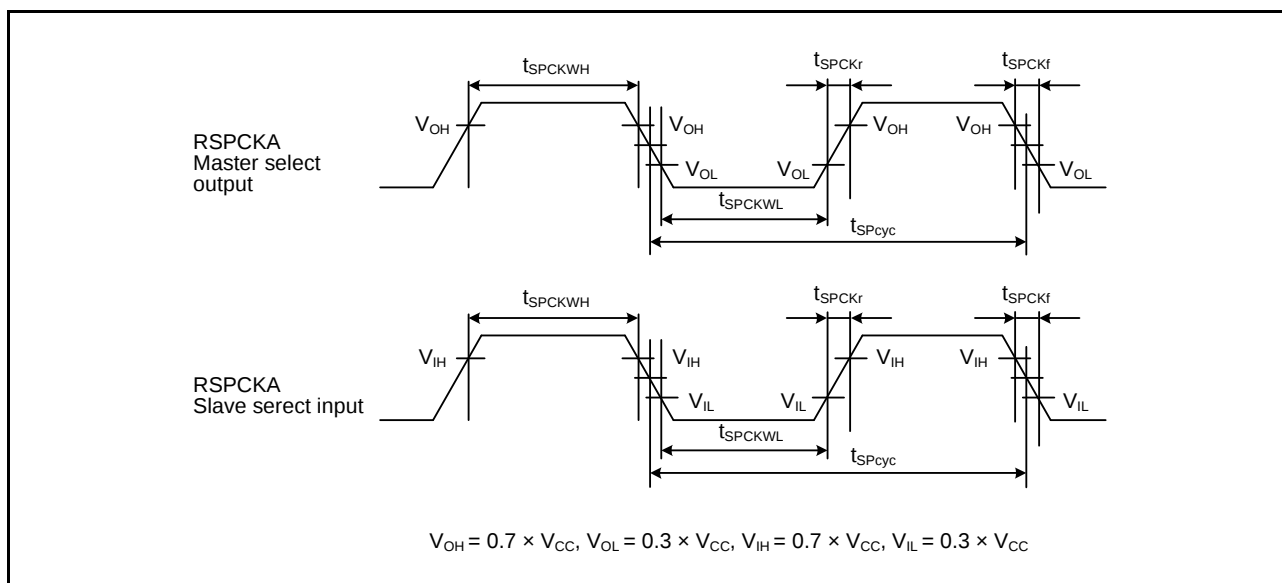


Figure 6.20 RSPI Clock Timing and Simple SPI Clock Timing

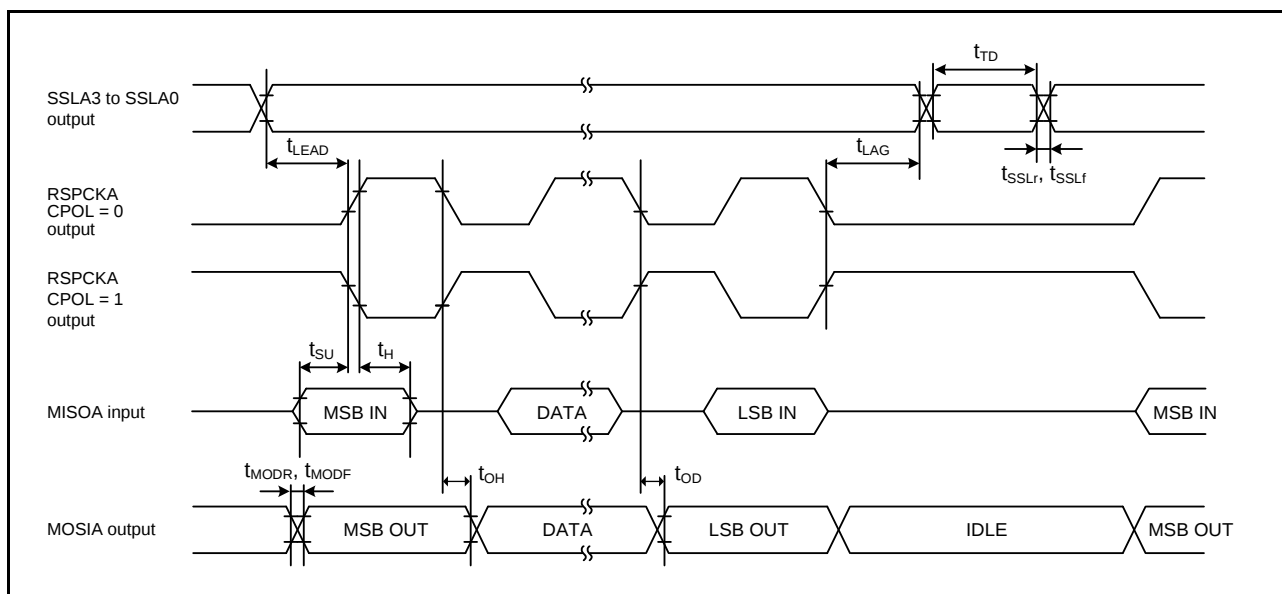


Figure 6.21 RSPI Timing (Master, CPHA = 0) and Simple SPI Timing (Master, CKPH = 1)

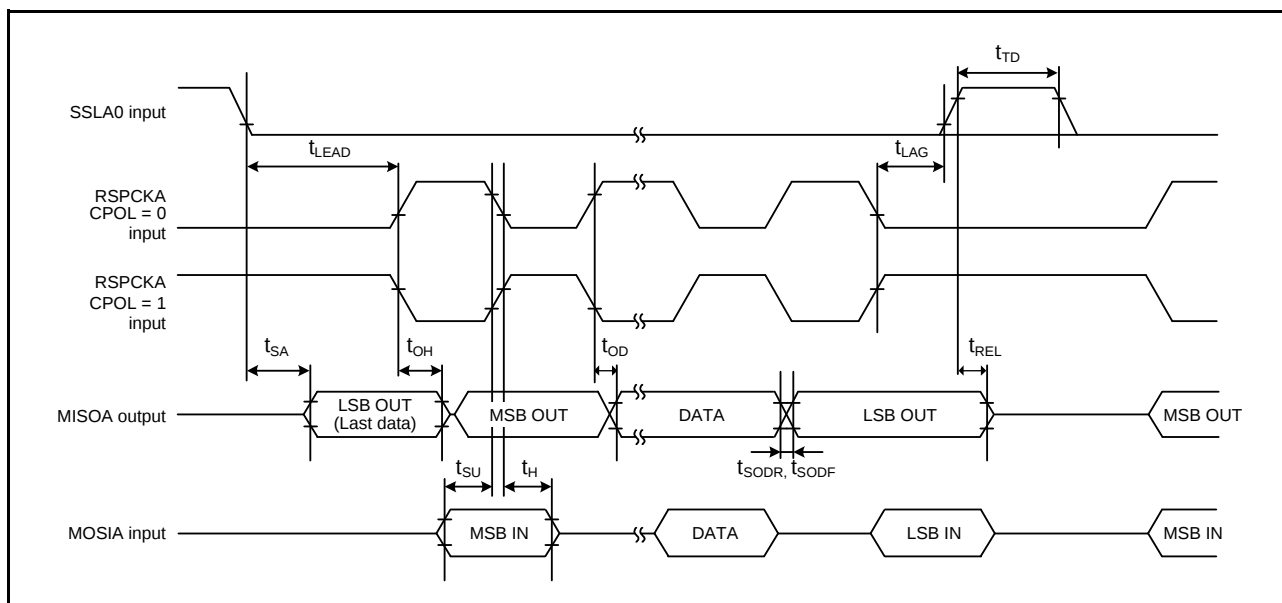


Figure 6.24 RSPCKA Timing (Slave, CPHA = 1) and Simple SPI Timing (Slave, CKPH = 0)

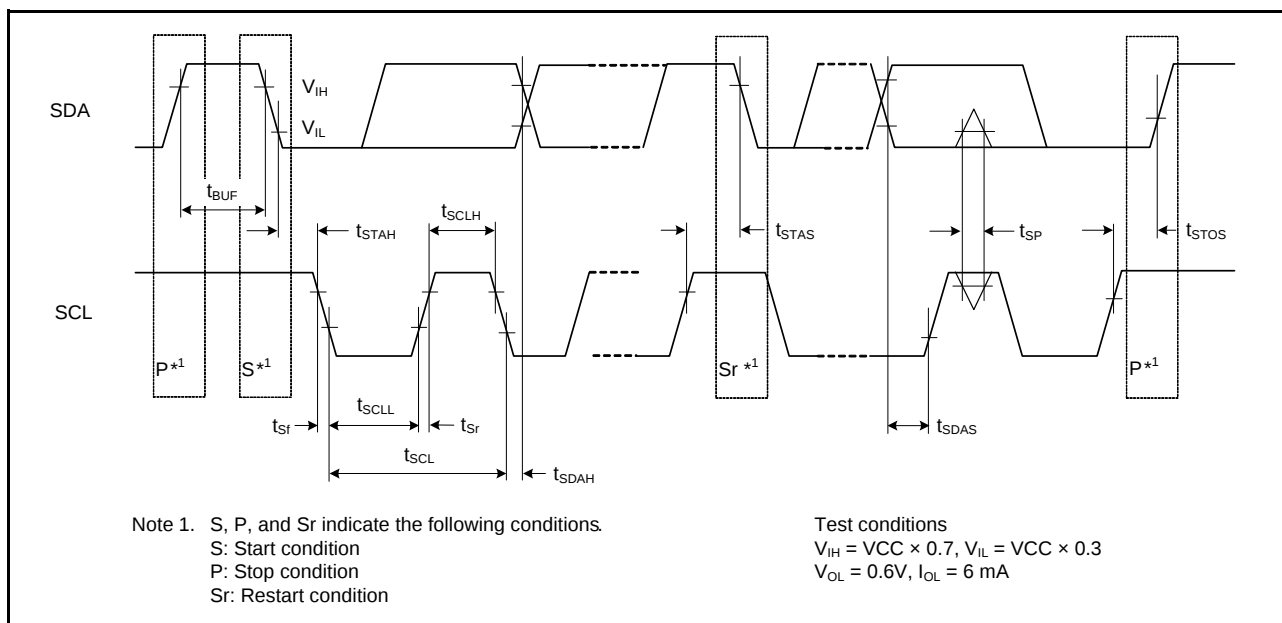


Figure 6.25 IIC Bus Interface Input/Output Timing and Simple IIC Bus Interface Input/Output Timing

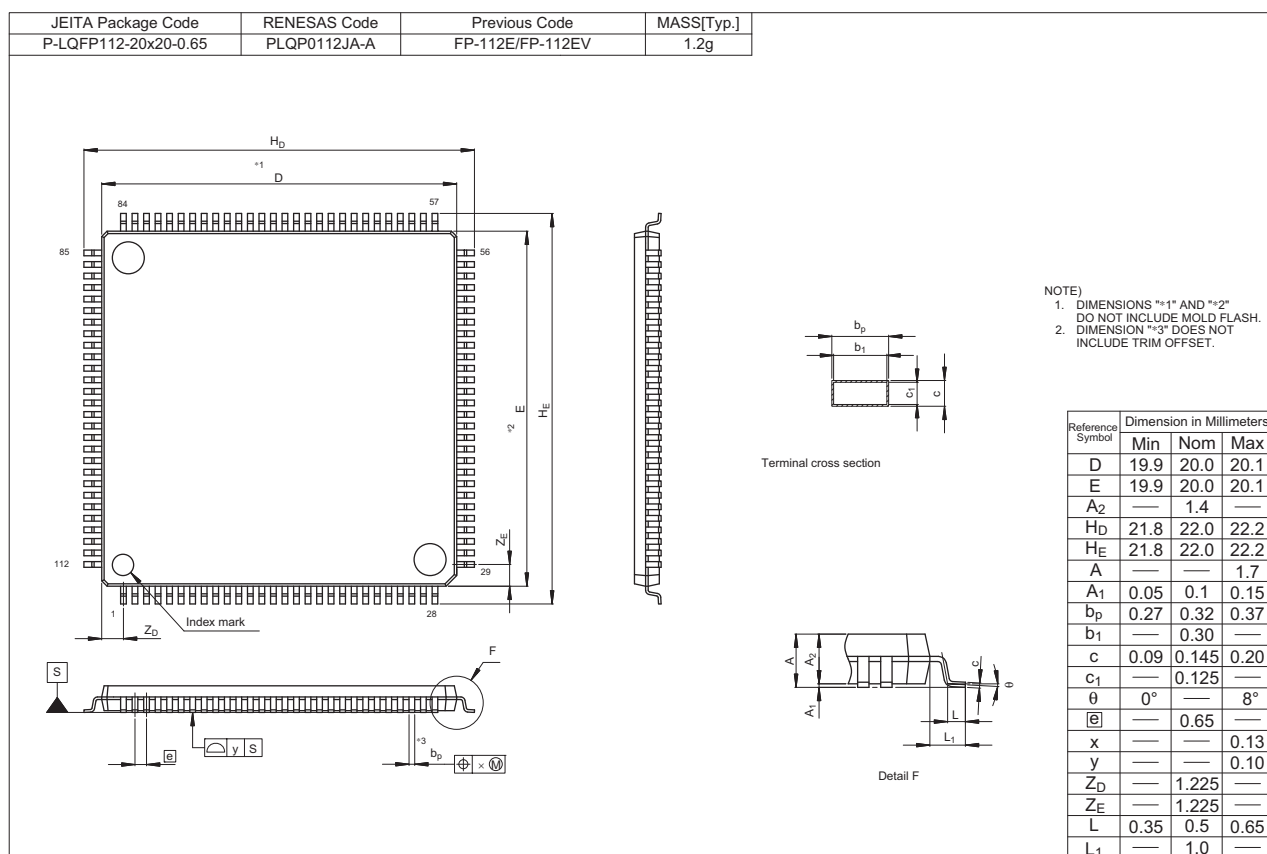


Figure C 112-Pin LQFP (PLQP0112JA-A)