Renesas Electronics America Inc - R5F563TEADFH#V0 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	69
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x10b, 8x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f563teadfh-v0

1. Overview

1.1 Outline of Specifications

Table 1.1 lists the specifications in outline, and Table 1.2 lists the functions of products.
Table 1.1 shows an outline of the maximum specifications, and the available peripheral modules and number of channels differ according to the number of pins on the package and the ROM capacity. For details, see Table 1.2, Comparison of Functions for Different Packages.

Table 1.1 Outline of Specifications (1/7)

Classification	Module/Function	Description
CPU	CPU	• Maximum operating frequency: 100 MHz • 32-bit RX CPU • Minimum instruction execution time: One instruction per state (cycle of the system clock) • Address space: 4-Gbyte linear • Register set of the CPU General purpose: Sixteen 32-bit registers Control: Nine 32-bit registers Accumulator: One 64-bit register • Basic instructions: 73 • Floating-point operation instructions: 8 • DSP instructions: 9 • Addressing modes: 10 • Data arrangement Instructions: Little endian Data: Selectable as little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits • Memory protection unit (MPU)
	FPU	• Single precision floating point (32 bits) • Data types and floating-point exceptions in conformance with the IEEE754 standard
Memory	ROM	• Capacity: 512 Kbytes, 384 Kbytes, 256 Kbytes, 64 Kbytes, 48 Kbytes, 32 Kbytes • 100 MHz, no-wait access • On-board programming: Programs can be modified through SCI or USB while the MCU is mounted on the board. • Off-board programming: Programs can be modified using parallel programmer. (only in 144-, 120-, 112- and 100-pin versions)
	RAM	• Capacity: 48 Kbytes, 32 Kbytes, 24 Kbytes, 8 Kbytes • 100 MHz, no-wait access
	E^2 data flash	• Capacity: 32 Kbytes, 8 Kbytes • Programming/erasing: 100,000 times • On-board programming: Programs can be modified through SCI or USB while the MCU is mounted on the board. Programming from the user program is possible.
MCU operating modes		[144-, 120-, 112- and 100-pin versions] Single-chip mode, on-chip ROM enabled extended mode, on-chip ROM disabled extended mode (switchable by software) [64- and 48-pin versions] Single-chip mode

Table 1.1 Outline of Specifications (4/7)

Classification	Module/Function	Description
Timers	General PWM timer (GPT)	• 16 bits x 8 channels • Counting up or down (saw-wave), counting up and down (triangle-wave) selectable for all channels • Select from among four count clocks (PCLKA/1, PCLKA/4, PCLKA/8, and PCLKA/16) for each channel • 2 input/output pins per channel • 2 output compare/input capture registers per channel • For the 2 output compare/input capture registers of each channel, 4 registers are provided as buffer registers and are capable of operating as comparison registers when buffering is not in use. • In output compare operation, buffer switching can be at peaks or troughs, enabling the generation of laterally asymmetrically PWM waveforms. • Registers for setting up frame intervals on each channel (with capability for generating interrupts on overflow or underflow) • Synchronizable operation of the several counters • Modes of synchronized operation (synchronized, or displaced by desired times for phase shifting) • Generation of dead times in PWM operation • Through combination of three counters, generation of automatic three-phase PWM waveforms incorporating dead times • Starting, clearing, and stopping counters in response to external or internal triggers • Internal trigger sources: Output of the internal comparator detection, software, and compare-match • The main clock can be used as a counter clock for measuring the timing of the edges of signals produced by frequency-dividing the dedicated clock signal for the IWDT (to detect abnormal oscillation). • A PWM delay with an accuracy of up to 1/32 times the period of the system clock (ICLK) can be generated to control the timing with which signals from the two PWM output pins from each of channels 0 to 3 rise and fall.
	Compare match timer (CMT)	• (16 bits × 2 channels) × 2 units • Select from among four internal clock signals (PCLK/8, PCLK/32, PCLK/128, PCLK/512)
	Watchdog timer (WDTA)	• 14 bits × 1 channel • Select from among 6 counter-input clock signals (PCLK/4, PCLK/64, PCLK/128, PCLK/512, PCLK/2048, PCLK/8192)
	Independent watchdog timer (IWDTa)	• 14 bits × 1 channel • Counter-input clock: Dedicated on-chip oscillator • Dedicated clock/1, dedicated clock/16, dedicated clock/32, dedicated clock/64, dedicated clock/128, dedicated clock/256
Communication function	USB 2.0 host/function module (USBa)	• Includes a UDC (USB Device Controller) and transceiver for USB 2.0 • Single port • Compliance with the USB 2.0 specification • Transfer rate: Full speed (12 Mbps) • Self-power mode and bus power mode are selectable • Supports the OTG (On-The-Go) • Incorporates 2 Kbytes of RAM as a transfer buffer
	Serial communications interfaces (SCIc, SCId)	• 5 channels (SCIc: 4 channels + SCId: 1 channel) • SCIc Serial communications modes: Asynchronous, clock synchronous, and smart-card interface Multi-processor function On-chip baud rate generator allows selection of the desired bit rate Choice of LSB-first or MSB-first transfer Simple I^2C Simple SPI • SCId (The following functions are added to SCIc) Supports the serial communications protocol, which contains the start frame and information frame Supports the LIN format

1.4 Pin Functions

Table 1.4 lists the pin functions.

Table 1.4 Pin Functions (1/5)

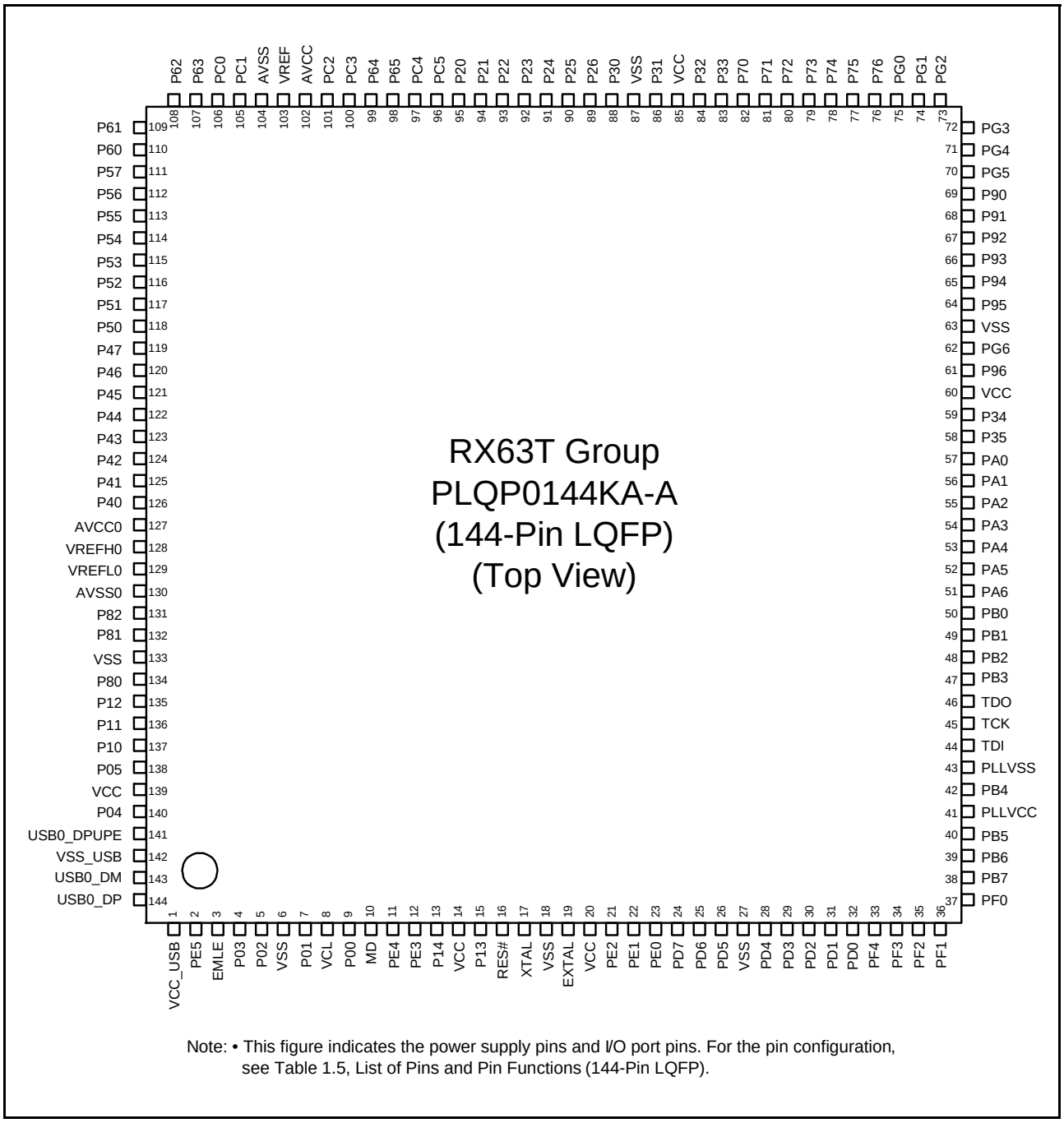
Classifications	Pin Name	I/O	Description
Power supply	VCC	—	Power supply pin. Connect it to the system power supply. Connect this pin to VSS via a 0.1-μF capacitor. The capacitor should be placed close to the pin
	VCL	—	Connect this pin to VSS via a 0.1-μF capacitor. The capacitor should be placed close to the pin
	VSS	—	Ground pin. Connect it to the system power supply (0 V)
	PLLVCC	—	Power supply pin. Connect it to the system power supply.
	PLLVSS	—	Ground pin. Connect it to the system power supply (0 V)
Clock	XTAL	Output	Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin
	EXTAL	Input	
	BCLK	Output	Outputs the external bus clock for external devices
Clock frequency accuracy measurement	CACREF	Input	Input for the trigger signal in measuring accuracy of the clock frequency
Operating mode control	MD	Input	Pin for setting the operating mode. The signal levels on these pins must not be changed during operation
System control	RES#	Input	Reset signal input pin. This LSI enters the reset state when this signal goes low
	EMLE	Input	Input pin for the on-chip emulator enable signal. When the on-chip emulator is used, this pin should be driven high. When not used, it should be driven low
On-chip emulator	FINEC	Input	Fine interface clock pin
	FINED	I/O	Fine interface pin
	TRST#	Input	On-chip emulator pins. When the EMLE pin is driven high, these pins are dedicated for the on-chip emulator.
	TMS	Input	
	TDI	Input	
	TCK	Input	
	TDO	Output	
	TRCLK	Output	This pin outputs the clock for synchronization with the trace data
	TRSYNC	Output	This pin indicates that output from the TRDATA0 to TRDATA3 pins is valid
	TRDATA0 to TRDATA3	Output	These pins output the trace information
Address bus	A0 to A19	Output	Output pins for the address
Data bus	D0 to D15	I/O	Input and output pins for the bidirectional data bus
Multiplexed bus	A0/D0 to A15/D15	I/O	Address/data multiplexed bus
Bus control	RD#	Output	Strobe signal which indicates that reading from the external bus interface space is in progress
	WR#	Output	Strobe signal which indicates that writing to the external bus interface space is in progress, in 1-write strobe mode
	WR0# to WR1#	Output	Strobe signals which indicate that either group of data bus pins (D7 to D0 and D15 to D8) is valid in writing to the external bus interface space, in byte strobe mode
	BC0# to BC1#	Output	Strobe signals which indicate that either group of data bus pins (D7 to D0 and D15 to D8) is valid in access to the external bus interface space, in 1-write strobe mode
	ALE	Output	Address latch signal when address/data multiplexed bus is selected
	WAIT#	Input	Input pin for wait request signals in access to the external space
	CS0# to CS3#	Output	Select signals for CS areas

Table 1.4 Pin Functions (4/5)

Classifications	Pin Name	I/O	Description
USB 2.0 host/function module	VCC_USB	Input	Power supply pin for USB
	VSS_USB	Input	Ground pin for USB
	USB0_DP	I/O	USB internal transceiver D + input and output pins
	USB0_DM	I/O	USB internal transceiver D - input and output pins
	USB0_EXICEN	Output	Low power control signal for OTG chip
	USB0_VBUSEN	Output	Supply enable signal of VBUS (5 V) to OTG chip
	USB0_ID	Input	Mini AB connector ID input pin for use in OTG operation
	USB0_DPRPD	Output	D+ signal pull-down control pin for use during host operation
	USB0_DRPD	Output	D- signal pull-down control pin for use during host operation
	USB0_DPUPE	Output	D+ signal pull-up control pin for use during function operation
	USB0_VBUS	Input	Pin for monitoring USB cable connection
	USB0_OVRCURA, USB0_OVRCURB	Input	Pin for detecting external over current
CAN module	CRX1	Input	Input pins
	CTX1	Output	Output pins
Serial peripheral interface	RSPCKA, RSPCKB	I/O	Clock input/output pins
	MOSIA, MOSIB	I/O	Inputs or outputs data output from the master
	MISOA, MISOB	I/O	Inputs or outputs data output from the slave
	SSLA0, SSLB0	I/O	Input or output pins for slave selection
	SSLA1 to SSLA3 SSLB1 to SSLB3	Output	Output pins for slave selection
12-bit A/D converter	AN000 to AN007 AN100 to AN103	Input	Input pins for the analog signals to be processed by the A/D converter
	ADTRG0#, ADTRG1#	Input	Input pins for the external trigger signals that start the A/D conversion
	CVREFH	Input	Input pin for the high-level reference voltage to the comparator
	CVREFL	Input	Input pin for the low-level reference voltage to the comparator
10-bit A/D converter	AN0 to AN19	Input	Input pins for the analog signals to be processed by the 10-bit A/D converter
	ADTRG#	Input	Input pins for the external trigger signals that start the A/D conversion
D/A converter	DA0, DA1	Output	Output pins for the analog signals to be processed by the 10-bit A/D converter
Analog power supply	AVCC0	—	Analog voltage supply pin for the 12-bit A/D converter. Connect this pin to VCC if the 12-bit A/D converter is not to be used
	AVSS0	—	Analog ground pin for the 12-bit A/D converter. Connect this pin to VSS if the 12-bit A/D converter is not to be used
	VREFH0	—	Reference voltage supply pin for the 12-bit A/D converter. Connect this pin to VCC if the 12-bit A/D converter is not to be used
	VREFL0	—	Reference ground pin for the 12-bit A/D converter. Connect this pin to VSS if the 12-bit A/D converter is not to be used
	AVCC	—	Analog voltage supply pin for the 10-bit A/D converter and the 10-bit D/A converter. Connect this pin to the power supply of the system if the A/D converter and the D/A converter are not to be used.
	AVSS	—	Ground pin for the 10-bit A/D converter and 10-bit D/A converter. Connect this pin to the power-supply ground for the system (0 V).
	VREF	—	Reference-voltage input pin for the 10-bit A/D converter and the 10-bit D/A converter. Connect this pin to the power supply for the system if the A/D converter and the D/A converter are not to be used.

1.5 Pin Assignments

Figure 1.3 to Figure 1.8 show the pin assignments. Table 1.5 to Table 1.10 show the lists of pins and pin functions.



Note: • This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.5, List of Pins and Pin Functions (144-Pin LQFP).

Figure 1.3 Pin Assignment (144-Pin LQFP)

Table 1.6 List of Pins and Pin Functions (120-Pin LQFP) (3/4)

Pin Number 120-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3, GPT, POE3, CAC)	Communications (SCIc, SCId, RSPI, RIIC, CAN, USB)	Interrupt	S12ADB, AD, DA
75	VSS						
76		P30	D10/[A10/D10]	MTIOC0B/MTCLKD	SCK0/SSLA0/SSLB0		
77		P26	CS0#		TXD1/SMOSI1/SSDA1/SDA1		
78		P25	CS1#		SCK1/SCL1		
79		P24	D11/[A11/D11]		CTS0#/RTS0#/SS0#/RSPCKA/RSPCKB	IRQ4	
80		P23	D12/[A12/D12]	CACREF	TXD0/SMOSI0/SSDA0/MOSIA/MOSIB/CTX1		
81		P22	D13/[A13/D13]		RXD0/SMISO0/SSCL0/MISOA/MISOB/CRX1		ADTRG#
82		P21	D14/[A14/D14]	MTCLKA		IRQ6-DS	ADTRG1#
83		P20	D15/[A15/D15]	MTCLKB		IRQ7-DS	ADTRG0#
84		P65	A0/BC0#				AN5
85		P64	A1				AN4
86	AVCC						
87	VREF						
88	AVSS						
89		P63	A2				AN3
90		P62	A3				AN2
91		P61	A4				AN1
92		P60	A5				AN0
93		P55					AN11/DA1
94		P54					AN10/DA0
95		P53	A6				AN9
96		P52	A7				AN8
97		P51					AN7
98		P50					AN6
99		P47					AN103/CVREFH
100		P46					AN102
101		P45					AN101
102		P44					AN100
103		P43					AN003/CVREFL
104		P42					AN002
105		P41					AN001
106		P40					AN000
107	AVCC0						
108	VREFH0						
109	VREFL0						
110	AVSS0						

Table 1.7 List of Pins and Pin Functions (112-Pin LQFP) (3/4)

Pin Number 112-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3, GPT, POE3, CAC)	Communications (SCIc, SCId, RSPI, RIIC, CAN)	Interrupt	S12ADB, AD, DA
74		P23	D12/[A12/ D12]	CACREF	TXD0/SMOSI0/ SSDA0/MOSIA/ MOSIB/CTX1		
75		P22	D13/[A13/ D13]		RXD0/SMISO0/ SSCL0/MISOA/ MISOB/CRX1		ADTRG#
76		P21	D14/[A14/ D14]	MTCLKA		IRQ6-DS	ADTRG1#
77		P20	D15/[A15/ D15]	MTCLKB		IRQ7-DS	ADTRG0#
78		P65	A0/BC0#				AN5
79		P64	A1				AN4
80	AVCC						
81	VREF						
82	AVSS						
83		P63	A2				AN3
84		P62	A3				AN2
85		P61	A4				AN1
86		P60	A5				AN0
87		P55					AN11/DA1
88		P54					AN10/ DA0
89		P53	A6				AN9
90		P52	A7				AN8
91		P51					AN7
92		P50					AN6
93		P47					AN103/ CVREFH
94		P46					AN102
95		P45					AN101
96		P44					AN100
97		P43					AN003/ CVREFL
98		P42					AN002
99		P41					AN001
100		P40					AN000
101	AVCC0						
102	VREFH0						
103	VREFL0						
104	AVSS0						
105		P82	WAIT#	MTIC5U	SCK12	IRQ3	
106		P81	A8	MTIC5V	TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12		
107		P80	A9	MTIC5W	RXD12/SMISO12/ SSCL12/RXDX12	IRQ5	
108		P12	CS3#				
109		P11	ALE	MTCLKC		IRQ1-DS	

Table 1.8 List of Pins and Pin Functions (100-Pin LQFP) (2/3)

Pin Number 100-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3, GPT, POE3, CAC)	Communications (SCIc, SCId, RSPI, RIIC, CAN)	Interrupt	S12ADB, AD, DA
37		PA4		MTIOC1B	TXD0/SMOSI0/ SSDA0/ RSPCKA/RSPCKB		ADTRG0#
38		PA3		MTIOC2A	SCK0/SSLA0/SSLB0		
39		PA2		MTIOC2B	RXD2/SMISO2/ SSCL2/ SSLA1/SSLB1		
40		PA1		MTIOC6A	TXD2/SMOSI2/ SSDA2/ SSLA2/SSLB2		
41		PA0		MTIOC6C	SCK2/SSLA3/SSLB3		
42	VCC						
43		P96	A13	POE4#	RXD1/SMISO1/SSCL1	IRQ4-DS	
44	VSS						
45		P95		MTIOC6B/GTIOC4A	TXD1/SMOSI1/SSDA1		
46		P94		MTIOC7A/GTIOC5A	CTS1#/RTS1#/SS1#		
47		P93		MTIOC7B/GTIOC6A	CTS2#/RTS2#/SS2#		
48		P92		MTIOC6D/GTIOC4B			
49		P91		MTIOC7C/GTIOC5B			
50		P90		MTIOC7D/GTIOC6B			
51		P76	D0/[A0/D0]	MTIOC4D/GTIOC2B			
52		P75	D1/[A1/D1]	MTIOC4C/GTIOC1B			
53		P74	D2/[A2/D2]	MTIOC3D/GTIOC0B			
54		P73	D3/[A3/D3]	MTIOC4B/GTIOC2A			
55		P72	D4/[A4/D4]	MTIOC4A/GTIOC1A			
56		P71	D5/[A5/D5]	MTIOC3B/GTIOC0A			
57		P70	D6/[A6/D6]	POE0#	CTS1#/RTS1#/SS1#	IRQ5-DS	
58		P33	D7/[A7/D7]	MTIOC3A/MTCLKA	SSLA3/SSLB3		
59		P32	D8/[A8/D8]	MTIOC3C/MTCLKB	SSLA2/SSLB2		
60	VCC						
61		P31	D9/[A9/D9]	MTIOC0A/MTCLKC	SSLA1/SSLB1		
62	VSS						
63		P30	D10/[A10/ D10]	MTIOC0B/MTCLKD	SCK0/SSLA0/SSLB0		
64		P24	D11/[A11/D11]		CTS0#/RTS0#/SS0#/ RSPCKA/RSPCKB	IRQ4	
65		P23	D12/[A12/ D12]	CACREF	TXD0/SMOSI0/ SSDA0/MOSIA/ MOSIB/CTX1		
66		P22	D13/[A13/ D13]		RXD0/SMISO0/ SSCL0/MISOA/ MISOB/CRX1		ADTRG#
67		P21	D14/[A14/ D14]	MTCLKA		IRQ6-DS	ADTRG1#
68		P20	D15/[A15/ D15]	MTCLKB		IRQ7-DS	ADTRG0#
69		P65	A0/BC0#				AN5
70		P64	A1				AN4

Table 4.1 List of I/O Registers (Address Order) (2/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 201Fh	DMAC0	DMA Activation Source Flag Control Register	DMCSL	8	8	2 ICLK		DMACA	
0008 2040h	DMAC1	DMA Source Address Register	DMSAR	32	32	2 ICLK			
0008 2044h	DMAC1	DMA Destination Address Register	DMDAR	32	32	2 ICLK			
0008 2048h	DMAC1	DMA Transfer Count Register	DMCRA	32	32	2 ICLK			
0008 204Ch	DMAC1	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK			
0008 2050h	DMAC1	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK			
0008 2053h	DMAC1	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK			
0008 2054h	DMAC1	DMA Address Mode Register	DMAMD	16	16	2 ICLK			
0008 205Ch	DMAC1	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK			
0008 205Dh	DMAC1	DMA Software Start Register	DMREQ	8	8	2 ICLK			
0008 205Eh	DMAC1	DMA Status Register	DMSTS	8	8	2 ICLK			
0008 205Fh	DMAC1	DMA Activation Source Flag Control Register	DMCSL	8	8	2 ICLK			
0008 2080h	DMAC2	DMA Source Address Register	DMSAR	32	32	2 ICLK			
0008 2084h	DMAC2	DMA Destination Address Register	DMDAR	32	32	2 ICLK			
0008 2088h	DMAC2	DMA Transfer Count Register	DMCRA	32	32	2 ICLK			
0008 208Ch	DMAC2	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK			
0008 2090h	DMAC2	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK			
0008 2093h	DMAC2	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK			
0008 2094h	DMAC2	DMA Address Mode Register	DMAMD	16	16	2 ICLK			
0008 209Ch	DMAC2	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK			
0008 209Dh	DMAC2	DMA Software Start Register	DMREQ	8	8	2 ICLK			
0008 209Eh	DMAC2	DMA Status Register	DMSTS	8	8	2 ICLK			
0008 209Fh	DMAC2	DMA Activation Source Flag Control Register	DMCSL	8	8	2 ICLK			
0008 20C0h	DMAC3	DMA Source Address Register	DMSAR	32	32	2 ICLK			
0008 20C4h	DMAC3	DMA Destination Address Register	DMDAR	32	32	2 ICLK			
0008 20C8h	DMAC3	DMA Transfer Count Register	DMCRA	32	32	2 ICLK			
0008 20CCh	DMAC3	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK			
0008 20D0h	DMAC3	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK			
0008 20D3h	DMAC3	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK			
0008 20D4h	DMAC3	DMA Address Mode Register	DMAMD	16	16	2 ICLK			
0008 20DCh	DMAC3	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK			
0008 20DDh	DMAC3	DMA Software Start Register	DMREQ	8	8	2 ICLK			
0008 20DEh	DMAC3	DMA Status Register	DMSTS	8	8	2 ICLK			
0008 20DFh	DMAC3	DMA Activation Source Flag Control Register	DMCSL	8	8	2 ICLK			
0008 2200h	DMAC	DMACA Module Activation Register	DMAST	8	8	2 ICLK			
0008 2400h	DTC	DTC Control Register	DTCCR	8	8	2ICLK		DTCa	
0008 2404h	DTC	DTC Vector Base Register	DTCVBR	32	32	2ICLK			
0008 2408h	DTC	DTC Address Mode Register	DTCADMOD	8	8	2ICLK			
0008 240Ch	DTC	DTC Module Start Register	DTCST	8	8	2ICLK			
0008 240Eh	DTC	DTC Status Register	DTCSTS	16	16	2ICLK			
0008 3002h	BSC	CS0 Mode Register	CS0MOD	16	16	1, 2 BCLK		Buses	Not present in versions with 64 or 48 pins.
0008 3004h	BSC	CS0 Wait Control Register 1	CS0WCR1	32	32	1, 2 BCLK			Not present in versions with 64 or 48 pins.
0008 3008h	BSC	CS0 Wait Control Register 2	CS0WCR2	32	32	1, 2 BCLK			Not present in versions with 64 or 48 pins.
0008 3012h	BSC	CS1 Mode Register	CS1MOD	16	16	1, 2 BCLK			Not present in versions with 64 or 48 pins.
0008 3014h	BSC	CS1 Wait Control Register 1	CS1WCR1	32	32	1, 2 BCLK			Not present in versions with 64 or 48 pins.
0008 3018h	BSC	CS1 Wait Control Register 2	CS1WCR2	32	32	1, 2 BCLK			Not present in versions with 64 or 48 pins.
0008 3022h	BSC	CS2 Mode Register	CS2MOD	16	16	1, 2 BCLK			Not present in versions with 64 or 48 pins.

Table 4.1 List of I/O Registers (Address Order) (5/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 703Eh	ICU	Interrupt Request Register 062	IR062	8	8	2 ICLK		ICUb	Not present in versions with 64 or 48 pins.
0008 7040h	ICU	Interrupt Request Register 064	IR064	8	8	2 ICLK			
0008 7041h	ICU	Interrupt Request Register 065	IR065	8	8	2 ICLK			
0008 7042h	ICU	Interrupt Request Register 066	IR066	8	8	2 ICLK			
0008 7043h	ICU	Interrupt Request Register 067	IR067	8	8	2 ICLK			
0008 7044h	ICU	Interrupt Request Register 068	IR068	8	8	2 ICLK			
0008 7045h	ICU	Interrupt Request Register 069	IR069	8	8	2 ICLK			
0008 7046h	ICU	Interrupt Request Register 070	IR070	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7047h	ICU	Interrupt Request Register 071	IR071	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 705Ah	ICU	Interrupt Request Register 090	IR090	8	8	2 ICLK			Not present in versions with 112, 100, 64 or 48 pins.
0008 7062h	ICU	Interrupt Request Register 098	IR098	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7066h	ICU	Interrupt Request Register 102	IR102	8	8	2 ICLK			
0008 7067h	ICU	Interrupt Request Register 103	IR103	8	8	2 ICLK			
0008 7068h	ICU	Interrupt Request Register 104	IR104	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7069h	ICU	Interrupt Request Register 105	IR105	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 706Ah	ICU	Interrupt Request Register 106	IR106	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7072h	ICU	Interrupt Request Register 114	IR114	8	8	2 ICLK			
0008 707Ah	ICU	Interrupt Request Register 122	IR122	8	8	2 ICLK			
0008 707Bh	ICU	Interrupt Request Register 123	IR123	8	8	2 ICLK			
0008 707Ch	ICU	Interrupt Request Register 124	IR124	8	8	2 ICLK			
0008 707Dh	ICU	Interrupt Request Register 125	IR125	8	8	2 ICLK			
0008 707Eh	ICU	Interrupt Request Register 126	IR126	8	8	2 ICLK			
0008 707Fh	ICU	Interrupt Request Register 127	IR127	8	8	2 ICLK			
0008 7080h	ICU	Interrupt Request Register 128	IR128	8	8	2 ICLK			
0008 7081h	ICU	Interrupt Request Register 129	IR129	8	8	2 ICLK			
0008 7082h	ICU	Interrupt Request Register 130	IR130	8	8	2 ICLK			
0008 7083h	ICU	Interrupt Request Register 131	IR131	8	8	2 ICLK			
0008 7084h	ICU	Interrupt Request Register 132	IR132	8	8	2 ICLK			
0008 7085h	ICU	Interrupt Request Register 133	IR133	8	8	2 ICLK			
0008 7086h	ICU	Interrupt Request Register 134	IR134	8	8	2 ICLK			
0008 7087h	ICU	Interrupt Request Register 135	IR135	8	8	2 ICLK			
0008 7088h	ICU	Interrupt Request Register 136	IR136	8	8	2 ICLK			
0008 7089h	ICU	Interrupt Request Register 137	IR137	8	8	2 ICLK			
0008 708Ah	ICU	Interrupt Request Register 138	IR138	8	8	2 ICLK			
0008 708Bh	ICU	Interrupt Request Register 139	IR139	8	8	2 ICLK			
0008 708Ch	ICU	Interrupt Request Register 140	IR140	8	8	2 ICLK			
0008 708Dh	ICU	Interrupt Request Register 141	IR141	8	8	2 ICLK			
0008 708Eh	ICU	Interrupt Request Register 142	IR142	8	8	2 ICLK			
0008 708Fh	ICU	Interrupt Request Register 143	IR143	8	8	2 ICLK			
0008 7090h	ICU	Interrupt Request Register 144	IR144	8	8	2 ICLK			
0008 7091h	ICU	Interrupt Request Register 145	IR145	8	8	2 ICLK			
0008 7092h	ICU	Interrupt Request Register 146	IR146	8	8	2 ICLK			
0008 7093h	ICU	Interrupt Request Register 147	IR147	8	8	2 ICLK			
0008 7094h	ICU	Interrupt Request Register 148	IR148	8	8	2 ICLK			
0008 7095h	ICU	Interrupt Request Register 149	IR149	8	8	2 ICLK			
0008 7096h	ICU	Interrupt Request Register 150	IR150	8	8	2 ICLK			
0008 7097h	ICU	Interrupt Request Register 151	IR151	8	8	2 ICLK			

Table 4.1 List of I/O Registers (Address Order) (44/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
000C 299Eh	GPT5	General PWM Timer Cycle Setting Buffer Register	GTPBR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK	GPT	Not present in versions with 64 or 48 pins.
000C 29A0h	GPT5	General PWM Timer Cycle Setting Double-Buffer Register	GTPDBR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 29A4h	GPT5	A/D Converter Start Request Timing Register A	GTADTRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 29A6h	GPT5	A/D Converter Start Request Timing Buffer Register A	GTADTBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 29A8h	GPT5	A/D Converter Start Request Timing Double-Buffer Register A	GTADTDBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 29ACh	GPT5	A/D Converter Start Request Timing Register B	GTADTRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 29AEh	GPT5	A/D Converter Start Request Timing Buffer Register B	GTADTBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 29B0h	GPT5	A/D Converter Start Request Timing Double-Buffer Register B	GTADTDBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 29B4h	GPT5	General PWM Timer Output Negate Control Register	GTONCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 29B6h	GPT5	General PWM Timer Dead Time Control Register	GTDTCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 29B8h	GPT5	General PWM Timer Dead Time Value Register U	GTDVU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 29BAh	GPT5	General PWM Timer Dead Time Value Register D	GTDVD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 29BCh	GPT5	General PWM Timer Dead Time Buffer Register U	GTDBU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 29BEh	GPT5	General PWM Timer Dead Time Buffer Register D	GTDBD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 29C0h	GPT5	General PWM Timer Output Protection Function Status Register	GTSOS	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 29C2h	GPT5	General PWM Timer Output Protection Function Temporary Release Register	GTSOTR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A00h	GPT6	General PWM Timer I/O Control Register	GTIOR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A02h	GPT6	General PWM Timer Interrupt Output Setting Register	GTINTAD	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A04h	GPT6	General PWM Timer Control Register	GTCR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A06h	GPT6	General PWM Timer Buffer Enable Register	GTBER	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A08h	GPT6	General PWM Timer Count Direction Register	GTUDC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A0Ah	GPT6	General PWM Timer Interrupt, A/D Converter Start Request Skipping Setting Register	GTITC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A0Ch	GPT6	General PWM Timer Status Register	GTST	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A0Eh	GPT6	General PWM Timer Counter	GTCNT	16	16	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A10h	GPT6	General PWM Timer Compare Capture Register A	GTCCRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A12h	GPT6	General PWM Timer Compare Capture Register B	GTCCRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A14h	GPT6	General PWM Timer Compare Capture Register C	GTCCRC	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A16h	GPT6	General PWM Timer Compare Capture Register D	GTCCRD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A18h	GPT6	General PWM Timer Compare Capture Register E	GTCCRE	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A1Ah	GPT6	General PWM Timer Compare Capture Register F	GTCCRF	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A1Ch	GPT6	General PWM Timer Cycle Setting Register	GTPR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A1Eh	GPT6	General PWM Timer Cycle Setting Buffer Register	GTPBR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A20h	GPT6	General PWM Timer Cycle Setting Double-Buffer Register	GTPDBR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.

Table 4.1 List of I/O Registers (Address Order) (47/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
000C3056h	DPC	Control Calculation Parameter Setting Register KQ2	PARAMKQ2	16	16	3 to 5 PCLKA	2, 3 ICLK	DPC	Not present in versions with 64 or 48 pins.
000C305Ah	DPC	Control Calculation Parameter Setting Register KF2	PARAMKF2	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C305Eh	DPC	Control Calculation Parameter Setting Register KP3	PARAMKP3	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3062h	DPC	Control Calculation Parameter Setting Register KI3	PARAMKI3	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3066h	DPC	Control Calculation Parameter Setting Register KQ3	PARAMKQ3	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C306Ah	DPC	Control Calculation Parameter Setting Register KF3	PARAMKF3	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C306Ch	DPC	Control Calculation Result Higher-Order Bits Store Register 0	RESULTU0	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C306Eh	DPC	Control Calculation Result Lower-Order Bits Store Register 0	RESULTL0	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3070h	DPC	Control Calculation Result Higher-Order Bits Store Register 1	RESULTU1	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3072h	DPC	Control Calculation Result Lower-Order Bits Store Register 1	RESULTL1	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3074h	DPC	Control Calculation Result Higher-Order Bits Store Register 2	RESULTU2	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3076h	DPC	Control Calculation Result Lower-Order Bits Store Register 2	RESULTL2	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3078h	DPC	Control Calculation Result Higher-Order Bits Store Register 3	RESULTU3	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C307Ah	DPC	Control Calculation Result Lower-Order Bits Store Register 3	RESULTL3	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C307Eh	DPC	Input Code Monitor Enable Register	TMONEN	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3082h	DPC	Maximum Input Code Monitor Register 0	TMONMAX0	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3086h	DPC	Minimum Input Code Monitor Register 0	TMONMIN0	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C308Ah	DPC	Maximum Input Code Monitor Register 1	TMONMAX1	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C308Eh	DPC	Minimum Input Code Monitor Register 1	TMONMIN1	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3092h	DPC	Maximum Input Code Monitor Register 2	TMONMAX2	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3096h	DPC	Minimum Input Code Monitor Register 2	TMONMIN2	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C309Ah	DPC	Maximum Input Code Monitor Register 3	TMONMAX3	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C309Eh	DPC	Minimum Input Code Monitor Register 3	TMONMIN3	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C30A2h	DPC	Overvoltage Output Error Judgment Threshold Setting Register 0	ERRVTH0	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C30A6h	DPC	Overvoltage Output Error Judgment Threshold Setting Register 1	ERRVTH1	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C30AAh	DPC	Overvoltage Output Error Judgment Threshold Setting Register 2	ERRVTH2	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C30AEh	DPC	Overvoltage Output Error Judgment Threshold Setting Register 3	ERRVTH3	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C30B2h	DPC	PWM Shut-Down at Overvoltage Output Error Setting Register	ERRDWN	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
007F C402h	FLASH	Flash Mode Register	FMODR	8	8	2, 3 FCLK	2, 3 ICLK	ROM/ E2 DataFlash Memory	
007F C410h	FLASH	Flash Access Status Register	FASTAT	8	8	2, 3 FCLK	2, 3 ICLK		
007F C411h	FLASH	Flash Access Error Interrupt Enable Register	FAEINT	8	8	2, 3 FCLK	2, 3 ICLK		
007F C412h	FLASH	Flash Ready Interrupt Enable Register	FRDYIE	8	8	2, 3 FCLK	2, 3 ICLK	ROM	
007F C440h	FLASH	E2 DataFlash Read Enable Register 0	DFLRE0	16	16	2, 3 FCLK	2, 3 ICLK	E2 DataFlash Memory	
007F C442h	FLASH	E2 DataFlash Read Enable Register 1	DFLRE1	16	16	2, 3 FCLK	2, 3 ICLK		
007F C450h	FLASH	E2 DataFlash P/E Enable Register 0	DFLWE0	16	16	2, 3 FCLK	2, 3 ICLK		
007F C452h	FLASH	E2 DataFlash P/E Enable Register 1	DFLWE1	16	16	2, 3 FCLK	2, 3 ICLK		

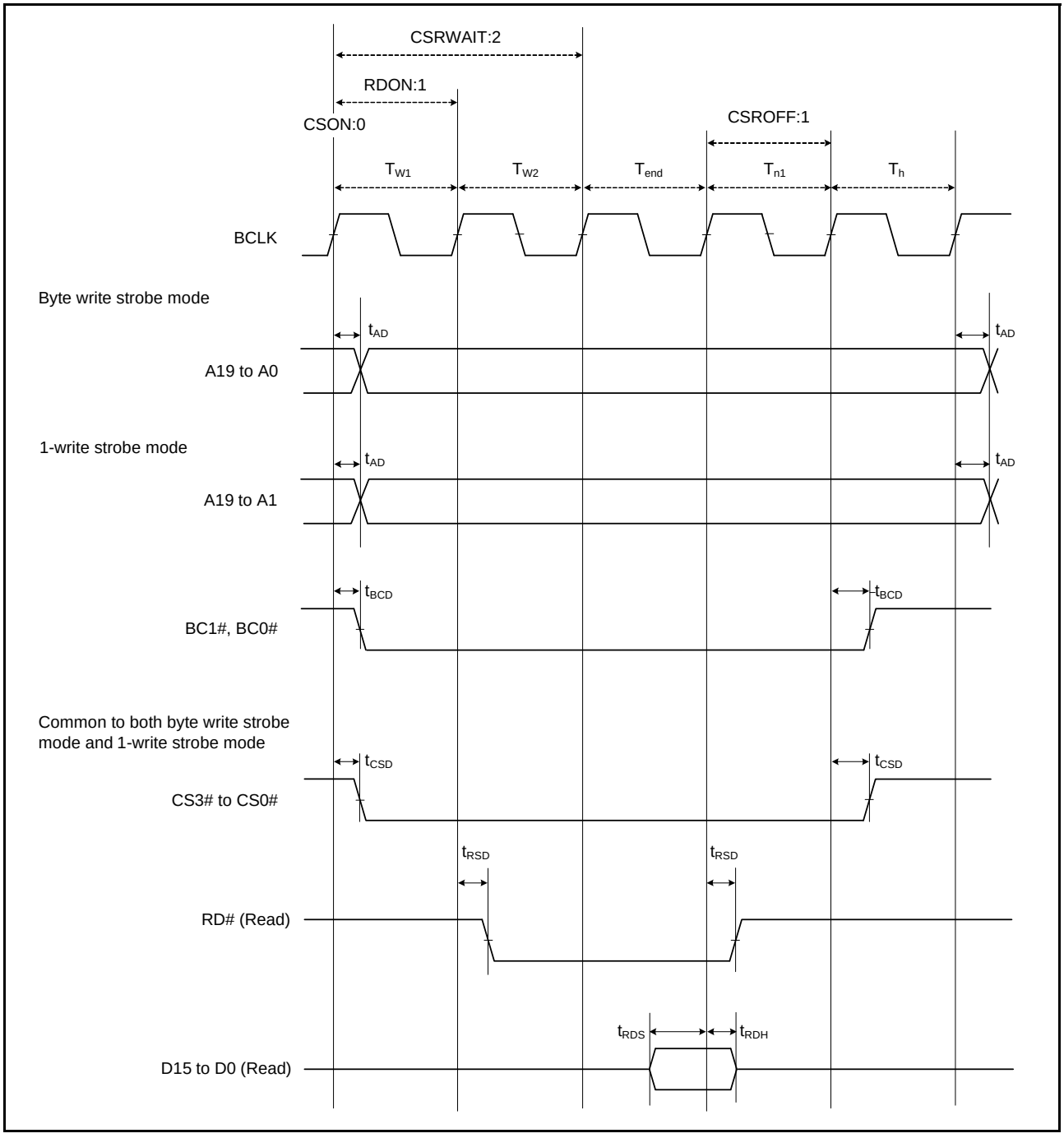


Figure 5.13 External Bus Timing/Normal Read Cycle (Bus Clock Synchronized)

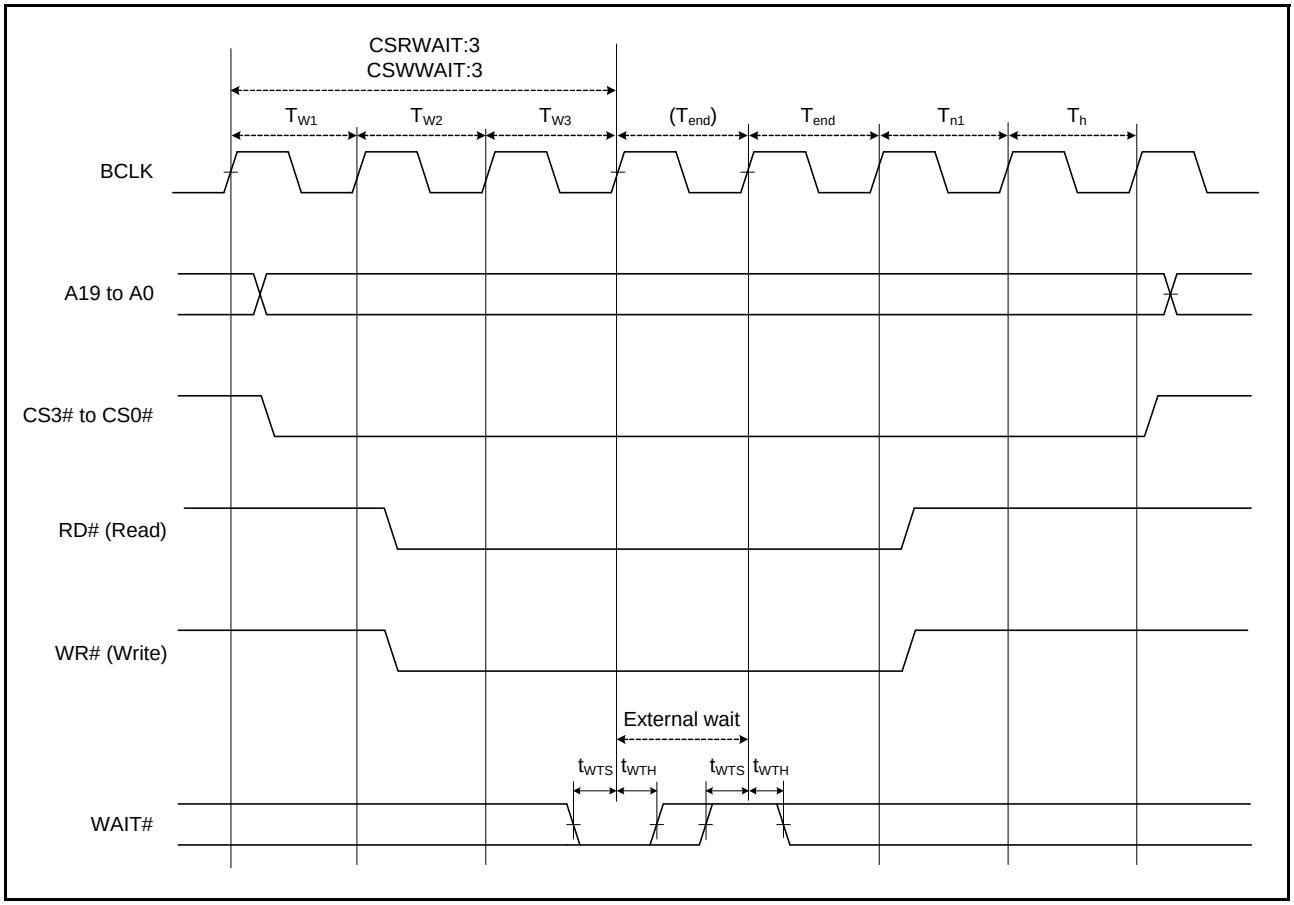


Figure 5.17 External Bus Timing/External Wait Control

Table 5.14 Bus Timing (Multiplexed Bus) (3)

Condition: PLLVCC = VCC_USB = AVCC0 = AVCC = VREF = 3.0 to 3.6 V
VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V, VREFH0 = 3.0 V to AVCC0
$T_a = T_{opr}$
Output load conditions: V_{OH} = VCC x 0.5, V_{OL} = VCC x 0.5, I_{OH} = –1.0 mA, I_{OL} = 1.0 mA, C = 30 pF

Item	Symbol	Min.	Max.	Unit	Test Conditions
Address delay time	t_{AD}	—	35	ns	Figure 5.18, Figure 5.19
Byte control delay time	t_{BCD}	—	30	ns	
CS# delay time	t_{CSD}	—	30	ns	
RD# delay time	t_{RSD}	—	30	ns	
ALE delay time	t_{ALED}	—	30	ns	
Read data setup time	t_{RDS}	20	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	—	30	ns	
Write data delay time	t_{WDD}	—	35	ns	
Write data hold time	t_{WDH}	0	—	ns	
WAIT# setup time	t_{WTS}	20	—	ns	Figure 5.17
WAIT# hold time	t_{WTH}	0.0	—	ns	

Table 5.16 Timing of On-Chip Peripheral Modules (3)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS =PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

High drive output is selected by the drive capacity control register.

Item				Symbol	Min.	Max.	Unit*1	Test Conditions
RSPI	RSPCK clock cycle	Master		t_{SPcyc}	2	4096	t_{Pcyc}	C = 30 pF, Figure 5.32
		Slave			8	4096		
	RSPCK clock high pulse width	Master		t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2 - 3$	—	ns	
		Slave			$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2$	—		
	RSPCK clock low pulse width	Master		t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2 - 3$	—	ns	
		Slave			$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2$	—		
	RSPCK clock rise/fall time	Output		t_{SPCKR}, t_{SPCKF}	—	5	ns	
		Input			—	1	µs	
	RSPCK clock fall time	Input		t_{SPCKF}	—	0.1	µs/V	
	Data input setup time	Master		t_{SU}	4	—	ns	C = 30 pF, Figure 5.33 to Figure 5.40
		Slave			$20 - t_{Pcyc}$	—		
	Data input hold time	Master	PCLKB division ratio set to a value other than 1/2	t_H	t_{Pcyc}	—	ns	
			PCLKB division ratio set to 1/2	t_{HF}	0	—		
		Slave		t_H	$20 + 2 \times t_{Pcyc}$	—		
	SSL setup time	Master		t_{LEAD}	1	8	t_{SPcyc}	
		Slave			4	—	t_{Pcyc}	
	SSL hold time	Master		t_{LAG}	1	8	t_{SPcyc}	
		Slave			4	—	t_{Pcyc}	
	Data output delay time	Master		t_{OD}	—	10	ns	
		Slave			—	$3 \times t_{Pcyc} + 40$		
	Data output hold time	Master		t_{OH}	0	—	ns	
		Slave			0	—		
	Successive transmission delay time	Master		t_{TD}	$t_{SPcyc} + 2 \times t_{Pcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	ns	
		Slave			$4 \times t_{Pcyc}$	—		
	MOSI and MISO rise/fall time	Output		t_{DR}, t_{DF}	—	5	ns	
		Input			—	1	µs	
	SSL rise/fall time	Output		t_{SSLr}, t_{SSLf}	—	15	ns	
		Input			—	1	µs	
	Slave access time			t_{SA}	—	4	t_{Pcyc}	Figure 5.39 and Figure 5.40
	Slave output release time			t_{REL}	—	3	t_{Pcyc}	

Note 1. t_{Pcyc}: PCLK cycle

Table 5.27 Power-on Reset Circuit and Voltage Detection Circuit Characteristics (2)

Condition: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0
$T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	V_{POR}	3.6	3.8	4.0	V	Figure 5.41
	Voltage detection circuit (LVD0)	V_{DET0}	4.0	4.2	4.4		Figure 5.42
	Voltage detection circuit (LVD1)*1	V_{DET1_8}	4.59	4.77	4.95		Figure 5.43
		V_{DET1_9}	4.05	4.23	4.41		
		V_{DET1_A}	4.32	4.50	4.68		
	Voltage detection circuit (LVD2)*2	V_{DET2_8}	4.59	4.77	4.95		Figure 5.44
		V_{DET2_9}	4.05	4.23	4.41		
		V_{DET2_A}	4.32	4.50	4.68		
Internal reset time	Power-on reset (POR)	t_{POR}		9.7		ms	Figure 5.41
	Voltage detection circuit (LVD0)	t_{LVD0}		9.7			Figure 5.42
	Voltage detection circuit (LVD1)	t_{LVD1}		0.9			Figure 5.43
	Voltage detection circuit (LVD2)	t_{LVD2}		0.9			Figure 5.44
Minimum VCC down time*3		t_{VOFF}	200	—	—	µs	Figure 5.41 to Figure 5.44
Response delay time		t_{DET}			200	µs	
LVD operation stabilization time (after LVD is enabled)		$Td_{(E-A)}$			3	µs	Figure 5.41 to Figure 5.44
Hysteresis width (LVD1 and LVD2)		V_{LVH}		80		mV	

Note 1. # in symbol $V_{DET1\_\#}$ indicates the value of the LVDLVLR.LVD1LVL[3:0] bits.
Note 2. # in symbol $V_{DET2\_\#}$ indicates the value of the LVDLVLR.LVD2LVL[3:0] bits.
Note 3. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{DET1}, and V_{DET2} for the POR/ LVD.

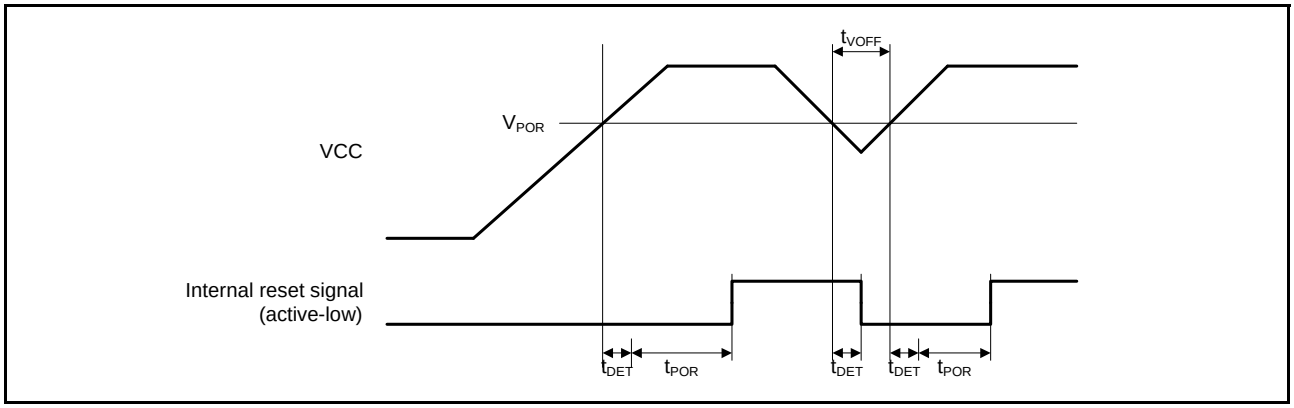


Figure 5.39 Power-on Reset Timing

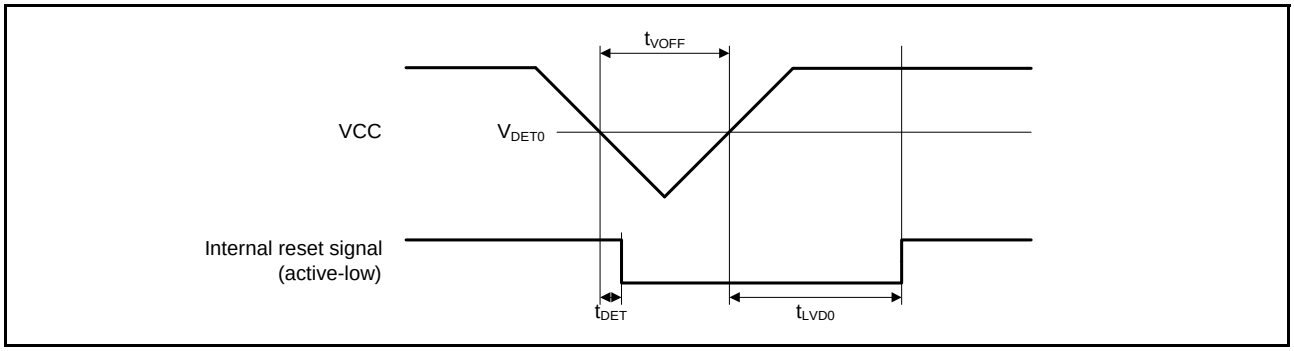


Figure 5.40 Voltage Detection Circuit Timing (V_{DET0})

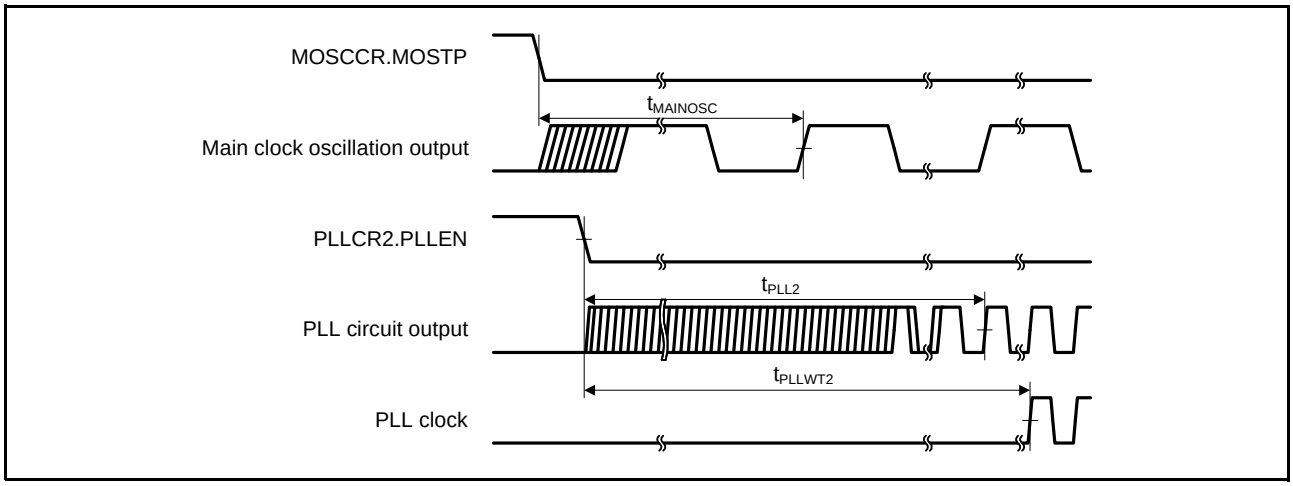


Figure 6.5 PLL Clock Oscillation Start Timing (PLL is Operated before Main Clock Oscillation Has Settled)

Table 6.13 Timing of On-Chip Peripheral Modules (3)

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item		Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI	SCK clock cycle output (master)	t_{SPcyc}	4	65536	t_{Pcyc}	Figure 6.20
	SCK clock cycle input (slave)		8	65536		
	SCK clock high pulse width	t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width	t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise/fall time	t_{SPCKR}, t_{SPCKF}	—	20	ns	
	Data input setup time	t_{SU}	40	—	ns	Figure 6.21 to Figure 6.24
	Data input hold time	t_{H}	40	—	ns	
	SS input setup time	t_{LEAD}	6	—	t_{Pcyc}	
	SS input hold time	t_{LAG}	6	—	t_{Pcyc}	
	Data output delay time	t_{OD}	—	40	ns	
	Data output hold time	t_{OH}	–10	—	ns	
	Data rise/fall time	t_{DR}, t_{DF}	—	20	ns	
	SS input rise/fall time	t_{SSLr}, t_{SSLf}	—	20	ns	
	Slave access time	t_{SA}	—	5	t_{Pcyc}	Figure 6.23 and Figure 6.24
	Slave output release time	t_{REL}	—	5	t_{Pcyc}	

Note 1. t_{Pcyc}: PCLK cycle

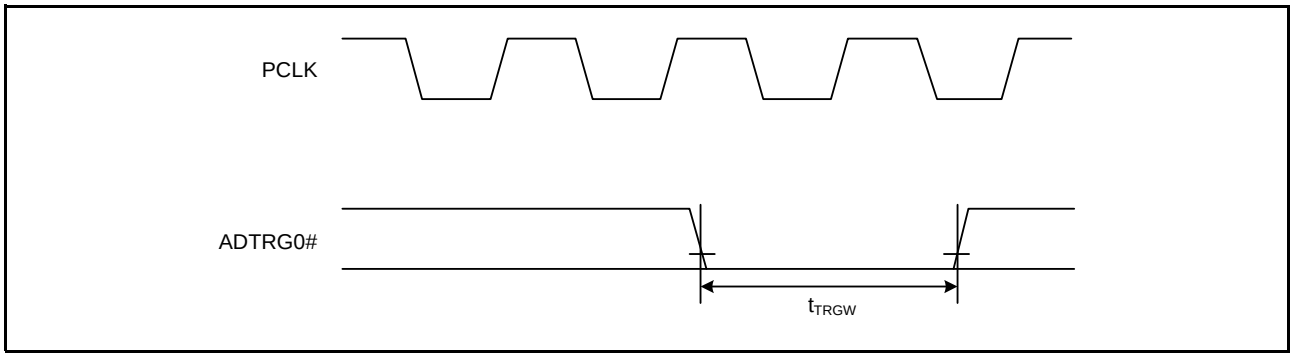


Figure 6.19 AD Converter External Trigger Input Timing

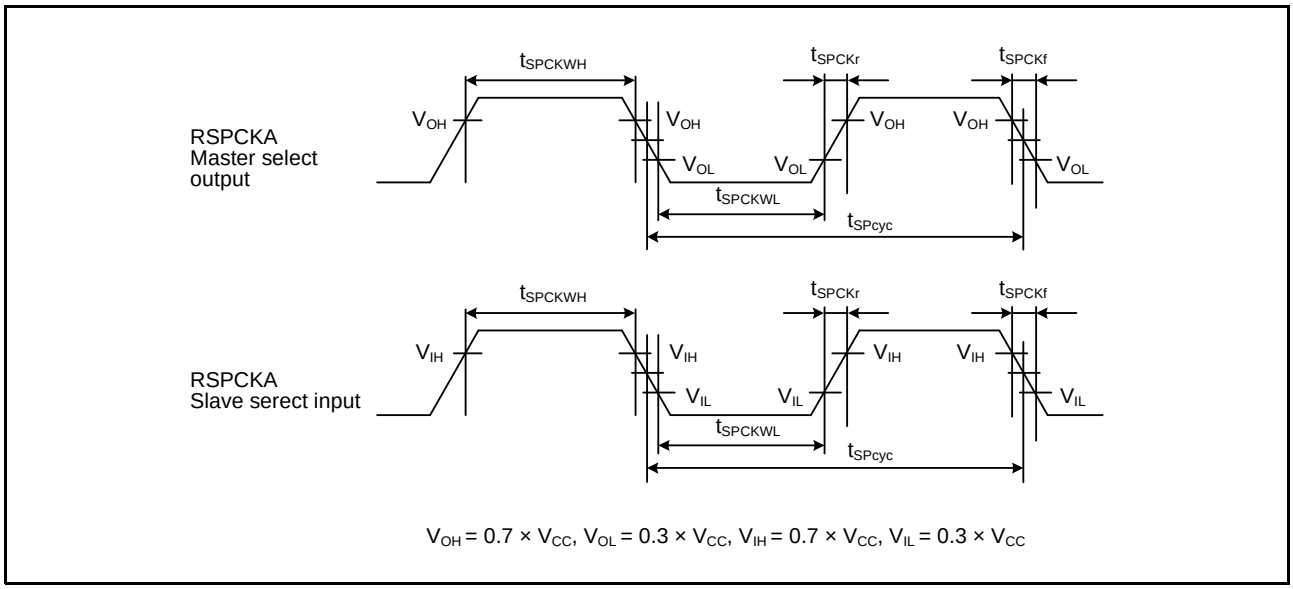


Figure 6.20 RSPI Clock Timing and Simple SPI Clock Timing

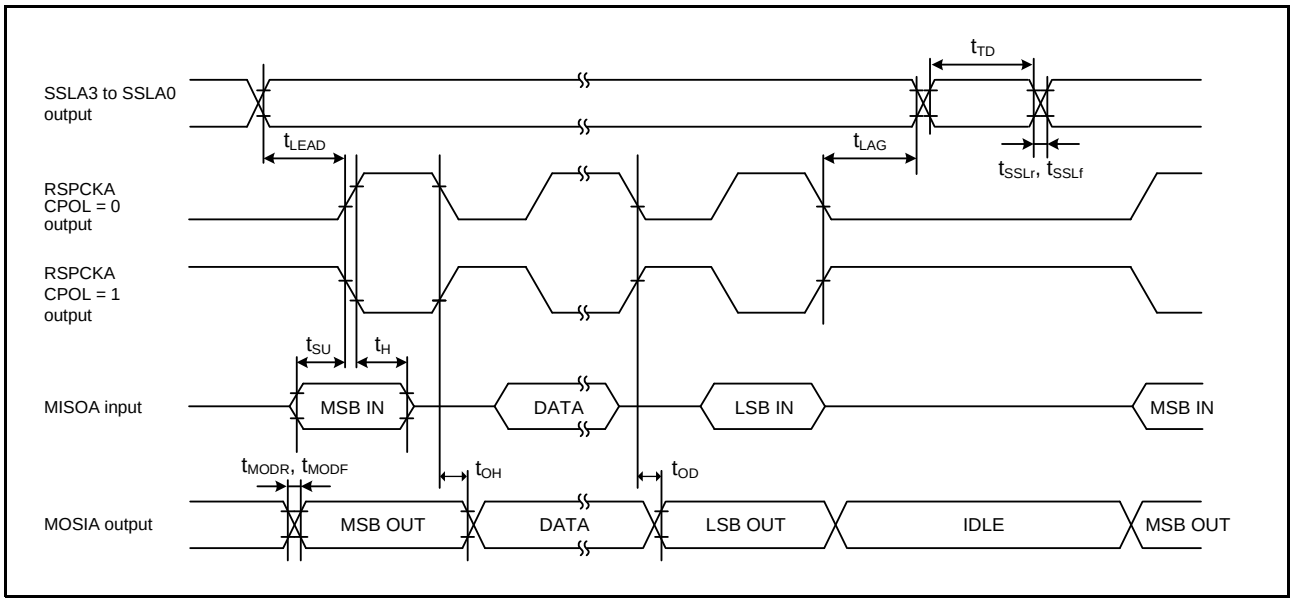


Figure 6.21 RSPI Timing (Master, CPHA = 0) and Simple SPI Timing (Master, CKPH = 1)

Rev.	Date	Description	
		Page	Summary
2.10	Sep 26, 2013	36 to 39	Table 1.7 List of Pins and Pin Functions (112-Pin LQFP), changed
		40 to 42	Table 1.8 List of Pins and Pin Functions (100-Pin LQFP), changed
		43 to 45	Table 1.9 List of Pins and Pin Functions (64-Pin LQFP), changed
		46 to 47	Table 1.10 List of Pins and Pin Functions (48-Pin LQFP), changed
		4. I/O Registers	
		56 to 103	Table 4.1 List of I/O Registers (Address Order), changed
		5. Electrical Characteristics [144-, 120-, 112- and 100-Pin Versions]	
		104	Table 5.1 Absolute Maximum Ratings, changed
		107	Table 5.4 DC Characteristics (3), Note 7, deleted
		108	Table 5.6 Permissible Power Consumption, added
		128	5.3.7 Timing of PWM Delay Generation Circuit, added
		128	Table 42.21 Timing of the PWM Delay Generation Circuit, added
		132	Figure 5.32 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKB Division Ratio Set to a Value Other Than 1/2) and Simple SPI Timing (Master, CKPH = 1), changed
		133	Figure 5.34 RSPI Timing (Slave, CPHA = 0) and Simple SPI Timing (Slave, CKPH = 0), changed
		134	Figure 5.35 RSPI Timing (Slave, CPHA = 1) and Simple SPI Timing (Slave, CKPH = 1), changed
		6. Electrical Characteristics [64- and 48-Pin Versions]	
		149	Table 6.1 Absolute Maximum Ratings, changed
		151	Table 6.3 DC Characteristics (2), Note 3, changed
		152	Table 6.5 Permissible Power Consumption, added