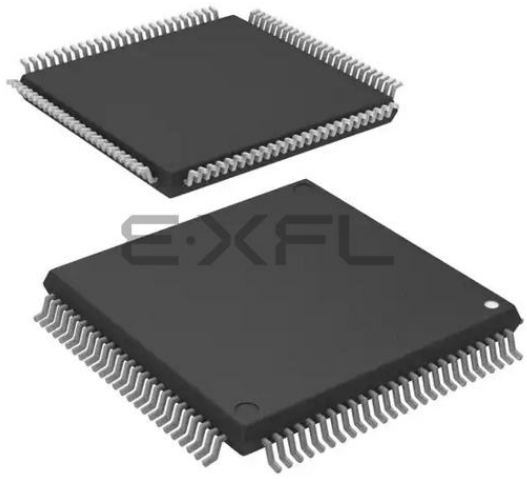
Renesas Electronics America Inc - R5F563TEADFP#V1 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	57
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x10b, 8x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f563teadfp-v1

Table 1.1 Outline of Specifications (3/7)

Classification	Module/Function	Description
I/O ports	General I/O ports	• 144-pin LQFP I/O pins: 81 Input pins: 29 Open-drain outputs: 27 • 120-pin LQFP I/O pins: 72 Input pin: 21 Open-drain outputs: 26 • 112-pin LQFP I/O pins: 69 Input pins: 21 Open-drain outputs: 20 • 100-pin LQFP I/O pins: 57 Input pins: 21 Open-drain outputs: 16 • 64-pin LQFP I/O pins: 39 Input pins: 9 Open-drain outputs: 10 5-V tolerance: 39 • 48-pin LQFP I/O pins: 25 Input pins: 7 Open-drain outputs: 8 5-V tolerance: 25
Timers	Multi-function timer pulse unit 3 (MTU3)	• (16 bits × 8 channels) • Maximum of 16 pulse-input/output and 3 pulse-input possible • Select eight clocks from among ten count clocks (PCLKA/1, PCLKA/4, PCLKA/16, PCLKA/64, PCLKA/256, PCLKA/1024, MTCLKA, MTCLKB, MTCLKC, and MTCLKD) for each channel (seven clocks for channel 1, four clocks for channel 5, and six clocks for channel 6 or 7) • 24 output compare/input capture registers • Counter-clearing operation (simultaneous clearing on compare match or input capture) • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous input and output to registers in synchronization with counter operations • Buffer operation specifiable • Capable of cascade-connected operation • Interrupts: 38 sources • Automatic transfer of register data • Pulse output modes Topple, PWM, complementary PWM, and reset-synchronous PWM modes • Complementary PWM output mode Outputs non-overlapping waveforms for controlling 3-phase inverters Automatic specification of dead times PWM duty cycle: Selectable as any value from 0% to 100% Delay can be applied to requests for A/D conversion. Non-generation of interrupt requests at peak or trough values of counters can be selected. Double buffering • Reset-synchronous PWM mode Three PWM waveforms and corresponding inverse waveforms are output with the desired duty cycles. • Phase-counting mode • Counter functionality for dead-time compensation • Generation of triggers for A/D converters • Differential timing for initiation of A/D conversion
	Port output enable 3 (POE3)	• Control of the high-impedance state of the MTU3 and GPT's waveform output pins • Six pins for input from signal sources: POE0, POE4, POE8, POE10, POE11, and POE12 • Initiation on detection of short-circuited outputs (detection of PWM outputs having simultaneously become an active level.) • Initiation by comparator-detection, oscillation-stoppage detection, or software • Software control of the states of pins for output control can also be added.

Table 1.7 List of Pins and Pin Functions (112-Pin LQFP) (2/4)

Pin Number 112-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3, GPT, POE3, CAC)	Communications (SCIc, SCId, RSPI, RIIC, CAN)	Interrupt	S12ADB, AD, DA
38		PB0	A14	MTIOC0D	MOSIA/MOSIB		
39		PA5		MTIOC1A	RXD0/SMISO0/ SSCL0/ MISOA/MISOB		ADTRG1#
40		PA4		MTIOC1B	TXD0/SMOSI0/ SSDA0/RSPCKA/ RSPCKB		ADTRG0#
41		PA3		MTIOC2A	SCK0/SSLA0/SSLB0		
42		PA2		MTIOC2B	RXD2/SMISO2/ SSCL2/ SSLA1/SSLB1		
43		PA1		MTIOC6A	TXD2/SMOSI2/ SSDA2/SSLA2/SSLB2		
44		PA0		MTIOC6C	SCK2/SSLA3/SSLB3		
45	VCC						
46		P96	A13	POE4#	RXD1/SMISO1/SSCL1	IRQ4-DS	
47	VSS						
48		P95		MTIOC6B/ GTIOC4A	TXD1/SMOSI1/SSDA1		
49		P94		MTIOC7A/ GTIOC5A	CTS1#/RTS1#/SS1#		
50		P93		MTIOC7B/ GTIOC6A	CTS2#/RTS2#/SS2#		
51		P92		MTIOC6D/GTIOC4B			
52		P91		MTIOC7C/GTIOC5B			
53		P90		MTIOC7D/GTIOC6B			
54	TRCLK	PG5		POE12#	SCK3		ADTRG#
55	TRDATA3	PG4		GTIOC6B	RXD3/SMISO3/SSCL3	IRQ6	
56	TRDATA2	PG3		GTIOC6A	TXD3/SMOSI3/SSDA3		
57	TRDATA1	PG2			SCK2	IRQ2	
58	TRDATA0	PG1		GTIOC7B	RXD2/SMISO2/SSCL2	IRQ1	
59	TRSYNC	PG0		GTIOC7A	TXD2/SMOSI2/SSDA2	IRQ0	
60		P76	D0/[A0/D0]	MTIOC4D/GTIOC2B			
61		P75	D1/[A1/D1]	MTIOC4C/GTIOC1B			
62		P74	D2/[A2/D2]	MTIOC3D/GTIOC0B			
63		P73	D3/[A3/D3]	MTIOC4B/GTIOC2A			
64		P72	D4/[A4/D4]	MTIOC4A/GTIOC1A			
65		P71	D5/[A5/D5]	MTIOC3B/GTIOC0A			
66		P70	D6/[A6/D6]	POE0#	CTS1#/RTS1#/SS1#	IRQ5-DS	
67		P33	D7/[A7/D7]	MTIOC3A/MTCLKA	SSLA3/SSLB3		
68		P32	D8/[A8/D8]	MTIOC3C/MTCLKB	SSLA2/SSLB2		
69	VCC						
70		P31	D9/[A9/D9]	MTIOC0A/MTCLKC	SSLA1/SSLB1		
71	VSS						
72		P30	D10/[A10/ D10]	MTIOC0B/MTCLKD	SCK0/SSLA0/SSLB0		
73		P24	D11/[A11/D11]		CTS0#/RTS0#/SS0#/ RSPCKA/RSPCKB	IRQ4	

Table 4.1 List of I/O Registers (Address Order) (10/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 71BBh	ICU	DTC Activation Enable Register 187	DTCER187	8	8	2 ICLK		ICUb	Not present in versions with 64 or 48 pins.
0008 71BCh	ICU	DTC Activation Enable Register 188	DTCER188	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 71BDh	ICU	DTC Activation Enable Register 189	DTCER189	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 71BFh	ICU	DTC Activation Enable Register 191	DTCER191	8	8	2 ICLK			Not present in versions with 112, 100, 64 or 48 pins.
0008 71C0h	ICU	DTC Activation Enable Register 192	DTCER192	8	8	2 ICLK			Not present in versions with 112, 100, 64 or 48 pins.
0008 71C3h	ICU	DTC Activation Enable Register 195	DTCER195	8	8	2 ICLK			
0008 71C4h	ICU	DTC Activation Enable Register 196	DTCER196	8	8	2 ICLK			
0008 71C6h	ICU	DTC Activation Enable Register 198	DTCER198	8	8	2 ICLK			
0008 71C7h	ICU	DTC Activation Enable Register 199	DTCER199	8	8	2 ICLK			
0008 71C8h	ICU	DTC Activation Enable Register 200	DTCER200	8	8	2 ICLK			
0008 71C9h	ICU	DTC Activation Enable Register 201	DTCER201	8	8	2 ICLK			
0008 71D6h	ICU	DTC Activation Enable Register 214	DTCER214	8	8	2 ICLK			
0008 71D7h	ICU	DTC Activation Enable Register 215	DTCER215	8	8	2 ICLK			
0008 71D9h	ICU	DTC Activation Enable Register 217	DTCER217	8	8	2 ICLK			
0008 71DAh	ICU	DTC Activation Enable Register 218	DTCER218	8	8	2 ICLK			
0008 71DCh	ICU	DTC Activation Enable Register 220	DTCER220	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 71DDh	ICU	DTC Activation Enable Register 221	DTCER221	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 71DFh	ICU	DTC Activation Enable Register 223	DTCER223	8	8	2 ICLK			Not present in versions with 100, 64 or 48 pins.
0008 71E0h	ICU	DTC Activation Enable Register 224	DTCER224	8	8	2 ICLK			Not present in versions with 100, 64 or 48 pins.
0008 71E2h	ICU	DTC Activation Enable Register 226	DTCER226	8	8	2 ICLK			
0008 71E3h	ICU	DTC Activation Enable Register 227	DTCER227	8	8	2 ICLK			
0008 71E4h	ICU	DTC Activation Enable Register 228	DTCER228	8	8	2 ICLK			
0008 71E5h	ICU	DTC Activation Enable Register 229	DTCER229	8	8	2 ICLK			
0008 71E6h	ICU	DTC Activation Enable Register 230	DTCER230	8	8	2 ICLK			
0008 71E7h	ICU	DTC Activation Enable Register 231	DTCER231	8	8	2 ICLK			
0008 71E8h	ICU	DTC Activation Enable Register 232	DTCER232	8	8	2 ICLK			
0008 71E9h	ICU	DTC Activation Enable Register 233	DTCER233	8	8	2 ICLK			
0008 71EAh	ICU	DTC Activation Enable Register 234	DTCER234	8	8	2 ICLK			
0008 71EBh	ICU	DTC Activation Enable Register 235	DTCER235	8	8	2 ICLK			
0008 71ECh	ICU	DTC Activation Enable Register 236	DTCER236	8	8	2 ICLK			
0008 71EEh	ICU	DTC Activation Enable Register 238	DTCER238	8	8	2 ICLK			
0008 71EFh	ICU	DTC Activation Enable Register 239	DTCER239	8	8	2 ICLK			
0008 71F0h	ICU	DTC Activation Enable Register 240	DTCER240	8	8	2 ICLK			
0008 71F1h	ICU	DTC Activation Enable Register 241	DTCER241	8	8	2 ICLK			
0008 71F2h	ICU	DTC Activation Enable Register 242	DTCER242	8	8	2 ICLK			
0008 71F4h	ICU	DTC Activation Enable Register 244	DTCER244	8	8	2 ICLK			
0008 71F5h	ICU	DTC Activation Enable Register 245	DTCER245	8	8	2 ICLK			
0008 71F6h	ICU	DTC Activation Enable Register 246	DTCER246	8	8	2 ICLK			
0008 71F7h	ICU	DTC Activation Enable Register 247	DTCER247	8	8	2 ICLK			
0008 71F8h	ICU	DTC Activation Enable Register 248	DTCER248	8	8	2 ICLK			
0008 71FAh	ICU	DTC Activation Enable Register 250	DTCER250	8	8	2 ICLK			
0008 71FBh	ICU	DTC Activation Enable Register 251	DTCER251	8	8	2 ICLK			
0008 7202h	ICU	Interrupt Request Enable Register 02	IER02	8	8	2 ICLK			
0008 7203h	ICU	Interrupt Request Enable Register 03	IER03	8	8	2 ICLK			
0008 7204h	ICU	Interrupt Request Enable Register 04	IER04	8	8	2 ICLK			
0008 7205h	ICU	Interrupt Request Enable Register 05	IER05	8	8	2 ICLK			

Table 4.1 List of I/O Registers (Address Order) (12/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 732C	ICU	Interrupt Source Priority Register 044	IPR044	8	8	2 ICLK		ICUb	Not present in versions with 64 or 48 pins.
0008 732Dh	ICU	Interrupt Source Priority Register 045	IPR045	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7331h	ICU	Interrupt Source Priority Register 049	IPR049	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7334h	ICU	Interrupt Source Priority Register 052	IPR052	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7336h	ICU	Interrupt Source Priority Register 054	IPR054	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7337h	ICU	Interrupt Source Priority Register 055	IPR055	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7338h	ICU	Interrupt Source Priority Register 056	IPR056	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7339h	ICU	Interrupt Source Priority Register 057	IPR057	8	8	2 ICLK			
0008 733Ah	ICU	Interrupt Source Priority Register 058	IPR058	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 733Bh	ICU	Interrupt Source Priority Register 059	IPR059	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 733Ch	ICU	Interrupt Source Priority Register 060	IPR060	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 733Dh	ICU	Interrupt Source Priority Register 061	IPR061	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 733Eh	ICU	Interrupt Source Priority Register 062	IPR062	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7340h	ICU	Interrupt Source Priority Register 064	IPR064	8	8	2 ICLK			
0008 7341h	ICU	Interrupt Source Priority Register 065	IPR065	8	8	2 ICLK			
0008 7342h	ICU	Interrupt Source Priority Register 066	IPR066	8	8	2 ICLK			
0008 7343h	ICU	Interrupt Source Priority Register 067	IPR067	8	8	2 ICLK			
0008 7344h	ICU	Interrupt Source Priority Register 068	IPR068	8	8	2 ICLK			
0008 7345h	ICU	Interrupt Source Priority Register 069	IPR069	8	8	2 ICLK			
0008 7346h	ICU	Interrupt Source Priority Register 070	IPR070	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7347h	ICU	Interrupt Source Priority Register 071	IPR071	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 735Ah	ICU	Interrupt Source Priority Register 090	IPR090	8	8	2 ICLK			Not present in versions with 112, 100, 64 or 48 pins.
0008 7362h	ICU	Interrupt Source Priority Register 098	IPR098	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7366h	ICU	Interrupt Source Priority Register 102	IPR102	8	8	2 ICLK			
0008 7367h	ICU	Interrupt Source Priority Register 103	IPR103	8	8	2 ICLK			
0008 7368h	ICU	Interrupt Source Priority Register 104	IPR104	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7369h	ICU	Interrupt Source Priority Register 105	IPR105	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 736Ah	ICU	Interrupt Source Priority Register 106	IPR106	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7372h	ICU	Interrupt Source Priority Register 114	IPR114	8	8	2 ICLK			
0008 737Ah	ICU	Interrupt Source Priority Register 122	IPR122	8	8	2 ICLK			
0008 737Eh	ICU	Interrupt Source Priority Register 126	IPR126	8	8	2 ICLK			
0008 7382h	ICU	Interrupt Source Priority Register 130	IPR130	8	8	2 ICLK			
0008 7385h	ICU	Interrupt Source Priority Register 133	IPR133	8	8	2 ICLK			
0008 7387h	ICU	Interrupt Source Priority Register 135	IPR135	8	8	2 ICLK			
0008 7389h	ICU	Interrupt Source Priority Register 137	IPR137	8	8	2 ICLK			
0008 738Bh	ICU	Interrupt Source Priority Register 139	IPR139	8	8	2 ICLK			
0008 738Dh	ICU	Interrupt Source Priority Register 141	IPR141	8	8	2 ICLK			
0008 7391h	ICU	Interrupt Source Priority Register 145	IPR145	8	8	2 ICLK			
0008 7392h	ICU	Interrupt Source Priority Register 146	IPR146	8	8	2 ICLK			
0008 7396h	ICU	Interrupt Source Priority Register 150	IPR150	8	8	2 ICLK			
0008 7397h	ICU	Interrupt Source Priority Register 151	IPR151	8	8	2 ICLK			

Table 4.1 List of I/O Registers (Address Order) (13/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 739Ah	ICU	Interrupt Source Priority Register 154	IPR154	8	8	2 ICLK		ICUb	
0008 739Eh	ICU	Interrupt Source Priority Register 158	IPR158	8	8	2 ICLK			
0008 73A1h	ICU	Interrupt Source Priority Register 161	IPR161	8	8	2 ICLK			
0008 73A3h	ICU	Interrupt Source Priority Register 163	IPR163	8	8	2 ICLK			
0008 73A5h	ICU	Interrupt Source Priority Register 165	IPR165	8	8	2 ICLK			
0008 73A6h	ICU	Interrupt Source Priority Register 166	IPR166	8	8	2 ICLK			
0008 73ABh	ICU	Interrupt Source Priority Register 171	IPR171	8	8	2 ICLK			
0008 73ACh	ICU	Interrupt Source Priority Register 172	IPR172	8	8	2 ICLK			
0008 73ADh	ICU	Interrupt Source Priority Register 173	IPR173	8	8	2 ICLK			
0008 73AEh	ICU	Interrupt Source Priority Register 174	IPR174	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 73B1h	ICU	Interrupt Source Priority Register 177	IPR177	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 73B4h	ICU	Interrupt Source Priority Register 180	IPR180	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 73B7h	ICU	Interrupt Source Priority Register 183	IPR183	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 73B9h	ICU	Interrupt Source Priority Register 185	IPR185	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 73BCh	ICU	Interrupt Source Priority Register 188	IPR188	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 73BEh	ICU	Interrupt Source Priority Register 190	IPR190	8	8	2 ICLK			Not present in versions with 112, 100, 64 or 48 pins.
0008 73C2h	ICU	Interrupt Source Priority Register 194	IPR194	8	8	2 ICLK			
0008 73C6h	ICU	Interrupt Source Priority Register 198	IPR198	8	8	2 ICLK			
0008 73C7h	ICU	Interrupt Source Priority Register 199	IPR199	8	8	2 ICLK			
0008 73C8h	ICU	Interrupt Source Priority Register 200	IPR200	8	8	2 ICLK			
0008 73C9h	ICU	Interrupt Source Priority Register 201	IPR201	8	8	2 ICLK			
0008 73D6h	ICU	Interrupt Source Priority Register 214	IPR214	8	8	2 ICLK			
0008 73D9h	ICU	Interrupt Source Priority Register 217	IPR217	8	8	2 ICLK			
0008 73DCh	ICU	Interrupt Source Priority Register 220	IPR220	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 73DFh	ICU	Interrupt Source Priority Register 223	IPR223	8	8	2 ICLK			Not present in versions with 100, 64 or 48 pins.
0008 73E2h	ICU	Interrupt Source Priority Register 226	IPR226	8	8	2 ICLK			
0008 73E5h	ICU	Interrupt Source Priority Register 229	IPR229	8	8	2 ICLK			
0008 73E8h	ICU	Interrupt Source Priority Register 232	IPR232	8	8	2 ICLK			
0008 73EBh	ICU	Interrupt Source Priority Register 235	IPR235	8	8	2 ICLK			
0008 73EEh	ICU	Interrupt Source Priority Register 238	IPR238	8	8	2 ICLK			
0008 73F1h	ICU	Interrupt Source Priority Register 241	IPR241	8	8	2 ICLK			
0008 73F4h	ICU	Interrupt Source Priority Register 244	IPR244	8	8	2 ICLK			
0008 73F7h	ICU	Interrupt Source Priority Register 247	IPR247	8	8	2 ICLK			
0008 73FAh	ICU	Interrupt Source Priority Register 250	IPR250	8	8	2 ICLK			
0008 7400h	ICU	DMAC Activation Request Select Register 0	DMRSR0	8	8	2 ICLK			
0008 7404h	ICU	DMAC Activation Request Select Register 1	DMRSR1	8	8	2 ICLK			
0008 7408h	ICU	DMAC Activation Request Select Register 2	DMRSR2	8	8	2 ICLK			
0008 740Ch	ICU	DMAC Activation Request Select Register 3	DMRSR3	8	8	2 ICLK			
0008 7500h	ICU	IRQ Control Register 0	IRQCR0	8	8	2 ICLK			
0008 7501h	ICU	IRQ Control Register 1	IRQCR1	8	8	2 ICLK			
0008 7502h	ICU	IRQ Control Register 2	IRQCR2	8	8	2 ICLK			
0008 7503h	ICU	IRQ Control Register 3	IRQCR3	8	8	2 ICLK			
0008 7504h	ICU	IRQ Control Register 4	IRQCR4	8	8	2 ICLK			
0008 7505h	ICU	IRQ Control Register 5	IRQCR5	8	8	2 ICLK			
0008 7506h	ICU	IRQ Control Register 6	IRQCR6	8	8	2 ICLK			Not present in versions with 64 or 48 pins.

Table 4.1 List of I/O Registers (Address Order) (20/48)

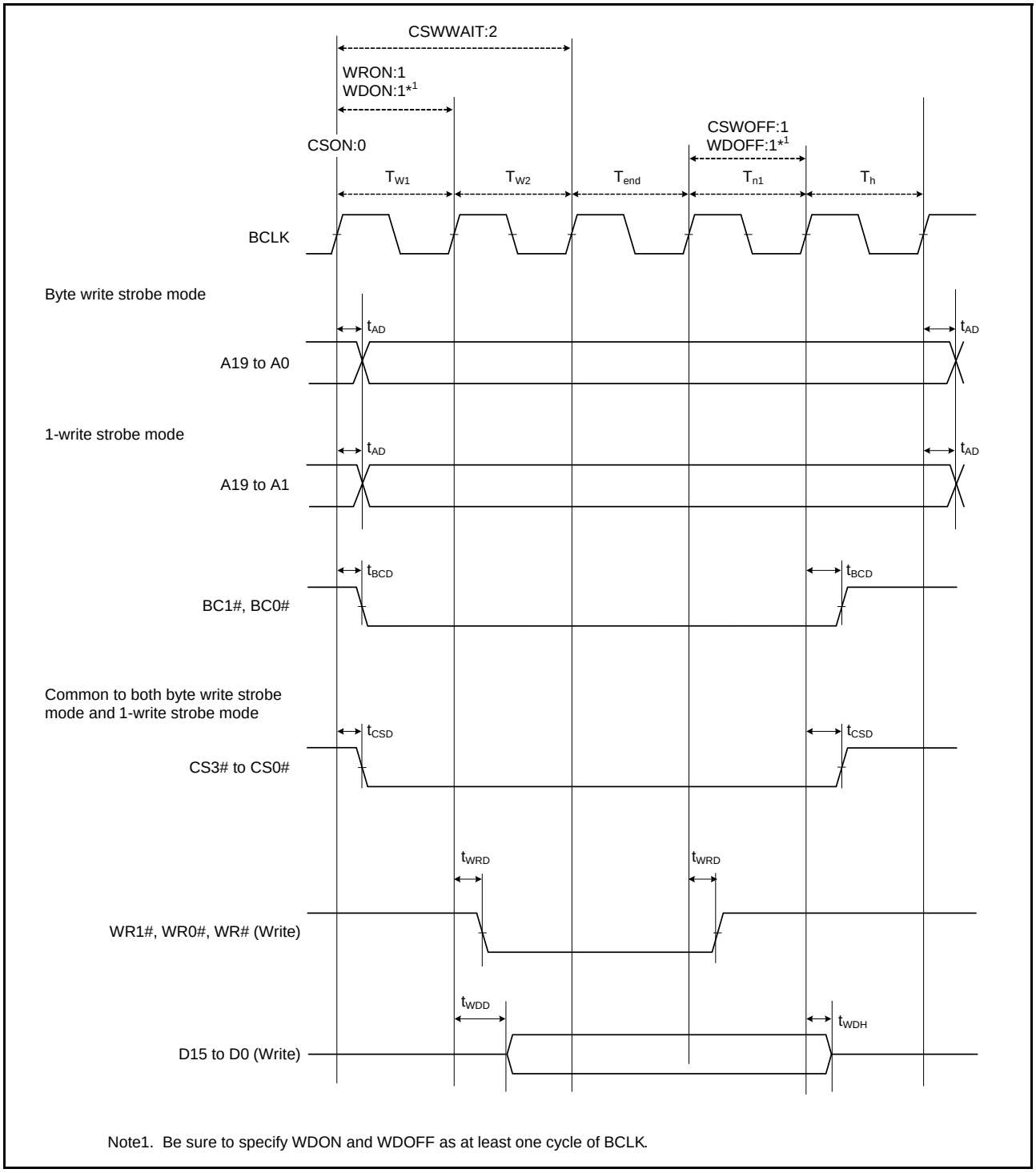
Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 9873h	AD	A/D Sampling State Register 1	ADSSTR1	8	8	2, 3 PCLKB	2 ICLK	AD	Not present in versions with 64 or 48 pins.
0008 9874h	AD	A/D Sampling State Register 2	ADSSTR2	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9875h	AD	A/D Sampling State Register 3	ADSSTR3	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9876h	AD	A/D Sampling State Register 4	ADSSTR4	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9877h	AD	A/D Sampling State Register 5	ADSSTR5	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9878h	AD	A/D Sampling State Register 6	ADSSTR6	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9879h	AD	A/D Sampling State Register 7	ADSSTR7	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 987Dh	AD	Digital Power Supply Control Circuit Output Register	ADDPCONR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64, or 48 pins.
0008 A000h	SCI0	Serial Mode Register	SMR	8	8	2, 3 PCLKB	2 ICLK	SCIc, SCId	
0008 A001h	SCI0	Bit Rate Register	BRR	8	8	2, 3 PCLKB	2 ICLK		
0008 A002h	SCI0	Serial Control Register	SCR	8	8	2, 3 PCLKB	2 ICLK		
0008 A003h	SCI0	Transmit Data Register	TDR	8	8	2, 3 PCLKB	2 ICLK		
0008 A004h	SCI0	Serial Status Register	SSR	8	8	2, 3 PCLKB	2 ICLK		
0008 A005h	SCI0	Receive Data Register	RDR	8	8	2, 3 PCLKB	2 ICLK		
0008 A006h	SCI0	Smart Card Mode Register	SCMR	8	8	2, 3 PCLKB	2 ICLK		
0008 A007h	SCI0	Serial Extended Mode Register	SEMR	8	8	2, 3 PCLKB	2 ICLK		
0008 A008h	SCI0	Noise Filter Setting Register	SNFR	8	8	2, 3 PCLKB	2 ICLK		
0008 A009h	SCI0	I^2C Mode Register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK		
0008 A00Ah	SCI0	I^2C Mode Register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK		
0008 A00Bh	SCI0	I^2C Mode Register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK		
0008 A00Ch	SCI0	I^2C Status Register	SISR	8	8	2, 3 PCLKB	2 ICLK		
0008 A00Dh	SCI0	SPI Mode Register	SPMR	8	8	2, 3 PCLKB	2 ICLK		
0008 A020h	SCI1	Serial Mode Register	SMR	8	8	2, 3 PCLKB	2 ICLK		
0008 A021h	SCI1	Bit Rate Register	BRR	8	8	2, 3 PCLKB	2 ICLK		
0008 A022h	SCI1	Serial Control Register	SCR	8	8	2, 3 PCLKB	2 ICLK		
0008 A023h	SCI1	Transmit Data Register	TDR	8	8	2, 3 PCLKB	2 ICLK		
0008 A024h	SCI1	Serial Status Register	SSR	8	8	2, 3 PCLKB	2 ICLK		
0008 A025h	SCI1	Receive Data Register	RDR	8	8	2, 3 PCLKB	2 ICLK		
0008 A026h	SCI1	Smart Card Mode Register	SCMR	8	8	2, 3 PCLKB	2 ICLK		
0008 A027h	SCI1	Serial Extended Mode Register	SEMR	8	8	2, 3 PCLKB	2 ICLK		
0008 A028h	SCI1	Noise Filter Setting Register	SNFR	8	8	2, 3 PCLKB	2 ICLK		
0008 A029h	SCI1	I^2C Mode Register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK		
0008 A02Ah	SCI1	I^2C Mode Register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK		
0008 A02Bh	SCI1	I^2C Mode Register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK		
0008 A02Ch	SCI1	I^2C Status Register	SISR	8	8	2, 3 PCLKB	2 ICLK		
0008 A02Dh	SCI1	SPI Mode Register	SPMR	8	8	2, 3 PCLKB	2 ICLK		
0008 A040h	SCI2	Serial Mode Register	SMR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 A041h	SCI2	Bit Rate Register	BRR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 A042h	SCI2	Serial Control Register	SCR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 A043h	SCI2	Transmit Data Register	TDR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 A044h	SCI2	Serial Status Register	SSR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 A045h	SCI2	Receive Data Register	RDR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 A046h	SCI2	Smart Card Mode Register	SCMR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.

Table 4.1 List of I/O Registers (Address Order) (37/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
000C 2006h	GPT	General PWM Timer Hardware Source Clear Control Register	GTHCCR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK	GPT	
000C 2008h	GPT	General PWM Timer Hardware Start Source Select Register	GTHSSR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 200Ah	GPT	General PWM Timer Hardware Stop/Clear Source Select Register	GTHPSR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 200Ch	GPT	General PWM Timer Write-Protection Register	GTWP	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 200Eh	GPT	General PWM Timer Sync Register	GTSYNC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2010h	GPT	General PWM Timer External Trigger Input Interrupt Register	GTETINT	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2014h	GPT	General PWM Timer Buffer Operation Disable Register	GTBDR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2018h	GPT	General PWM Timer Start Write-Protection Register	GTSWP	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2080h	GPT	LOCO Count Control Register	LCCR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2082h	GPT	LOCO Count Status Register	LCST	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2084h	GPT	LOCO Count Value Register	LCNT	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2086h	GPT	LOCO Count Result Average Register	LCNTA	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2088h	GPT	LOCO Count Result Register 0	LCNT00	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 208Ah	GPT	LOCO Count Result Register 1	LCNT01	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 208Ch	GPT	LOCO Count Result Register 2	LCNT02	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 208Eh	GPT	LOCO Count Result Register 3	LCNT03	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2090h	GPT	LOCO Count Result Register 4	LCNT04	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2092h	GPT	LOCO Count Result Register 5	LCNT05	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2094h	GPT	LOCO Count Result Register 6	LCNT06	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2096h	GPT	LOCO Count Result Register 7	LCNT07	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2098h	GPT	LOCO Count Result Register 8	LCNT08	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 209Ah	GPT	LOCO Count Result Register 9	LCNT09	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 209Ch	GPT	LOCO Count Result Register 10	LCNT10	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 209Eh	GPT	LOCO Count Result Register 11	LCNT11	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 20A0h	GPT	LOCO Count Result Register 12	LCNT12	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 20A2h	GPT	LOCO Count Result Register 13	LCNT13	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 20A4h	GPT	LOCO Count Result Register 14	LCNT14	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 20A6h	GPT	LOCO Count Result Register 15	LCNT15	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 20A8h	GPT	LOCO Count Upper Permissible Deviation Register	LCNTDU	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 20AAh	GPT	LOCO Count Lower Permissible Deviation Register	LCNTDL	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2100h	GPT0	General PWM Timer I/O Control Register	GTIOR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2102h	GPT0	General PWM Timer Interrupt Output Setting Register	GTINTAD	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2104h	GPT0	General PWM Timer Control Register	GTCR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2106h	GPT0	General PWM Timer Buffer Enable Register	GTBER	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2108h	GPT0	General PWM Timer Count Direction Register	GTUDC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 210Ah	GPT0	General PWM Timer Interrupt, A/D Converter Start Request Skipping Setting Register	GTITC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 210Ch	GPT0	General PWM Timer Status Register	GTST	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 210Eh	GPT0	General PWM Timer Counter	GTCNT	16	16	2 to 5 PCLKA	2, 3 ICLK		
000C 2110h	GPT0	General PWM Timer Compare Capture Register A	GTCCRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2112h	GPT0	General PWM Timer Compare Capture Register B	GTCCRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2114h	GPT0	General PWM Timer Compare Capture Register C	GTCCRC	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2116h	GPT0	General PWM Timer Compare Capture Register D	GTCCRD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2118h	GPT0	General PWM Timer Compare Capture Register E	GTCCRE	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		

Table 4.1 List of I/O Registers (Address Order) (43/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
000C 291Ah	GPT4	General PWM Timer Compare Capture Register F	GTCCRF	16	16, 32	2 to 5 PCLKA	2, 3 ICLK	GPT	Not present in versions with 64 or 48 pins.
000C 291Ch	GPT4	General PWM Timer Cycle Setting Register	GTPR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 291Eh	GPT4	General PWM Timer Cycle Setting Buffer Register	GTPBR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2920h	GPT4	General PWM Timer Cycle Setting Double-Buffer Register	GTPDBR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2924h	GPT4	A/D Converter Start Request Timing Register A	GTADTRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2926h	GPT4	A/D Converter Start Request Timing Buffer Register A	GTADTBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2928h	GPT4	A/D Converter Start Request Timing Double-Buffer Register A	GTADTDBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 292Ch	GPT4	A/D Converter Start Request Timing Register B	GTADTRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 292Eh	GPT4	A/D Converter Start Request Timing Buffer Register B	GTADTBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2930h	GPT4	A/D Converter Start Request Timing Double-Buffer Register B	GTADTDBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2934h	GPT4	General PWM Timer Output Negate Control Register	GTONCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2936h	GPT4	General PWM Timer Dead Time Control Register	GTDTCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2938h	GPT4	General PWM Timer Dead Time Value Register U	GTDVU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 293Ah	GPT4	General PWM Timer Dead Time Value Register D	GTDVD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 293Ch	GPT4	General PWM Timer Dead Time Buffer Register U	GTDBU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 293Eh	GPT4	General PWM Timer Dead Time Buffer Register D	GTDBD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2940h	GPT4	General PWM Timer Output Protection Function Status Register	GTSOS	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2942h	GPT4	General PWM Timer Output Protection Function Temporary Release Register	GTSOTR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2980h	GPT5	General PWM Timer I/O Control Register	GTIOR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2982h	GPT5	General PWM Timer Interrupt Output Setting Register	GTINTAD	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2984h	GPT5	General PWM Timer Control Register	GTCR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2986h	GPT5	General PWM Timer Buffer Enable Register	GTBER	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2988h	GPT5	General PWM Timer Count Direction Register	GTUDC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 298Ah	GPT5	General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register	GTITC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 298Ch	GPT5	General PWM Timer Status Register	GTST	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 298Eh	GPT5	General PWM Timer Counter	GTCNT	16	16	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2990h	GPT5	General PWM Timer Compare Capture Register A	GTCCRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2992h	GPT5	General PWM Timer Compare Capture Register B	GTCCRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2994h	GPT5	General PWM Timer Compare Capture Register C	GTCCRC	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2996h	GPT5	General PWM Timer Compare Capture Register D	GTCCRD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2998h	GPT5	General PWM Timer Compare Capture Register E	GTCCRE	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 299Ah	GPT5	General PWM Timer Compare Capture Register F	GTCCRF	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 299Ch	GPT5	General PWM Timer Cycle Setting Register	GTPR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.



Note1. Be sure to specify WDON and WDOFF as at least one cycle of BCLK.

Figure 5.14 External Bus Timing/Normal Write Cycle (Bus Clock Synchronized)

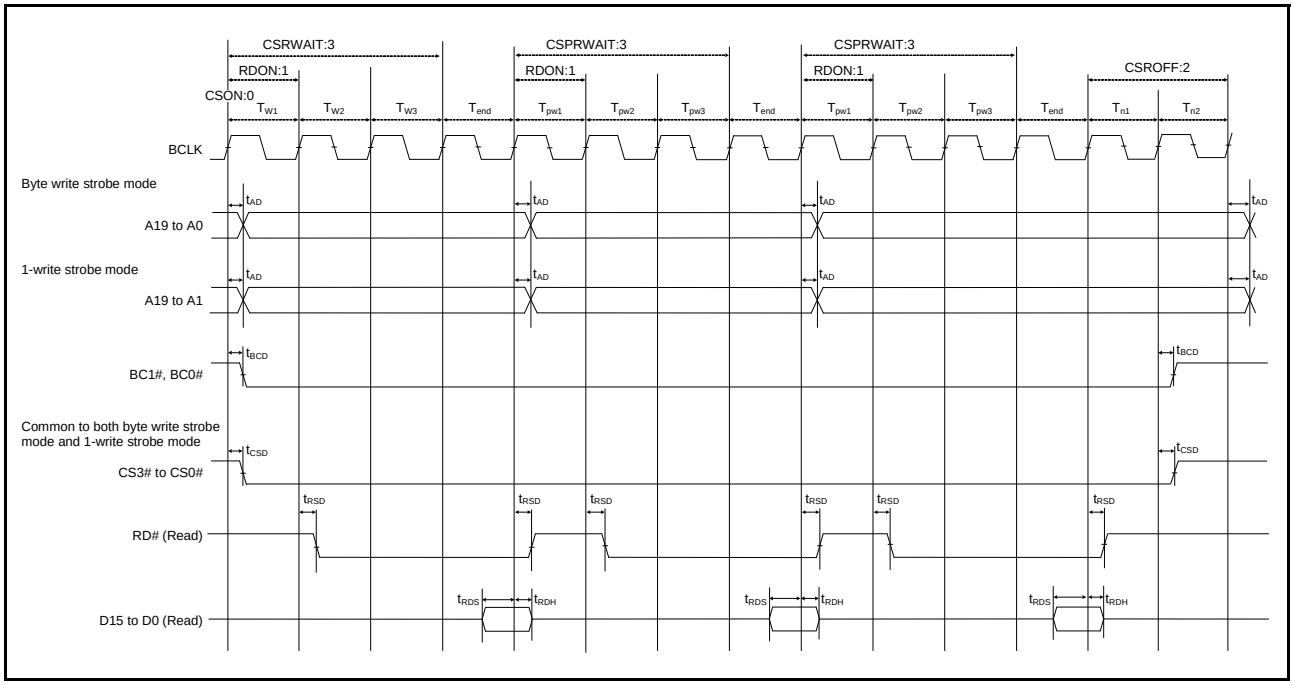
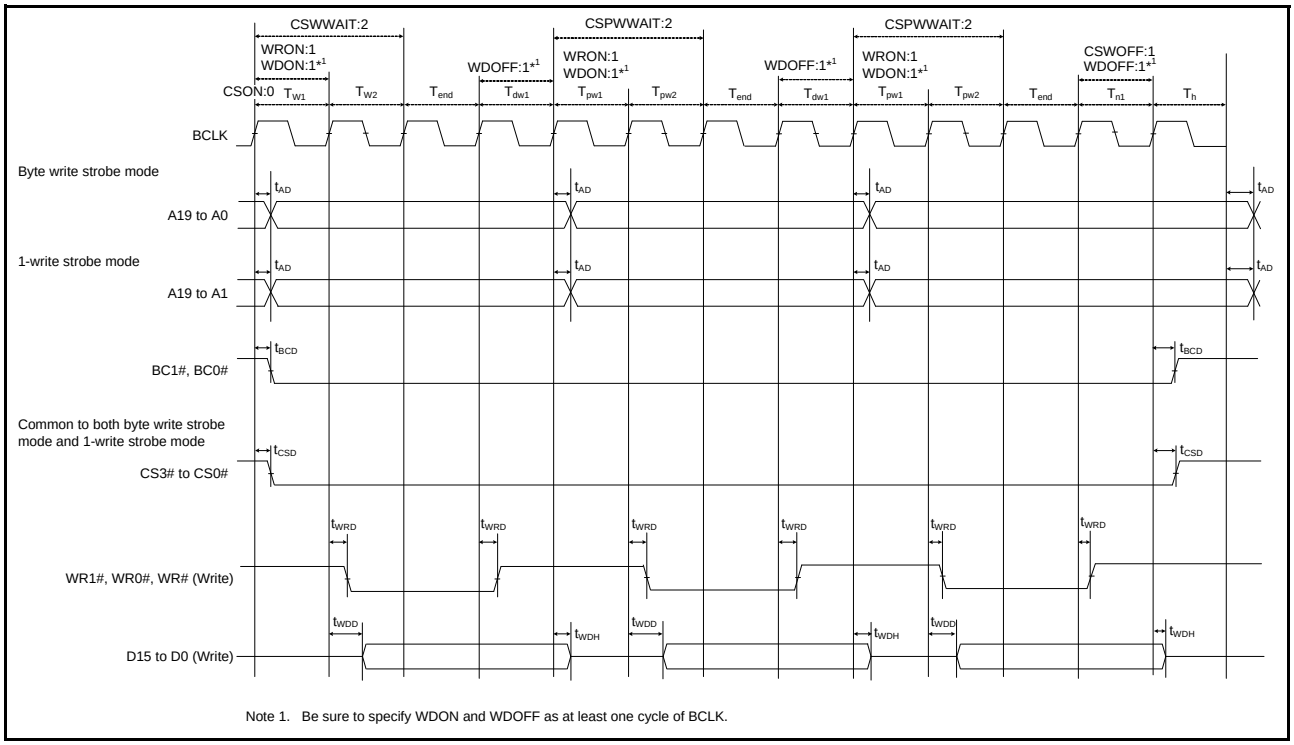


Figure 5.15 External Bus Timing/Page Read Cycle (Bus Clock Synchronized)



Note 1. Be sure to specify WDON and WDOFF as at least one cycle of BCLK.

Figure 5.16 External Bus Timing/Page Write Cycle (Bus Clock Synchronized)

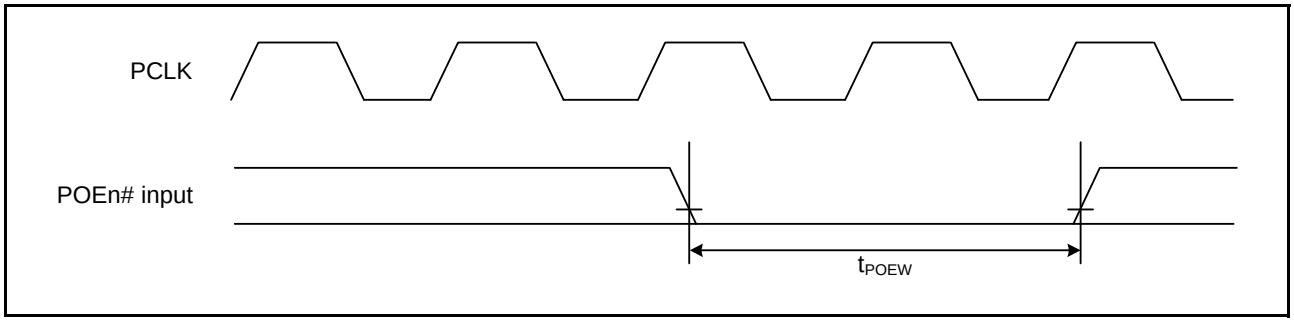


Figure 5.25 POE3# Input Timing

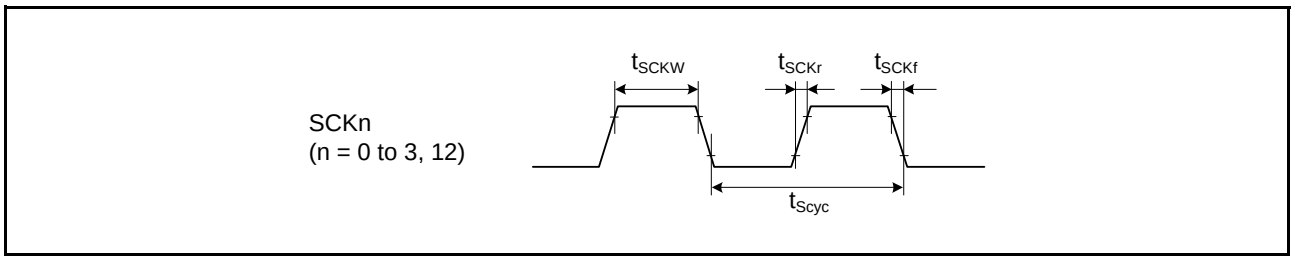


Figure 5.26 SCK Clock Input Timing

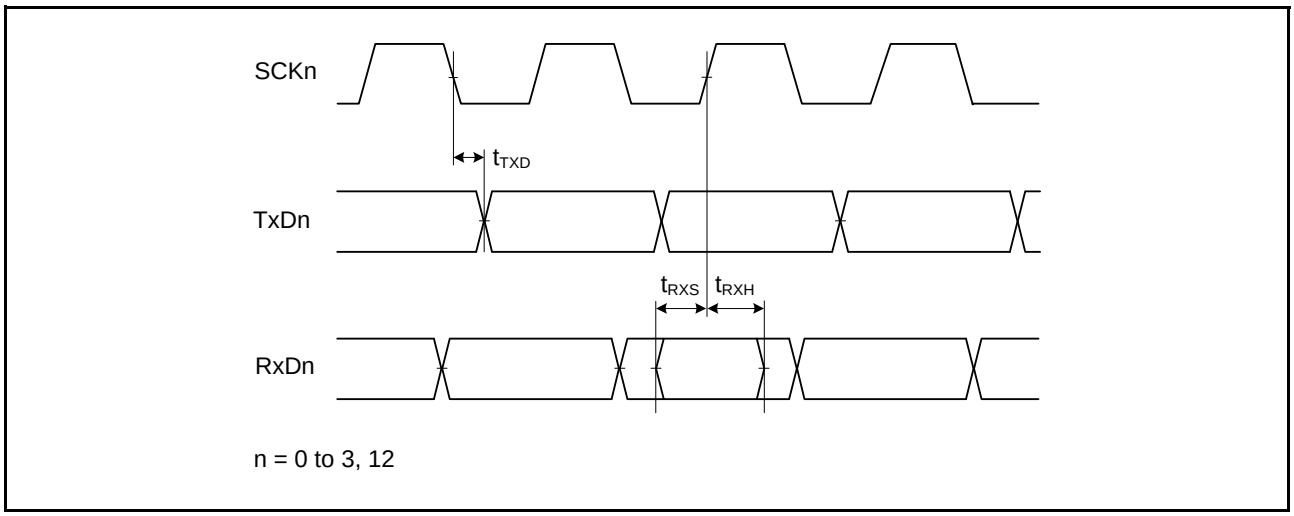


Figure 5.27 SCI Input/Output Timing: Clock Synchronous Mode

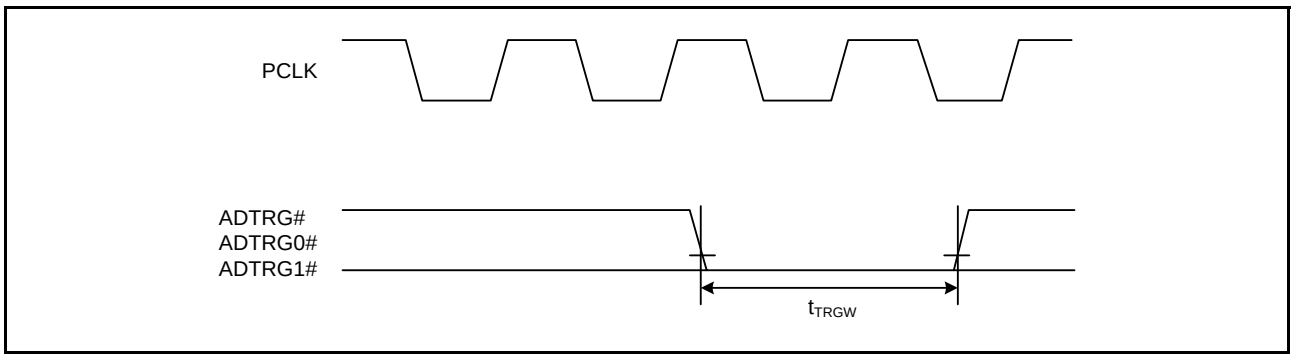


Figure 5.28 AD Converter External Trigger Input Timing

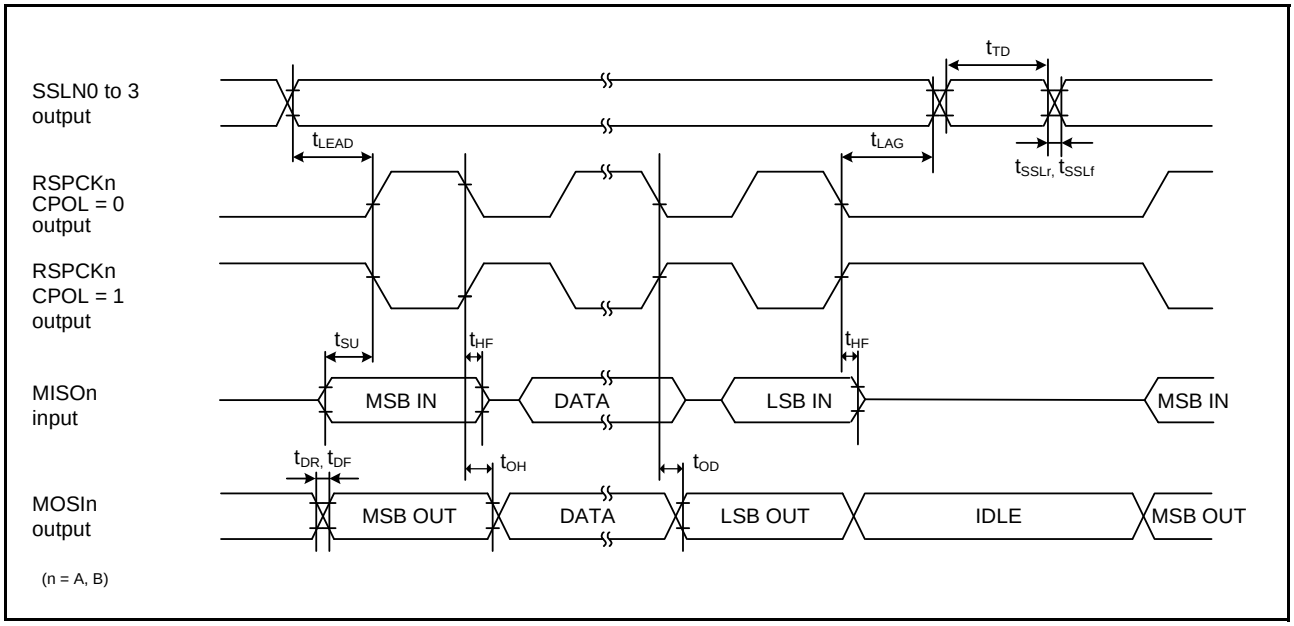


Figure 5.31 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKB Division Ratio Set to 1/2)

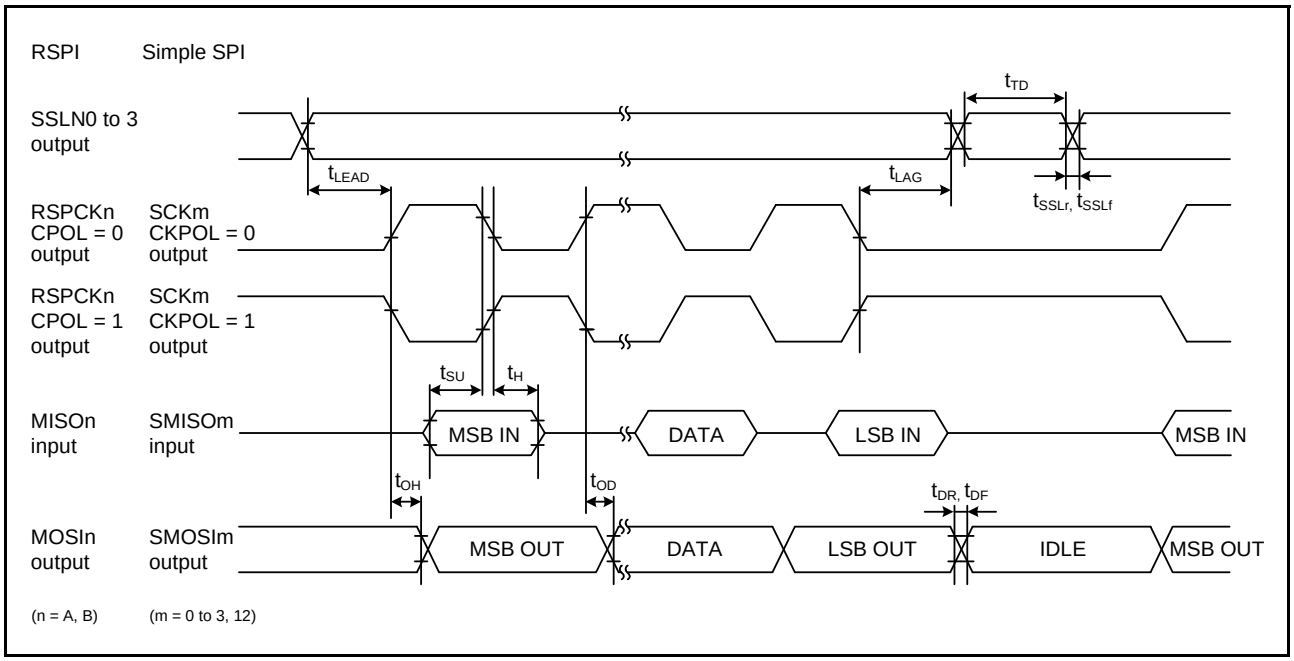


Figure 5.32 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKB Division Ratio Set to a Value Other Than 1/2) and Simple SPI Timing (Master, CKPH = 0)

Table 5.24 Comparator Characteristics

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Analog input capacitance	C_{in}	—	—	8	pF	
REFH pin offset voltage	V_{off}	—	—	5	mV	
REFL pin offset voltage		—	—	5	mV	
REFH input voltage range	V_{in}	1.7	—	AVcc – 0.3	V	
REFL input voltage range		0.3	—	AVcc – 1.7	V	
REFH reply time	t_{CR}	—	—	500	ns	VI = VREF±25mV
REFL reply time	t_{CF}	—	—	500	ns	

5.6 D/A Conversion Characteristics

Table 5.25 D/A Conversion Characteristics

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	10	10	10	Bit	
Conversion time	—	—	3.0	µs	20-pF capacitive load
Absolute accuracy	—	±2.0	±4.0	LSB	2-MΩ resistive load
	—	—	±3.0	LSB	4-MΩ resistive load
	—	—	±2.0	LSB	10-MΩ resistive load
RO output resistance	—	3.6	—	kΩ	

Table 5.27 Power-on Reset Circuit and Voltage Detection Circuit Characteristics (2)

Condition: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0
$T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	V_{POR}	3.6	3.8	4.0	V	Figure 5.41
	Voltage detection circuit (LVD0)	V_{DET0}	4.0	4.2	4.4		Figure 5.42
	Voltage detection circuit (LVD1)*1	V_{DET1_8}	4.59	4.77	4.95		Figure 5.43
		V_{DET1_9}	4.05	4.23	4.41		
		V_{DET1_A}	4.32	4.50	4.68		
	Voltage detection circuit (LVD2)*2	V_{DET2_8}	4.59	4.77	4.95		Figure 5.44
		V_{DET2_9}	4.05	4.23	4.41		
		V_{DET2_A}	4.32	4.50	4.68		
Internal reset time	Power-on reset (POR)	t_{POR}		9.7		ms	Figure 5.41
	Voltage detection circuit (LVD0)	t_{LVD0}		9.7			Figure 5.42
	Voltage detection circuit (LVD1)	t_{LVD1}		0.9			Figure 5.43
	Voltage detection circuit (LVD2)	t_{LVD2}		0.9			Figure 5.44
Minimum VCC down time*3		t_{VOFF}	200	—	—	µs	Figure 5.41 to Figure 5.44
Response delay time		t_{DET}			200	µs	
LVD operation stabilization time (after LVD is enabled)		$Td_{(E-A)}$			3	µs	Figure 5.41 to Figure 5.44
Hysteresis width (LVD1 and LVD2)		V_{LVH}		80		mV	

Note 1. # in symbol $V_{DET1\_\#}$ indicates the value of the LVDLVLR.LVD1LVL[3:0] bits.
Note 2. # in symbol $V_{DET2\_\#}$ indicates the value of the LVDLVLR.LVD2LVL[3:0] bits.
Note 3. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{DET1}, and V_{DET2} for the POR/ LVD.

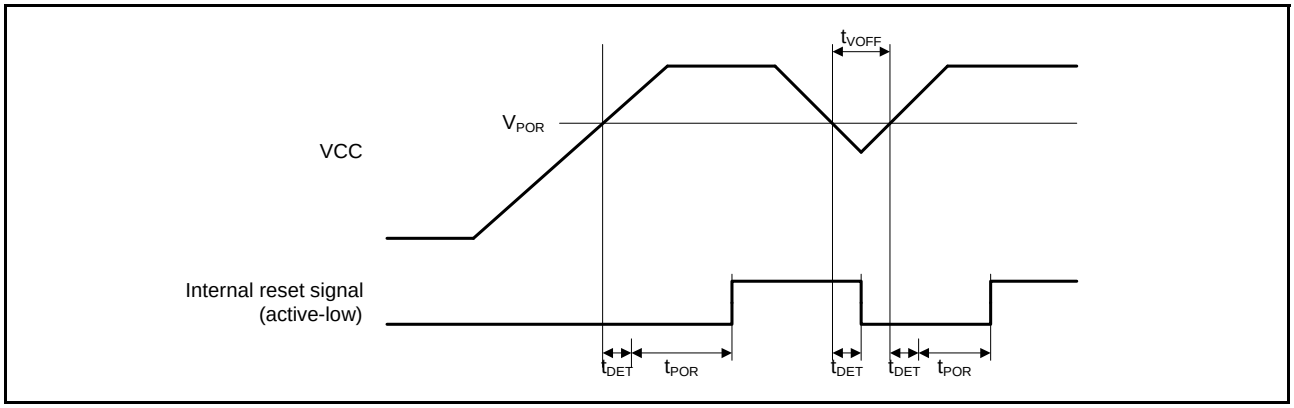


Figure 5.39 Power-on Reset Timing

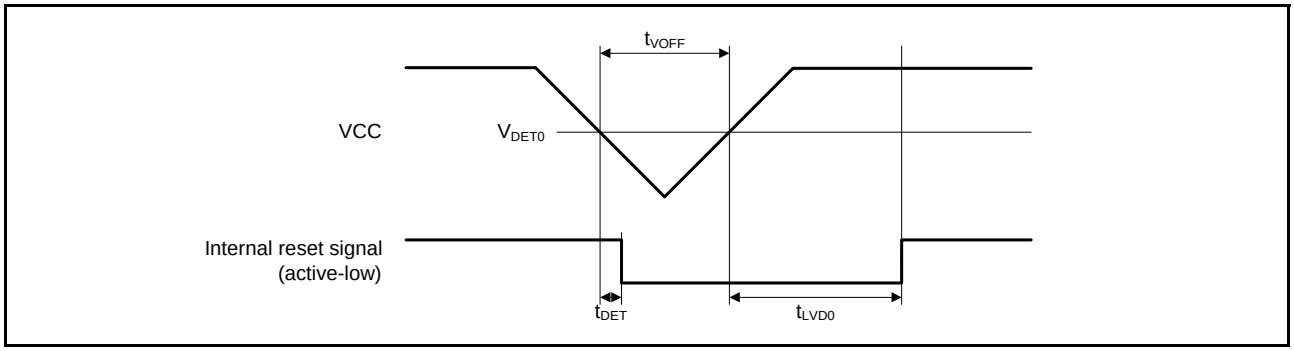


Figure 5.40 Voltage Detection Circuit Timing (V_{DET0})

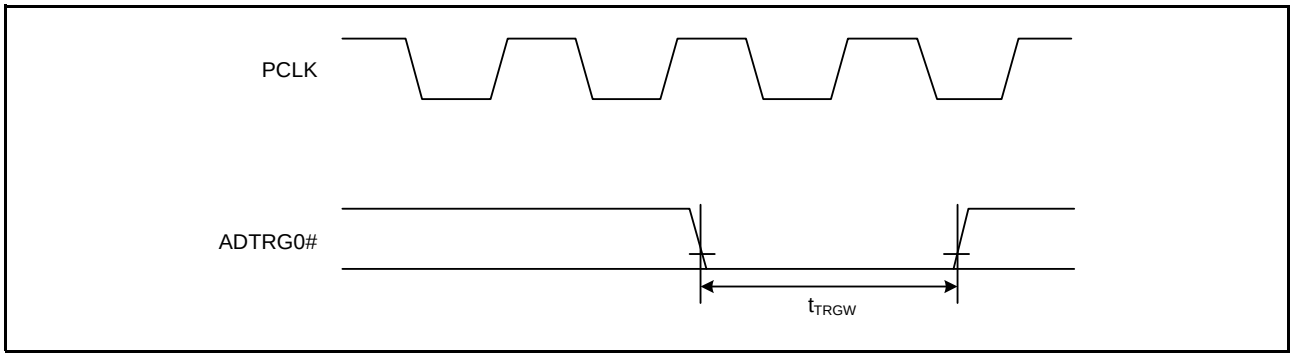


Figure 6.19 AD Converter External Trigger Input Timing

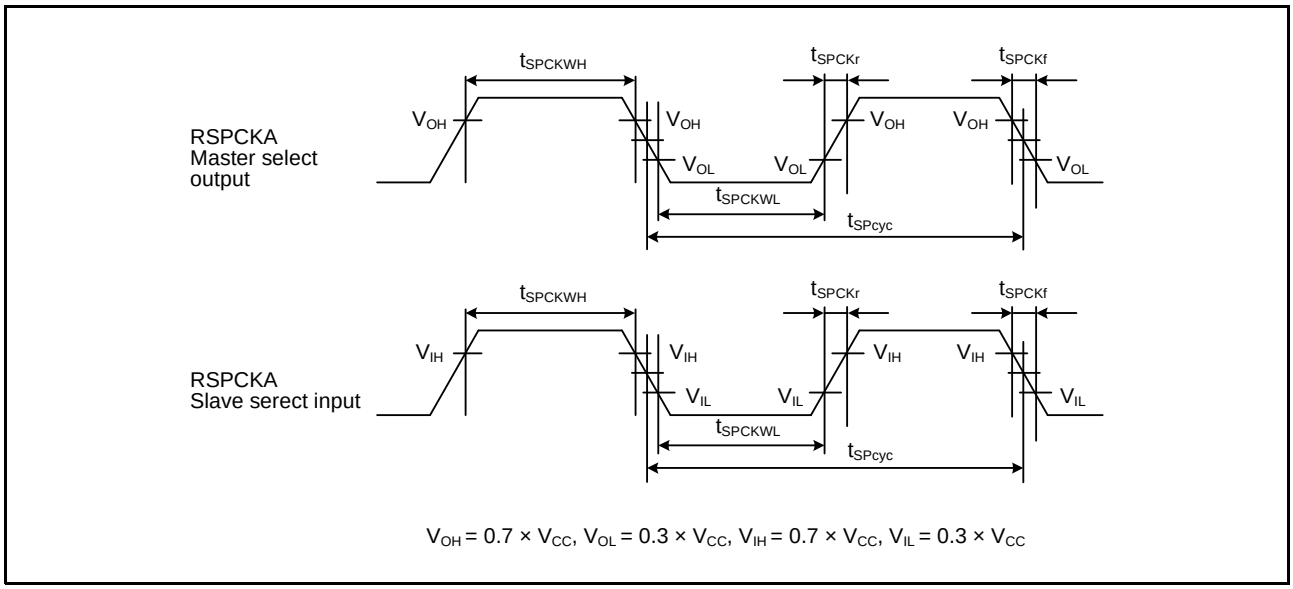


Figure 6.20 RSPI Clock Timing and Simple SPI Clock Timing

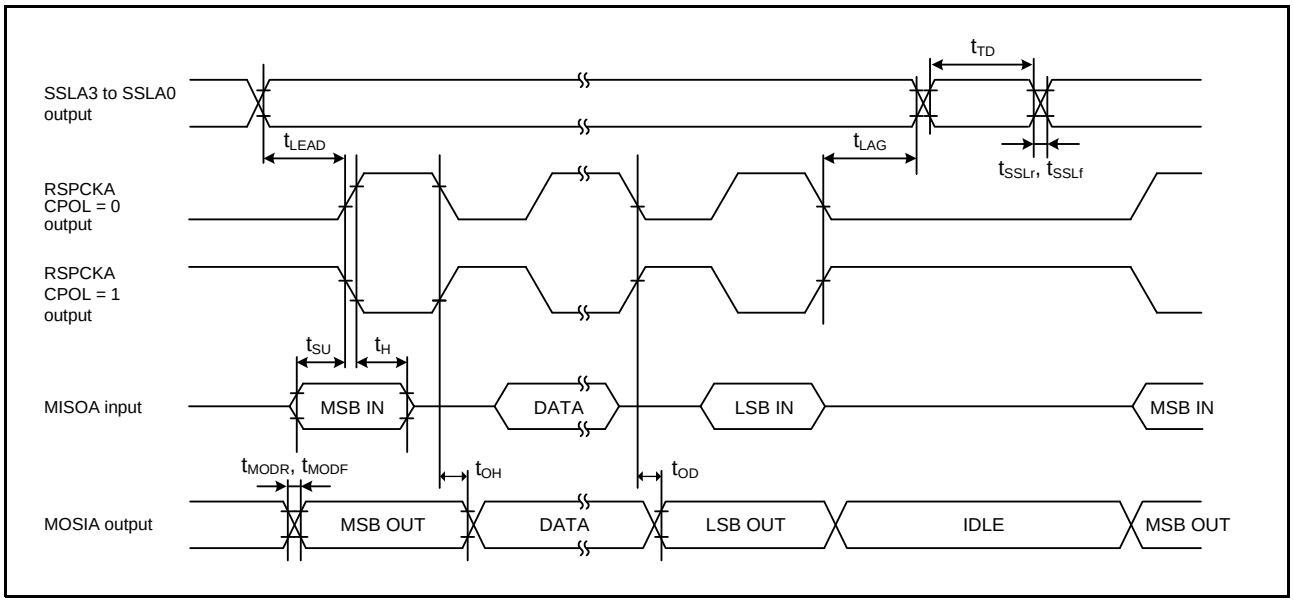


Figure 6.21 RSPI Timing (Master, CPHA = 0) and Simple SPI Timing (Master, CKPH = 1)

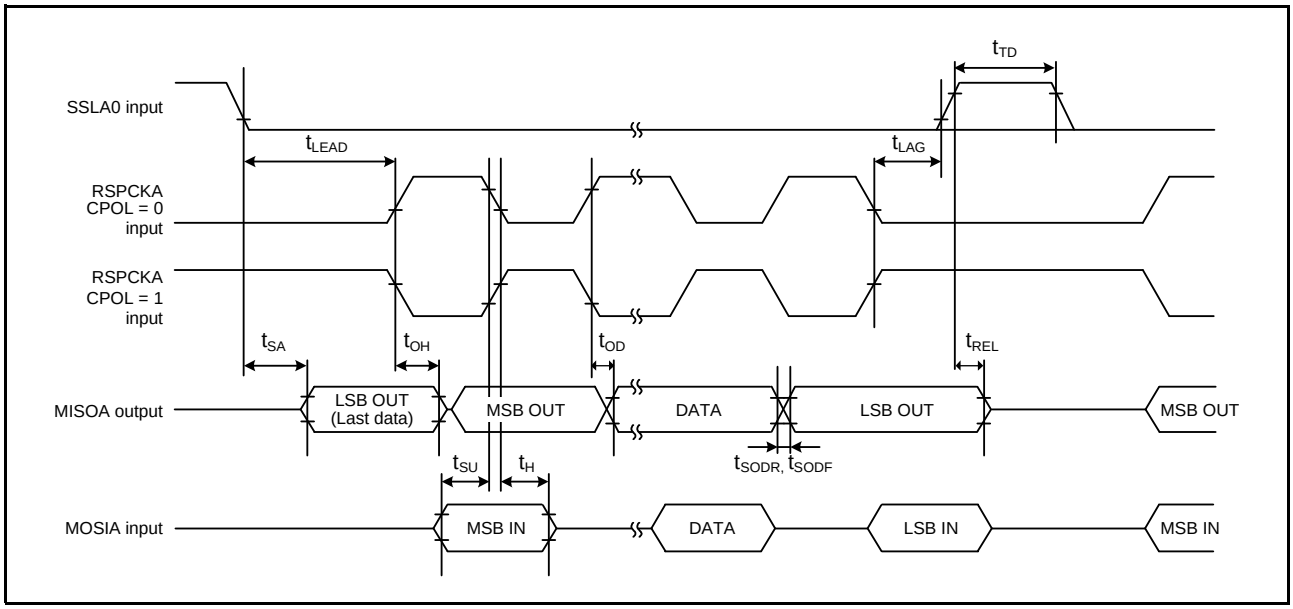
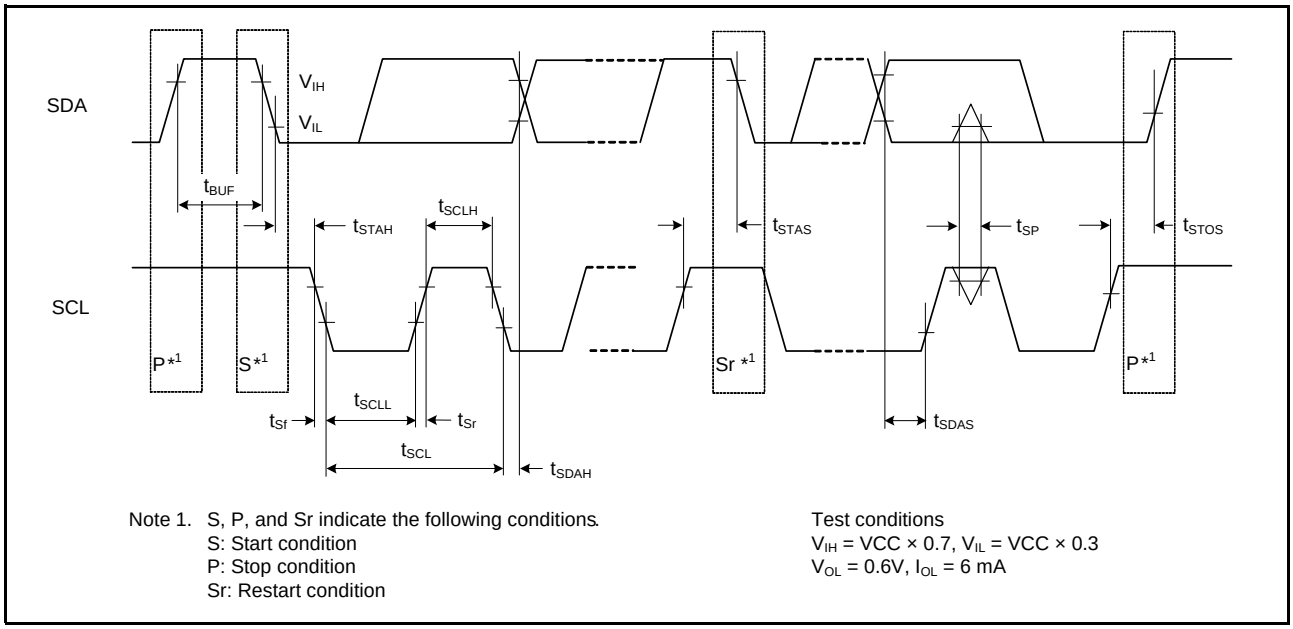


Figure 6.24 RSPI Timing (Slave, CPHA = 1) and Simple SPI Timing (Slave, CKPH = 0)



Note 1. S, P, and Sr indicate the following conditions.
S: Start condition
P: Stop condition
Sr: Restart condition

Test conditions
V_{IH} = VCC × 0.7, V_{IL} = VCC × 0.3
V_{OL} = 0.6V, I_{OL} = 6 mA

Figure 6.25 RIIC Bus Interface Input/Output Timing and Simple IIC Bus Interface Input/Output Timing

6.4 A/D Conversion Characteristics

Table 6.16 12-Bit A/D Conversion Characteristics

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item		min	typ	max	Unit	Test Conditions
Resolution		12	12	12	Bit	
Conversion time *1 (ADCLK = 50 MHz)	When the sample-and-hold circuit is in use per pin	1.6	—	—	µs	Sampling by the sample-and-hold circuit in 30 states. Sampling by the A/D converter in 20 states.
	When the sample-and-hold circuit is not in use per pin	1.0	—	—	µs	Sampling by the A/D converter in 20 states.
Analog input capacitance		—	—	6	pF	
Integral nonlinearity error		—	—	±4.0	LSB	
Offset error		—	—	±7.5	LSB	
Full-scale error		—	—	±7.5	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy	Sample and hold circuit in use	—	—	±8.0	LSB	AVin = 0.25 to AV_{REFH}–0.25
	Sample and hold circuit not in use	—	—	±8.0	LSB	AVin = AV_{REFL} to AV_{REFH}
Permissible signal source impedance		—	—	3.0	kΩ	

Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Table 6.17 Comparator Characteristics

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item	Symbol	Min	Typ	Max.	Unit	Test Conditions
Analog input capacitance	Cin	—	—	6	pF	
REFH pin offset voltage	Voff	—	—	5	mV	
REFL pin offset voltage		—	—	5	mV	
REFH input voltage range	Vin	1.7	—	AVcc – 0.3	V	
REFL input voltage range		0.3	—	AVcc – 1.7	V	
REFH reply time	tCR	—	—	0.5	µs	
REFL reply time	tCF	—	—	0.5	µs	

6.5 Power-on Reset Circuit and Voltage Detection Circuit Characteristics

Table 6.18 Power-on Reset Circuit and Voltage Detection Circuit Characteristics

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	V_{POR}	2.5	2.6	2.7	V	Figure 6.26
	Voltage detection circuit (LVD0)	V_{DET0}	2.7	2.8	2.9		Figure 6.27
	Voltage detection circuit (LVD1)	V_{DET1}	2.80	2.95	3.10		
	Voltage detection circuit (LVD2)	V_{DET2}	2.80	2.95	3.10		
Internal reset time	Power-on reset (POR)	t_{POR}	—	4.6		ms	Figure 6.26
	Voltage detection circuit (LVD0)	t_{LVD0}	—	4.6			Figure 6.27
	Voltage detection circuit (LVD1)	t_{LVD1}	—	0.9			Figure 6.28
	Voltage detection circuit (LVD2)	t_{LVD2}	—	0.9			Figure 6.29
Minimum VCC down time*1		t_{VOFF}	200	—	—	µs	Figure 6.26, Figure 6.27
Response delay time		t_{det}			200	µs	Figure 6.26 to Figure 6.29
LVD operation stabilization time (after LVD is enabled)		$Td_{(E-A)}$			3	µs	Figure 6.28 Figure 6.29
Hysteresis width (LVD1 and LVD2)		V_{LVH}		80		mV	

Note 1. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{DET1}, and V_{DET2} for the POR/ LVD.

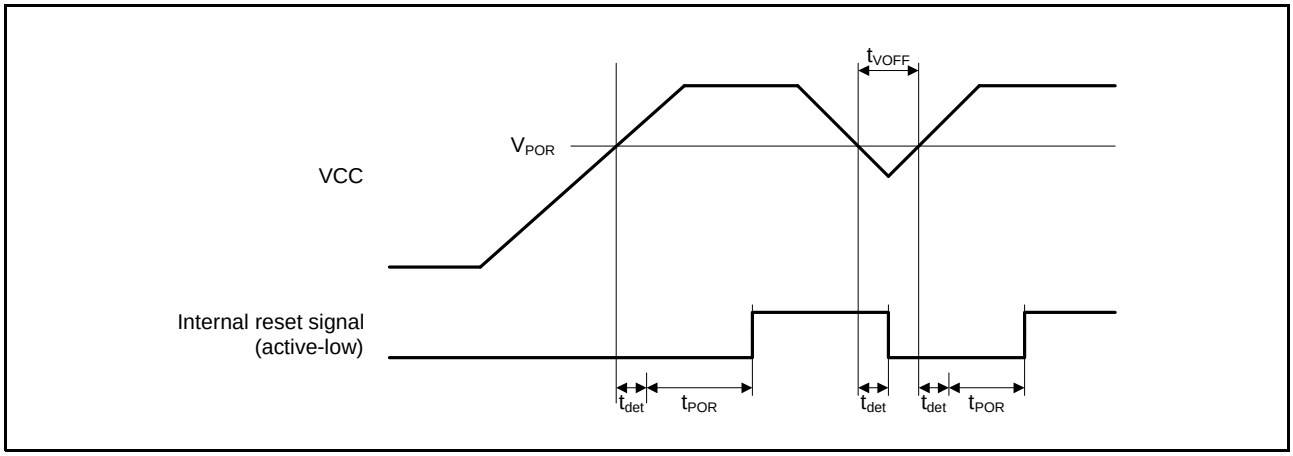


Figure 6.26 Power-on Reset Timing

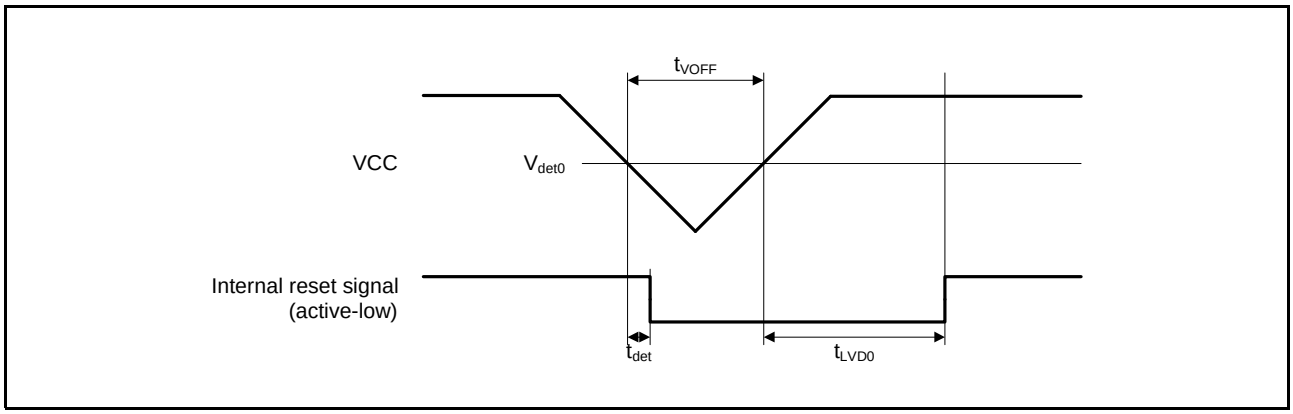


Figure 6.27 Voltage Detection Circuit Timing (V_{det0})

Classifications

- Items with Technical Update document number: Changes according to the corresponding issued Technical Update
- Items without Technical Update document number: Minor changes that do not require Technical Update to be issued

Rev.	Date	Description		Classification
		Page	Summary	
2.20	Mar 31, 2016	1. Overview		
		2 to 8	Table 1.1 Outline of Specifications, Note 1 changed	TN-RX*-A086A/E
		10 to 13	Table 1.3 List of Products, changed	TN-RX*-A086A/E
		16	Table 1.4 Pin Functions, changed	
		27 to 30	Table 1.5 List of Pins and Pin Functions (144-Pin LQFP), changed	
		30	Table 1.5 List of Pins and Pin Functions (144-Pin LQFP), Note 1 added	
		31 to 34	Table 1.6 List of Pins and Pin Functions (120-Pin LQFP), changed	
		35 to 38	Table 1.7 List of Pins and Pin Functions (112-Pin LQFP), changed	
		38	Table 1.7 List of Pins and Pin Functions (112-Pin LQFP), Note 1 added	
		4. I/O Registers		
		54	(4) Notes on Sleep Mode and Mode Transition, added	TN-RX*-A140A/E
		55 to 102	Table 4.1 List of I/O Registers (Address Order), changed	TN-RX*-A086A/E, TN-RX*-A140A/E
		5. Electrical Characteristics [144-, 120-, 112- and 100-Pin Versions]		
		103	Table 5.1 Absolute Maximum Ratings, changed	TN-RX*-A086A/E
		106	Table 5.4 DC Characteristics (3), changed	
		107	Table 5.5 Permissible Output Currents, changed	
		108	Table 5.6 Permissible Power Consumption (G version product only), title changed, notes added	TN-RX*-A086A/E
		111	Table 5.9 Clock Timing, changed	TN-RX*-A097A/E
		112	Figure 5.6 LOCO, IWDTCLK Clock Oscillation Start Timing, title changed	TN-RX*-A097A/E
		112	Figure 5.6 LOCO, IWDTCLK Clock Oscillation Start Timing, changed	TN-RX*-A097A/E
		124	Table 5.16 Timing of On-Chip Peripheral Modules (1), changed	TN-RX*-A121A/E
		125	Table 5.16 Timing of On-Chip Peripheral Modules (2), changed	TN-RX*-A121A/E
		126	Table 5.16 Timing of On-Chip Peripheral Modules (3), changed	TN-RX*-A121A/E
		127	Table 5.16 Timing of On-Chip Peripheral Modules (4), changed	
		129	Table 5.17 Timing of the PWM Delay Generation Circuit	TN-RX*-A086A/E
		132	Figure 5.30 RSPI Timing (Master, CPHA = 0) (Bit Rate: PCLKB Division Ratio Set to a Value Other Than 1/2) and Simple SPI Timing (Master, CKPH = 1), title and figure changed	
		133	Figure 5.32 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKB Division Ratio Set to a Value Other Than 1/2) and Simple SPI Timing (Master, CKPH = 0), title changed	
		134	Figure 5.34 RSPI Timing (Slave, CPHA = 0) and Simple SPI Timing (Slave, CKPH = 1), title changed	
		135	Figure 5.35 RSPI Timing (Slave, CPHA = 1) and Simple SPI Timing (Slave, CKPH = 0), title changed	
		136	Table 5.18 On-Chip USB Full-Speed Characteristics (DP and DM Pin Characteristics), Condition 1, 2 changed	TN-RX*-A086A/E
		143	Table 5.26 Power-on Reset Circuit and Voltage Detection Circuit Characteristics (1), changed	
		6. Electrical Characteristics [64- and 48-Pin Versions]		
		150	Table 6.1 Absolute Maximum Ratings, changed	TN-RX*-A086A/E
		153	Table 6.5 Permissible Power Consumption (G version product only), title changed, note added	TN-RX*-A086A/E
		154	Table 6.7 Clock Timing, changed	TN-RX*-A097A/E
		155	Figure 6.3 LOCO, IWDTCLK Clock Oscillation Start Timing, title changed	TN-RX*-A097A/E
		155	Figure 6.3 LOCO, IWDTCLK Clock Oscillation Start Timing, changed	TN-RX*-A097A/E
		161	Table 6.12 Timing of On-Chip Peripheral Modules (2), changed	
		170	Table 6.18 Power-on Reset Circuit and Voltage Detection Circuit Characteristics, changed	