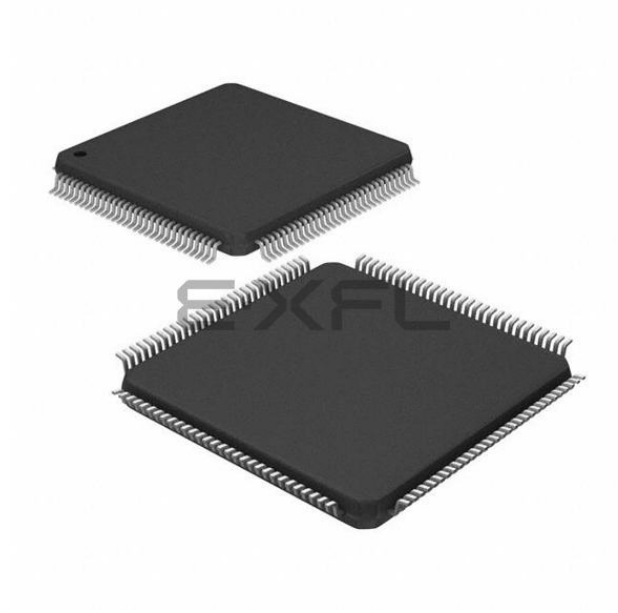
# Renesas Electronics America Inc - R5F563TEBDFA#V0 Datasheet



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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Not For New Designs |
| Core Processor | RX |
| Core Size | 32-Bit Single-Core |
| Speed | 100MHz |
| Connectivity | CANbus, EBI/EMI, I²C, LINbus, SCI, SPI, USB |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 72 |
| Program Memory Size | 512KB (512K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 32K x 8 |
| RAM Size | 48K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 3.6V |
| Data Converters | A/D 12x10b, 8x12b; D/A 2x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 120-LQFP |
| Supplier Device Package | 120-LQFP (16x16) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f563tebdfa-v0 |

**Table 1.1 Outline of Specifications (5/7)**

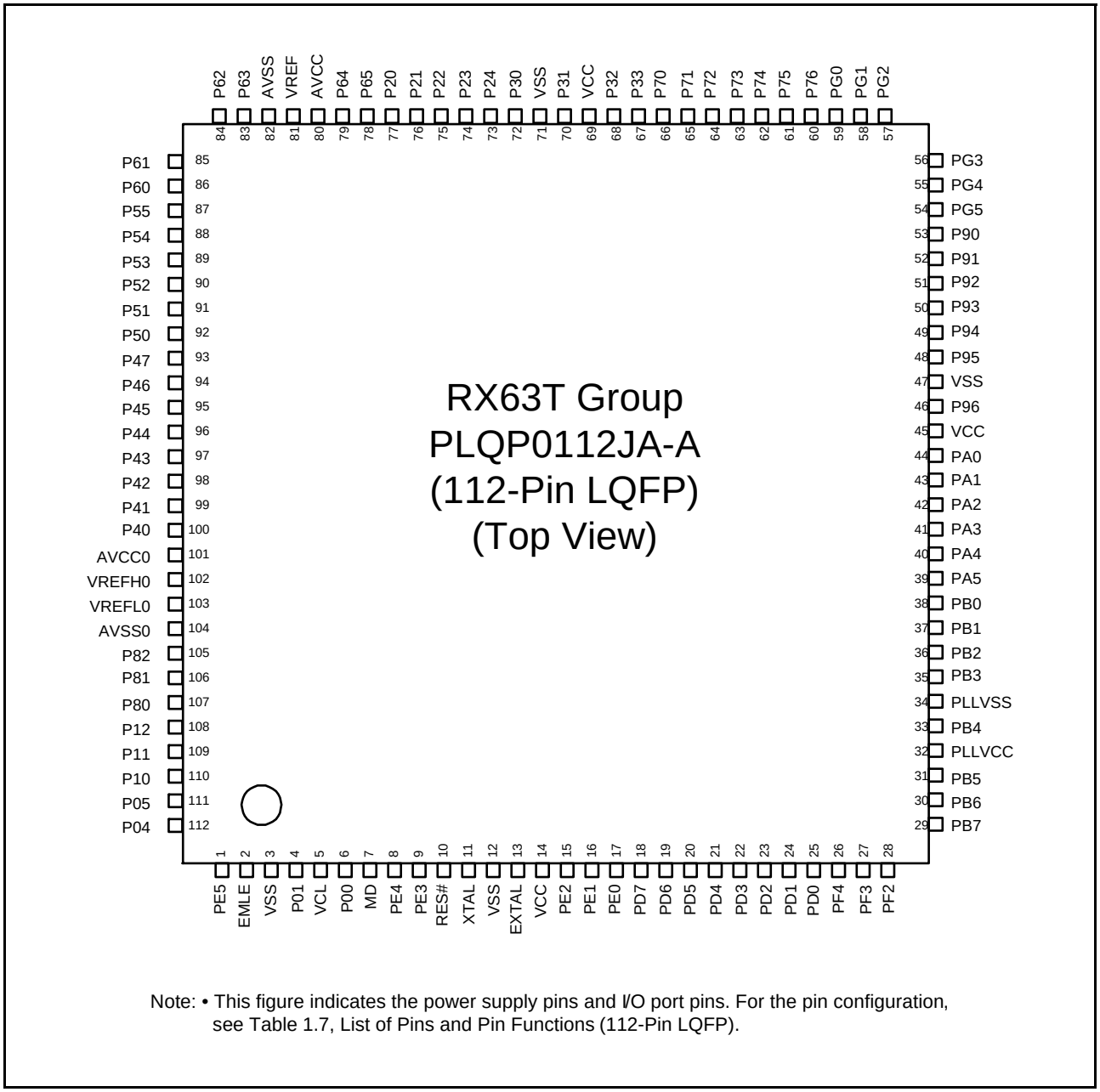
| Classification | Module/Function | Description |
|---|---|---|
| Communication function | $I^2C$ bus interfaces (RIIC) | • 2 channels<br>Communication formats<br>$I^2C$ bus format/SMBus format<br>Supports the multi-master<br>Max. transfer rate: 400 kbps |
| | CAN module (CAN) | • 1 channels<br>• Compliance with the ISO11898-1 specification (standard frame and extended frame)<br>• 32 mailboxes per channel |
| | Serial peripheral interfaces (RSPI) | • 2 channels<br>• RSPI transfer facility<br>Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPCK (RSPI clock) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines)<br>Capable of handling serial transfer as a master or slave<br>• Data formats<br>Switching between MSB first and LSB first<br>The number of bits in each transfer can be changed to any number of bits from 8 to 16, or to 20, 24, or 32 bits.<br>128-bit buffers for transmission and reception<br>Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits)<br>• Buffered structure<br>Double buffers for both transmission and reception<br>• Max. transfer rate<br>In master mode: [144-, 120-, 112- and 100-pin versions]<br>25 Mbps<br>[64- and 48-pin versions]<br>12.5 Mbps<br>In slave mode: 6.25 Mbps |
| 12-bit A/D converter (S12ADB) [144-, 120-, 112- and 100-pin versions] | | • 12 bits (4 channels x 2 unit)<br>• 12-bit resolution<br>• Conversion time<br>1.0 μs per channel (clock for S12ADB, PCLKD (A/D conversion clock ADCLK) = 50 MHz, AVCC0 = 4.0 to 5.5 V)<br>2.0 μs per channel (clock for S12ADB, PCLKD (A/D conversion clock ADCLK) = 25 MHz, AVCC0 = 3.0 to 3.6 V)<br>• Operating modes<br>Scan mode (single-cycle scan mode/continuous scan mode/group scan mode)<br>Group A priority control (only for the group scan mode)<br>• Sample-and-hold function<br>A common sample-and-hold circuit for units is included.<br>Additionally, sample-and-hold circuit for each unit is included. (three channels per unit)<br>• Self-diagnostic function<br>The self-diagnostic function internally generates three analog input voltages (VREFL0, VREFH0 x 1/2, VREFH0).<br>• Double trigger mode (duplication of A/D converted data)<br>• Input signal amplification function using programmable gain amplifier (three channels per unit)<br>Amplification factors: 2.0 times, 2.5 times, 3.077 times, 3.636 times, 4.0 times, 4.444 times, 5.0 times, 5.714 times, 6.667 times, 10.0 times, 13.333 times (total of 11 steps)<br>• Three ways to start A/D conversion<br>Conversion can be started by software, a conversion start trigger from a timer (MTU3 or GPT), or an external trigger signal.<br>• Window comparators (three channels per unit) |

**Table 1.2 Comparison of Functions for Different Packages**

| Functions | | | RX63T Group | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Package** | | | **144 Pins** | **120 Pins** | **112 Pins** | **100 Pins** | **64 Pins** | **48 Pins** |
| External bus | | | 16 bits | | | | — | |
| External address space | | | 1 Mbyte × 4 areas | | | | — | |
| DMA | DMA controller (DMACA) | | Ch. 0 to 3 | | | | | |
| | Data transfer controller (DTCa) | | Supported | | | | | |
| Interrupt controller (ICUb) | NMI pin | | Supported | | | | | |
| | IRQ pin | | Supported (x 8) | | | | Supported (x 6) | |
| Timers | Multi-function timer pulse unit 3 (MTU3)*1 | | Ch. 0 to 7 | | | | | |
| | General PWM timer (GPT)*1 | Generation of delays in PWM, not supported | Ch. 0 to 7 | | | | Ch. 0 to 3 | |
| | | Generation of delays in PWM, supported | Ch. 0 to 3 | | | | — | |
| | Port output enable 3 (POE3) | | Supported (POE pins × 6) | | | Supported (POE pins × 5) | Supported (POE pins × 4) | |
| | Compare match timer (CMT) | | Ch. 0 to 3 | | | | | |
| | Watchdog timer (WDTA) | | Supported | | | | | |
| | Independent watchdog timer (IWDTa) | | Supported | | | | | |
| Communication function | USB2.0 host/function module (USBa) | | Ch. 0 | | — | | | |
| | Serial communications interfaces (SCIc) | | Ch. 0 to 3 | | | Ch. 0 to 2 | Ch. 0, 1 | |
| | Serial communications interfaces (SCId) | | Ch. 12 | | | | | |
| | $I^2C$ bus interfaces (RIIC) | | Ch. 0, 1 | | Ch. 0 | | | |
| | Serial peripheral interfaces (RSPI) | | Ch. 0, 1 | | | | Ch. 0 | |
| | CAN module (CAN) (as an optional function)*1 | | Ch. 0 | | | | — | |
| 12-bit A/D converter (S12ADB) | | | 4 channels × 2 units | | | | 8 channels × 1 unit (AN000 to 007) | 8 channels × 1 unit (AN000 to 004, 007) |
| | Three-channel simultaneous sampling function | | 2 units | | | | 1 unit | |
| | Programmable gain amplifier | | 3 channels × 2 units | | | | — | |
| | Window comparator | | 3 channels × 2 units | | | | 3 channels × 1 unit | |
| 10-bit A/D converter (ADA) | | | 20 channels | 12 channels | | | — | |
| D/A converter (DAa) | | | Ch. 0, 1 | | | | — | |
| Clock Frequency Accuracy Measurement Circuit | | | Supported | | | | | |
| Digital power supply controller (DPC)*2 | | | Supported | | | | Not supported | |

Note 1. For the MTU3 and GPT, the number of pins will differ with the package. See the list of pins and pin functions for details. In addition, the CAN module is an optional function. For details, see Table 1.3.

Note 2. Not provided for the product ID code O.




Note: • This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.7, List of Pins and Pin Functions (112-Pin LQFP).

**Figure 1.5 Pin Assignment (112-Pin LQFP)**

**Table 1.5 List of Pins and Pin Functions (144-Pin LQFP) (1/4)**

| Pin Number 144-Pin LQFP | Power Supply Clock System Control | I/O Port | Bus | Timer (MTU3, GPT, POE3, CAC) | Communications (SCIc, SCId, RSPI, RIIC, CAN, USB) | Interrupt | S12ADB, AD, DA |
|---|---|---|---|---|---|---|---|
| 1 | VCC_USB | | | | | | |
| 2 | | PE5 | BCLK | | USB0_VBUS | IRQ0 | |
| 3 | EMLE | | | | | | |
| 4 | TRSYNC | P03 | | | RXD2/SMISO2/SSCL2 | IRQ7 | |
| 5 | TRDATA3 | P02 | | | TXD2/SMOSI2/SSDA2 | | |
| 6 | VSS | | | | | | |
| 7 | | P01 | RD# | | CTS0#/RTS0#/SS0#/ USB0_DRPD | | |
| 8 | VCL | | | | | | |
| 9 | | P00 | CS1# | CACREF | | | |
| 10 | MD/FINED | | | | | | |
| 11 | | PE4 | A10 | POE10#/MTCLKC | | IRQ1 | |
| 12 | | PE3 | A11 | POE11#/MTCLKD | | IRQ2-DS | |
| 13 | TRDATA2 | P14 | | | SCK2 | | |
| 14 | VCC | | | | | | |
| 15 | | P13 | | | CTS2#/RTS2#/SS2#/ USB0_VBUSEN | | |
| 16 | RES# | | | | | | |
| 17 | XTAL | | | | | | |
| 18 | VSS | | | | | | |
| 19 | EXTAL | | | | | | |
| 20 | VCC | | | | | | |
| 21 | | PE2 | | POE10# | | NMI | |
| 22 | | PE1 | WR0#/WR# | | CTS12#/RTS12#/ SS12#/SSLA3/SSLB3/ USB0_OVRCURA | | |
| 23 | | PE0 | WR1#/BC1#/ WAIT# | | SSLA2/SSLB2/CRX1/ USB0_OVRCURB | IRQ7 | |
| 24 | | PD7 | | GTIOC0A | CTS0#/RTS0#/SS0#/ SSLA1/SSLB1/CTX1 | | |
| 25 | | PD6 | | GTIOC0B | SSLA0/SSLB0 | | |
| 26 | | PD5 | | GTIOC1A | RXD1/SMISO1/SSCL1 | IRQ6 | |
| 27 | VSS | | | | | | |
| 28 | | PD4 | | GTIOC1B | SCK1 | | |
| 29 | | PD3 | | GTIOC2A | TXD1/SMOSI1/SSDA1 | | |
| 30 | | PD2 | CS2# | GTIOC2B | MOSIA/MOSIB/ USB0_ID | | |
| 31 | | PD1 | CS0# | GTIOC3A | MISOA/MISOB/ USB0_EXICEN | | |
| 32 | | PD0 | A12 | GTIOC3B | RSPCKA/RSPCKB | | |
| 33 | | PF4 | CS3# | | | | |
| 34 | | PF3 | | | TXD1/SMOSI1/SSDA1 | | |
| 35 | | PF2 | CS1# | | RXD1/SMISO1/SSCL1 | IRQ5 | |
| 36 | TRST# | PF1 | | | | | |
| 37 | TMS | PF0 | | | | | |
| 38 | | PB7 | A19 | | SCK12 | | |

**Table 1.7 List of Pins and Pin Functions (112-Pin LQFP) (2/4)**

| Pin Number 112-Pin LQFP | Power Supply Clock System Control | I/O Port | Bus | Timer (MTU3, GPT, POE3, CAC) | Communications (SCIc, SCId, RSPI, RIIC, CAN) | Interrupt | S12ADB, AD, DA |
|---|---|---|---|---|---|---|---|
| 38 | | PB0 | A14 | MTIOC0D | MOSIA/MOSIB | | |
| 39 | | PA5 | | MTIOC1A | RXD0/SMISO0/ SSCL0/ MISOA/MISOB | | ADTRG1# |
| 40 | | PA4 | | MTIOC1B | TXD0/SMOSI0/ SSDA0/RSPCKA/ RSPCKB | | ADTRG0# |
| 41 | | PA3 | | MTIOC2A | SCK0/SSLA0/SSLB0 | | |
| 42 | | PA2 | | MTIOC2B | RXD2/SMISO2/ SSCL2/ SSLA1/SSLB1 | | |
| 43 | | PA1 | | MTIOC6A | TXD2/SMOSI2/ SSDA2/SSLA2/SSLB2 | | |
| 44 | | PA0 | | MTIOC6C | SCK2/SSLA3/SSLB3 | | |
| 45 | VCC | | | | | | |
| 46 | | P96 | A13 | POE4# | RXD1/SMISO1/SSCL1 | IRQ4-DS | |
| 47 | VSS | | | | | | |
| 48 | | P95 | | MTIOC6B/ GTIOC4A | TXD1/SMOSI1/SSDA1 | | |
| 49 | | P94 | | MTIOC7A/ GTIOC5A | CTS1#/RTS1#/SS1# | | |
| 50 | | P93 | | MTIOC7B/ GTIOC6A | CTS2#/RTS2#/SS2# | | |
| 51 | | P92 | | MTIOC6D/GTIOC4B | | | |
| 52 | | P91 | | MTIOC7C/GTIOC5B | | | |
| 53 | | P90 | | MTIOC7D/GTIOC6B | | | |
| 54 | TRCLK | PG5 | | POE12# | SCK3 | | ADTRG# |
| 55 | TRDATA3 | PG4 | | GTIOC6B | RXD3/SMISO3/SSCL3 | IRQ6 | |
| 56 | TRDATA2 | PG3 | | GTIOC6A | TXD3/SMOSI3/SSDA3 | | |
| 57 | TRDATA1 | PG2 | | | SCK2 | IRQ2 | |
| 58 | TRDATA0 | PG1 | | GTIOC7B | RXD2/SMISO2/SSCL2 | IRQ1 | |
| 59 | TRSYNC | PG0 | | GTIOC7A | TXD2/SMOSI2/SSDA2 | IRQ0 | |
| 60 | | P76 | D0/[A0/D0] | MTIOC4D/GTIOC2B | | | |
| 61 | | P75 | D1/[A1/D1] | MTIOC4C/GTIOC1B | | | |
| 62 | | P74 | D2/[A2/D2] | MTIOC3D/GTIOC0B | | | |
| 63 | | P73 | D3/[A3/D3] | MTIOC4B/GTIOC2A | | | |
| 64 | | P72 | D4/[A4/D4] | MTIOC4A/GTIOC1A | | | |
| 65 | | P71 | D5/[A5/D5] | MTIOC3B/GTIOC0A | | | |
| 66 | | P70 | D6/[A6/D6] | POE0# | CTS1#/RTS1#/SS1# | IRQ5-DS | |
| 67 | | P33 | D7/[A7/D7] | MTIOC3A/MTCLKA | SSLA3/SSLB3 | | |
| 68 | | P32 | D8/[A8/D8] | MTIOC3C/MTCLKB | SSLA2/SSLB2 | | |
| 69 | VCC | | | | | | |
| 70 | | P31 | D9/[A9/D9] | MTIOC0A/MTCLKC | SSLA1/SSLB1 | | |
| 71 | VSS | | | | | | |
| 72 | | P30 | D10/[A10/ D10] | MTIOC0B/MTCLKD | SCK0/SSLA0/SSLB0 | | |
| 73 | | P24 | D11/[A11/D11] | | CTS0#/RTS0#/SS0#/ RSPCKA/RSPCKB | IRQ4 | |

# 2. CPU

The RX CPU has sixteen general-purpose registers, nine control registers, and one accumulator used for DSP instructions.

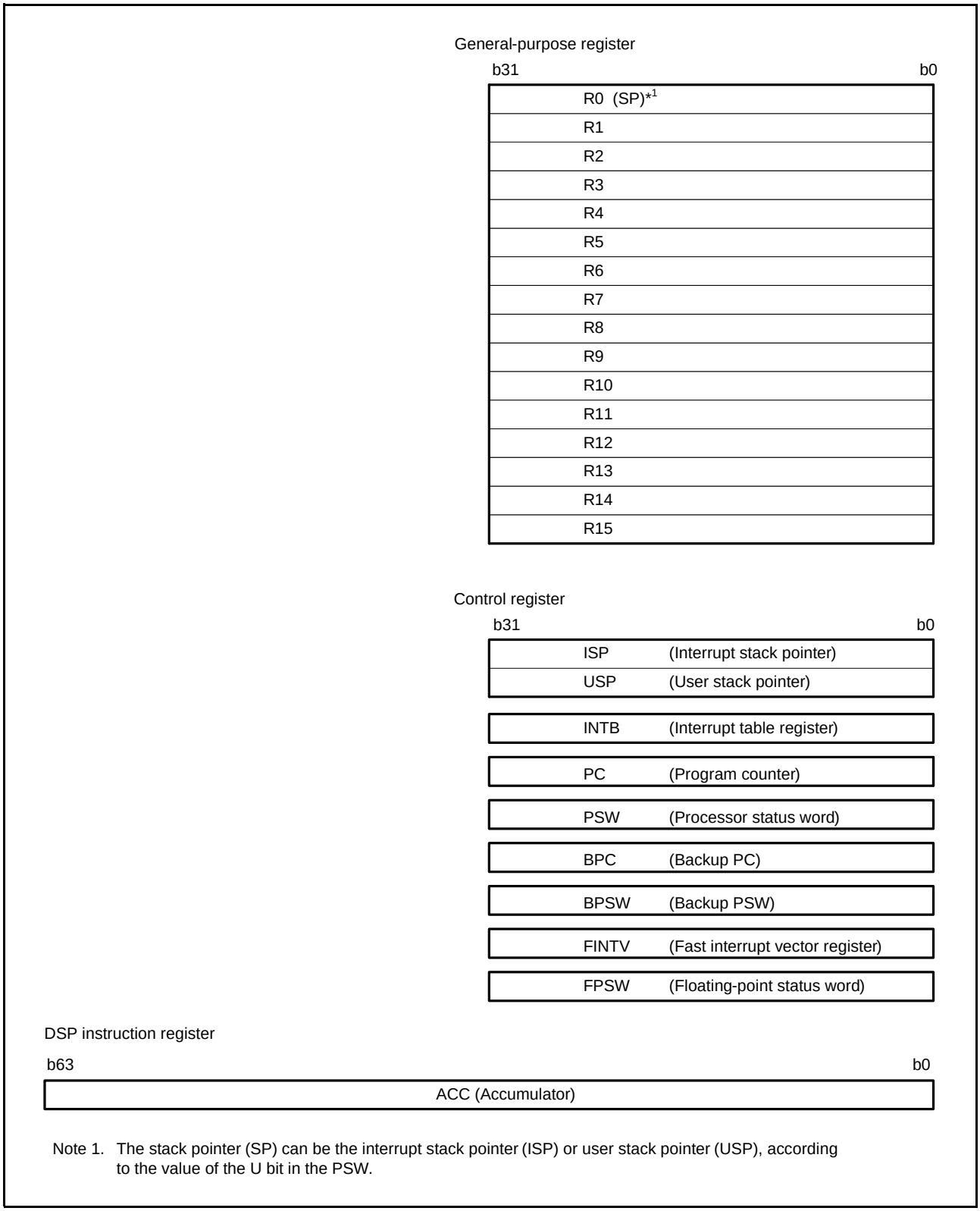



**Figure 2.1 Register Set of the CPU**

**Table 4.1 List of I/O Registers (Address Order) (20/48)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Module Name | Remarks |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | | |
| 0008 9873h | AD | A/D Sampling State Register 1 | ADSSTR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | AD | Not present in versions with 64 or 48 pins. |
| 0008 9874h | AD | A/D Sampling State Register 2 | ADSSTR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 64 or 48 pins. |
| 0008 9875h | AD | A/D Sampling State Register 3 | ADSSTR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 64 or 48 pins. |
| 0008 9876h | AD | A/D Sampling State Register 4 | ADSSTR4 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 64 or 48 pins. |
| 0008 9877h | AD | A/D Sampling State Register 5 | ADSSTR5 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 64 or 48 pins. |
| 0008 9878h | AD | A/D Sampling State Register 6 | ADSSTR6 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 64 or 48 pins. |
| 0008 9879h | AD | A/D Sampling State Register 7 | ADSSTR7 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 64 or 48 pins. |
| 0008 987Dh | AD | Digital Power Supply Control Circuit Output Register | ADDPCONR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 64, or 48 pins. |
| 0008 A000h | SCI0 | Serial Mode Register | SMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIc, SCId | |
| 0008 A001h | SCI0 | Bit Rate Register | BRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 A002h | SCI0 | Serial Control Register | SCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 A003h | SCI0 | Transmit Data Register | TDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 A004h | SCI0 | Serial Status Register | SSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 A005h | SCI0 | Receive Data Register | RDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 A006h | SCI0 | Smart Card Mode Register | SCMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 A007h | SCI0 | Serial Extended Mode Register | SEMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 A008h | SCI0 | Noise Filter Setting Register | SNFR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 A009h | SCI0 | $I^2C$ Mode Register 1 | SIMR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 A00Ah | SCI0 | $I^2C$ Mode Register 2 | SIMR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 A00Bh | SCI0 | $I^2C$ Mode Register 3 | SIMR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 A00Ch | SCI0 | $I^2C$ Status Register | SISR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 A00Dh | SCI0 | SPI Mode Register | SPMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 A020h | SCI1 | Serial Mode Register | SMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 A021h | SCI1 | Bit Rate Register | BRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 A022h | SCI1 | Serial Control Register | SCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 A023h | SCI1 | Transmit Data Register | TDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 A024h | SCI1 | Serial Status Register | SSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 A025h | SCI1 | Receive Data Register | RDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 A026h | SCI1 | Smart Card Mode Register | SCMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 A027h | SCI1 | Serial Extended Mode Register | SEMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 A028h | SCI1 | Noise Filter Setting Register | SNFR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 A029h | SCI1 | $I^2C$ Mode Register 1 | SIMR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 A02Ah | SCI1 | $I^2C$ Mode Register 2 | SIMR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 A02Bh | SCI1 | $I^2C$ Mode Register 3 | SIMR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 A02Ch | SCI1 | $I^2C$ Status Register | SISR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 A02Dh | SCI1 | SPI Mode Register | SPMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 A040h | SCI2 | Serial Mode Register | SMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 64 or 48 pins. |
| 0008 A041h | SCI2 | Bit Rate Register | BRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 64 or 48 pins. |
| 0008 A042h | SCI2 | Serial Control Register | SCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 64 or 48 pins. |
| 0008 A043h | SCI2 | Transmit Data Register | TDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 64 or 48 pins. |
| 0008 A044h | SCI2 | Serial Status Register | SSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 64 or 48 pins. |
| 0008 A045h | SCI2 | Receive Data Register | RDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 64 or 48 pins. |
| 0008 A046h | SCI2 | Smart Card Mode Register | SCMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 64 or 48 pins. |

**Table 4.1 List of I/O Registers (Address Order) (24/48)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Module Name | Remarks |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | | |
| 0008 C086h | PORT3 | Open Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports | Not present in versions with 144, 120, 112, or 100 pins. |
| 0008 C087h | PORT3 | Open Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 120, 112, 100, 64 or 48 pins. |
| 0008 C090h | PORT8 | Open Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 64 or 48 pins. |
| 0008 C092h | PORT9 | Open Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 144, 120, 112, 100 or 48 pins. |
| 0008 C093h | PORT9 | Open Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 48 pins. |
| 0008 C094h | PORTA | Open Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 64 or 48 pins. |
| 0008 C095h | PORTA | Open Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 64 or 48 pins. |
| 0008 C096h | PORTB | Open Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 C097h | PORTB | Open Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 C09Ah | PORTD | Open Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 C09Bh | PORTD | Open Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 C09Eh | PORTF | Open Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 100, 64, or 48 pins. |
| 0008 C0A0h | PORTG | Open Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 100, 64, or 48 pins. |
| 0008 C0A1h | PORTG | Open Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 100, 64, or 48 pins. |
| 0008 C0F2h | PORT | Driving Ability Control Register 1 | DSCR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 64 or 48 pins. |
| 0008 C0F3h | PORT | Driving Ability Control Register 2 | DSCR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 64 or 48 pins. |
| 0008 C100h | MPC | CS Output Enable Register | PFCSE | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC | Not present in versions with 64 or 48 pins. |
| 0008 C102h | MPC | CS Output Pin Select Register 0 | PFCSS0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 64 or 48 pins. |
| 0008 C104h | MPC | Address Output Enable Register 0 | PFAOE0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 64 or 48 pins. |
| 0008 C105h | MPC | Address Output Enable Register 1 | PFAOE1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 64 or 48 pins. |
| 0008 C106h | MPC | External Bus Control Register 0 | PFBCR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 64 or 48 pins. |
| 0008 C107h | MPC | External Bus Control Register 1 | PFBCR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 64 or 48 pins. |
| 0008 C114h | MPC | USB0 Control Register | PFUSB0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 112, 100, 64, or 48 pins. |
| 0008 C11Fh | MPC | Write-Protect Register | PWPR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 C140h | MPC | P00 Pin Function Control Register | P00PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 48 pins. |
| 0008 C141h | MPC | P01 Pin Function Control Register | P01PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 48 pins. |
| 0008 C142h | MPC | P02 Pin Function Control Register | P02PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 120, 112, 100, 64, or 48 pins. |
| 0008 C143h | MPC | P03 Pin Function Control Register | P03PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 120, 112, 100, 64, or 48 pins. |
| 0008 C148h | MPC | P10 Pin Function Control Register | P10PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 48 pins. |
| 0008 C149h | MPC | P11 Pin Function Control Register | P11PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 48 pins. |
| 0008 C14Ah | MPC | P12 Pin Function Control Register | P12PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 100, 64, or 48 pins. |
| 0008 C14Bh | MPC | P13 Pin Function Control Register | P13PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | Not present in versions with 112, 100, 64, or 48 pins. |

**Table 4.1 List of I/O Registers (Address Order) (39/48)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Module Name | Remarks |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | | |
| 000C 21A6h | GPT1 | A/D Converter Start Request Timing Buffer Register A | GTADTBRA | 16 | 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | GPT | |
| 000C 21A8h | GPT1 | A/D Converter Start Request Timing Double-Buffer Register A | GTADTDBRA | 16 | 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | |
| 000C 21ACh | GPT1 | A/D Converter Start Request Timing Register B | GTADTRB | 16 | 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | |
| 000C 21AEh | GPT1 | A/D Converter Start Request Timing Buffer Register B | GTADTBRB | 16 | 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | |
| 000C 21B0h | GPT1 | A/D Converter Start Request Timing Double-Buffer Register B | GTADTDBRB | 16 | 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | |
| 000C 21B4h | GPT1 | General PWM Timer Output Negate Control Register | GTONCR | 16 | 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | |
| 000C 21B6h | GPT1 | General PWM Timer Dead Time Control Register | GTDTCR | 16 | 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | |
| 000C 21B8h | GPT1 | General PWM Timer Dead Time Value Register U | GTDVU | 16 | 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | |
| 000C 21BAh | GPT1 | General PWM Timer Dead Time Value Register D | GTDVD | 16 | 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | |
| 000C 21BCh | GPT1 | General PWM Timer Dead Time Buffer Register U | GTDBU | 16 | 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | |
| 000C 21BEh | GPT1 | General PWM Timer Dead Time Buffer Register D | GTDBD | 16 | 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | |
| 000C 21C0h | GPT1 | General PWM Timer Output Protection Function Status Register | GTSOS | 16 | 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | |
| 000C 21C2h | GPT1 | General PWM Timer Output Protection Function Temporary Release Register | GTSOTR | 16 | 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | |
| 000C 2200h | GPT2 | General PWM Timer I/O Control Register | GTIOR | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | |
| 000C 2202h | GPT2 | General PWM Timer Interrupt Output Setting Register | GTINTAD | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | |
| 000C 2204h | GPT2 | General PWM Timer Control Register | GTCR | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | |
| 000C 2206h | GPT2 | General PWM Timer Buffer Enable Register | GTBER | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | |
| 000C 2208h | GPT2 | General PWM Timer Count Direction Register | GTUDC | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | |
| 000C 220Ah | GPT2 | General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register | GTITC | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | |
| 000C 220Ch | GPT2 | General PWM Timer Status Register | GTST | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | |
| 000C 220Eh | GPT2 | General PWM Timer Counter | GTCNT | 16 | 16 | 2 to 5 PCLKA | 2, 3 ICLK | | |
| 000C 2210h | GPT2 | General PWM Timer Compare Capture Register A | GTCCRA | 16 | 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | |
| 000C 2212h | GPT2 | General PWM Timer Compare Capture Register B | GTCCRB | 16 | 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | |
| 000C 2214h | GPT2 | General PWM Timer Compare Capture Register C | GTCCRC | 16 | 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | |
| 000C 2216h | GPT2 | General PWM Timer Compare Capture Register D | GTCCRD | 16 | 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | |
| 000C 2218h | GPT2 | General PWM Timer Compare Capture Register E | GTCCRE | 16 | 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | |
| 000C 221Ah | GPT2 | General PWM Timer Compare Capture Register F | GTCCRF | 16 | 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | |
| 000C 221Ch | GPT2 | General PWM Timer Cycle Setting Register | GTPR | 16 | 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | |
| 000C 221Eh | GPT2 | General PWM Timer Cycle Setting Buffer Register | GTPBR | 16 | 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | |
| 000C 2220h | GPT2 | General PWM Timer Cycle Setting Double-Buffer Register | GTPDBR | 16 | 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | |
| 000C 2224h | GPT2 | A/D Converter Start Request Timing Register A | GTADTRA | 16 | 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | |
| 000C 2226h | GPT2 | A/D Converter Start Request Timing Buffer Register A | GTADTBRA | 16 | 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | |
| 000C 2228h | GPT2 | A/D Converter Start Request Timing Double-Buffer Register A | GTADTDBRA | 16 | 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | |
| 000C 222Ch | GPT2 | A/D Converter Start Request Timing Register B | GTADTRB | 16 | 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | |
| 000C 222Eh | GPT2 | A/D Converter Start Request Timing Buffer Register B | GTADTBRB | 16 | 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | |

**Table 4.1 List of I/O Registers (Address Order) (45/48)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Module Name | Remarks |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | | |
| 000C 2A24h | GPT6 | A/D Converter Start Request Timing Register A | GTADTRA | 16 | 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | GPT | Not present in versions with 64 or 48 pins. |
| 000C 2A26h | GPT6 | A/D Converter Start Request Timing Buffer Register A | GTADTBRA | 16 | 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 2A28h | GPT6 | A/D Converter Start Request Timing Double-Buffer Register A | GTADTDBRA | 16 | 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 2A2Ch | GPT6 | A/D Converter Start Request Timing Register B | GTADTRB | 16 | 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 2A2Eh | GPT6 | A/D Converter Start Request Timing Buffer Register B | GTADTBRB | 16 | 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 2A30h | GPT6 | A/D Converter Start Request Timing Double-Buffer Register B | GTADTDBRB | 16 | 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 2A34h | GPT6 | General PWM Timer Output Negate Control Register | GTONCR | 16 | 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 2A36h | GPT6 | General PWM Timer Dead Time Control Register | GTDTCR | 16 | 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 2A38h | GPT6 | General PWM Timer Dead Time Value Register U | GTDVU | 16 | 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 2A3Ah | GPT6 | General PWM Timer Dead Time Value Register D | GTDVD | 16 | 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 2A3Ch | GPT6 | General PWM Timer Dead Time Buffer Register U | GTDBU | 16 | 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 2A3Eh | GPT6 | General PWM Timer Dead Time Buffer Register D | GTDBD | 16 | 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 2A40h | GPT6 | General PWM Timer Output Protection Function Status Register | GTSOS | 16 | 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 2A42h | GPT6 | General PWM Timer Output Protection Function Temporary Release Register | GTSOTR | 16 | 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 2A80h | GPT7 | General PWM Timer I/O Control Register | GTIOR | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 2A82h | GPT7 | General PWM Timer Interrupt Output Setting Register | GTINTAD | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 2A84h | GPT7 | General PWM Timer Control Register | GTCR | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 2A86h | GPT7 | General PWM Timer Buffer Enable Register | GTBER | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 2A88h | GPT7 | General PWM Timer Count Direction Register | GTUDC | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 2A8Ah | GPT7 | General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register | GTITC | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 2A8Ch | GPT7 | General PWM Timer Status Register | GTST | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 2A8Eh | GPT7 | General PWM Timer Counter | GTCNT | 16 | 16 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 2A90h | GPT7 | General PWM Timer Compare Capture Register A | GTCCRA | 16 | 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 2A92h | GPT7 | General PWM Timer Compare Capture Register B | GTCCRB | 16 | 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 2A94h | GPT7 | General PWM Timer Compare Capture Register C | GTCCRC | 16 | 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 2A96h | GPT7 | General PWM Timer Compare Capture Register D | GTCCRD | 16 | 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 2A98h | GPT7 | General PWM Timer Compare Capture Register E | GTCCRE | 16 | 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 2A9Ah | GPT7 | General PWM Timer Compare Capture Register F | GTCCRF | 16 | 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 2A9Ch | GPT7 | General PWM Timer Cycle Setting Register | GTPR | 16 | 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 2A9Eh | GPT7 | General PWM Timer Cycle Setting Buffer Register | GTPBR | 16 | 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 2AA0h | GPT7 | General PWM Timer Cycle Setting Double-Buffer Register | GTPDBR | 16 | 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 2AA4h | GPT7 | A/D Converter Start Request Timing Register A | GTADTRA | 16 | 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 2AA6h | GPT7 | A/D Converter Start Request Timing Buffer Register A | GTADTBRA | 16 | 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |

**Table 4.1 List of I/O Registers (Address Order) (48/48)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Module Name | Remarks |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | | |
| 007F FFB0h | FLASH | Flash Status Register 0 | FSTATR0 | 8 | 8 | 2, 3 FCLK | 2, 3 ICLK | ROM | |
| 007F FFB1h | FLASH | Flash Status Register 1 | FSTATR1 | 8 | 8 | 2, 3 FCLK | 2, 3 ICLK | | |
| 007F FFB2h | FLASH | Flash P/E Mode Entry Register | FENTRYR | 16 | 16 | 2, 3 FCLK | 2, 3 ICLK | ROM/ E2 DataFlash Memory | |
| 007F FFB4h | FLASH | Flash Protection Register | FPROTR | 16 | 16 | 2, 3 FCLK | 2, 3 ICLK | ROM | |
| 007F FFB6h | FLASH | Flash Reset Register | FRESETR | 16 | 16 | 2, 3 FCLK | 2, 3 ICLK | | |
| 007F FFBAh | FLASH | FCU Command Register | FCMDR | 16 | 16 | 2, 3 FCLK | 2, 3 ICLK | | |
| 007F FFC8h | FLASH | FCU Processing Switching Register | FCPSR | 16 | 16 | 2, 3 FCLK | 2, 3 ICLK | | |
| 007F FFCAh | FLASH | E2 DataFlash Blank Check Control Register | DFLBCCNT | 16 | 16 | 2, 3 FCLK | 2, 3 ICLK | E2 DataFlash Memory | |
| 007F FFCCh | FLASH | Flash P/E Status Register | FPESTAT | 16 | 16 | 2, 3 FCLK | 2, 3 ICLK | ROM | |
| 007F FFCEh | FLASH | E2 DataFlash Blank Check Status Register | DFLBCSTAT | 16 | 16 | 2, 3 FCLK | 2, 3 ICLK | E2 DataFlash Memory | |
| 007F FFE8h | FLASH | Peripheral Clock Notification Register | PCKAR | 16 | 16 | 2, 3 FCLK | 2, 3 ICLK | ROM | |

Note: • This table shows the maximum specifications of I/O registers. The I/O registers of individual products correspond to the list of functions given as Table 1.2. For details, refer to Table 1.2, Comparison of Functions for Different Packages.
Note 1. When the register is accessed while the USB is operating, a delay may be generated in accessing.
Note 2. Odd addresses are not accessible in 16-bit units. Obtain 16-bit access to the two registers by access to the address of TMOCNTL.
Note 3. Pins USB0 and RIIC1 are not present in 112-pin products.
Note 4. Pins USB0, RIIC1, and SCI3 are not present in 100-pin products.
Note 5. Pins GPT4 to GPT7, USB0, RSPI1, RIIC1, SCI2, SCI3, CAN1, AD, and S12AD1 are not present in 64- and 48-pin products.

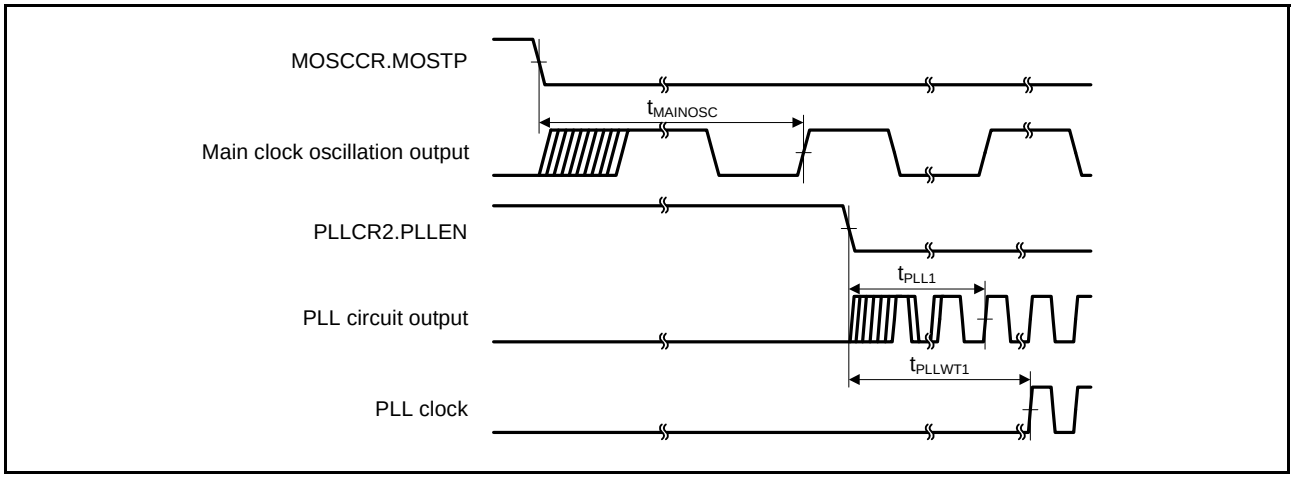



**Figure 5.7 PLL Clock Oscillation Start Timing (PLL is Operated after Main Clock Oscillation Has Settled)**

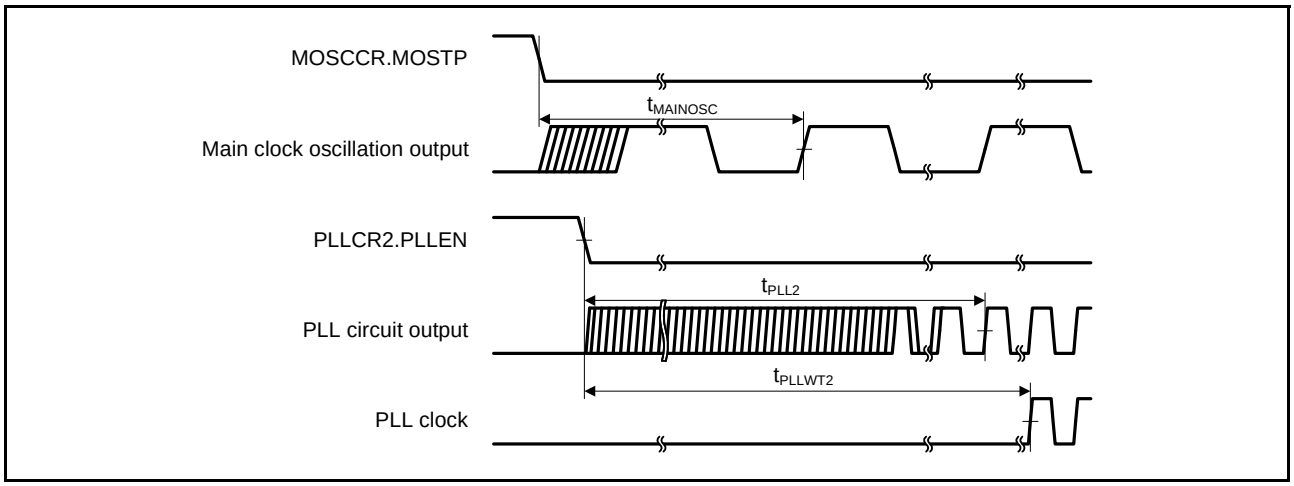



**Figure 5.8 PLL Clock Oscillation Start Timing (PLL is Operated before Main Clock Oscillation Has Settled)**

## 5.3.5 Bus Timing

**Table 5.12 Bus Timing (1)**

Condition: VCC = PLLVCC = VCC_USB = AVCC0 = AVCC = 3.0 to 3.6 V,
VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC
$T_a = T_{opr}$
Output load conditions: $V_{OH}$ = VCC x 0.5, $V_{OL}$ = VCC x 0.5, $I_{OH}$ = –1.0 mA, $I_{OL}$ = 1.0 mA, C = 30 pF

| Item | Symbol | Min. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|
| Address delay time | $t_{AD}$ | — | 30 | ns | Figure 5.13 to Figure 5.16 |
| Byte control delay time | $t_{BCD}$ | — | 30 | ns | |
| CS# delay time | $t_{CSD}$ | — | 30 | ns | |
| RD# delay time | $t_{RSD}$ | — | 30 | ns | |
| Read data setup time | $t_{RDS}$ | 20 | — | ns | |
| Read data hold time | $t_{RDH}$ | 0 | — | ns | |
| WR# delay time | $t_{WRD}$ | — | 30 | ns | |
| Write data delay time | $t_{WDD}$ | — | 35 | ns | |
| Write data hold time | $t_{WDH}$ | 0 | — | ns | |
| WAIT# setup time | $t_{WTS}$ | 20 | — | ns | Figure 5.17 |
| WAIT# hold time | $t_{WTH}$ | 0 | — | ns | |

**Table 5.13 Bus Timing (2)**

Condition: VCC = PLLVCC = AVCC0 = AVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V,
VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
$T_a = T_{opr}$
Output load conditions: $V_{OH}$ = VCC x 0.5, $V_{OL}$ = VCC x 0.5, $I_{OH}$ = –1.0 mA, $I_{OL}$ = 1.0 mA, C = 30 pF

| Item | Symbol | Min. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|
| Address delay time | $t_{AD}$ | — | 15 | ns | Figure 5.13 to Figure 5.16 |
| Byte control delay time | $t_{BCD}$ | — | 15 | ns | |
| CS# delay time | $t_{CSD}$ | — | 15 | ns | |
| RD# delay time | $t_{RSD}$ | — | 15 | ns | |
| Read data setup time | $t_{RDS}$ | 15 | — | ns | |
| Read data hold time | $t_{RDH}$ | 0 | — | ns | |
| WR# delay time | $t_{WRD}$ | — | 15 | ns | |
| Write data delay time | $t_{WDD}$ | — | 15 | ns | |
| Write data hold time | $t_{WDH}$ | 0 | — | ns | |
| WAIT# setup time | $t_{WTS}$ | 15 | — | ns | Figure 5.17 |
| WAIT# hold time | $t_{WTH}$ | 0 | — | ns | |

### Table 5.16 Timing of On-Chip Peripheral Modules (3)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS =PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. $T_a$ is common to conditions 1 to 3.

High drive output is selected by the drive capacity control register.

| Item | | | | Symbol | Min. | Max. | Unit*1 | Test Conditions |
|---|---|---|---|---|---|---|---|---|
| RSPI | RSPCK clock cycle | Master | | $t_{SPcyc}$ | 2 | 4096 | $t_{Pcyc}$ | C = 30 pF, Figure 5.32 |
| | | Slave | | | 8 | 4096 | | |
| | RSPCK clock high pulse width | Master | | $t_{SPCKWH}$ | $(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2 - 3$ | — | ns | |
| | | Slave | | | $(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2$ | — | | |
| | RSPCK clock low pulse width | Master | | $t_{SPCKWL}$ | $(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2 - 3$ | — | ns | |
| | | Slave | | | $(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2$ | — | | |
| | RSPCK clock rise/fall time | Output | | $t_{SPCKR}$, $t_{SPCKF}$ | — | 5 | ns | |
| | | Input | | | — | 1 | µs | |
| | RSPCK clock fall time | Input | | $t_{SPCKF}$ | — | 0.1 | µs/V | |
| | Data input setup time | Master | | $t_{SU}$ | 4 | — | ns | C = 30 pF, Figure 5.33 to Figure 5.40 |
| | | Slave | | | $20 - t_{Pcyc}$ | — | | |
| | Data input hold time | Master | PCLKB division ratio set to a value other than 1/2 | $t_H$ | $t_{Pcyc}$ | — | ns | |
| | | | PCLKB division ratio set to 1/2 | $t_{HF}$ | 0 | — | | |
| | | Slave | | $t_H$ | $20 + 2 \times t_{Pcyc}$ | — | | |
| | SSL setup time | Master | | $t_{LEAD}$ | 1 | 8 | $t_{SPcyc}$ | |
| | | Slave | | | 4 | — | $t_{Pcyc}$ | |
| | SSL hold time | Master | | $t_{LAG}$ | 1 | 8 | $t_{SPcyc}$ | |
| | | Slave | | | 4 | — | $t_{Pcyc}$ | |
| | Data output delay time | Master | | $t_{OD}$ | — | 10 | ns | |
| | | Slave | | | — | $3 \times t_{Pcyc} + 40$ | | |
| | Data output hold time | Master | | $t_{OH}$ | 0 | — | ns | |
| | | Slave | | | 0 | — | | |
| | Successive transmission delay time | Master | | $t_{TD}$ | $t_{SPcyc} + 2 \times t_{Pcyc}$ | $8 \times t_{SPcyc} + 2 \times t_{Pcyc}$ | ns | |
| | | Slave | | | $4 \times t_{Pcyc}$ | — | | |
| | MOSI and MISO rise/fall time | Output | | $t_{DR}$, $t_{DF}$ | — | 5 | ns | |
| | | Input | | | — | 1 | µs | |
| | SSL rise/fall time | Output | | $t_{SSLr}$, $t_{SSLf}$ | — | 15 | ns | |
| | | Input | | | — | 1 | µs | |
| | Slave access time | | | $t_{SA}$ | — | 4 | $t_{Pcyc}$ | Figure 5.39 and Figure 5.40 |
| | Slave output release time | | | $t_{REL}$ | — | 3 | $t_{Pcyc}$ | |

Note 1. $t_{Pcyc}$: PCLK cycle

### Table 5.16 Timing of On-Chip Peripheral Modules (5)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. $T_a$ is common to conditions 1 to 3.

| Item | | Symbol | Min.*1,*2 | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| RIIC (Standard-mode) | SCL input cycle time | $t_{SCL}$ | $6(12) \times t_{IICcyc} + 1300$ | — | ns | Figure 5.36 |
| | SCL input high pulse width | $t_{SCLH}$ | $3(6) \times t_{IICcyc} + 300$ | — | ns | |
| | SCL input low pulse width | $t_{SCLL}$ | $3(6) \times t_{IICcyc} + 300$ | — | ns | |
| | SCL, SDA input rise time | $t_{Sr}$ | — | 1000 | ns | |
| | SCL, SDA input fall time | $t_{Sf}$ | — | 300 | ns | |
| | SCL, SDA input spike pulse removal time | $t_{SP}$ | 0 | $1(4) \times t_{IICcyc}$ | ns | |
| | SDA input bus free time | $t_{BUF}$ | $3(6) \times t_{IICcyc} + 300$ | — | ns | |
| | Start condition input hold time | $t_{STAH}$ | $t_{IICcyc} + 300$ | — | ns | |
| | Restart condition input setup time | $t_{STAS}$ | 1000 | — | ns | |
| | Stop condition input setup time | $t_{STOS}$ | 1000 | — | ns | |
| | Data input setup time | $t_{SDAS}$ | $t_{IICcyc} + 50$ | — | ns | |
| | Data input hold time | $t_{SDAH}$ | 0 | — | ns | |
| | SCL, SDA capacitive load | $C_b$ | — | 400 | pF | |
| RIIC (Fast-mode) | SCL input cycle time | $t_{SCL}$ | $6(12) \times t_{IICcyc} + 600$ | — | ns | |
| | SCL input high pulse width | $t_{SCLH}$ | $3(6) \times t_{IICcyc} + 300$ | — | ns | |
| | SCL input low pulse width | $t_{SCLL}$ | $3(6) \times t_{IICcyc} + 300$ | — | ns | |
| | SCL, SDA input rise time | $t_{Sr}$ | $20 + 0.1C_b$ | 300 | ns | |
| | SCL, SDA input fall time | $t_{Sf}$ | $20 + 0.1C_b$ | 300 | ns | |
| | SCL, SDA input spike pulse removal time | $t_{SP}$ | 0 | $1(4) \times t_{IICcyc}$ | ns | |
| | SDA input bus free time | $t_{BUF}$ | $3(6) \times t_{IICcyc} + 300$ | — | ns | |
| | Start condition input hold time | $t_{STAH}$ | $t_{IICcyc} + 300$ | — | ns | |
| | Restart condition input setup time | $t_{STAS}$ | 300 | — | ns | |
| | Stop condition input setup time | $t_{STOS}$ | 300 | — | ns | |
| | Data input setup time | $t_{SDAS}$ | $t_{IICcyc} + 50$ | — | ns | |
| | Data input hold time | $t_{SDAH}$ | 0 | — | ns | |
| | SCL, SDA capacitive load | $C_b$ | — | 400 | pF | |

Note: • $t_{IICcyc}$: RIIC internal reference clock (IICϕ) cycle

Note 1. The value within parentheses is applicable when the value of the ICMR3.NF[1:0] bits is 11b while the digital filter is enabled by the setting ICFER.NFE = 1.

Note 2. Cb is the total capacitance of the bus lines.

## 5.5 A/D Conversion Characteristics

### Table 5.19 10-Bit A/D Conversion Characteristics (1)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. $T_a$ is common to conditions 1 to 3.

| Item | | | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Resolution | | | 10 | 10 | 10 | Bit | |
| Conversion time*1 (Operation at ADCLK = 100 MHz) | With 0.1-µF external capacitor | AN0 to AN7 | 0.5 | — | — | µs | Sampling in 25 states |
| | | Other channels | 0.75 | — | — | µs | Sampling in 50 states |
| | Without 0.1-µF external capacitor Permissible signal source impedance (max.) = 1 kΩ | AN0 to AN7 | 0.6 | — | — | µs | Sampling in 35 states |
| | | Other channels | 0.75 | — | — | µs | Sampling in 50 states |
| Analog input capacitance | | | — | — | 6 | pF | |
| Integral nonlinearity error | | | — | — | ±3.0 | LSB | |
| Offset error | | | — | — | ±2.0 | LSB | |
| Full-scale error | | | — | — | ±3.0 | LSB | |
| Quantization error | | | — | ±0.5 | — | LSB | |
| Absolute accuracy | | | — | — | ±6.0 | LSB | |

Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

## 6.3 AC Characteristics

### Table 6.6 Operation Frequency Value

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = $T_{opr}$

| Item | | Symbol | Min. | Typ | Max. | Unit |
|---|---|---|---|---|---|---|
| Operation frequency | System clock (ICLK) | f | — | — | 100 | MHz |
| | Peripheral module clock PCLK | | — | — | 50 | |
| | Timer module clock (PCLKA) | | — | — | 100 | |
| | S12AD clock (PCLKD) | | — | — | 50 | |
| | Flash clock (FCLK) | | —*1 | — | 50 | |

Note 1. The FCLK must run at a frequency of at least 4 MHz when changing the ROM or E2 DataFlash memory contents.

### 6.3.1 Clock Timing

### Table 6.7 Clock Timing

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = $T_{opr}$

| Item | | Symbol | Min | Typ | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| EXTAL external clock input cycle time | | $t_{EXcyc}$ | 50 | — | — | ns | Figure 6.1 |
| EXTAL external clock input high pulse width | | $t_{EXH}$ | 20 | — | — | ns | |
| EXTAL external clock input low pulse width | | $t_{EXL}$ | 20 | — | — | ns | |
| EXTAL external clock rising time | | $t_{EXr}$ | — | — | 5 | ns | |
| EXTAL external clock falling time | | $t_{EXf}$ | — | — | 5 | ns | |
| EXTAL external clock input wait time*1 | | $t_{EXWT}$ | 1 | — | — | ms | |
| Main clock oscillator oscillation frequency | | $f_{MAIN}$ | 4 | — | 16 | MHz | |
| Main clock oscillation stabilization time (crystal) | | $t_{MAINOSC}$ | — | — | —*2 | ms | Figure 6.2 |
| Main clock oscillation stabilization wait time (crystal) | | $t_{MAINOSCWT}$ | — | — | —*3 | ms | |
| LOCO, IWDTCLK clock cycle time | | $t_{cyc}$ | 6.96 | 8 | 9.4 | µs | |
| LOCO, IWDTCLK clock oscillation frequency | | $f_{LOCO}$ | 106.25 | 125 | 143.75 | kHz | |
| LOCO, IWDTCLK clock oscillation stabilization wait time | | $t_{LOCOWT}$ | — | — | 20 | µs | Figure 6.2 |
| PLL clock oscillation stabilization time | PLL operation started after main clock oscillation has settled | $t_{PLL1}$ | — | — | 500 | µs | Figure 6.4 |
| PLL clock oscillation stabilization wait time | | $t_{PLLWT1}$ | — | — | —*4 | ms | |
| PLL clock oscillation stabilization time PLL | PLL operation started before main clock oscillation has settled | $t_{PLL2}$ | — | — | $t_{MAINOSC}$ + $t_{PLL1}$ | ms | Figure 6.5 |
| PLL clock oscillation stabilization wait time | | $t_{PLLWT2}$ | — | — | —*4 | ms | |

Note 1. This is the time until the clock is used after clearing the main clock oscillator stop bit (MOSCCR.MOSTP) to 0 (selecting operation).
Note 2. When using a main clock, ask the manufacturer of the oscillator to evaluate its oscillation. Refer to the results of evaluation provided by the manufacturer for the oscillation stabilization time.
Note 3. This is calculated from the formula below, where n is the number of cycles set by the MOSCWTCR.MSTS[4:0] bits.

$$t_{MAINOSCWT} = t_{MAINOSC} + \frac{n + 16384}{f_{MAIN}}$$

### 6.3.3 Timing of Recovery from Low Power Consumption Modes

**Table 6.9 Timing of Recovery from Low Power Consumption Modes**

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = $T_{opr}$

| Item | | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|
| Recovery time after cancellation of software standby mode | Crystal resonator connected to main clock oscillator | Main clock oscillator operating | $t_{SBYMC}$ | 10 | — | — | ms | Figure 6.8 |
| | | Main clock oscillator and PLL circuit operating | $t_{SBYPC}$ | 10 | — | — | ms | |
| | External clock input to main clock oscillator | Main clock oscillator operating | $t_{SBYEX}$ | 1 | — | — | ms | |
| | | Main clock oscillator and PLL circuit operating | $t_{SBYPE}$ | 1 | — | — | ms | |
| | Low-speed clock oscillator or IWDT-specific low-speed clock oscillator operating | | $t_{SBYLO}$ | — | — | 800 | µs | |
| Recovery time after cancellation of deep software standby mode | | | $t_{DSBY}$ | — | — | 1 | ms | Figure 6.9 |
| Wait time after cancellation of deep software standby mode | | | $t_{DSBYWT}$ | 45 | — | 46 | $t_{cyc}$ | |

Note: • The wait time varies depending on the state in which each oscillator was when the WAIT instruction was executed. The recovery time when multiple oscillators are operating is the same period as that when the oscillator, which takes the longest time for recovery among the operating oscillators, is operating alone.

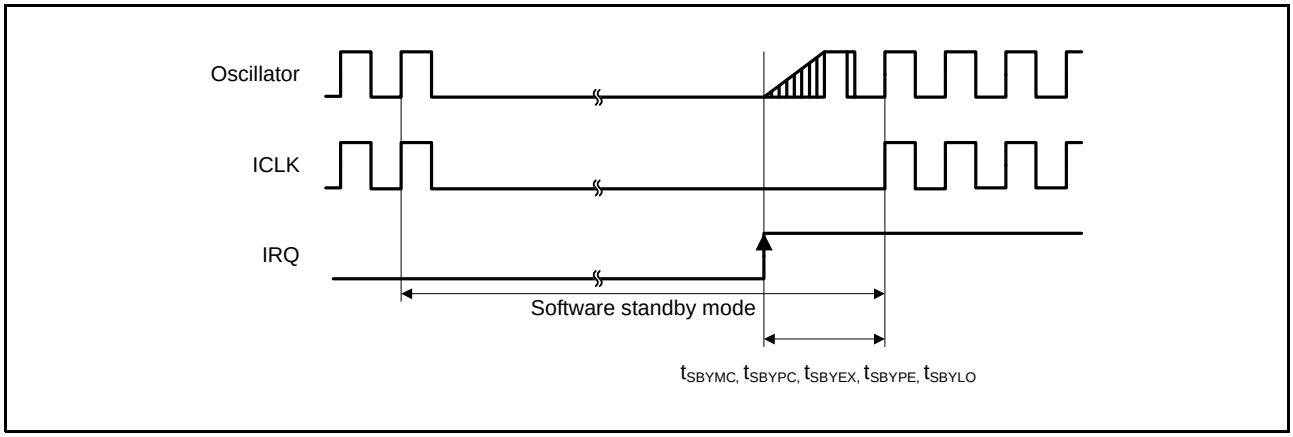



**Figure 6.8 Software Standby Mode Cancellation Timing**

**Table 6.12 Timing of On-Chip Peripheral Modules (2)**

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = $T_{opr}$

| Item | | | Symbol | Min. | Max. | Unit*1 | Test Conditions |
|---|---|---|---|---|---|---|---|
| RSPI | RSPCK clock cycle | Master | $t_{SPcyc}$ | 2 | 4096 | $t_{Pcyc}$ | Figure 6.20 |
| | | Slave | | 8 | 4096 | | |
| | RSPCK clock high pulse width | Master | $t_{SPCKWH}$ | $(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2 - 3$ | — | ns | |
| | | Slave | | $(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2$ | — | | |
| | RSPCK clock low pulse width | Master | $t_{SPCKWL}$ | $(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2 - 3$ | — | ns | |
| | | Slave | | $(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2$ | — | | |
| | RSPCK clock rise/fall time | Output | $t_{SPCKR}$, $t_{SPCKF}$ | — | 5 | ns | |
| | | Input | | — | 1 | µs | |
| | Data input setup time | Master | $t_{SU}$ | 15 | — | ns | Figure 6.21 to Figure 6.24 |
| | | | | 20 | — | | |
| | | Slave | | $20 - t_{Pcyc}$ | — | | |
| | Data input hold time | Master | $t_H$ | 0 | — | ns | |
| | | Slave | | $20 + 2 \times t_{Pcyc}$ | — | | |
| | SSL setup time | Master | $t_{LEAD}$ | 1 | 8 | $t_{SPcyc}$ | |
| | | Slave | | 4 | — | $t_{Pcyc}$ | |
| | SSL hold time | Master | $t_{LAG}$ | 1 | 8 | $t_{SPcyc}$ | |
| | | Slave | | 4 | — | $t_{Pcyc}$ | |
| | Data output delay time | Master | $t_{OD}$ | — | 18 | ns | |
| | | Slave | | — | $3 \times t_{Pcyc} + 40$ | | |
| | Data output hold time | Master | $t_{OH}$ | 0 | — | ns | |
| | | Slave | | 0 | — | | |
| | Successive transmission delay time | Master | $t_{TD}$ | $t_{SPcyc} + 2 \times t_{Pcyc}$ | $8 \times t_{SPcyc} + 2 \times t_{Pcyc}$ | ns | |
| | | Slave | | $4 \times t_{Pcyc}$ | — | | |
| | MOSI rise/fall time | Output | $t_{MODR}$, $t_{MODF}$ | — | 5 | ns | |
| | | Input | | — | 1 | µs | |
| | MISO rise/fall time | Output | $t_{MODR}$, $t_{MODF}$ | — | 5 | ns | |
| | | Input | | — | 1 | µs | |
| | SSL rise/fall time | Output | $t_{SSLr}$, $t_{SSLf}$ | — | 15 | ns | |
| | | Input | | — | 1 | µs | |
| | Slave access time | | $t_{SA}$ | — | 4 | $t_{Pcyc}$ | Figure 6.23 and Figure 6.24 |
| | Slave output release time | | $t_{REL}$ | — | 3 | $t_{Pcyc}$ | |

Note 1. $t_{Pcyc}$: PCLK cycle

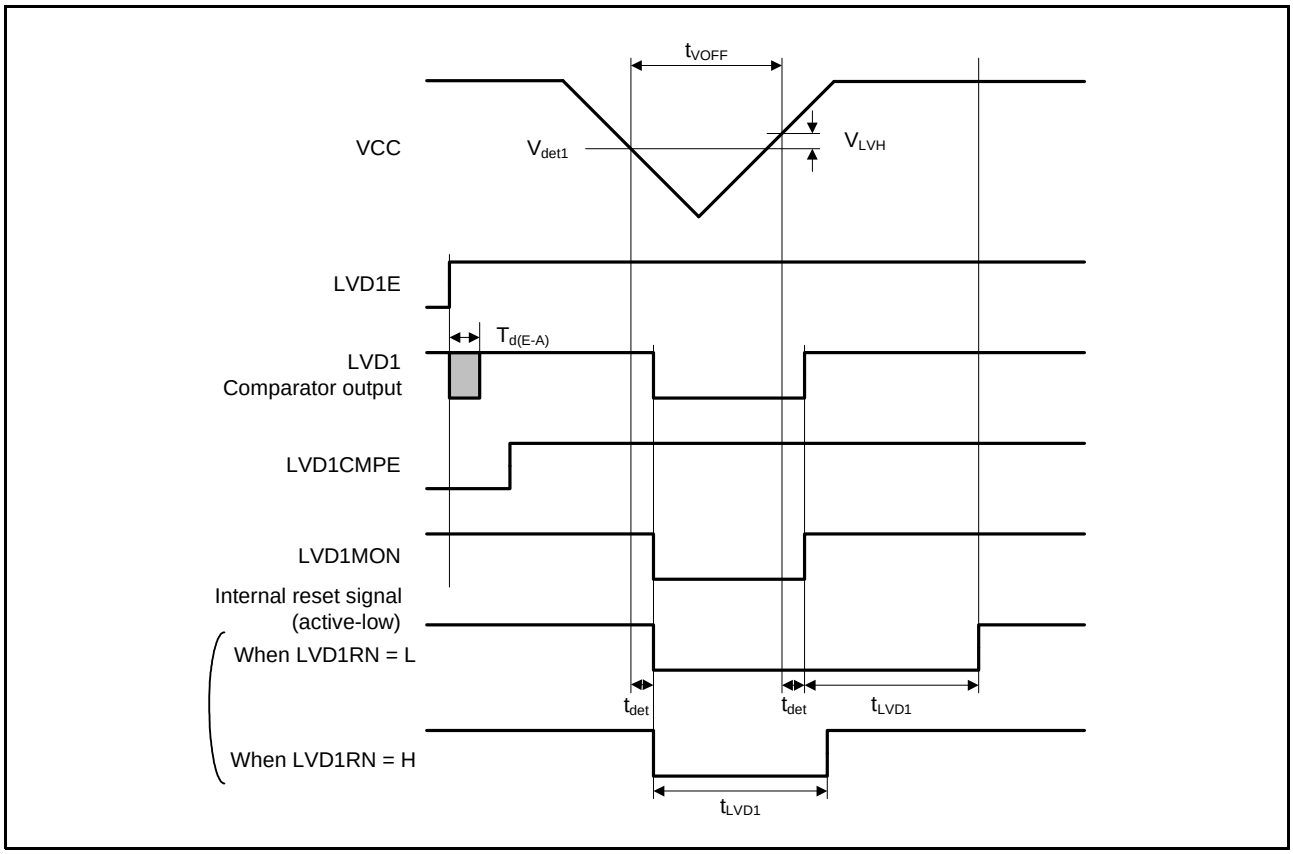



**Figure 6.28 Voltage Detection Circuit Timing ($V_{det1}$)**

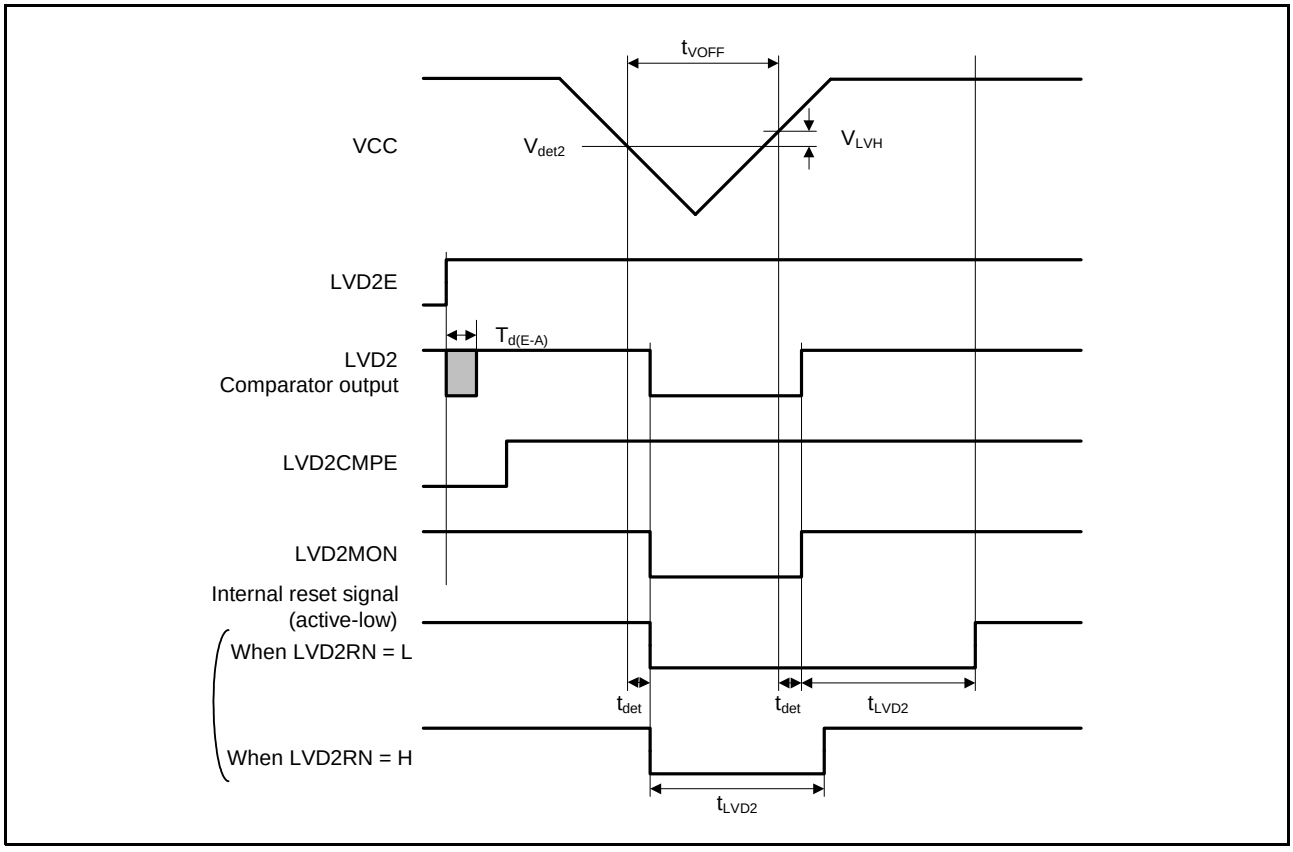



**Figure 6.29 Voltage Detection Circuit Timing ($V_{det2}$)**