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Details

Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	81
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 20x10b, 8x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f563tebdfb-v0

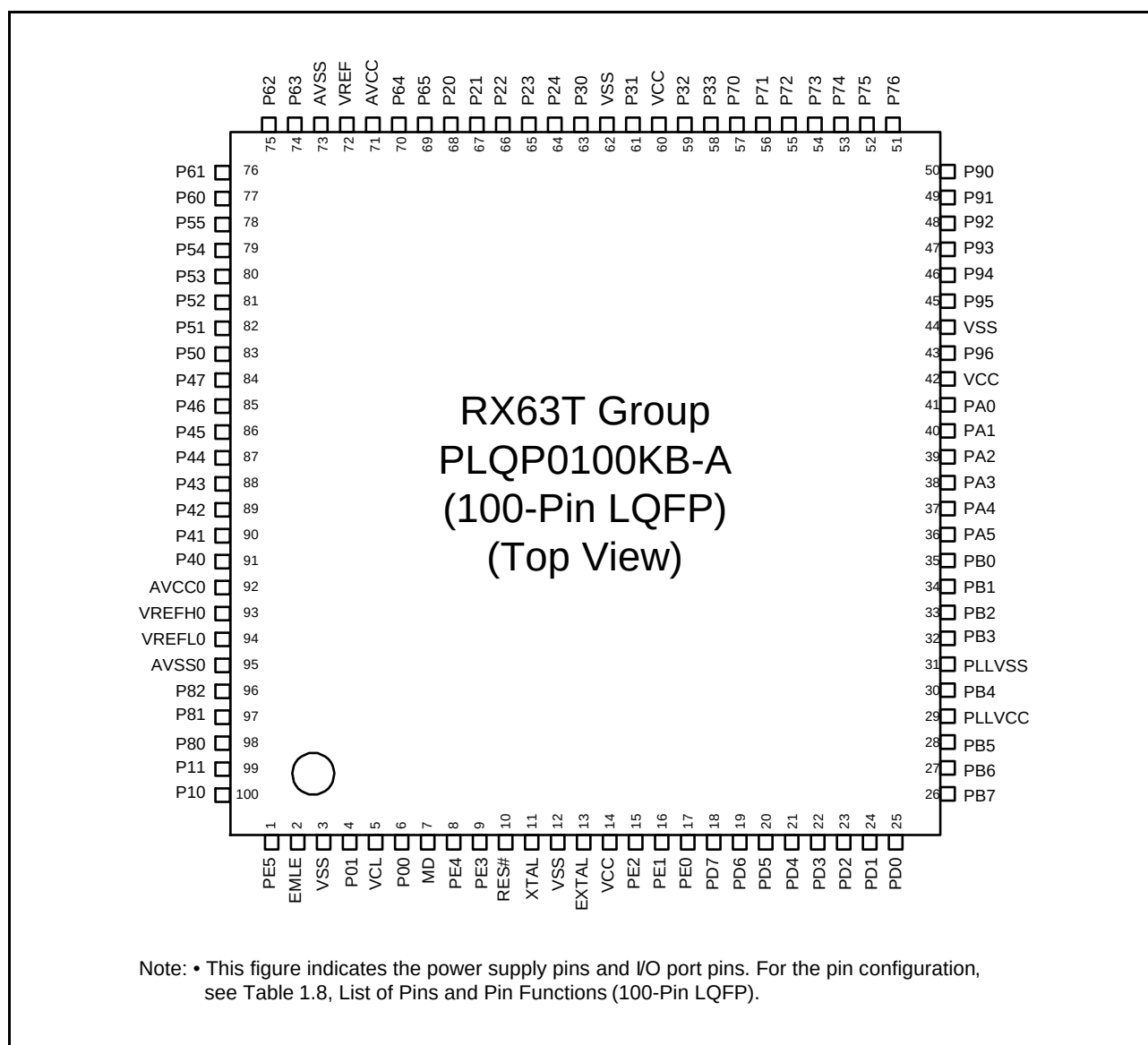


Figure 1.6 Pin Assignment (100-Pin LQFP)

Table 1.7 List of Pins and Pin Functions (112-Pin LQFP) (1/4)

Pin Number 112-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3, GPT, POE3, CAC)	Communications (SCIc, SCId, RSPI, RIIC, CAN)	Interrupt	S12ADB, AD, DA
1		PE5	BCLK			IRQ0	
2	EMLE						
3	VSS						
4		P01	RD#		CTS0#/RTS0#/SS0#		
5	VCL						
6		P00	CS1#	CACREF			
7	MD/FINED						
8		PE4	A10	POE10#/MTCLKC		IRQ1	
9		PE3	A11	POE11#/MTCLKD		IRQ2-DS	
10	RES#						
11	XTAL						
12	VSS						
13	EXTAL						
14	VCC						
15		PE2		POE10#		NMI	
16		PE1	WR0#/WR#		CTS12#/RTS12#/ SS12#/SSLA3/SSLB3		
17		PE0	WR1#/BC1#/ WAIT#		SSLA2/SSLB2/CRX1	IRQ7	
18		PD7		GTIOC0A	CTS0#/RTS0#/SS0#/ SSLA1/SSLB1/CTX1		
19		PD6		GTIOC0B	SSLA0/SSLB0		
20		PD5		GTIOC1A	RXD1/SMISO1/SSCL1	IRQ6	
21		PD4		GTIOC1B	SCK1		
22		PD3		GTIOC2A	TXD1/SMOSI1/SSDA1		
23		PD2	CS2#	GTIOC2B	MOSIA/MOSIB		
24		PD1	CS0#	GTIOC3A	MISOA/MISOB		
25		PD0	A12	GTIOC3B	RSPCKA/RSPCKB		
26	TDI	PF4	CS3#		RXD1*1		
27	TCK/FINEC	PF3			TXD1/SMOSI1/SSDA1		
28	TDO	PF2	CS1#		RXD1/SMISO1/ SSCL1/TXD1*1	IRQ5	
29		PB7	A19		SCK12		
30		PB6	A18		RXD12/SMISO12/ SSCL12/RXD12/ CRX1	IRQ2	
31		PB5	A17		TXD12/SMOSI12/ SSDA12/TXD12/ SIOX12/CTX1		
32	PLLVCC						
33		PB4	A16	POE8#/GTETRGO		IRQ3-DS	
34	PLLVSS						
35		PB3	A15	MTIOC0A/CACREF	SCK0		
36		PB2		MTIOC0B	TXD0/SMOSI0/ SSDA0/SDA0		
37		PB1		MTIOC0C	RXD0/SMISO0/ SSCL0/SCL0	IRQ4	

2.2.1 Register Associated with DSP Instructions

(1) Accumulator (ACC)

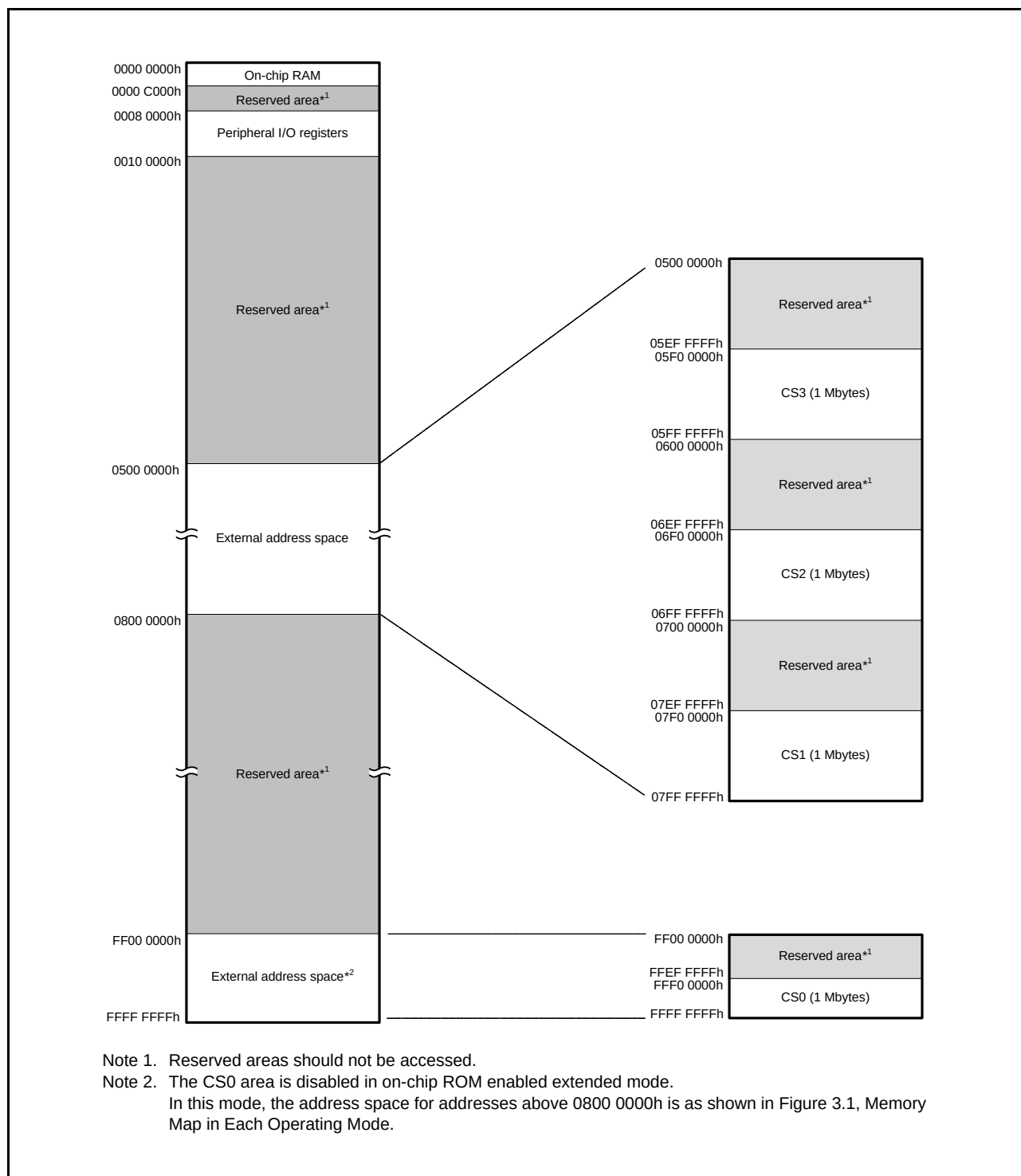
The accumulator (ACC) is a 64-bit register used for DSP instructions. The accumulator is also used for the multiply and multiply-and-accumulate instructions; EMUL, EMULU, FMUL, MUL, and RMPA, in which case the prior value in the accumulator is modified by execution of the instruction.

Use the MVTACHI and MVTACLO instructions for writing to the accumulator. The MVTACHI and MVTACLO instructions write data to the higher-order 32 bits (bits 63 to 32) and the lower-order 32 bits (bits 31 to 0), respectively. Use the MVFACHI and MVFACMI instructions for reading data from the accumulator. The MVFACHI and MVFACMI instructions read data from the higher-order 32 bits (bits 63 to 32) and the middle 32 bits (bits 47 to 16), respectively.

3.2 External Address Space

The external address space is divided into up to four CS areas (CS0 to CS3), each corresponding to the CSn# signal output from a CSn# (n = 0 to 3) pin.

Figure 3.2 shows the address ranges corresponding to the individual CS areas (CS0 to CS3) in on-chip ROM disabled extended mode.



**Figure 3.2 Correspondence between External Address Spaces and CS Areas
(In On-Chip ROM Disabled Extended Mode)**

Table 4.1 List of I/O Registers (Address Order) (6/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK $\geq$ PCLK	ICLK $<$ PCLK		
0008 7098h	ICU	Interrupt Request Register 152	IR152	8	8	2 ICLK		ICUb	
0008 7099h	ICU	Interrupt Request Register 153	IR153	8	8	2 ICLK			
0008 709Ah	ICU	Interrupt Request Register 154	IR154	8	8	2 ICLK			
0008 709Bh	ICU	Interrupt Request Register 155	IR155	8	8	2 ICLK			
0008 709Ch	ICU	Interrupt Request Register 156	IR156	8	8	2 ICLK			
0008 709Dh	ICU	Interrupt Request Register 157	IR157	8	8	2 ICLK			
0008 709Eh	ICU	Interrupt Request Register 158	IR158	8	8	2 ICLK			
0008 70A1h	ICU	Interrupt Request Register 161	IR161	8	8	2 ICLK			
0008 70A2h	ICU	Interrupt Request Register 162	IR162	8	8	2 ICLK			
0008 70A3h	ICU	Interrupt Request Register 163	IR163	8	8	2 ICLK			
0008 70A4h	ICU	Interrupt Request Register 164	IR164	8	8	2 ICLK			
0008 70A5h	ICU	Interrupt Request Register 165	IR165	8	8	2 ICLK			
0008 70A6h	ICU	Interrupt Request Register 166	IR166	8	8	2 ICLK			
0008 70A7h	ICU	Interrupt Request Register 167	IR167	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70A8h	ICU	Interrupt Request Register 168	IR168	8	8	2 ICLK			
0008 70A9h	ICU	Interrupt Request Register 169	IR169	8	8	2 ICLK			
0008 70AAh	ICU	Interrupt Request Register 170	IR170	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70ABh	ICU	Interrupt Request Register 171	IR171	8	8	2 ICLK			
0008 70ACh	ICU	Interrupt Request Register 172	IR172	8	8	2 ICLK			
0008 70ADh	ICU	Interrupt Request Register 173	IR173	8	8	2 ICLK			
0008 70AEh	ICU	Interrupt Request Register 174	IR174	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70AFh	ICU	Interrupt Request Register 175	IR175	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70B0h	ICU	Interrupt Request Register 176	IR176	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70B1h	ICU	Interrupt Request Register 177	IR177	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70B2h	ICU	Interrupt Request Register 178	IR178	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70B3h	ICU	Interrupt Request Register 179	IR179	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70B4h	ICU	Interrupt Request Register 180	IR180	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70B5h	ICU	Interrupt Request Register 181	IR181	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70B6h	ICU	Interrupt Request Register 182	IR182	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70B7h	ICU	Interrupt Request Register 183	IR183	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70B8h	ICU	Interrupt Request Register 184	IR184	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70B9h	ICU	Interrupt Request Register 185	IR185	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70BAh	ICU	Interrupt Request Register 186	IR186	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70BBh	ICU	Interrupt Request Register 187	IR187	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70BCh	ICU	Interrupt Request Register 188	IR188	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70BDh	ICU	Interrupt Request Register 189	IR189	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70BEh	ICU	Interrupt Request Register 190	IR190	8	8	2 ICLK			Not present in versions with 112, 100, 64 or 48 pins.
0008 70BFh	ICU	Interrupt Request Register 191	IR191	8	8	2 ICLK			Not present in versions with 112, 100, 64 or 48 pins.

Table 4.1 List of I/O Registers (Address Order) (17/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 83B2h	RSP11	RSP1 Command Register 1	SPCMD1	16	16	2, 3 PCLKB	2 ICLK	RSP1	Not present in versions with 64 or 48 pins.
0008 83B4h	RSP11	RSP1 Command Register 2	SPCMD2	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 83B6h	RSP11	RSP1 Command Register 3	SPCMD3	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 83B8h	RSP11	RSP1 Command Register 4	SPCMD4	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 83BAh	RSP11	RSP1 Command Register 5	SPCMD5	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 83BCh	RSP11	RSP1 Command Register 6	SPCMD6	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 83BEh	RSP11	RSP1 Command Register 7	SPCMD7	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9000h	S12AD	A/D Control Register	ADCSR	16	16	2, 3 PCLKB	2 ICLK	S12ADB	
0008 9004h	S12AD	A/D Channel Select Register A	ADANSA	16	16	2, 3 PCLKB	2 ICLK		
0008 9008h	S12AD	A/D-Converted Value Addition Mode Select Register	ADADS	16	16	2, 3 PCLKB	2 ICLK		
0008 900Ch	S12AD	A/D-Converted Value Addition Count Select Register	ADADC	8	8	2, 3 PCLKB	2 ICLK		
0008 900Eh	S12AD	A/D Control Extended Register	ADCER	16	16	2, 3 PCLKB	2 ICLK		
0008 9010h	S12AD	A/D Start Trigger Select Register	ADSTRGR	16	16	2, 3 PCLKB	2 ICLK		
0008 9014h	S12AD	A/D Channel Select Register B	ADANSB	16	16	2, 3 PCLKB	2 ICLK		
0008 9018h	S12AD	A/D Data-Doubling Register	ADDBLDR	16	16	2, 3 PCLKB	2 ICLK		
0008 901Eh	S12AD	A/D Self-Diagnosis Data Register	ADRD	16	16	2, 3 PCLKB	2 ICLK		
0008 9020h	S12AD	A/D Data Register 0	ADDR0	16	16	2, 3 PCLKB	2 ICLK		
0008 9022h	S12AD	A/D Data Register 1	ADDR1	16	16	2, 3 PCLKB	2 ICLK		
0008 9024h	S12AD	A/D Data Register 2	ADDR2	16	16	2, 3 PCLKB	2 ICLK		
0008 9026h	S12AD	A/D Data Register 3	ADDR3	16	16	2, 3 PCLKB	2 ICLK		
0008 9028h	S12AD	A/D Data Register 4	ADDR4	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 144, 120, 112, or 100 pins.
0008 902Ah	S12AD	A/D Data Register 5	ADDR5	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 144, 120, 112, or 100 pins.
0008 902Ch	S12AD	A/D Data Register 6	ADDR6	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 144, 120, 112, or 100 pins.
0008 902Eh	S12AD	A/D Data Register 7	ADDR7	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 144, 120, 112, or 100 pins.
0008 9060h	S12AD	A/D Sampling State Register 0	ADSSTR0	8	8	2, 3 PCLKB	2 ICLK		
0008 9066h	S12AD	A/D Sample and Hold Circuit Control Register	ADSHCR	16	16	2, 3 PCLKB	2 ICLK		
0008 9073h	S12AD	A/D Sampling State Register 1	ADSSTR1	8	8	2, 3 PCLKB	2 ICLK		
0008 9074h	S12AD	A/D Sampling State Register 2	ADSSTR2	8	8	2, 3 PCLKB	2 ICLK		
0008 9075h	S12AD	A/D Sampling State Register 3	ADSSTR3	8	8	2, 3 PCLKB	2 ICLK		
0008 9076h	S12AD	A/D Sampling State Register 4	ADSSTR4	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 144, 120, 112, or 100 pins.
0008 9077h	S12AD	A/D Sampling State Register 5	ADSSTR5	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 144, 120, 112, or 100 pins.
0008 9078h	S12AD	A/D Sampling State Register 6	ADSSTR6	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 144, 120, 112, or 100 pins.
0008 9079h	S12AD	A/D Sampling State Register 7	ADSSTR7	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 144, 120, 112, or 100 pins.
0008 9080h	S12AD	A/D Group Scan Priority Control Register	ADGSPCR	16	16	2, 3 PCLKB	2 ICLK		
0008 9084h	S12AD	A/D Data-Doubling Register A	ADDBLDRA	16	16	2, 3 PCLKB	2 ICLK		
0008 9086h	S12AD	A/D Data-Doubling Register B	ADDBLDRB	16	16	2, 3 PCLKB	2 ICLK		
0008 908Ah	S12AD	A/D Programmable Gain Amplifier Register	ADPG	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.

Table 4.1 List of I/O Registers (Address Order) (26/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 C174h	MPC	P64 Pin Function Control Register	P64PFS	8	8	2, 3 PCLKB	2 ICLK	MPC	Not present in versions with 64 or 48 pins.
0008 C175h	MPC	P65 Pin Function Control Register	P65PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C178h	MPC	P70 Pin Function Control Register	P70PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C179h	MPC	P71 Pin Function Control Register	P71PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C17Ah	MPC	P72 Pin Function Control Register	P72PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C17Bh	MPC	P73 Pin Function Control Register	P73PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C17Ch	MPC	P74 Pin Function Control Register	P74PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C17Dh	MPC	P75 Pin Function Control Register	P75PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C17Eh	MPC	P76 Pin Function Control Register	P76PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C180h	MPC	P80 Pin Function Control Register	P80PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C181h	MPC	P81 Pin Function Control Register	P81PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C182h	MPC	P82 Pin Function Control Register	P82PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C188h	MPC	P90 Pin Function Control Register	P90PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C189h	MPC	P91 Pin Function Control Register	P91PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 48 pins.
0008 C18Ah	MPC	P92 Pin Function Control Register	P92PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 48 pins.
0008 C18Bh	MPC	P93 Pin Function Control Register	P93PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 48 pins.
0008 C18Ch	MPC	P94 Pin Function Control Register	P94PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 48 pins.
0008 C18Dh	MPC	P95 Pin Function Control Register	P95PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C18Eh	MPC	P96 Pin Function Control Register	P96PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C190h	MPC	PA0 Pin Function Control Register	PA0PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C191h	MPC	PA1 Pin Function Control Register	PA1PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C192h	MPC	PA2 Pin Function Control Register	PA2PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C193h	MPC	PA3 Pin Function Control Register	PA3PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C194h	MPC	PA4 Pin Function Control Register	PA4PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 48 pins.
0008 C195h	MPC	PA5 Pin Function Control Register	PA5PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 48 pins.
0008 C196h	MPC	PA6 Pin Function Control Register	PA6PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64 or 48 pins.
0008 C198h	MPC	PB0 Pin Function Control Register	PB0PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C199h	MPC	PB1 Pin Function Control Register	PB1PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C19Ah	MPC	PB2 Pin Function Control Register	PB2PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C19Bh	MPC	PB3 Pin Function Control Register	PB3PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C19Ch	MPC	PB4 Pin Function Control Register	PB4PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C19Dh	MPC	PB5 Pin Function Control Register	PB5PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C19Eh	MPC	PB6 Pin Function Control Register	PB6PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C19Fh	MPC	PB7 Pin Function Control Register	PB7PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 48 pins.
0008 C1A0h	MPC	PC0 Pin Function Control Register	PC0PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 C1A1h	MPC	PC1 Pin Function Control Register	PC1PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 C1A2h	MPC	PC2 Pin Function Control Register	PC2PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64, or 48 pins.

Table 4.1 List of I/O Registers (Address Order) (38/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
000C 211Ah	GPT0	General PWM Timer Compare Capture Register F	GTCCRF	16	16, 32	2 to 5 PCLKA	2, 3 ICLK	GPT	
000C 211Ch	GPT0	General PWM Timer Cycle Setting Register	GTPR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 211Eh	GPT0	General PWM Timer Cycle Setting Buffer Register	GTPBR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2120h	GPT0	General PWM Timer Cycle Setting Double-Buffer Register	GTPDBR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2124h	GPT0	A/D Converter Start Request Timing Register A	GTADTRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2126h	GPT0	A/D Converter Start Request Timing Buffer Register A	GTADTBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2128h	GPT0	A/D Converter Start Request Timing Double-Buffer Register A	GTADTDBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 212Ch	GPT0	A/D Converter Start Request Timing Register B	GTADTRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 212Eh	GPT0	A/D Converter Start Request Timing Buffer Register B	GTADTBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2130h	GPT0	A/D Converter Start Request Timing Double-Buffer Register B	GTADTDBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2134h	GPT0	General PWM Timer Output Negate Control Register	GTONCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2136h	GPT0	General PWM Timer Dead Time Control Register	GTDTCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2138h	GPT0	General PWM Timer Dead Time Value Register U	GTDVU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 213Ah	GPT0	General PWM Timer Dead Time Value Register D	GTDVD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 213Ch	GPT0	General PWM Timer Dead Time Buffer Register U	GTDBU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 213Eh	GPT0	General PWM Timer Dead Time Buffer Register D	GTDBD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2140h	GPT0	General PWM Timer Output Protection Function Status Register	GTSOS	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2142h	GPT0	General PWM Timer Output Protection Function Temporary Release Register	GTSOTR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2180h	GPT1	General PWM Timer I/O Control Register	GTIOR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2182h	GPT1	General PWM Timer Interrupt Output Setting Register	GTINTAD	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2184h	GPT1	General PWM Timer Control Register	GTCR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2186h	GPT1	General PWM Timer Buffer Enable Register	GTBER	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2188h	GPT1	General PWM Timer Count Direction Register	GTUDC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 218Ah	GPT1	General PWM Timer Interrupt, A/D Converter Start Request Skipping Setting Register	GTITC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 218Ch	GPT1	General PWM Timer Status Register	GTST	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 218Eh	GPT1	General PWM Timer Counter	GTCNT	16	16	2 to 5 PCLKA	2, 3 ICLK		
000C 2190h	GPT1	General PWM Timer Compare Capture Register A	GTCCRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2192h	GPT1	General PWM Timer Compare Capture Register B	GTCCRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2194h	GPT1	General PWM Timer Compare Capture Register C	GTCCRC	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2196h	GPT1	General PWM Timer Compare Capture Register D	GTCCRD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2198h	GPT1	General PWM Timer Compare Capture Register E	GTCCRE	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 219Ah	GPT1	General PWM Timer Compare Capture Register F	GTCCRF	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 219Ch	GPT1	General PWM Timer Cycle Setting Register	GTPR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 219Eh	GPT1	General PWM Timer Cycle Setting Buffer Register	GTPBR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 21A0h	GPT1	General PWM Timer Cycle Setting Double-Buffer Register	GTPDBR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 21A4h	GPT1	A/D Converter Start Request Timing Register A	GTADTRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		

Table 4.1 List of I/O Registers (Address Order) (47/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK $\geq$ PCLK	ICLK $<$ PCLK		
000C3056h	DPC	Control Calculation Parameter Setting Register KQ2	PARAMKQ2	16	16	3 to 5 PCLKA	2, 3 ICLK	DPC	Not present in versions with 64 or 48 pins.
000C305Ah	DPC	Control Calculation Parameter Setting Register KF2	PARAMKF2	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C305Eh	DPC	Control Calculation Parameter Setting Register KP3	PARAMKP3	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3062h	DPC	Control Calculation Parameter Setting Register KI3	PARAMKI3	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3066h	DPC	Control Calculation Parameter Setting Register KQ3	PARAMKQ3	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C306Ah	DPC	Control Calculation Parameter Setting Register KF3	PARAMKF3	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C306Ch	DPC	Control Calculation Result Higher-Order Bits Store Register 0	RESULTU0	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C306Eh	DPC	Control Calculation Result Lower-Order Bits Store Register 0	RESULTL0	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3070h	DPC	Control Calculation Result Higher-Order Bits Store Register 1	RESULTU1	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3072h	DPC	Control Calculation Result Lower-Order Bits Store Register 1	RESULTL1	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3074h	DPC	Control Calculation Result Higher-Order Bits Store Register 2	RESULTU2	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3076h	DPC	Control Calculation Result Lower-Order Bits Store Register 2	RESULTL2	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3078h	DPC	Control Calculation Result Higher-Order Bits Store Register 3	RESULTU3	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C307Ah	DPC	Control Calculation Result Lower-Order Bits Store Register 3	RESULTL3	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C307Eh	DPC	Input Code Monitor Enable Register	TMONEN	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3082h	DPC	Maximum Input Code Monitor Register 0	TMONMAX0	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3086h	DPC	Minimum Input Code Monitor Register 0	TMONMIN0	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C308Ah	DPC	Maximum Input Code Monitor Register 1	TMONMAX1	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C308Eh	DPC	Minimum Input Code Monitor Register 1	TMONMIN1	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3092h	DPC	Maximum Input Code Monitor Register 2	TMONMAX2	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3096h	DPC	Minimum Input Code Monitor Register 2	TMONMIN2	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C309Ah	DPC	Maximum Input Code Monitor Register 3	TMONMAX3	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C309Eh	DPC	Minimum Input Code Monitor Register 3	TMONMIN3	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C30A2h	DPC	Overvoltage Output Error Judgment Threshold Setting Register 0	ERRVTH0	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C30A6h	DPC	Overvoltage Output Error Judgment Threshold Setting Register 1	ERRVTH1	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C30AAh	DPC	Overvoltage Output Error Judgment Threshold Setting Register 2	ERRVTH2	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C30AEh	DPC	Overvoltage Output Error Judgment Threshold Setting Register 3	ERRVTH3	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C30B2h	DPC	PWM Shut-Down at Overvoltage Output Error Setting Register	ERRDWN	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
007F C402h	FLASH	Flash Mode Register	FMODR	8	8	2, 3 FCLK	2, 3 ICLK	ROM/ E2 DataFlash Memory	
007F C410h	FLASH	Flash Access Status Register	FASTAT	8	8	2, 3 FCLK	2, 3 ICLK		
007F C411h	FLASH	Flash Access Error Interrupt Enable Register	FAEINT	8	8	2, 3 FCLK	2, 3 ICLK		
007F C412h	FLASH	Flash Ready Interrupt Enable Register	FRDYIE	8	8	2, 3 FCLK	2, 3 ICLK	ROM	
007F C440h	FLASH	E2 DataFlash Read Enable Register 0	DFLRE0	16	16	2, 3 FCLK	2, 3 ICLK	E2 DataFlash Memory	
007F C442h	FLASH	E2 DataFlash Read Enable Register 1	DFLRE1	16	16	2, 3 FCLK	2, 3 ICLK		
007F C450h	FLASH	E2 DataFlash P/E Enable Register 0	DFLWE0	16	16	2, 3 FCLK	2, 3 ICLK		
007F C452h	FLASH	E2 DataFlash P/E Enable Register 1	DFLWE1	16	16	2, 3 FCLK	2, 3 ICLK		

5.3.2 Clock Timing

Table 5.9 Clock Timing

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

T_a = T_{opr}. T_a is common to conditions 1 to 3.

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BCLK pin output cycle time	Only condition 3	t _{Bcyc}	20	—	—	ns	Figure 5.3
	Other than condition 3	t _{Bcyc}	40	—	—	ns	
BCLK pin output high pulse width		t _{CH}	5	—	—	ns	Figure 5.4
BCLK pin output low pulse width		t _{CL}	5	—	—	ns	
BCLK pin output rising time		t _{Cr}	—	—	5	ns	
BCLK pin output falling time		t _{Cf}	—	—	5	ns	
EXTAL external clock input cycle time		t _{EXcyc}	70	—	—	ns	
EXTAL external clock input high pulse width		t _{EXH}	35	—	—	ns	Figure 5.5
EXTAL external clock input low pulse width		t _{EXL}	35	—	—	ns	
EXTAL external clock rising time		t _{EXr}	—	—	5	ns	
EXTAL external clock falling time		t _{EXf}	—	—	5	ns	
EXTAL external clock input wait time*1		t _{EXWT}	1	—	—	ms	
Main clock oscillator oscillation frequency		f _{MAIN}	8	—	12.5	MHz	Figure 5.6
Main clock oscillator stabilization time (crystal)		t _{MAINOSC}	—	—	*2	ms	
Main clock oscillator stabilization wait time (crystal)		t _{MAINOSCW}	—	—	*3	ms	
LOCO, IWDTCCLK clock cycle time		t _{LOCOCYC}	6.96	8	9.4	μs	Figure 5.7
LOCO, IWDTCCLK clock oscillation frequency		f _{LOCO}	106.25	125	143.75	kHz	
LOCO, IWDTCCLK clock oscillation stabilization wait time		t _{LOCOWT}	—	—	20	μs	
PLL clock frequency		f _{PLL}	104	—	200	MHz	Figure 5.8
PLL clock oscillation stabilization time	PLL operation started after main clock oscillation has settled	t _{PLL1}	—	—	500	μs	
PLL clock oscillation stabilization wait time		t _{PLLWT1}	—	—	*4	ms	
PLL clock oscillation stabilization time	PLL operation started before main clock oscillation has settled	t _{PLL2}	—	—	t _{MAINOSC} + t _{PLL1}	ms	Figure 5.8
PLL clock oscillation stabilization wait time		t _{PLLWT2}	—	—	*4	ms	

Note 1. This is the time until the clock is used after clearing the main clock oscillator stop bit (MOSCCR.MOSTP) to 0 (selecting operation).

Note 2. When using a main clock, ask the manufacturer of the oscillator to evaluate its oscillation. Refer to the results of evaluation provided by the manufacturer for the oscillation stabilization time.

Note 3. This is calculated from the formula below, where n is the number of cycles set by the MOSCWTCR.MSTS[4:0] bits.

$$t_{\text{MAINOSCW}} = t_{\text{MAINOSC}} + \frac{n + 16384}{f_{\text{MAIN}}}$$

5.3.4 Control Signal Timing

Table 5.11 Control Signal Timing

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
NMI pulse width	t_{NMIW}	200	—	—	ns	$t_c(PCLK) \times 2 \leq 200$ ns, Figure 5.11
		$t_c(PCLK) \times 2$	—	—	ns	$t_c(PCLK) > 200$ ns, Figure 5.11
IRQ pulse width	t_{IRQW}	200	—	—	ns	$t_c(PCLK) \leq 200$ ns, Figure 5.12
		$t_c(PCLK) \times 2$	—	—	ns	$t_c(PCLK) > 200$ ns, Figure 5.12

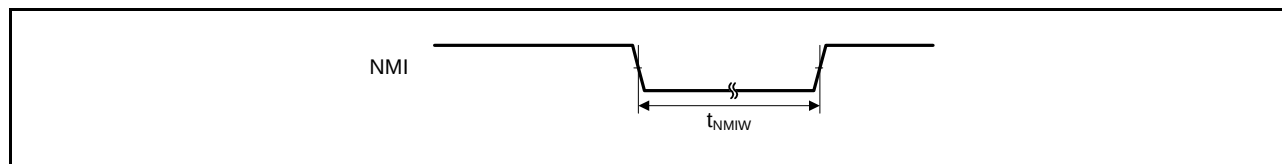


Figure 5.11 NMI Interrupt Input Timing

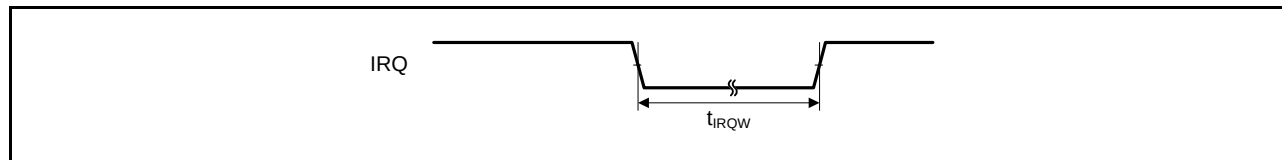


Figure 5.12 IRQ Interrupt Input Timing

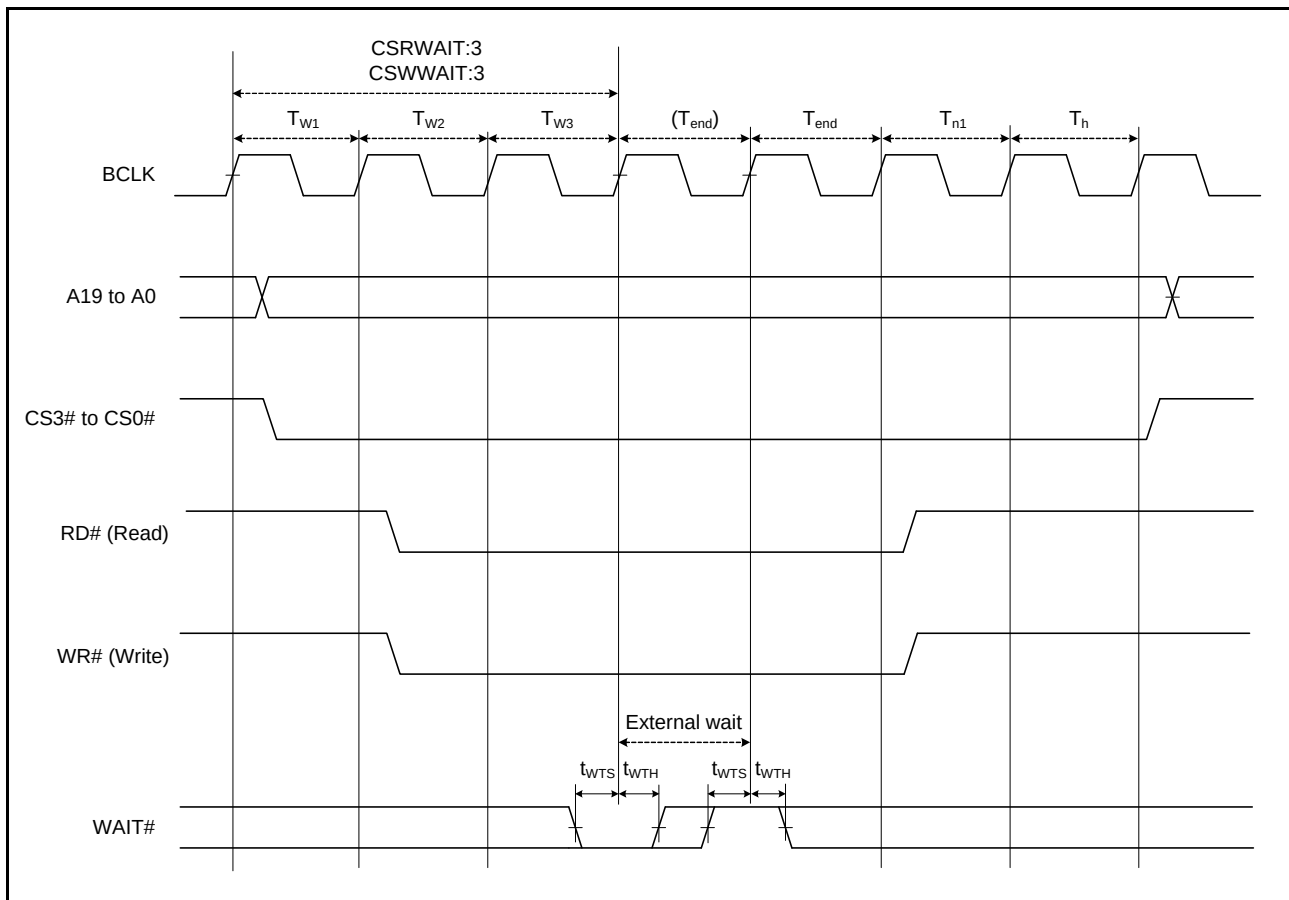


Figure 5.17 External Bus Timing/External Wait Control

Table 5.14 Bus Timing (Multiplexed Bus) (3)

Condition: PLLVCC = VCC_USB = AVCC0 = AVCC = VREF = 3.0 to 3.6 V

VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V, VREFH0 = 3.0 V to AVCC0

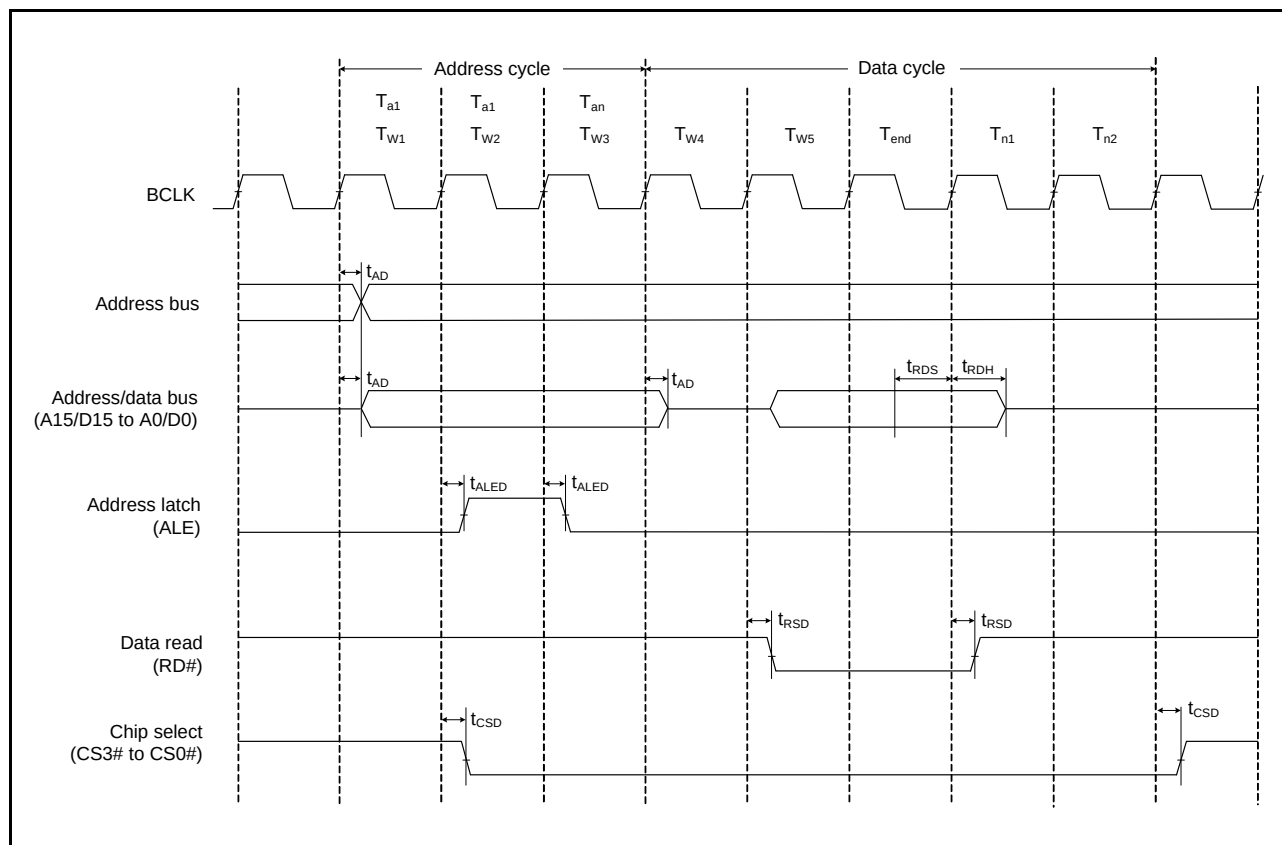
$T_a = T_{opr}$

Output load conditions: $V_{OH} = VCC \times 0.5$, $V_{OL} = VCC \times 0.5$, $I_{OH} = -1.0 \text{ mA}$, $I_{OL} = 1.0 \text{ mA}$, $C = 30 \text{ pF}$

Item	Symbol	Min.	Max.	Unit	Test Conditions
Address delay time	t_{AD}	—	35	ns	Figure 5.18, Figure 5.19
Byte control delay time	t_{BCD}	—	30	ns	
CS# delay time	t_{CSD}	—	30	ns	
RD# delay time	t_{RSD}	—	30	ns	
ALE delay time	t_{ALED}	—	30	ns	
Read data setup time	t_{RDS}	20	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	—	30	ns	
Write data delay time	t_{WDD}	—	35	ns	
Write data hold time	t_{WDH}	0	—	ns	
WAIT# setup time	t_{WTS}	20	—	ns	Figure 5.17
WAIT# hold time	t_{WTH}	0.0	—	ns	

Table 5.15 Bus Timing (Multiplexed Bus) (4)Condition: $V_{CC} = PLLVCC = AVCC0 = AVCC = VREF = 4.0$ to 5.5 V, $V_{CC_USB} = 3.0$ to 3.6 V $V_{SS} = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0$ V, $VREFH0 = 4.0$ V to $AVCC0$ $T_a = T_{opr}$ Output load conditions: $V_{OH} = V_{CC} \times 0.5$, $V_{OL} = V_{CC} \times 0.5$, $I_{OH} = -1.0$ mA, $I_{OL} = 1.0$ mA, $C = 30$ pF

Item	Symbol	Min.	Max.	Unit	Test Conditions
Address delay time	t_{AD}	—	15	ns	Figure 5.18, Figure 5.19
Byte control delay time	t_{BCD}	—	15	ns	
CS# delay time	t_{CSD}	—	15	ns	
RD# delay time	t_{RSD}	—	15	ns	
ALE delay time	t_{ALED}	—	15	ns	
Read data setup time	t_{RDS}	15	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	—	15	ns	
Write data delay time	t_{WDD}	—	15	ns	
Write data hold time	t_{WDH}	0	—	ns	
WAIT# setup time	t_{WTS}	15	—	ns	Figure 5.17
WAIT# hold time	t_{WTH}	0.0	—	ns	

**Figure 5.18 Example of External Bus Timing/Read Access Operation (Multiplexed)**

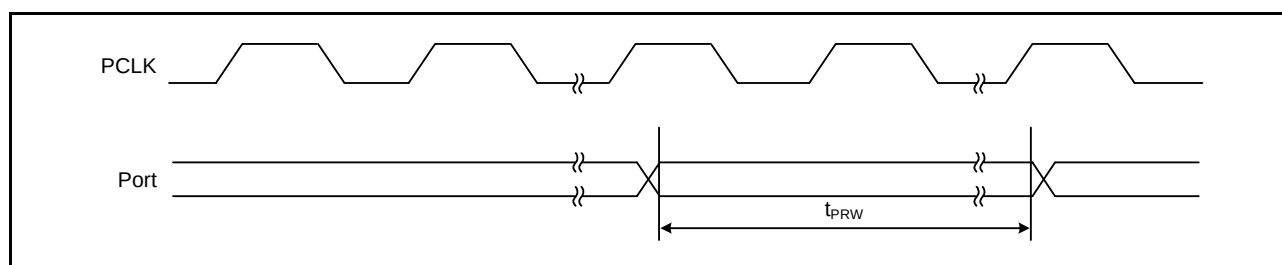


Figure 5.20 I/O port Input Timing

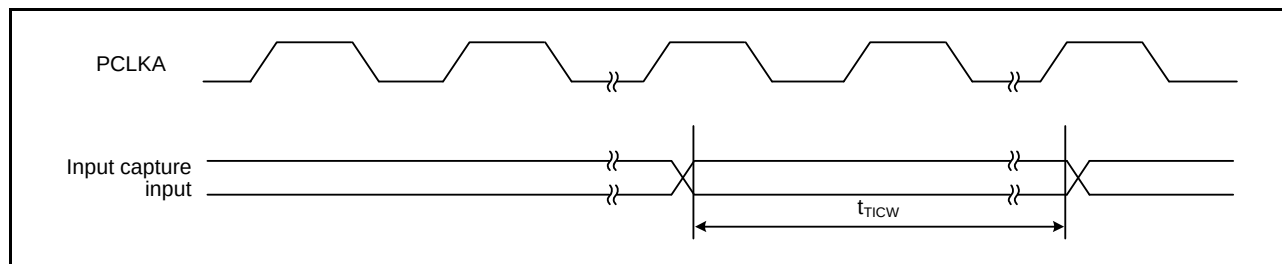


Figure 5.21 MTU3 Input/Output Timing

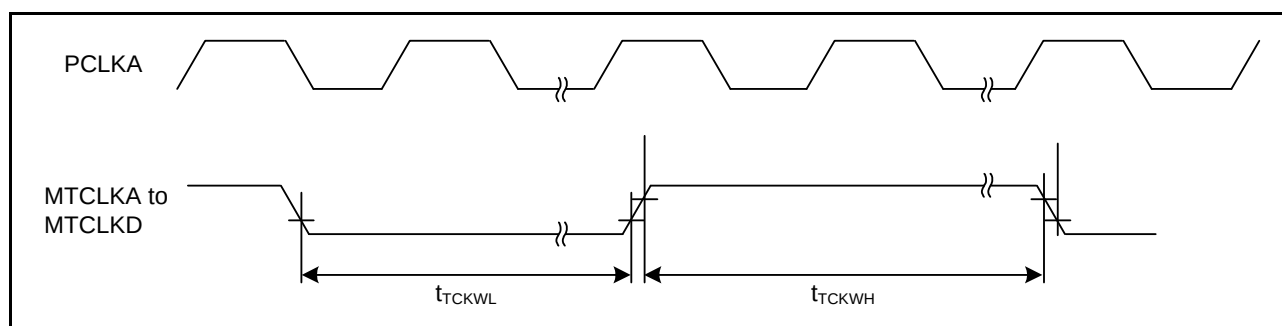


Figure 5.22 MTU3 Clock Input Timing

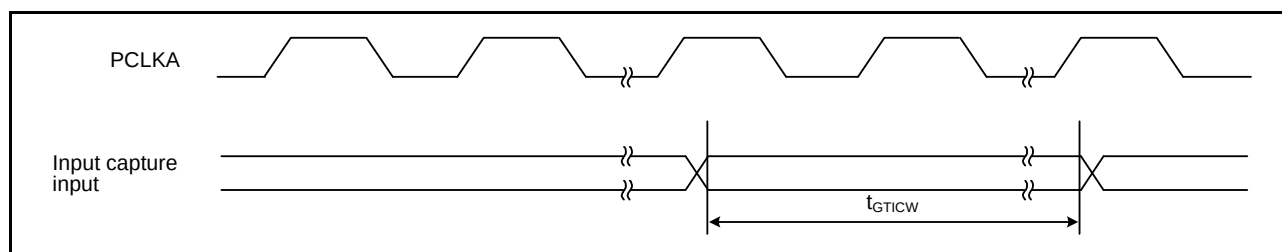


Figure 5.23 GPT Input Capture Input Timing

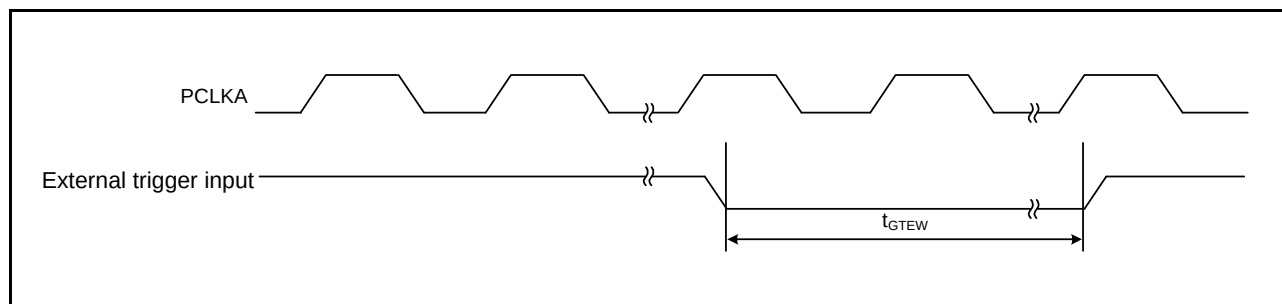


Figure 5.24 GPT External Trigger Input Timing

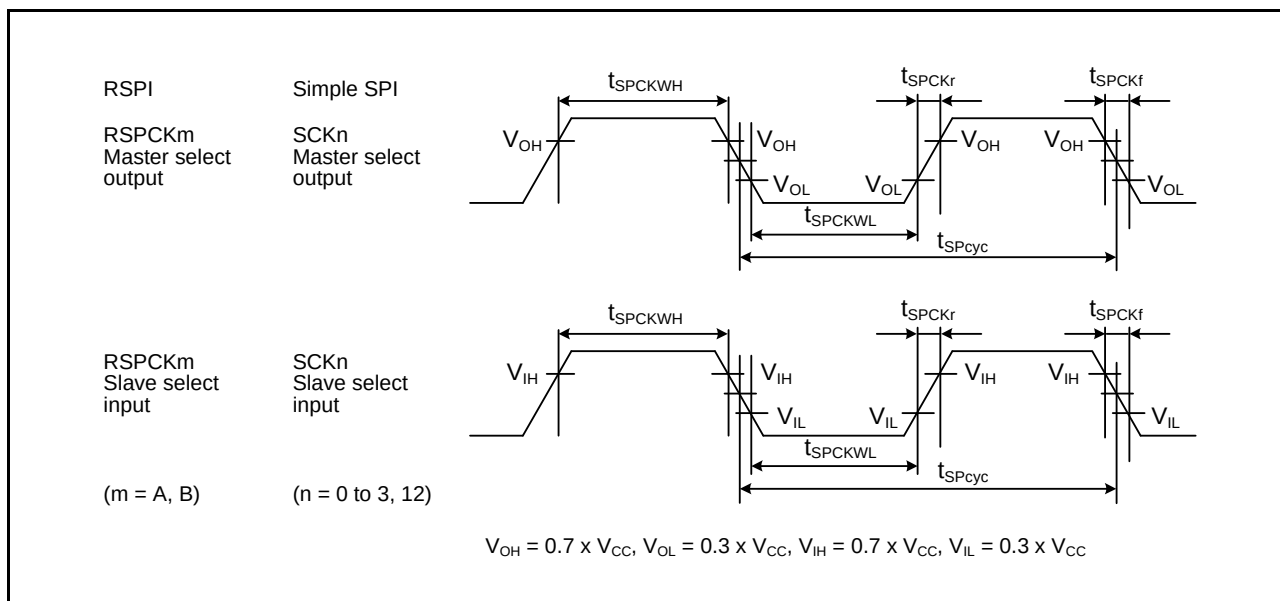


Figure 5.29 RSPI Clock Timing and Simple SPI Clock Timing

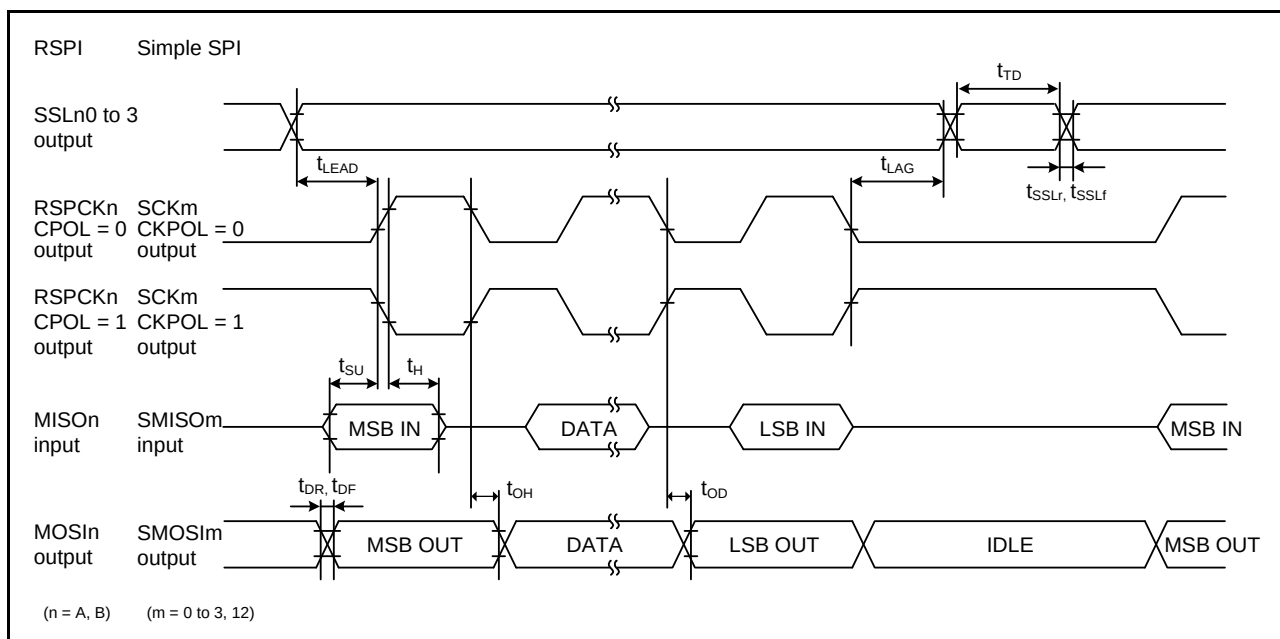


Figure 5.30 RSPI Timing (Master, CPHA = 0) (Bit Rate: PCLKB Division Ratio Set to a Value Other Than 1/2) and Simple SPI Timing (Master, CKPH = 1)

Table 5.20 10-Bit A/D Conversion Characteristics (2)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: $V_{CC} = PLLVCC = VCC_USB = 2.7$ to 3.6 V, $VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0$ V
 $AVCC0 = AVCC = VREF = 3.0$ to 3.6 V, $VREFH0 = 3.0$ V to $AVCC0$

Condition 2: $V_{CC} = PLLVCC = VCC_USB = 2.7$ to 3.6 V, $VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0$ V
 $AVCC0 = AVCC = VREF = 4.0$ to 5.5 V, $VREFH0 = 4.0$ V to $AVCC0$

Condition 3: $V_{CC} = PLLVCC = 4.0$ to 5.5 V, $VCC_USB = 3.0$ to 3.6 V, $VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0$ V
 $AVCC0 = AVCC = VREF = 4.0$ to 5.5 V, $VREFH0 = 4.0$ V to $AVCC0$

$T_a = T_{opr}$ is common to conditions 1 to 3.

Item			Min.	Typ.	Max.	Unit	Test Conditions
Resolution			10	10	10	Bit	
Conversion time*1 (Operation at ADCLK = 50 MHz)	Without 0.1-μF external capacitor Permissible signal source impedance (max.) = 1 kΩ	AN0 to AN7	0.8	—	—	μs	Sampling in 15 states
		Other channels	1.0	—	—	μs	Sampling in 25 states
Analog input capacitance			—	—	6	pF	
Integral nonlinearity error			—	—	±2.0	LSB	
Offset error			—	—	±2.0	LSB	
Full-scale error			—	—	±3.0	LSB	
Quantization error			—	±0.5	—	LSB	
Absolute accuracy			—	—	±4.0	LSB	

Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Table 6.13 Timing of On-Chip Peripheral Modules (3)

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
 AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
 Ta = T_{opr}

Item		Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI	SCK clock cycle output (master)	t _{SPcyc}	4	65536	t _{Pcyc}	Figure 6.20
	SCK clock cycle input (slave)		8	65536		
	SCK clock high pulse width	t _{SPCKWH}	0.4	0.6	t _{SPcyc}	
	SCK clock low pulse width	t _{SPCKWL}	0.4	0.6	t _{SPcyc}	
	SCK clock rise/fall time	t _{SPCKR} , t _{SPCKF}	—	20	ns	
	Data input setup time	t _{SU}	40	—	ns	Figure 6.21 to Figure 6.24
	Data input hold time	t _H	40	—	ns	
	SS input setup time	t _{LEAD}	6	—	t _{Pcyc}	
	SS input hold time	t _{LAG}	6	—	t _{Pcyc}	
	Data output delay time	t _{OD}	—	40	ns	
	Data output hold time	t _{OH}	−10	—	ns	
	Data rise/fall time	t _{DR} , t _{DF}	—	20	ns	
	SS input rise/fall time	t _{SSLr} , t _{SSLf}	—	20	ns	
	Slave access time	t _{SA}	—	5	t _{Pcyc}	Figure 6.23 and Figure 6.24
	Slave output release time	t _{REL}	—	5	t _{Pcyc}	

Note 1. t_{Pcyc}: PCLK cycle

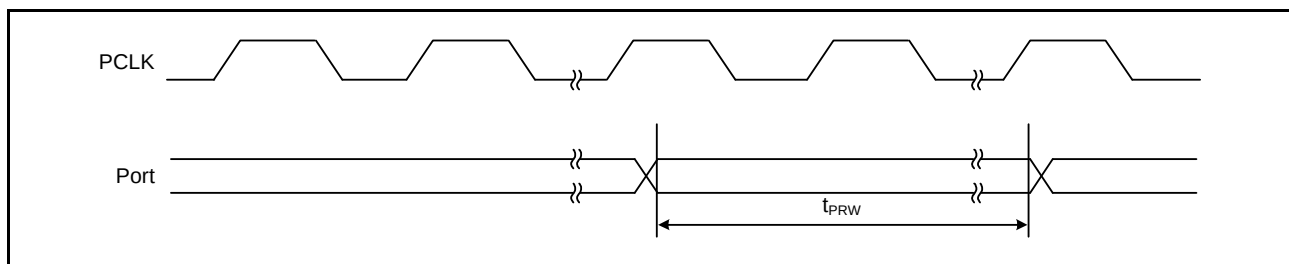
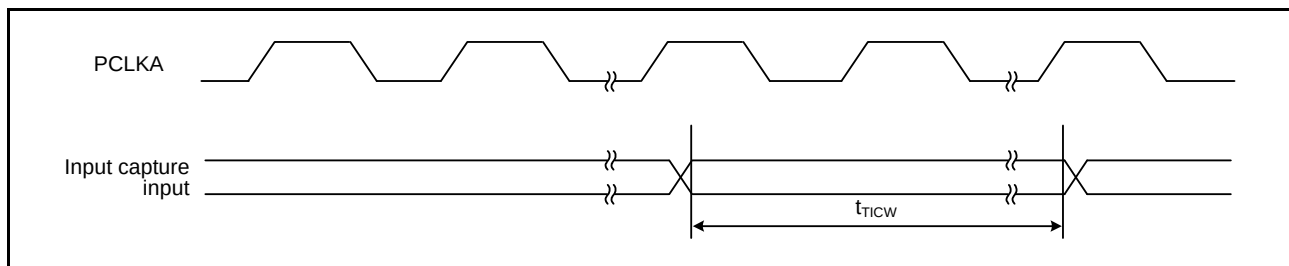
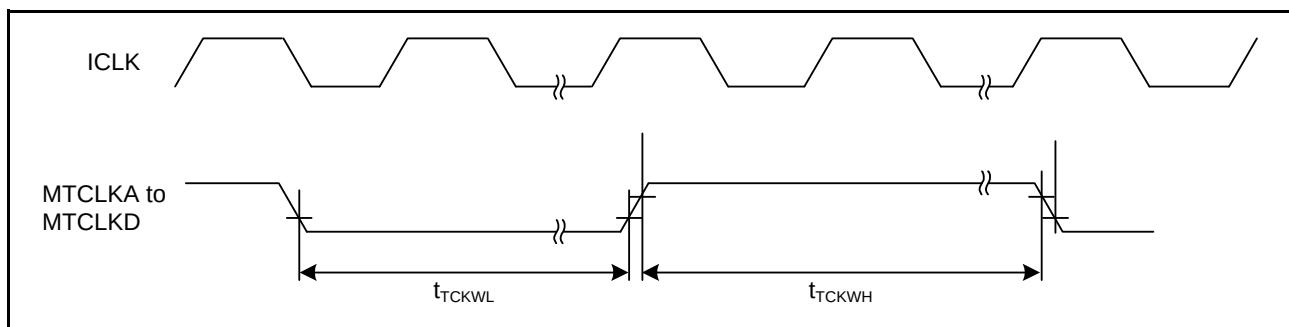
Table 6.15 Timing of On-Chip Peripheral Modules (5)

Conditions: $V_{CC} = 2.7$ to 3.6 V, $V_{SS} = AVSS0 = VREFL0 = 0$ V,
 $AVCC0 = 3.0$ to 3.6 V, $VREFH0 = 3.0$ V to $AVCC0$,
 $T_a = T_{opr}$

Item		Symbol	Min.*1, *2	Max.	Unit	Test Conditions
Simple IIC (Standard-mode)	SCL, SDAinput rise time	t_{Sr}	—	1000	ns	Figure 6.25
	SCL, SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	$4 \times t_{IICcyc}$	ns	
	Data input setup time	t_{SDAS}	250	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
Simple IIC (Fast-mode)	SCL, SDA input rise time	t_{Sr}	$20 + 0.1C_b$	300	ns	
	SCL, SDA input fall time	t_{Sf}	$20 + 0.1C_b$	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	$4 \times t_{IICcyc}$	ns	
	Data input setup time	t_{SDAS}	100	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note 1. The value in parentheses is used when ICMR3.NF[1:0] are set to 11b while a digital filter is enabled with ICFER.NFE = 1.

Note 2. C_b indicates the total capacity of the bus line.

**Figure 6.12 I/O port Input Timing****Figure 6.13 MTU3 Input/Output Timing****Figure 6.14 MTU3 Clock Input Timing**

6.8 E² DataFlash Characteristic**Table 6.22 E² DataFlash (Flash Memory for Data Storage) Characteristics (1)**

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V

AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Temperature range for the programming/erasure operation: T_a = T_{opr} T_a is common to conditions 1 to 3.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Reprogram/erase cycle*1	N _{DPEC}	100000	—	—	Times	
Data hold time	t _{DDRP}	30*2	—	—	Year	Ta = +85°C

Note 1. Definition of reprogram/erase cycle:

The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 128-byte programming is performed 16 times for different addresses in 2-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. The value is obtained from the reliability test.

Table 6.23 E² DataFlash (Flash Memory for Data Storage) Characteristics (2)

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,

AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,

Ta = T_{opr}

Item		Symbol	min	typ	max	Unit	Test Condition
Programming time	2 bytes	t _{DP2}	—	0.25	2	ms	FCLK = 50 MHz
Erasure time	32 bytes	t _{DE32}	—	2	20	ms	FCLK = 50 MHz N _{DPEC} ≤ 100
	32 bytes	t _{DE32}	—	4	20	ms	FCLK = 50 MHz N _{DPEC} > 100
Blank check time	2 bytes	t _{DBC2}	—	—	30	μs	FCLK = 50 MHz
Suspend delay time during programming		t _{DSPD}	—	—	120	μs	Figure 6.31 PCLKB = 50 MHz
First suspend delay time during erasing (in suspend priority mode)		t _{DSESD1}	—	—	120	μs	
Second suspend delay time during erasing (in suspend priority mode)		t _{DSESD2}	—	—	300	μs	
Suspend delay time during erasing (in erasure priority mode)		t _{DSEED}	—	—	300	μs	

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

¾ The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

¾ The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

¾ The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

¾ When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

¾ The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.