Renesas Electronics America Inc - R5F563TEBDFH#V0 Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	69
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 12x10b, 8x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f563tebdfh-v0

1. Overview

1.1 Outline of Specifications

Table 1.1 lists the specifications in outline, and Table 1.2 lists the functions of products.
Table 1.1 shows an outline of the maximum specifications, and the available peripheral modules and number of channels differ according to the number of pins on the package and the ROM capacity. For details, see Table 1.2, Comparison of Functions for Different Packages.

Table 1.1 Outline of Specifications (1/7)

Classification	Module/Function	Description
CPU	CPU	• Maximum operating frequency: 100 MHz • 32-bit RX CPU • Minimum instruction execution time: One instruction per state (cycle of the system clock) • Address space: 4-Gbyte linear • Register set of the CPU General purpose: Sixteen 32-bit registers Control: Nine 32-bit registers Accumulator: One 64-bit register • Basic instructions: 73 • Floating-point operation instructions: 8 • DSP instructions: 9 • Addressing modes: 10 • Data arrangement Instructions: Little endian Data: Selectable as little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits • Memory protection unit (MPU)
	FPU	• Single precision floating point (32 bits) • Data types and floating-point exceptions in conformance with the IEEE754 standard
Memory	ROM	• Capacity: 512 Kbytes, 384 Kbytes, 256 Kbytes, 64 Kbytes, 48 Kbytes, 32 Kbytes • 100 MHz, no-wait access • On-board programming: Programs can be modified through SCI or USB while the MCU is mounted on the board. • Off-board programming: Programs can be modified using parallel programmer. (only in 144-, 120-, 112- and 100-pin versions)
	RAM	• Capacity: 48 Kbytes, 32 Kbytes, 24 Kbytes, 8 Kbytes • 100 MHz, no-wait access
	E^2 data flash	• Capacity: 32 Kbytes, 8 Kbytes • Programming/erasing: 100,000 times • On-board programming: Programs can be modified through SCI or USB while the MCU is mounted on the board. Programming from the user program is possible.
MCU operating modes		[144-, 120-, 112- and 100-pin versions] Single-chip mode, on-chip ROM enabled extended mode, on-chip ROM disabled extended mode (switchable by software) [64- and 48-pin versions] Single-chip mode

Table 1.4 Pin Functions (5/5)

Classifications	Pin Name	I/O	Description
I/O ports	P00 to P05	I/O	6-bit input/output pins
	P10 to P14	I/O	5-bit input/output pins
	P20 to P26	I/O	7-bit input/output pins
	P30 to P35	I/O	6-bit input/output pins
	P40 to P47	Input	8-bit input pins
	P50 to P57	Input	8-bit input pins
	P60 to P65	Input	6-bit input pins
	P70 to P76	I/O	7-bit input/output pins
	P80 to P82	I/O	3-bit input/output pins
	P90 to P96	I/O	7-bit input/output pins
	PA0 to PA6	I/O	7-bit input/output pins
	PB0 to PB7	I/O	8-bit input/output pins
	PC0 to PC5	Input	6-bit input pins
	PD0 to PD7	I/O	8-bit input/output pins
	PE0, PE1, PE3 to PE5	I/O	6-bit input/output pins
	PE2	Input	1-bit input pin
	PF0 to PF4	I/O	5-bit input/output pins
	PG0 to PG6	I/O	7-bit input/output pins

Table 1.5 List of Pins and Pin Functions (144-Pin LQFP) (3/4)

Pin Number 144-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3, GPT, POE3, CAC)	Communications (SCIc, SCId, RSPI, RIIC, CAN, USB)	Interrupt	S12ADB, AD, DA
72		PG3		GTIOC6A	TXD3/SMOSI3/SSDA3		
73		PG2			SCK2	IRQ2	
74		PG1		GTIOC7B	RXD2/SMISO2/SSCL2	IRQ1	
75		PG0		GTIOC7A	TXD2/SMOSI2/SSDA2	IRQ0	
76		P76	D0/[A0/D0]	MTIOC4D/GTIOC2B			
77		P75	D1/[A1/D1]	MTIOC4C/GTIOC1B			
78		P74	D2/[A2/D2]	MTIOC3D/GTIOC0B			
79		P73	D3/[A3/D3]	MTIOC4B/GTIOC2A			
80		P72	D4/[A4/D4]	MTIOC4A/GTIOC1A			
81		P71	D5/[A5/D5]	MTIOC3B/GTIOC0A			
82		P70	D6/[A6/D6]	POE0#	CTS1#/RTS1#/SS1#	IRQ5-DS	
83		P33	D7/[A7/D7]	MTIOC3A/MTCLKA	SSLA3/SSLB3		
84		P32	D8/[A8/D8]	MTIOC3C/MTCLKB	SSLA2/SSLB2		
85	VCC						
86		P31	D9/[A9/D9]	MTIOC0A/MTCLKC	SSLA1/SSLB1		
87	VSS						
88		P30	D10/[A10/D10]	MTIOC0B/MTCLKD	SCK0/SSLA0/SSLB0		
89		P26	CS0#		TXD1/SMOSI1/SSDA1/SDA1		
90		P25	CS1#		SCK1/SCL1		
91		P24	D11/[A11/D11]		CTS0#/RTS0#/SS0#/RSPCKA/RSPCKB	IRQ4	
92		P23	D12/[A12/D12]	CACREF	TXD0/SMOSI0/SSDA0/MOSIA/MOSIB/CTX1		
93		P22	D13/[A13/D13]		RXD0/SMISO0/SSCL0/MISOA/MISOB/CRX1		ADTRG#
94		P21	D14/[A14/D14]	MTCLKA		IRQ6-DS	ADTRG1#
95		P20	D15/[A15/D15]	MTCLKB		IRQ7-DS	ADTRG0#
96		PC5					AN19
97		PC4					AN18
98		P65	A0/BC0#				AN5
99		P64	A1				AN4
100		PC3					AN17
101		PC2					AN16
102	AVCC						
103	VREF						
104	AVSS						
105		PC1					AN15
106		PC0					AN14
107		P63	A2				AN3
108		P62	A3				AN2
109		P61	A4				AN1

Table 1.6 List of Pins and Pin Functions (120-Pin LQFP) (4/4)

Pin Number 120-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3, GPT, POE3, CAC)	Communications (SCIc, SCId, RSPI, RIIC, CAN, USB)	Interrupt	S12ADB, AD, DA
111		P82	WAIT#	MTIC5U	SCK12	IRQ3	
112		P81	A8	MTIC5V	TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12		
113		P80	A9	MTIC5W	RXD12/SMISO12/ SSCL12/RXDX12	IRQ5	
114		P12	CS3#		USB0_DPRPD		
115		P11	ALE	MTCLKC		IRQ1-DS	
116		P10		MTCLKD		IRQ0-DS	
117					USB0_DPUPE		
118	VSS_USB						
119					USB0_DM		
120					USB0_DP		

Table 1.7 List of Pins and Pin Functions (112-Pin LQFP) (2/4)

Pin Number 112-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3, GPT, POE3, CAC)	Communications (SCIc, SCId, RSPI, RIIC, CAN)	Interrupt	S12ADB, AD, DA
38		PB0	A14	MTIOC0D	MOSIA/MOSIB		
39		PA5		MTIOC1A	RXD0/SMISO0/ SSCL0/ MISOA/MISOB		ADTRG1#
40		PA4		MTIOC1B	TXD0/SMOSI0/ SSDA0/RSPCKA/ RSPCKB		ADTRG0#
41		PA3		MTIOC2A	SCK0/SSLA0/SSLB0		
42		PA2		MTIOC2B	RXD2/SMISO2/ SSCL2/ SSLA1/SSLB1		
43		PA1		MTIOC6A	TXD2/SMOSI2/ SSDA2/SSLA2/SSLB2		
44		PA0		MTIOC6C	SCK2/SSLA3/SSLB3		
45	VCC						
46		P96	A13	POE4#	RXD1/SMISO1/SSCL1	IRQ4-DS	
47	VSS						
48		P95		MTIOC6B/ GTIOC4A	TXD1/SMOSI1/SSDA1		
49		P94		MTIOC7A/ GTIOC5A	CTS1#/RTS1#/SS1#		
50		P93		MTIOC7B/ GTIOC6A	CTS2#/RTS2#/SS2#		
51		P92		MTIOC6D/GTIOC4B			
52		P91		MTIOC7C/GTIOC5B			
53		P90		MTIOC7D/GTIOC6B			
54	TRCLK	PG5		POE12#	SCK3		ADTRG#
55	TRDATA3	PG4		GTIOC6B	RXD3/SMISO3/SSCL3	IRQ6	
56	TRDATA2	PG3		GTIOC6A	TXD3/SMOSI3/SSDA3		
57	TRDATA1	PG2			SCK2	IRQ2	
58	TRDATA0	PG1		GTIOC7B	RXD2/SMISO2/SSCL2	IRQ1	
59	TRSYNC	PG0		GTIOC7A	TXD2/SMOSI2/SSDA2	IRQ0	
60		P76	D0/[A0/D0]	MTIOC4D/GTIOC2B			
61		P75	D1/[A1/D1]	MTIOC4C/GTIOC1B			
62		P74	D2/[A2/D2]	MTIOC3D/GTIOC0B			
63		P73	D3/[A3/D3]	MTIOC4B/GTIOC2A			
64		P72	D4/[A4/D4]	MTIOC4A/GTIOC1A			
65		P71	D5/[A5/D5]	MTIOC3B/GTIOC0A			
66		P70	D6/[A6/D6]	POE0#	CTS1#/RTS1#/SS1#	IRQ5-DS	
67		P33	D7/[A7/D7]	MTIOC3A/MTCLKA	SSLA3/SSLB3		
68		P32	D8/[A8/D8]	MTIOC3C/MTCLKB	SSLA2/SSLB2		
69	VCC						
70		P31	D9/[A9/D9]	MTIOC0A/MTCLKC	SSLA1/SSLB1		
71	VSS						
72		P30	D10/[A10/ D10]	MTIOC0B/MTCLKD	SCK0/SSLA0/SSLB0		
73		P24	D11/[A11/D11]		CTS0#/RTS0#/SS0#/ RSPCKA/RSPCKB	IRQ4	

3. Address Space

3.1 Address Space

This MCU has a 4-Gbyte address space, consisting of the range of addresses from 0000 0000h to FFFF FFFFh. That is, linear access to an address space of up to 4 Gbytes is possible, and this contains both program and data areas.
Figure 3.1 shows the memory maps in the respective operating modes. Accessible areas will differ according to the operating mode and states of control bits.

4.1 I/O Register Addresses (Address Order)

Table 4.1 List of I/O Registers (Address Order) (1/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 0000h	SYSTEM	Mode Monitor Register	MDMONR	16	16	3 ICLK		Operating Modes	
0008 0002h	SYSTEM	Mode Status Register	MDSR	16	16	3 ICLK			Not present in versions with 64 or 48 pins.
0008 0006h	SYSTEM	System Control Register 0	SYSCR0	16	16	3 ICLK			
0008 0008h	SYSTEM	System Control Register 1	SYSCR1	16	16	3 ICLK			
0008 000Ch	SYSTEM	Standby Control Register	SBYCR	16	16	3 ICLK		Low Power Consumption	
0008 0010h	SYSTEM	Module Stop Control Register A	MSTPCRA	32	32	3 ICLK			
0008 0014h	SYSTEM	Module Stop Control Register B	MSTPCRB	32	32	3 ICLK			
0008 0018h	SYSTEM	Module Stop Control Register C	MSTPCRC	32	32	3 ICLK			
0008 0020h	SYSTEM	System Clock Control Register	SCKCR	32	32	3 ICLK		Clock Generation Circuit	
0008 0024h	SYSTEM	System Clock Control Register 2	SCKCR2	16	16	3 ICLK			Not present in versions with 64 or 48 pins.
0008 0026h	SYSTEM	System Clock Control Register 3	SCKCR3	16	16	3 ICLK			
0008 0028h	SYSTEM	PLL Control Register	PLLCR	16	16	3 ICLK			
0008 002Ah	SYSTEM	PLL Control Register 2	PLLCR2	8	8	3 ICLK			
0008 0030h	SYSTEM	External Bus Clock Control Register	BCKCR	8	8	3 ICLK			Not present in versions with 64 or 48 pins.
0008 0032h	SYSTEM	Main Clock Oscillator Control Register	MOSCCR	8	8	3 ICLK			
0008 0034h	SYSTEM	Low-Speed On-Chip Oscillator Control Register	LOCOCR	8	8	3 ICLK			
0008 0035h	SYSTEM	IWDT-Dedicated On-Chip Oscillator Control Register	ILOCOCR	8	8	3 ICLK			
0008 0040h	SYSTEM	Oscillation Stop Detection Control Register	OSTDCR	8	8	3 ICLK			
0008 0041h	SYSTEM	Oscillation Stop Detection Status Register	OSTDSR	8	8	3 ICLK			
0008 00A2h	SYSTEM	Main Clock Oscillator Wait Control Register	MOSCWTCR	8	8	3 ICLK		Low Power Consumption	
0008 00A6h	SYSTEM	PLL Wait Control Register	PLLWTCR	8	8	3 ICLK			
0008 00C0h	SYSTEM	Reset Status Register 2	RSTSR2	8	8	3 ICLK		Resets	
0008 00C2h	SYSTEM	Software Reset Register	SWRR	16	16	3 ICLK			
0008 00E0h	SYSTEM	Voltage Monitoring 1 Circuit Control Register 1	LVD1CR1	8	8	3 ICLK		LVDA	
0008 00E1h	SYSTEM	Voltage Monitoring 1 Circuit Status Register	LVD1SR	8	8	3 ICLK			
0008 00E2h	SYSTEM	Voltage Monitoring 2 Circuit Control Register 1	LVD2CR1	8	8	3 ICLK			
0008 00E3h	SYSTEM	Voltage Monitoring 2 Circuit Status Register	LVD2SR	8	8	3 ICLK			
0008 03FEh	SYSTEM	Protect Register	PRCR	16	16	3 ICLK		Register Write Protection Function	
0008 1300h	BSC	Bus Error Status Clear Register	BERCLR	8	8	2 ICLK		Buses	
0008 1304h	BSC	Bus Error Monitoring Enable Register	BEREN	8	8	2 ICLK			
0008 1308h	BSC	Bus Error Status Register 1	BERSR1	8	8	2 ICLK			
0008 130Ah	BSC	Bus Error Status Register 2	BERSR2	16	16	2 ICLK			
0008 1310h	BSC	Bus Priority Control Register	BUSPRI	16	16	2 ICLK			
0008 2000h	DMAC0	DMA Source Address Register	DMSAR	32	32	2 ICLK		DMACA	
0008 2004h	DMAC0	DMA Destination Address Register	DMDAR	32	32	2 ICLK			
0008 2008h	DMAC0	DMA Transfer Count Register	DMCRA	32	32	2 ICLK			
0008 200Ch	DMAC0	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK			
0008 2010h	DMAC0	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK			
0008 2013h	DMAC0	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK			
0008 2014h	DMAC0	DMA Address Mode Register	DMAMD	16	16	2 ICLK			
0008 2018h	DMAC0	DMA Offset Register	DMOFR	32	32	2 ICLK			
0008 201Ch	DMAC0	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK			
0008 201Dh	DMAC0	DMA Software Start Register	DMREQ	8	8	2 ICLK			
0008 201Eh	DMAC0	DMA Status Register	DMSTS	8	8	2 ICLK			

Table 4.1 List of I/O Registers (Address Order) (8/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 711Bh	ICU	DTC Activation Enable Register 027	DTCER027	8	8	2 ICLK		ICUb	
0008 711Ch	ICU	DTC Activation Enable Register 028	DTCER028	8	8	2 ICLK			
0008 711Dh	ICU	DTC Activation Enable Register 029	DTCER029	8	8	2 ICLK			
0008 711Eh	ICU	DTC Activation Enable Register 030	DTCER030	8	8	2 ICLK			
0008 711Fh	ICU	DTC Activation Enable Register 031	DTCER031	8	8	2 ICLK			
0008 7121h	ICU	DTC Activation Enable Register 033	DTCER033	8	8	2 ICLK			Not present in versions with 112, 100, 64 or 48 pins.
0008 7122h	ICU	DTC Activation Enable Register 034	DTCER034	8	8	2 ICLK			Not present in versions with 112, 100, 64 or 48 pins.
0008 7127h	ICU	DTC Activation Enable Register 039	DTCER039	8	8	2 ICLK			
0008 7128h	ICU	DTC Activation Enable Register 040	DTCER040	8	8	2 ICLK			
0008 712Ah	ICU	DTC Activation Enable Register 042	DTCER042	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 712Bh	ICU	DTC Activation Enable Register 043	DTCER043	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7131h	ICU	DTC Activation Enable Register 049	DTCER049	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7132h	ICU	DTC Activation Enable Register 050	DTCER050	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7133h	ICU	DTC Activation Enable Register 051	DTCER051	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7134h	ICU	DTC Activation Enable Register 052	DTCER052	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7135h	ICU	DTC Activation Enable Register 053	DTCER053	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7136h	ICU	DTC Activation Enable Register 054	DTCER054	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7137h	ICU	DTC Activation Enable Register 055	DTCER055	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7138h	ICU	DTC Activation Enable Register 056	DTCER056	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 713Ah	ICU	DTC Activation Enable Register 058	DTCER058	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 713Bh	ICU	DTC Activation Enable Register 059	DTCER059	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 713Ch	ICU	DTC Activation Enable Register 060	DTCER060	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 713Dh	ICU	DTC Activation Enable Register 061	DTCER061	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 713Eh	ICU	DTC Activation Enable Register 062	DTCER062	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7140h	ICU	DTC Activation Enable Register 064	DTCER064	8	8	2 ICLK			
0008 7141h	ICU	DTC Activation Enable Register 065	DTCER065	8	8	2 ICLK			
0008 7142h	ICU	DTC Activation Enable Register 066	DTCER066	8	8	2 ICLK			
0008 7143h	ICU	DTC Activation Enable Register 067	DTCER067	8	8	2 ICLK			
0008 7144h	ICU	DTC Activation Enable Register 068	DTCER068	8	8	2 ICLK			
0008 7145h	ICU	DTC Activation Enable Register 069	DTCER069	8	8	2 ICLK			
0008 7146h	ICU	DTC Activation Enable Register 070	DTCER070	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7147h	ICU	DTC Activation Enable Register 071	DTCER071	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7162h	ICU	DTC Activation Enable Register 098	DTCER098	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7166h	ICU	DTC Activation Enable Register 102	DTCER102	8	8	2 ICLK			
0008 7167h	ICU	DTC Activation Enable Register 103	DTCER103	8	8	2 ICLK			
0008 7168h	ICU	DTC Activation Enable Register 104	DTCER104	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7169h	ICU	DTC Activation Enable Register 105	DTCER105	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 717Eh	ICU	DTC Activation Enable Register 126	DTCER126	8	8	2 ICLK			

Table 4.1 List of I/O Registers (Address Order) (16/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 8330h	RIIC1	I²C Bus Bit Rate Low-Level Register	ICBRL	8	8	2, 3 PCLKB	2 ICLK	RIIC	Not present in versions with 112, 100, 64, or 48 pins.
0008 8331h	RIIC1	I²C Bus Bit Rate High-Level Register	ICBRH	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
0008 8332h	RIIC1	I²C Bus Transmit Data Register	ICDRT	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
0008 8333h	RIIC1	I²C Bus Receive Data Register	ICDRR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
0008 8380h	RSPI0	RSPI Control Register	SPCR	8	8	2, 3 PCLKB	2 ICLK	RSPI	
0008 8381h	RSPI0	RSPI Slave Select Polarity Register	SSLP	8	8	2, 3 PCLKB	2 ICLK		
0008 8382h	RSPI0	RSPI Pin Control Register	SPPCR	8	8	2, 3 PCLKB	2 ICLK		
0008 8383h	RSPI0	RSPI Status Register	SPSR	8	8	2, 3 PCLKB	2 ICLK		
0008 8384h	RSPI0	RSPI Data Register	SPDR	32	16, 32	2, 3 PCLKB	2 ICLK		
0008 8388h	RSPI0	RSPI Sequence Control Register	SPSCR	8	8	2, 3 PCLKB	2 ICLK		
0008 8389h	RSPI0	RSPI Sequence Status Register	SPSSR	8	8	2, 3 PCLKB	2 ICLK		
0008 838Ah	RSPI0	RSPI Bit Rate Register	SPBR	8	8	2, 3 PCLKB	2 ICLK		
0008 838Bh	RSPI0	RSPI Data Control Register	SPDCR	8	8	2, 3 PCLKB	2 ICLK		
0008 838Ch	RSPI0	RSPI Clock Delay Register	SPCKD	8	8	2, 3 PCLKB	2 ICLK		
0008 838Dh	RSPI0	RSPI Slave Select Negation Delay Register	SSLND	8	8	2, 3 PCLKB	2 ICLK		
0008 838Eh	RSPI0	RSPI Next-Access Delay Register	SPND	8	8	2, 3 PCLKB	2 ICLK		
0008 838Fh	RSPI0	RSPI Control Register 2	SPCR2	8	8	2, 3 PCLKB	2 ICLK		
0008 8390h	RSPI0	RSPI Command Register 0	SPCMD0	16	16	2, 3 PCLKB	2 ICLK		
0008 8392h	RSPI0	RSPI Command Register 1	SPCMD1	16	16	2, 3 PCLKB	2 ICLK		
0008 8394h	RSPI0	RSPI Command Register 2	SPCMD2	16	16	2, 3 PCLKB	2 ICLK		
0008 8396h	RSPI0	RSPI Command Register 3	SPCMD3	16	16	2, 3 PCLKB	2 ICLK		
0008 8398h	RSPI0	RSPI Command Register 4	SPCMD4	16	16	2, 3 PCLKB	2 ICLK		
0008 839Ah	RSPI0	RSPI Command Register 5	SPCMD5	16	16	2, 3 PCLKB	2 ICLK		
0008 839Ch	RSPI0	RSPI Command Register 6	SPCMD6	16	16	2, 3 PCLKB	2 ICLK		
0008 839Eh	RSPI0	RSPI Command Register 7	SPCMD7	16	16	2, 3 PCLKB	2 ICLK		
0008 83A0h	RSPI1	RSPI Control Register	SPCR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 83A1h	RSPI1	RSPI Slave Select Polarity Register	SSLP	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 83A2h	RSPI1	RSPI Pin Control Register	SPPCR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 83A3h	RSPI1	RSPI Status Register	SPSR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 83A4h	RSPI1	RSPI Data Register	SPDR	32	16, 32	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 83A8h	RSPI1	RSPI Sequence Control Register	SPSCR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 83A9h	RSPI1	RSPI Sequence Status Register	SPSSR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 83AAh	RSPI1	RSPI Bit Rate Register	SPBR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 83ABh	RSPI1	RSPI Data Control Register	SPDCR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 83ACh	RSPI1	RSPI Clock Delay Register	SPCKD	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 83ADh	RSPI1	RSPI Slave Select Negation Delay Register	SSLND	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 83AEh	RSPI1	RSPI Next-Access Delay Register	SPND	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 83AFh	RSPI1	RSPI Control Register 2	SPCR2	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 83B0h	RSPI1	RSPI Command Register 0	SPCMD0	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.

Table 4.1 List of I/O Registers (Address Order) (28/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 C293h	SYSTEM	Main Clock Oscillator Forced Oscillation Control Register	MOFCR	8	8	4, 5 PCLKB	2, 3 ICLK	Clock Generation Circuit	
0008 C296h	FLASH	Flash P/E Protection Register	FWEPROR	8	8	4, 5 PCLKB	2, 3 ICLK	ROM	
0008 C297h	SYSTEM	Voltage Monitoring Circuit Control Register	LVCMPCR	8	8	4, 5 PCLKB	2, 3 ICLK	LVDA	
0008 C298h	SYSTEM	Voltage Detection Level Select Register	LVDLVLR	8	8	4, 5 PCLKB	2, 3 ICLK		
0008 C29Ah	SYSTEM	Voltage Monitoring 1 Circuit Control Register 0	LVD1CR0	8	8	4, 5 PCLKB	2, 3 ICLK		
0008 C29Bh	SYSTEM	Voltage Monitoring 2 Circuit Control Register 0	LVD2CR0	8	8	4, 5 PCLKB	2, 3 ICLK		
0008 C2A0h to 0008 C2BFh	SYSTEM	Deep Standby Backup Register 0 to 31	DPSBKR0 to 31	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption	
0008 C300h	ICU	Group 0 Interrupt Source Register	GRP00	32	32	1, 2 PCLKB	2 ICLK	ICUb	Not present in versions with 64 or 48 pins.
0008 C330h	ICU	Group 12 Interrupt Source Register	GRP12	32	32	1, 2 PCLKB	2 ICLK		
0008 C340h	ICU	Group 0 Interrupt Enable Register	GEN00	32	32	1, 2 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C370h	ICU	Group 12 Interrupt Enable Register	GEN12	32	32	1, 2 PCLKB	2 ICLK		
0008 C380h	ICU	Group 0 Interrupt Clear Register	GCR00	32	32	1, 2 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C4C0h	POE	Input Level Control/Status Register 1	ICSR1	16	8, 16	2, 3 PCLKB	2 ICLK	POE3	
0008 C4C2h	POE	Output Level Control/Status Register 1	OCSR1	16	8, 16	2, 3 PCLKB	2 ICLK		
0008 C4C4h	POE	Input Level Control/Status Register 2	ICSR2	16	8, 16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C4C6h	POE	Output Level Control/Status Register 2	OCSR2	16	8, 16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C4C8h	POE	Input Level Control/Status Register 3	ICSR3	16	8, 16	2, 3 PCLKB	2 ICLK		
0008 C4CAh	POE	Software Port Output Enable Register	SPOER	8	8	2, 3 PCLKB	2 ICLK		
0008 C4CBh	POE	Port Output Enable Control Register 1	POECR1	8	8	2, 3 PCLKB	2 ICLK		
0008 C4CCh	POE	Port Output Enable Control Register 2	POECR2	16	16	2, 3 PCLKB	2 ICLK		
0008 C4CEh	POE	Port Output Enable Control Register 3	POECR3	16	16	2, 3 PCLKB	2 ICLK		
0008 C4D0h	POE	Port Output Enable Control Register 4	POECR4	16	16	2, 3 PCLKB	2 ICLK		
0008 C4D2h	POE	Port Output Enable Control Register 5	POECR5	16	16	2, 3 PCLKB	2 ICLK		
0008 C4D4h	POE	Port Output Enable Control Register 6	POECR6	16	16	2, 3 PCLKB	2 ICLK		
0008 C4D6h	POE	Input Level Control/Status Register 4	ICSR4	16	8, 16	2, 3 PCLKB	2 ICLK		
0008 C4D8h	POE	Input Level Control/Status Register 5	ICSR5	16	8, 16	2, 3 PCLKB	2 ICLK		
0008 C4DAh	POE	Active Level Setting Register 1	ALR1	16	8, 16	2, 3 PCLKB	2 ICLK		
0008 C4DCh	POE	Input Level Control/Status Register 6	ICSR6	16	16	2, 3 PCLKB	2 ICLK		
0008 C4DEh	POE	Active Level Setting Register 2	ALR2	16	8, 16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C4E0h	POE	Input Level Control/Status Register 7	ICSR7	16	8, 16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C4E2h	POE	Port Output Enable Control Register 7	POECR7	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C4E4h	POE	Port Output Enable Control Register 8	POECR8	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0009 1200h to 0009 13FFh	CAN1	Mailbox Register 0 to 31	MB0 to 31	128	8, 16, 32	2, 3 PCLKB	2 ICLK	CAN	Not present in versions with 64 or 48 pins.
0009 1400h to 0009 141Ch	CAN1	Mask Register 0 to 7	MKR0 to 7	32	8, 16, 32	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0009 1420h	CAN1	FIFO Received ID Compare Register 0 and 1	FIDCR0	32	8, 16, 32	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0009 1424h	CAN1	FIFO Received ID Compare Register 0 and 1	FIDCR1	32	8, 16, 32	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0009 1428h	CAN1	Mask Invalid Register	MKIVLR	32	8, 16, 32	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0009 142Ch	CAN1	Mailbox Interrupt Enable Register	MIER	32	8, 16, 32	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0009 1820h to 0009 183Fh	CAN1	Message Control Register 0 to 31	MCTL0 to 31	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.

5. Electrical Characteristics [144-, 120-, 112- and 100-Pin Versions]

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

Conditions: VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V

Item		Symbol	Value	Unit
Power supply voltage		VCC, PLLVCC	–0.3 to +6.5	V
USB power supply voltage		VCC_USB*1	–0.3 to +6.5	V
Analog power supply voltage		AVCC0, AVCC*2	–0.3 to +6.5	V
Reference power supply voltage		VREFH0*2	–0.3 to AVCC0 + 0.3	V
		VREF*2	–0.3 to AVCC0 + 0.3	V
Input voltage (except for ports 4 to 6, C, USB0_DP, and USB0_DM)		V_{in}	–0.3 to VCC + 0.3	V
Input voltage (USB0_DP and USB0_DM)		V_{in}	–0.3 to VCC_USB + 0.3	V
Input voltage (port 4)		V_{in}	–0.3 to AVCC0 + 0.3	V
Input voltage (ports 5, 6, and C)		V_{in}	–0.3 to AVCC + 0.3	V
Analog input voltage (port 4)		V_{AN}	–0.3 to AVCC0 + 0.3	V
Analog input voltage (ports 5, 6, and C)		V_{AN}	–0.3 to AVCC + 0.3	V
Operating temperature	D version product	T_{opr}	–40 to +85	ºC
	G version product	T_{opr}	–40 to +105	ºC
Storage temperature		T_{stg}	–55 to +125	ºC

Caution: Permanent damage to the LSI may result if absolute maximum ratings are exceeded.

Note 1. When the USB is not in use, do not leave the VCC_USB and VSS_USB pins open.
Connect the VCC_USB pin to VCC, and the VSS_USB pin to VSS, respectively.

Note 2. When the A/D converter is not in use, do not leave the AVCC0, VREFH0, VREFL0, AVSS0, AVCC, VREF, and AVSS pins open.
- When the 12-bit A/D converter is not in use
  Connect the AVCC0 pin to AVCC, the VREFH0 pin to VREF, and the AVSS0 and VREFL0 pins to AVSS, respectively.
- When the 10-bit A/D converter is not in use
  Connect the AVCC pin to AVCC0, the VREF pin to VREFH0, and the AVSS pin to AVSS0, respectively.
- When the 12-bit A/D converter and 10-bit A/D converter are not in use
  Connect the AVCC0, VREFH0, AVCC, and VREF pins to VCC, and the AVSS0, VREFL0, and AVSS pins to VSS, respectively.

Table 5.16 Timing of On-Chip Peripheral Modules (3)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS =PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

High drive output is selected by the drive capacity control register.

Item				Symbol	Min.	Max.	Unit*1	Test Conditions
RSPI	RSPCK clock cycle	Master		t_{SPcyc}	2	4096	t_{Pcyc}	C = 30 pF, Figure 5.32
		Slave			8	4096		
	RSPCK clock high pulse width	Master		t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2 - 3$	—	ns	
		Slave			$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2$	—		
	RSPCK clock low pulse width	Master		t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2 - 3$	—	ns	
		Slave			$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2$	—		
	RSPCK clock rise/fall time	Output		t_{SPCKR}, t_{SPCKF}	—	5	ns	
		Input			—	1	µs	
	RSPCK clock fall time	Input		t_{SPCKF}	—	0.1	µs/V	
	Data input setup time	Master		t_{SU}	4	—	ns	C = 30 pF, Figure 5.33 to Figure 5.40
		Slave			$20 - t_{Pcyc}$	—		
	Data input hold time	Master	PCLKB division ratio set to a value other than 1/2	t_H	t_{Pcyc}	—	ns	
			PCLKB division ratio set to 1/2	t_{HF}	0	—		
		Slave		t_H	$20 + 2 \times t_{Pcyc}$	—		
	SSL setup time	Master		t_{LEAD}	1	8	t_{SPcyc}	
		Slave			4	—	t_{Pcyc}	
	SSL hold time	Master		t_{LAG}	1	8	t_{SPcyc}	
		Slave			4	—	t_{Pcyc}	
	Data output delay time	Master		t_{OD}	—	10	ns	
		Slave			—	$3 \times t_{Pcyc} + 40$		
	Data output hold time	Master		t_{OH}	0	—	ns	
		Slave			0	—		
	Successive transmission delay time	Master		t_{TD}	$t_{SPcyc} + 2 \times t_{Pcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	ns	
		Slave			$4 \times t_{Pcyc}$	—		
	MOSI and MISO rise/fall time	Output		t_{DR}, t_{DF}	—	5	ns	
		Input			—	1	µs	
	SSL rise/fall time	Output		t_{SSLr}, t_{SSLf}	—	15	ns	
		Input			—	1	µs	
	Slave access time			t_{SA}	—	4	t_{Pcyc}	Figure 5.39 and Figure 5.40
	Slave output release time			t_{REL}	—	3	t_{Pcyc}	

Note 1. t_{Pcyc}: PCLK cycle

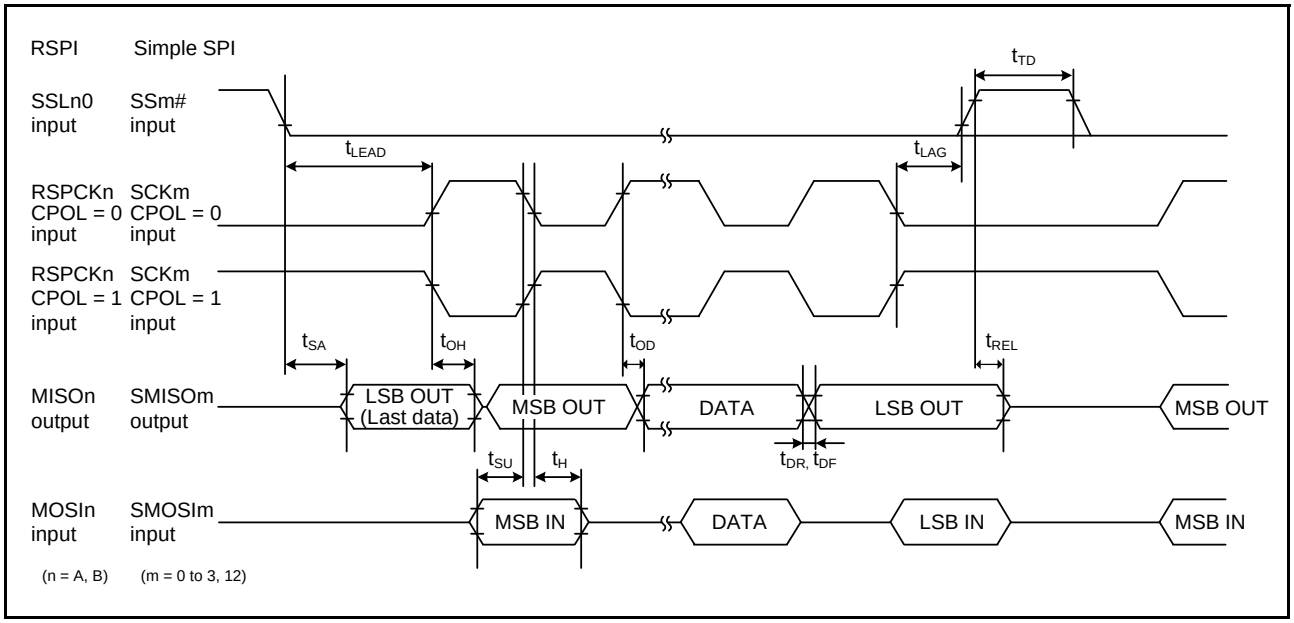
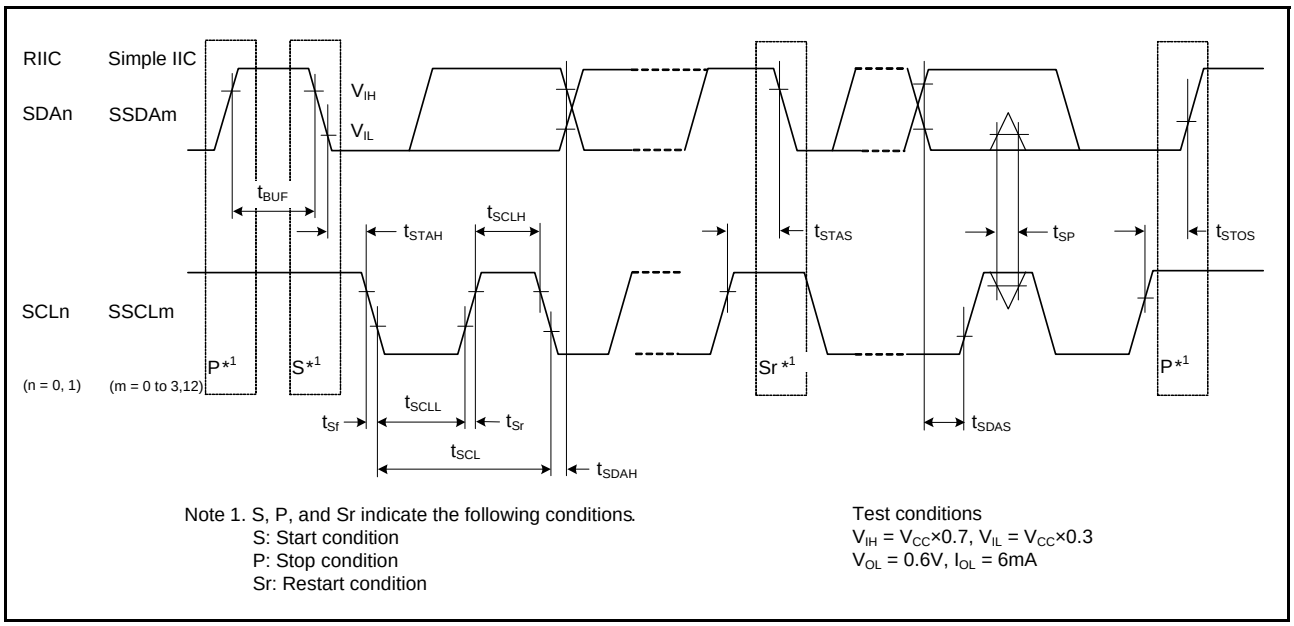


Figure 5.35 RSPI Timing (Slave, CPHA = 1) and Simple SPI Timing (Slave, CKPH = 0)



Note 1. S, P, and Sr indicate the following conditions.
S: Start condition
P: Stop condition
Sr: Restart condition

Test conditions
$V_{IH} = V_{CC} \times 0.7$, $V_{IL} = V_{CC} \times 0.3$
$V_{OL} = 0.6V$, $I_{OL} = 6mA$

Figure 5.36 RIIC Bus Interface Input/Output Timing and Simple IIC Bus Interface Input/Output Timing

Table 5.21 12-Bit A/D Conversion Characteristics (1)

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

$T_a = T_{opr}$

Item		Min.	Typ.	Max.	Unit	Test Conditions
Resolution		12	12	12	Bit	
Conversion time*1 (ADCLK = 25 MHz)	Without 0.1-µF external capacitor Permissible signal source impedance (max.) = 1.0 kΩ	2.0	—	—	µs	Sampling in 20 states
Analog input capacitance		—	—	8	pF	
Sample and hold circuit in use	Integral nonlinearity error	—	—	±4.0	LSB	AVin = 0.25 to AV_{REFH}–0.25
	Offset error	—	—	±4.0	LSB	
	Full-scale error	—	—	±4.0	LSB	
	Quantization error	—	±0.5	—	LSB	
	Absolute accuracy	—	—	±8.0	LSB	
Sample and hold circuit not in use	Integral nonlinearity error	—	—	±3.0	LSB	AVin = AV_{REFL} to AV_{REFH}
	Offset error	—	—	±3.0	LSB	
	Full-scale error	—	—	±3.0	LSB	
	Quantization error	—	±0.5	—	LSB	
	Absolute accuracy	—	—	±6.0	LSB	

Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Table 5.22 12-Bit A/D Conversion Characteristics (2)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” and “Condition 2” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 2: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. T_a is common to conditions 2 and 3.

Item		Min.	Typ.	Max.	Unit	Test Conditions
Resolution		12	12	12	Bit	
Conversion time*1 (ADCLK = 50 MHz)	Without 0.1-µF external capacitor Permissible signal source impedance (max.) = 1.0 kΩ	1.0	—	—	µs	Sampling in 20 states
Analog input capacitance		—	—	6	pF	
Sample and hold circuit in use	Integral nonlinearity error	—	—	±6.0	LSB	AVin = 0.25 to AV_{REFH}–0.25
	Offset error	—	—	±6.0	LSB	
	Full-scale error	—	—	±6.0	LSB	
	Quantization error	—	±0.5	—	LSB	
	Absolute accuracy	—	—	±8.0	LSB	
Sample and hold circuit not in use	Integral nonlinearity error	—	—	±3.0	LSB	AVin = AV_{REFL} to AV_{REFH}
	Offset error	—	—	±3.0	LSB	
	Full-scale error	—	—	±3.0	LSB	
	Quantization error	—	±0.5	—	LSB	
	Absolute accuracy	—	—	±6.0	LSB	

Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

6. Electrical Characteristics [64- and 48-Pin Versions]

6.1 Absolute Maximum Ratings

Table 6.1 Absolute Maximum Ratings

Item		Symbol	Value	Unit
Power supply voltage		VCC	–0.3 to +4.6	V
Input voltage (except for ports for 5 V tolerant*1 and port 4)		Vin	–0.3 to VCC+0.3	V
Input voltage (port 4)		Vin	–0.3 to AVCC0+0.3	V
Input voltage (ports for 5 V tolerant)*1		Vin	–0.3 to +5.8	V
Analog power supply voltage		AVCC0*2	–0.3 to +4.6	V
Reference power supply voltage		VREFH0*2	–0.3 to AVCC0+0.3	V
Analog input voltage (port 4)		V_{AN}	–0.3 to AVCC0+0.3	V
Operating temperature	D version product	Topr	–40 to +85	°C
	G version product	Topr	–40 to +105	°C
Storage temperature		Tstg	–55 to +125	°C

Caution: Permanent damage to the LSI may result if absolute maximum ratings are exceeded.

Note 1. Ports 0, 1, 2, 3, 7, 9, A, B, and D are 5 V tolerant.

Note 2. When the A/D converter is not in use, do not leave the AVCC0, VREFH0, VREFL0, and AVSS0 pins open. Connect the AVCC0 and VREFH0 pins to VCC, and the AVSS0 and VREFL0 pins to VSS, respectively.

6.2 DC Characteristics

Table 6.2 DC Characteristics (1)

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	IRQ input pin MTU3 input pin POE3 input pin SCI input pin A/D trigger input pin GPT input pin RES#, NMI	V_{IH}	VCC × 0.8	—	VCC + 0.3	V	
		V_{IL}	–0.3	—	VCC × 0.2		
		ΔV_T	VCC × 0.06	—	—		
	RIIC input pin (IICBus operating)	V_{IH}	VCC × 0.7	—	5.8		
		V_{IL}	–0.3	—	VCC × 0.3		
		ΔV_T	VCC × 0.05	—	—		
	Port 4 (also used as an analog port)	V_{IH}	AVCC0 × 0.8	—	AVCC0 + 0.3		
		V_{IL}	–0.3	—	AVCC0×0.2		
	Ports for 5 V tolerant*1	V_{IH}	VCC × 0.8	—	5.8		
		V_{IL}	–0.3	—	VCC × 0.2		
Input high voltage (except for Schmitt trigger input pin)	MD pin, EMLE	V_{IH}	VCC × 0.9	—	VCC + 0.3		
	EXTAL, TCK, RSPI input pin		VCC × 0.8	—	VCC + 0.3		
	RIIC input pin (SMBus operating)		2.1	—	VCC + 0.3		
Input low voltage (except for Schmitt trigger input pin)	MD pin, EMLE	V_{IL}	–0.3	—	VCC × 0.1		
	EXTAL, TCK, RSPI input pin		–0.3	—	VCC × 0.2		
	RIIC input pin (SMBus operating)		–0.3	—	0.8		
Output high voltage	All output pins	V_{OH}	VCC – 0.5	—	—	V	I_{OH} = –1 mA
Output low voltage	All output pins (except for RIIC pins)	V_{OL}	—	—	0.5	V	I_{OL} = 1.0 mA
	RIIC pins		—	—	0.4		I_{OL} = 3 mA
			—	—	0.6		I_{OL} = 6 mA
Input leakage current	RES#, MD pin, EMLE, Ports 4 and PE2	$\lvert I_{in} \rvert$	—	—	1.0	µA	V_{in} = 0V, V_{in} = VCC
Three-state leakage current (off state)	Ports for 5V tolerant	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	V_{in} = 0V, V_{in} = 5.5 V
			—	—	5.0		
Input capacitance	All input pins (except for ports PB1 and PB2)	C_{in}	—	—	15	pF	V_{in} = 0V, f = 1 MHz, T_a = 25ºC
	Ports PB1 and PB2		—	—	30		

Note 1. Ports 0, 1, 2, 3, 7, 9, A, B, and D are 5 V tolerant.

6.3 AC Characteristics

Table 6.6 Operation Frequency Value

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item		Symbol	Min.	Typ	Max.	Unit
Operation frequency	System clock (ICLK)	f	—	—	100	MHz
	Peripheral module clock PCLK		—	—	50	
	Timer module clock (PCLKA)		—	—	100	
	S12AD clock (PCLKD)		—	—	50	
	Flash clock (FCLK)		—*1	—	50	

Note 1. The FCLK must run at a frequency of at least 4 MHz when changing the ROM or E2 DataFlash memory contents.

6.3.1 Clock Timing

Table 6.7 Clock Timing

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item		Symbol	Min	Typ	Max.	Unit	Test Conditions
EXTAL external clock input cycle time		t_{EXcyc}	50	—	—	ns	Figure 6.1
EXTAL external clock input high pulse width		t_{EXH}	20	—	—	ns	
EXTAL external clock input low pulse width		t_{EXL}	20	—	—	ns	
EXTAL external clock rising time		t_{EXr}	—	—	5	ns	
EXTAL external clock falling time		t_{EXf}	—	—	5	ns	
EXTAL external clock input wait time*1		t_{EXWT}	1	—	—	ms	
Main clock oscillator oscillation frequency		f_{MAIN}	4	—	16	MHz	
Main clock oscillation stabilization time (crystal)		$t_{MAINOSC}$	—	—	—*2	ms	Figure 6.2
Main clock oscillation stabilization wait time (crystal)		$t_{MAINOSCWT}$	—	—	—*3	ms	
LOCO, IWDTCLK clock cycle time		t_{cyc}	6.96	8	9.4	µs	
LOCO, IWDTCLK clock oscillation frequency		f_{LOCO}	106.25	125	143.75	kHz	
LOCO, IWDTCLK clock oscillation stabilization wait time		t_{LOCOWT}	—	—	20	µs	Figure 6.2
PLL clock oscillation stabilization time	PLL operation started after main clock oscillation has settled	t_{PLL1}	—	—	500	µs	Figure 6.4
PLL clock oscillation stabilization wait time		t_{PLLWT1}	—	—	—*4	ms	
PLL clock oscillation stabilization time PLL	PLL operation started before main clock oscillation has settled	t_{PLL2}	—	—	$t_{MAINOSC}$ + t_{PLL1}	ms	Figure 6.5
PLL clock oscillation stabilization wait time		t_{PLLWT2}	—	—	—*4	ms	

Note 1. This is the time until the clock is used after clearing the main clock oscillator stop bit (MOSCCR.MOSTP) to 0 (selecting operation).
Note 2. When using a main clock, ask the manufacturer of the oscillator to evaluate its oscillation. Refer to the results of evaluation provided by the manufacturer for the oscillation stabilization time.
Note 3. This is calculated from the formula below, where n is the number of cycles set by the MOSCWTCR.MSTS[4:0] bits.

$$t_{MAINOSCWT} = t_{MAINOSC} + \frac{n + 16384}{f_{MAIN}}$$

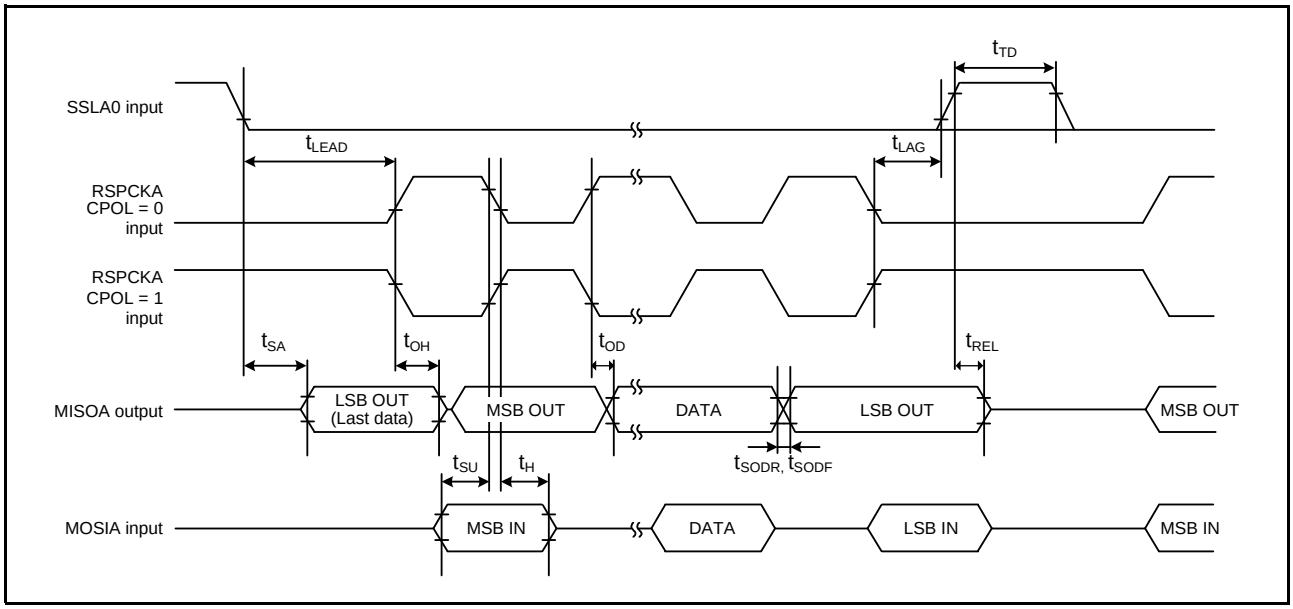
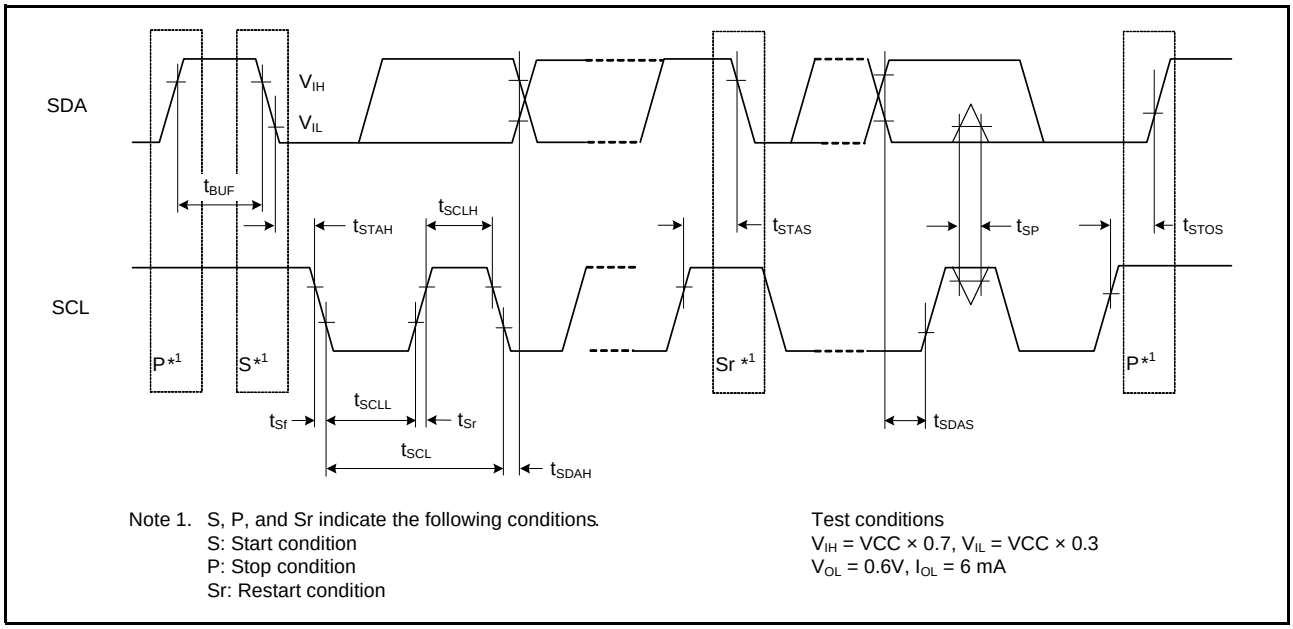


Figure 6.24 RSPI Timing (Slave, CPHA = 1) and Simple SPI Timing (Slave, CKPH = 0)



Note 1. S, P, and Sr indicate the following conditions.
S: Start condition
P: Stop condition
Sr: Restart condition

Test conditions
V_{IH} = VCC × 0.7, V_{IL} = VCC × 0.3
V_{OL} = 0.6V, I_{OL} = 6 mA

Figure 6.25 RIIC Bus Interface Input/Output Timing and Simple IIC Bus Interface Input/Output Timing

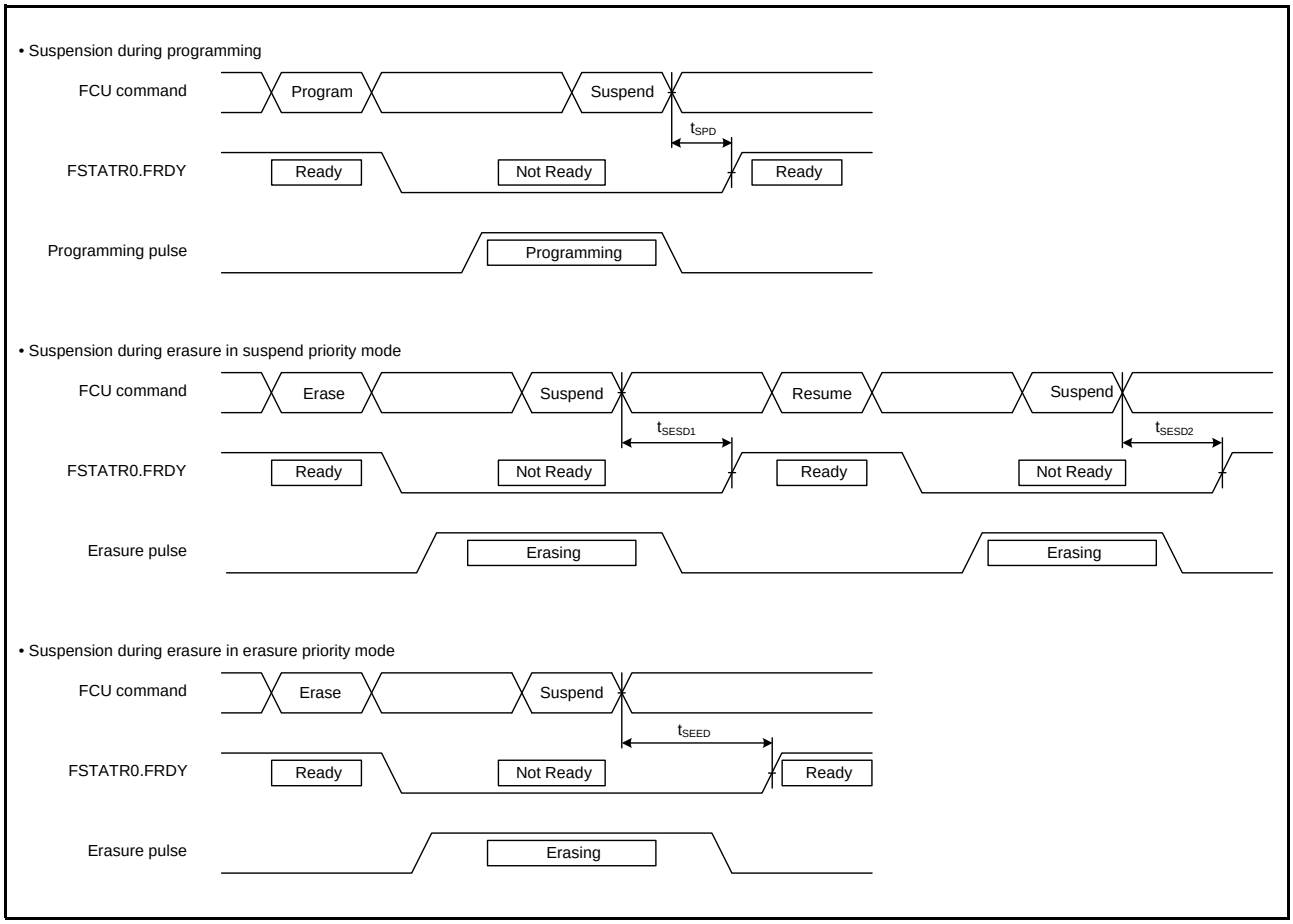
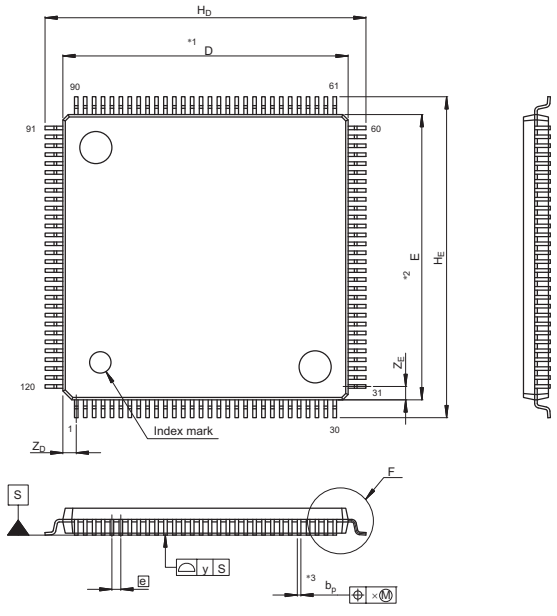
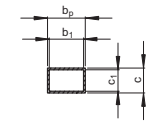


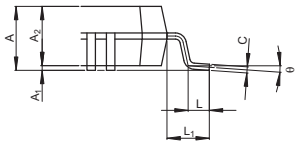
Figure 6.31 Flash Memory Program/Erase Suspend Timing

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP120-16x16-0.50	PLQP0120KA-A	—	0.9g





Terminal cross section



Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	15.9	16.0	16.1
E	15.9	16.0	16.1
A_2	—	1.4	—
H_D	17.8	18.0	18.2
H_E	17.8	18.0	18.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.17	0.22	0.27
b_1	—	0.20	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	0.75	—
Z_E	—	0.75	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure B 120-Pin LQFP (PLQP0120KA-A)