Renesas Electronics America Inc - R5F563TEBDFH#V1 Datasheet

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What is "Embedded - Microcontrollers"?

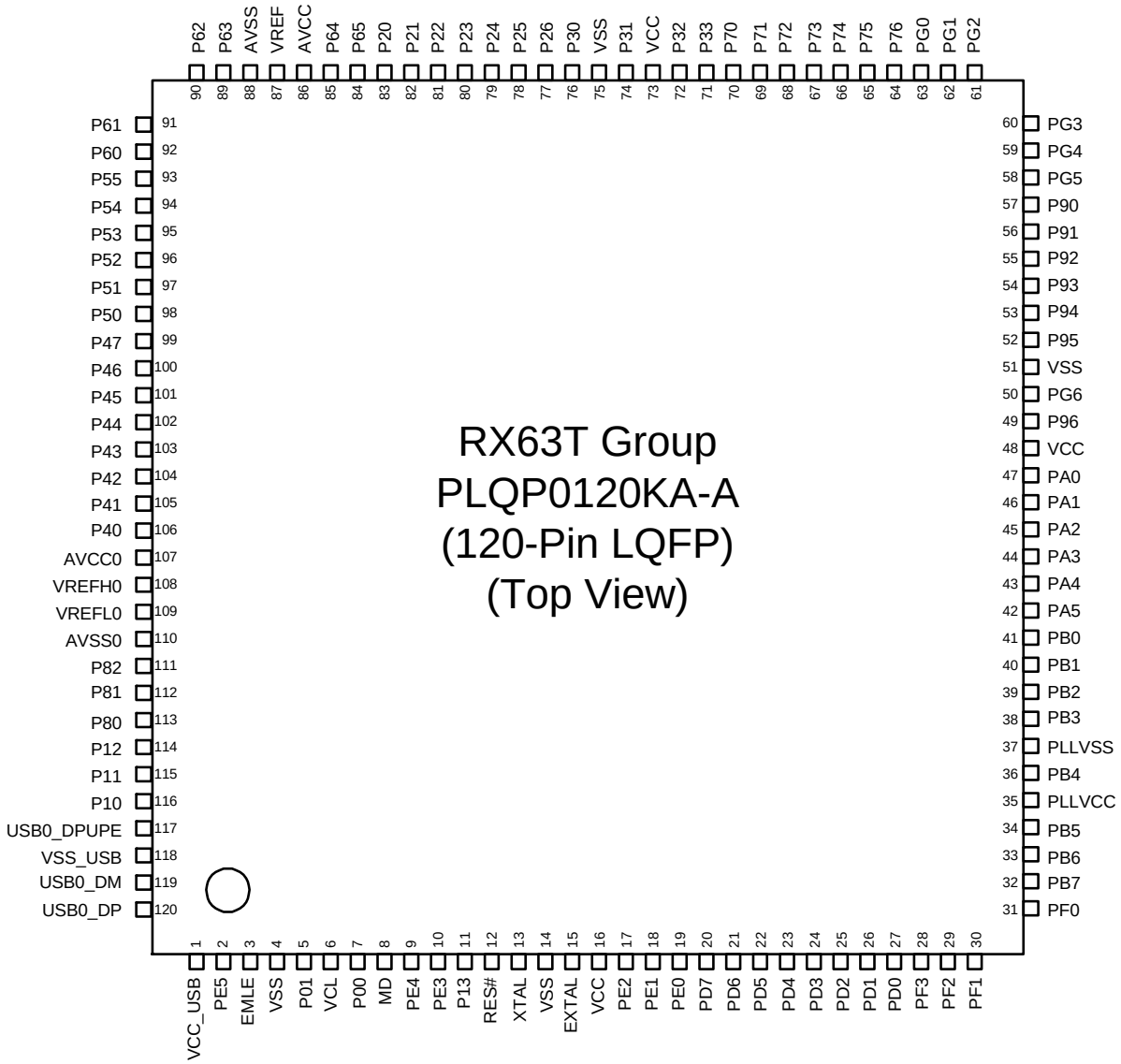
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	69
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 12x10b, 8x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f563tebdfh-v1

Table 1.1 Outline of Specifications (3/7)

Classification	Module/Function	Description
I/O ports	General I/O ports	• 144-pin LQFP I/O pins: 81 Input pins: 29 Open-drain outputs: 27 • 120-pin LQFP I/O pins: 72 Input pin: 21 Open-drain outputs: 26 • 112-pin LQFP I/O pins: 69 Input pins: 21 Open-drain outputs: 20 • 100-pin LQFP I/O pins: 57 Input pins: 21 Open-drain outputs: 16 • 64-pin LQFP I/O pins: 39 Input pins: 9 Open-drain outputs: 10 5-V tolerance: 39 • 48-pin LQFP I/O pins: 25 Input pins: 7 Open-drain outputs: 8 5-V tolerance: 25
Timers	Multi-function timer pulse unit 3 (MTU3)	• (16 bits × 8 channels) • Maximum of 16 pulse-input/output and 3 pulse-input possible • Select eight clocks from among ten count clocks (PCLKA/1, PCLKA/4, PCLKA/16, PCLKA/64, PCLKA/256, PCLKA/1024, MTCLKA, MTCLKB, MTCLKC, and MTCLKD) for each channel (seven clocks for channel 1, four clocks for channel 5, and six clocks for channel 6 or 7) • 24 output compare/input capture registers • Counter-clearing operation (simultaneous clearing on compare match or input capture) • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous input and output to registers in synchronization with counter operations • Buffer operation specifiable • Capable of cascade-connected operation • Interrupts: 38 sources • Automatic transfer of register data • Pulse output modes Topple, PWM, complementary PWM, and reset-synchronous PWM modes • Complementary PWM output mode Outputs non-overlapping waveforms for controlling 3-phase inverters Automatic specification of dead times PWM duty cycle: Selectable as any value from 0% to 100% Delay can be applied to requests for A/D conversion. Non-generation of interrupt requests at peak or trough values of counters can be selected. Double buffering • Reset-synchronous PWM mode Three PWM waveforms and corresponding inverse waveforms are output with the desired duty cycles. • Phase-counting mode • Counter functionality for dead-time compensation • Generation of triggers for A/D converters • Differential timing for initiation of A/D conversion
	Port output enable 3 (POE3)	• Control of the high-impedance state of the MTU3 and GPT's waveform output pins • Six pins for input from signal sources: POE0, POE4, POE8, POE10, POE11, and POE12 • Initiation on detection of short-circuited outputs (detection of PWM outputs having simultaneously become an active level.) • Initiation by comparator-detection, oscillation-stoppage detection, or software • Software control of the states of pins for output control can also be added.



Note: • This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.6, List of Pins and Pin Functions (120-Pin LQFP).

Figure 1.4 Pin Assignment (120-Pin LQFP)

Table 1.6 List of Pins and Pin Functions (120-Pin LQFP) (2/4)

Pin Number 120-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3, GPT, POE3, CAC)	Communications (SCIc, SCId, RSPI, RIIC, CAN, USB)	Interrupt	S12ADB, AD, DA
37	PLLVSS						
38		PB3	A15	MTIOC0A/CACREF	SCK0		
39		PB2		MTIOC0B	TXD0/SMOSI0/ SSDA0/SDA0		
40		PB1		MTIOC0C	RXD0/SMISO0/ SSCL0/SCL0	IRQ4	
41		PB0	A14	MTIOC0D	MOSIA/MOSIB		
42		PA5		MTIOC1A	RXD0/SMISO0/ SSCL0/ MISOA/MISOB		ADTRG1#
43		PA4		MTIOC1B	TXD0/SMOSI0/ SSDA0/RSPCKA/ RSPCKB		ADTRG0#
44		PA3		MTIOC2A	SCK0/SSLA0/SSLB0		
45		PA2		MTIOC2B	RXD2/SMISO2/ SSCL2/ SSLA1/SSLB1		
46		PA1		MTIOC6A	TXD2/SMOSI2/ SSDA2/SSLA2/SSLB2		
47		PA0		MTIOC6C	SCK2/SSLA3/SSLB3		
48	VCC						
49		P96	A13	POE4#	RXD1/SMISO1/SSCL1	IRQ4-DS	
50		PG6	CS2#		SCK1		
51	VSS						
52		P95		MTIOC6B/GTIOC4A	TXD1/SMOSI1/SSDA1		
53		P94		MTIOC7A/GTIOC5A	CTS1#/RTS1#/SS1#		
54		P93		MTIOC7B/GTIOC6A	CTS2#/RTS2#/SS2#		
55		P92		MTIOC6D/GTIOC4B			
56		P91		MTIOC7C/GTIOC5B			
57		P90		MTIOC7D/GTIOC6B			
58	TRCLK	PG5		POE12#	SCK3		ADTRG#
59	TRDATA3	PG4		GTIOC6B	RXD3/SMISO3/SSCL3	IRQ6	
60	TRDATA2	PG3		GTIOC6A	TXD3/SMOSI3/SSDA3		
61	TRDATA1	PG2			SCK2	IRQ2	
62	TRDATA0	PG1		GTIOC7B	RXD2/SMISO2/SSCL2	IRQ1	
63	TRSYNC	PG0		GTIOC7A	TXD2/SMOSI2/SSDA2	IRQ0	
64		P76	D0/[A0/D0]	MTIOC4D/GTIOC2B			
65		P75	D1/[A1/D1]	MTIOC4C/GTIOC1B			
66		P74	D2/[A2/D2]	MTIOC3D/GTIOC0B			
67		P73	D3/[A3/D3]	MTIOC4B/GTIOC2A			
68		P72	D4/[A4/D4]	MTIOC4A/GTIOC1A			
69		P71	D5/[A5/D5]	MTIOC3B/GTIOC0A			
70		P70	D6/[A6/D6]	POE0#	CTS1#/RTS1#/SS1#	IRQ5-DS	
71		P33	D7/[A7/D7]	MTIOC3A/MTCLKA	SSLA3/SSLB3		
72		P32	D8/[A8/D8]	MTIOC3C/MTCLKB	SSLA2/SSLB2		
73	VCC						
74		P31	D9/[A9/D9]	MTIOC0A/MTCLKC	SSLA1/SSLB1		

Table 1.8 List of Pins and Pin Functions (100-Pin LQFP) (3/3)

Pin Number 100-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3, GPT, POE3, CAC)	Communications (SCIc, SCId, RSPI, RIIC, CAN)	Interrupt	S12ADB, AD, DA
71	AVCC						
72	VREF						
73	AVSS						
74		P63	A2				AN3
75		P62	A3				AN2
76		P61	A4				AN1
77		P60	A5				AN0
78		P55					AN11/DA1
79		P54					AN10/ DA0
80		P53	A6				AN9
81		P52	A7				AN8
82		P51					AN7
83		P50					AN6
84		P47					AN103/ CVREFH
85		P46					AN102
86		P45					AN101
87		P44					AN100
88		P43					AN003/ CVREFL
89		P42					AN002
90		P41					AN001
91		P40					AN000
92	AVCC0						
93	VREFH0						
94	VREFL0						
95	AVSS0						
96		P82	WAIT#	MTIC5U	SCK12	IRQ3	
97		P81	A8	MTIC5V	TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12		
98		P80	A9	MTIC5W	RXD12/SMISO12/ SSCL12/RXDX12	IRQ5	
99		P11	ALE	MTCLKC		IRQ1-DS	
100		P10		MTCLKD		IRQ0-DS	

2. CPU

The RX CPU has sixteen general-purpose registers, nine control registers, and one accumulator used for DSP instructions.

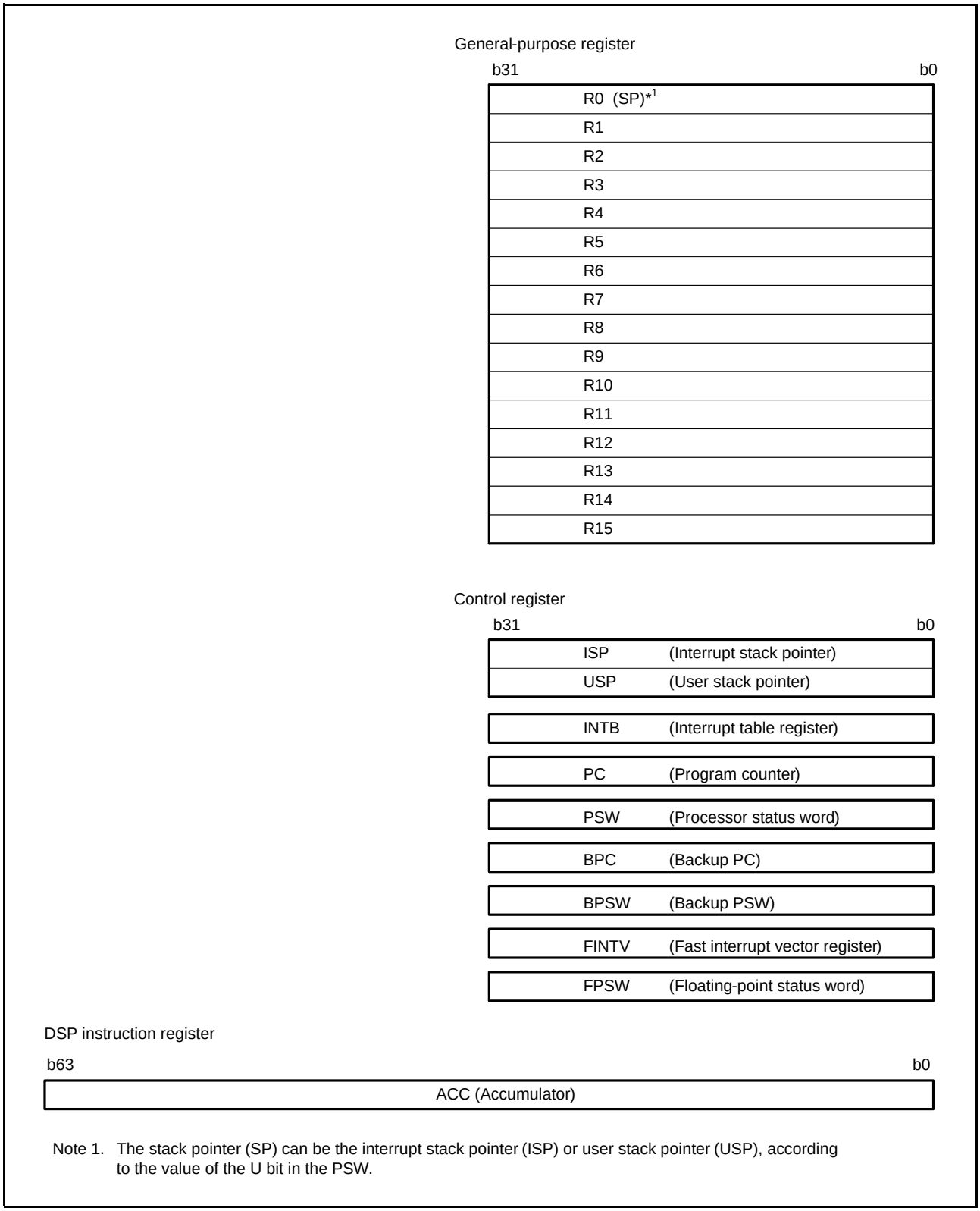


Figure 2.1 Register Set of the CPU

2.1 General-Purpose Registers (R0 to R15)

This CPU has sixteen general-purpose registers (R0 to R15). R1 to R15 can be used as data registers or address registers. R0, a general-purpose register, also functions as the stack pointer (SP).
The stack pointer is switched to operate as the interrupt stack pointer (ISP) or user stack pointer (USP) by the value of the stack pointer select bit (U) in the processor status word (PSW).

2.2 Control Registers

(1) Interrupt Stack Pointer (ISP)/User Stack Pointer (USP)

The stack pointer (SP) can be either of two types, the interrupt stack pointer (ISP) or the user stack pointer (USP). Whether the stack pointer operates as the ISP or USP depends on the value of the stack pointer select bit (U) in the processor status word (PSW).
Set the ISP or USP to a multiple of four, as this reduces the numbers of cycles required to execute interrupt sequences and instructions entailing stack manipulation.

(2) Interrupt Table Register (INTB)

The interrupt table register (INTB) specifies the address where the relocatable vector table starts.

(3) Program Counter (PC)

The program counter (PC) indicates the address of the instruction being executed.

(4) Processor Status Word (PSW)

The processor status word (PSW) indicates the results of instruction execution or the state of the CPU.

(5) Backup PC (BPC)

The backup PC (BPC) is provided to speed up response to interrupts.
After a fast interrupt has been generated, the contents of the program counter (PC) are saved in the BPC register.

(6) Backup PSW (BPSW)

The backup PSW (BPSW) is provided to speed up response to interrupts.
After a fast interrupt has been generated, the contents of the processor status word (PSW) are saved in the BPSW. The allocation of bits in the BPSW corresponds to that in the PSW.

(7) Fast Interrupt Vector Register (FINTV)

The fast interrupt vector register (FINTV) is provided to speed up response to interrupts.
The FINTV register specifies a branch destination address when a fast interrupt has been generated.

(8) Floating-Point Status Word (FPSW)

The floating-point status word (FPSW) indicates the results of floating-point operations.
When an exception handling enable bit (Ej) enables the exception handling (Ej = 1), the exception cause can be identified by checking the corresponding Cj flag in the exception handling routine. If the exception handling is masked (Ej = 0), the occurrence of exception can be checked by reading the Fj flag at the end of a series of processing. Once the Fj flag has been set to 1, this value is retained until it is cleared to 0 by software (j = X, U, Z, O, or V).

2.2.1 Register Associated with DSP Instructions

(1) Accumulator (ACC)

The accumulator (ACC) is a 64-bit register used for DSP instructions. The accumulator is also used for the multiply and multiply-and-accumulate instructions; EMUL, EMULU, FMUL, MUL, and RMPA, in which case the prior value in the accumulator is modified by execution of the instruction.
Use the MVTACHI and MVTACLO instructions for writing to the accumulator. The MVTACHI and MVTACLO instructions write data to the higher-order 32 bits (bits 63 to 32) and the lower-order 32 bits (bits 31 to 0), respectively.
Use the MVFACHI and MVFACMI instructions for reading data from the accumulator. The MVFACHI and MVFACMI instructions read data from the higher-order 32 bits (bits 63 to 32) and the middle 32 bits (bits 47 to 16), respectively.

Table 4.1 List of I/O Registers (Address Order) (22/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 B308h	SCI12	Noise Filter Setting Register	SNFR	8	8	2, 3 PCLKB	2 ICLK	SCIc, SCId	
0008 B309h	SCI12	I^2C Mode Register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK		
0008 B30Ah	SCI12	I^2C Mode Register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK		
0008 B30Bh	SCI12	I^2C Mode Register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK		
0008 B30Ch	SCI12	I^2C Status Register	SISR	8	8	2, 3 PCLKB	2 ICLK		
0008 B30Dh	SCI12	SPI Mode Register	SPMR	8	8	2, 3 PCLKB	2 ICLK		
0008 B320h	SCI12	Extended Serial Module Enable Register	ESMER	8	8	2, 3 PCLKB	2 ICLK		
0008 B321h	SCI12	Control Register 0	CR0	8	8	2, 3 PCLKB	2 ICLK		
0008 B322h	SCI12	Control Register 1	CR1	8	8	2, 3 PCLKB	2 ICLK		
0008 B323h	SCI12	Control Register 2	CR2	8	8	2, 3 PCLKB	2 ICLK		
0008 B324h	SCI12	Control Register 3	CR3	8	8	2, 3 PCLKB	2 ICLK		
0008 B325h	SCI12	Port Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK		
0008 B326h	SCI12	Interrupt Control Register	ICR	8	8	2, 3 PCLKB	2 ICLK		
0008 B327h	SCI12	Status Register	STR	8	8	2, 3 PCLKB	2 ICLK		
0008 B328h	SCI12	Status Clear Register	STCR	8	8	2, 3 PCLKB	2 ICLK		
0008 B329h	SCI12	Control Field 0 Data Register	CF0DR	8	8	2, 3 PCLKB	2 ICLK		
0008 B32Ah	SCI12	Control Field 0 Compare Enable Register	CF0CR	8	8	2, 3 PCLKB	2 ICLK		
0008 B32Bh	SCI12	Control Field 0 Receive Data Register	CF0RR	8	8	2, 3 PCLKB	2 ICLK		
0008 B32Ch	SCI12	Primary Control Field 1 Data Register	PCF1DR	8	8	2, 3 PCLKB	2 ICLK		
0008 B32Dh	SCI12	Primary Control Field 1 Data Register	SCF1DR	8	8	2, 3 PCLKB	2 ICLK		
0008 B32Eh	SCI12	Secondary Control Field 1 Data Register	CF1CR	8	8	2, 3 PCLKB	2 ICLK		
0008 B32Fh	SCI12	Control Field 1 Receive Data Register	CF1RR	8	8	2, 3 PCLKB	2 ICLK		
0008 B330h	SCI12	Timer Control Register	TCR	8	8	2, 3 PCLKB	2 ICLK		
0008 B331h	SCI12	Timer Mode Register	TMR	8	8	2, 3 PCLKB	2 ICLK		
0008 B332h	SCI12	Timer Prescaler Register	TPRE	8	8	2, 3 PCLKB	2 ICLK		
0008 B333h	SCI12	Timer Count Register	TCNT	8	8	2, 3 PCLKB	2 ICLK		
0008 C000h	PORT0	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports	Not present in versions with 48 pins.
0008 C001h	PORT1	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 48 pins.
0008 C002h	PORT2	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK		
0008 C003h	PORT3	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK		
0008 C007h	PORT7	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK		
0008 C008h	PORT8	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C009h	PORT9	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 48 pins.
0008 C00Ah	PORTA	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK		
0008 C00Bh	PORTB	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK		
0008 C00Dh	PORTD	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK		
0008 C00Eh	PORTE	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C00Fh	PORTF	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 100, 64, or 48 pins.
0008 C010h	PORTG	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 100, 64, or 48 pins.
0008 C020h	PORT0	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 48 pins.
0008 C021h	PORT1	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 48 pins.
0008 C022h	PORT2	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK		
0008 C023h	PORT3	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK		
0008 C027h	PORT7	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK		
0008 C028h	PORT8	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C029h	PORT9	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 48 pins.

Table 4.1 List of I/O Registers (Address Order) (25/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 C14Ch	MPC	P14 Pin Function Control Register	P14PFS	8	8	2, 3 PCLKB	2 ICLK	MPC	Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 C150h	MPC	P20 Pin Function Control Register	P20PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C151h	MPC	P21 Pin Function Control Register	P21PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C152h	MPC	P22 Pin Function Control Register	P22PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C153h	MPC	P23 Pin Function Control Register	P23PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C154h	MPC	P24 Pin Function Control Register	P24PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C155h	MPC	P25 Pin Function Control Register	P25PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
0008 C156h	MPC	P26 Pin Function Control Register	P26PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 112, 100, 64, or 48 pins.
0008 C158h	MPC	P30 Pin Function Control Register	P30PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C159h	MPC	P31 Pin Function Control Register	P31PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 48 pins.
0008 C15Ah	MPC	P32 Pin Function Control Register	P32PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 48 pins.
0008 C15Bh	MPC	P33 Pin Function Control Register	P33PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 48 pins.
0008 C15Ch	MPC	P34 Pin Function Control Register	P34PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 C15Dh	MPC	P35 Pin Function Control Register	P35PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 C160h	MPC	P40 Pin Function Control Register	P40PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C161h	MPC	P41 Pin Function Control Register	P41PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C162h	MPC	P42 Pin Function Control Register	P42PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C163h	MPC	P43 Pin Function Control Register	P43PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C164h	MPC	P44 Pin Function Control Register	P44PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C165h	MPC	P45 Pin Function Control Register	P45PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 48 pins.
0008 C166h	MPC	P46 Pin Function Control Register	P46PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 48 pins.
0008 C167h	MPC	P47 Pin Function Control Register	P47PFS	8	8	2, 3 PCLKB	2 ICLK		
0008 C168h	MPC	P50 Pin Function Control Register	P50PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C169h	MPC	P51 Pin Function Control Register	P51PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C16Ah	MPC	P52 Pin Function Control Register	P52PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C16Bh	MPC	P53 Pin Function Control Register	P53PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C16Ch	MPC	P54 Pin Function Control Register	P54PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C16Dh	MPC	P55 Pin Function Control Register	P55PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C16Eh	MPC	P56 Pin Function Control Register	P56PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 C16Fh	MPC	P57 Pin Function Control Register	P57PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 120, 112, 100, 64, or 48 pins.
0008 C170h	MPC	P60 Pin Function Control Register	P60PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C171h	MPC	P61 Pin Function Control Register	P61PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C172h	MPC	P62 Pin Function Control Register	P62PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 C173h	MPC	P63 Pin Function Control Register	P63PFS	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.

Table 4.1 List of I/O Registers (Address Order) (40/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
000C 2230h	GPT2	A/D Converter Start Request Timing Double-Buffer Register B	GTADTDBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK	GPT	
000C 2234h	GPT2	General PWM Timer Output Negate Control Register	GTONCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2236h	GPT2	General PWM Timer Dead Time Control Register	GTDTCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2238h	GPT2	General PWM Timer Dead Time Value Register U	GTDVU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 223Ah	GPT2	General PWM Timer Dead Time Value Register D	GTDVD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 223Ch	GPT2	General PWM Timer Dead Time Buffer Register U	GTDBU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 223Eh	GPT2	General PWM Timer Dead Time Buffer Register D	GTDBD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2240h	GPT2	General PWM Timer Output Protection Function Status Register	GTSOS	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2242h	GPT2	General PWM Timer Output Protection Function Temporary Release Register	GTSOTR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2280h	GPT3	General PWM Timer I/O Control Register	GTIOR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2282h	GPT3	General PWM Timer Interrupt Output Setting Register	GTINTAD	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2284h	GPT3	General PWM Timer Control Register	GTCR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2286h	GPT3	General PWM Timer Buffer Enable Register	GTBER	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2288h	GPT3	General PWM Timer Count Direction Register	GTUDC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 228Ah	GPT3	General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register	GTITC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 228Ch	GPT3	General PWM Timer Status Register	GTST	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 228Eh	GPT3	General PWM Timer Counter	GTCNT	16	16	2 to 5 PCLKA	2, 3 ICLK		
000C 2290h	GPT3	General PWM Timer Compare Capture Register A	GTCCRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2292h	GPT3	General PWM Timer Compare Capture Register B	GTCCRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2294h	GPT3	General PWM Timer Compare Capture Register C	GTCCRC	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2296h	GPT3	General PWM Timer Compare Capture Register D	GTCCRD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 2298h	GPT3	General PWM Timer Compare Capture Register E	GTCCRE	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 229Ah	GPT3	General PWM Timer Compare Capture Register F	GTCCRF	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 229Ch	GPT3	General PWM Timer Cycle Setting Register	GTPR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 229Eh	GPT3	General PWM Timer Cycle Setting Buffer Register	GTPBR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 22A0h	GPT3	General PWM Timer Cycle Setting Double-Buffer Register	GTPDBR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 22A4h	GPT3	A/D Converter Start Request Timing Register A	GTADTRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 22A6h	GPT3	A/D Converter Start Request Timing Buffer Register A	GTADTBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 22A8h	GPT3	A/D Converter Start Request Timing Double-Buffer Register A	GTADTDBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 22ACh	GPT3	A/D Converter Start Request Timing Register B	GTADTRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 22AEh	GPT3	A/D Converter Start Request Timing Buffer Register B	GTADTBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 22B0h	GPT3	A/D Converter Start Request Timing Double-Buffer Register B	GTADTDBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 22B4h	GPT3	General PWM Timer Output Negate Control Register	GTONCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 22B6h	GPT3	General PWM Timer Dead Time Control Register	GTDTCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		
000C 22B8h	GPT3	General PWM Timer Dead Time Value Register U	GTDVU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		

Table 5.3 DC Characteristics (2)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

The following relation applies when the USB is in use under condition 1 or condition 2: Vcc = PLLVcc = Vcc_USB = 3.0 to 3.6 V.

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output high voltage	All output pins (except for P52, P53, P60 to P65, P71 to P76, P90 to P95, and USB0_DPUPE)	V_{OH}	VCC – 0.5	—	—	V	I_{OH} = –1 mA
	P52, P53, and P60 to P65		AVCC – 0.5	—	—		I_{OH} = –1 mA
	USB0_DPUPE		VCC_USB – 0.5				I_{OH} = –1 mA
	P71 to P76, and P90 to P95		VCC – 1.0	—	—		I_{OH} = –5 mA
Output low voltage	All output pins (except for P71 to P76, P90 to P95, and RIIC pins)	V_{OL}	—	—	0.5	V	I_{OL} = 1.0 mA
	P71 to P76, and P90 to P95		—	—	1.1		I_{OL} = 15 mA
	RIIC pins		—	—	0.4		I_{OL} = 3 mA
			—	—	0.6		I_{OL} = 6 mA
Input leakage current	RES#, MD pin, EMLE, Port 4, Ports P50, P51, P54 to P57, and Port C	$\lvert I_{in} \rvert$	—	—	1.0	µA	V_{in} = 0 V, V_{in} = VCC
Three-state leakage current (off state)	Port 0, Port 1, Ports P20 to P24, Port 3, Ports P52, P53, Ports 6 to A, Ports PB0, PB3 to PB7, and Ports D to G	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	V_{in} = 0 V, V_{in} = VCC
	Ports P25, P26, PB1, and PB2		—	—	5.0		
Input capacitance	All output pins (except for P25, P26, PB1, and PB2)	C_{in}	—	—	15	pF	V_{in} = 0 V, f = 1 MHz, T_a = 25 ºC
	Ports P25, P26, PB1, and PB2		—	—	30		

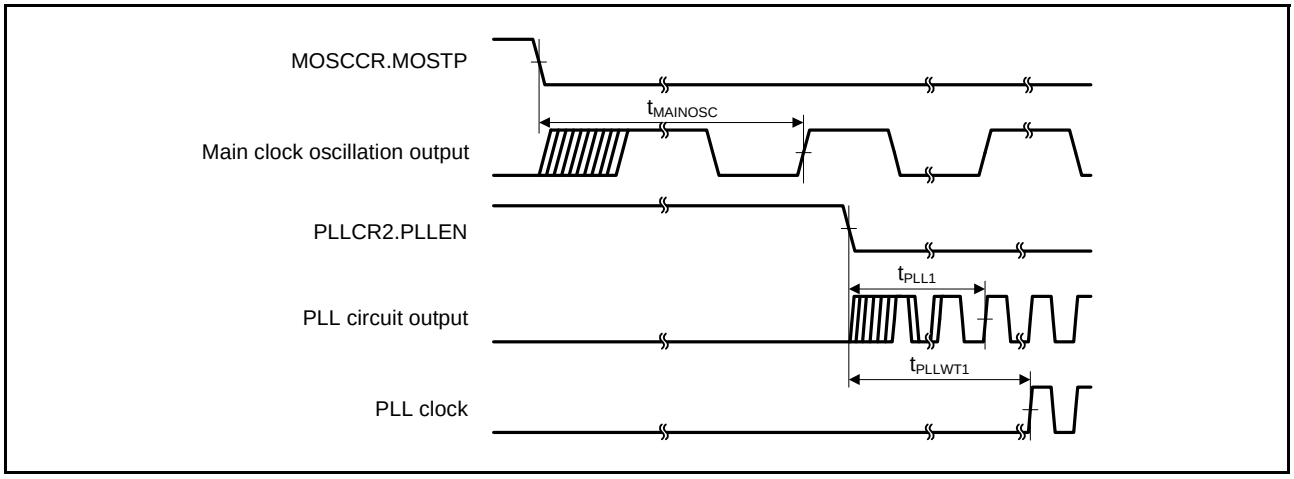


Figure 5.7 PLL Clock Oscillation Start Timing (PLL is Operated after Main Clock Oscillation Has Settled)

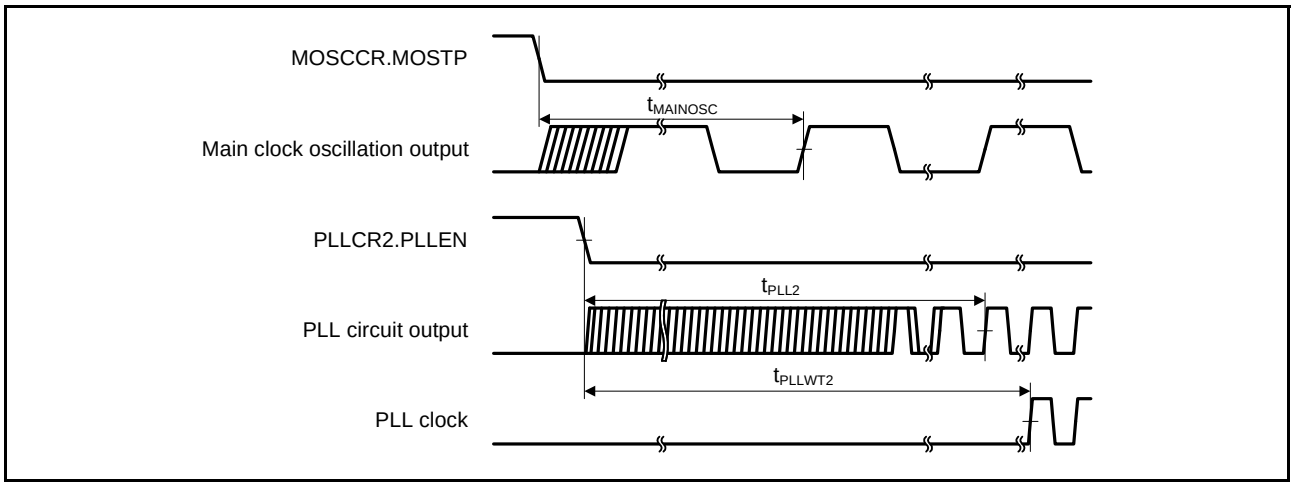


Figure 5.8 PLL Clock Oscillation Start Timing (PLL is Operated before Main Clock Oscillation Has Settled)

Table 5.16 Timing of On-Chip Peripheral Modules (2)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
SCI	Input clock cycle	Asynchronous	t_{Scyc}	4	—	t_{Pcyc}	C = 30 pF Figure 5.29
		Clock synchronous		6	—		
	Input clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time		t_{SCKr}	—	20	ns	
	Input clock fall time		t_{SCKf}	—	20	ns	
	Output clock cycle	Asynchronous	t_{Scyc}	16	—	t_{Pcyc}	
		Clock synchronous		4	—		
	Output clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time		t_{SCKr}	—	20	ns	
	Output clock fall time		t_{SCKf}	—	20	ns	
	Transmit data delay time	Clock synchronous	t_{TXD}	—	40	ns	Figure 5.30
	Receive data setup time	Clock synchronous	t_{RXS}	40	—	ns	
	Receive data hold time	Clock synchronous	t_{RXH}	40	—	ns	
	Receive data fall time		t_{TICTF}	—	0.1	µs/V	When Noise Cancellation Function is not used.
A/D converter	10-bit A/D converter trigger input pulse width		t_{TRGW}	1.5	—	t_{Pcyc}	Figure 5.31
	12-bit A/D converter trigger input pulse width			1.5	—		
CAC	CACREF input pulse width	$t_{Pcyc} \leq t_{cac}$*2	t_{CACREF}	4.5 t_{cac} + 3 t_{Pcyc}	—	ns	
		$t_{Pcyc} > t_{cac}$*2		5 t_{cac} + 6.5 t_{Pcyc}	—	ns	
	CACREF input fall time		$t_{CACREFTF}$	—	0.1	µs/V	

Note 1. t_{Pcyc}: PCLK cycle, t_{PAcye}: PCLKA cycle
Note 2. t_{cac}: CAC count clock source cycle.

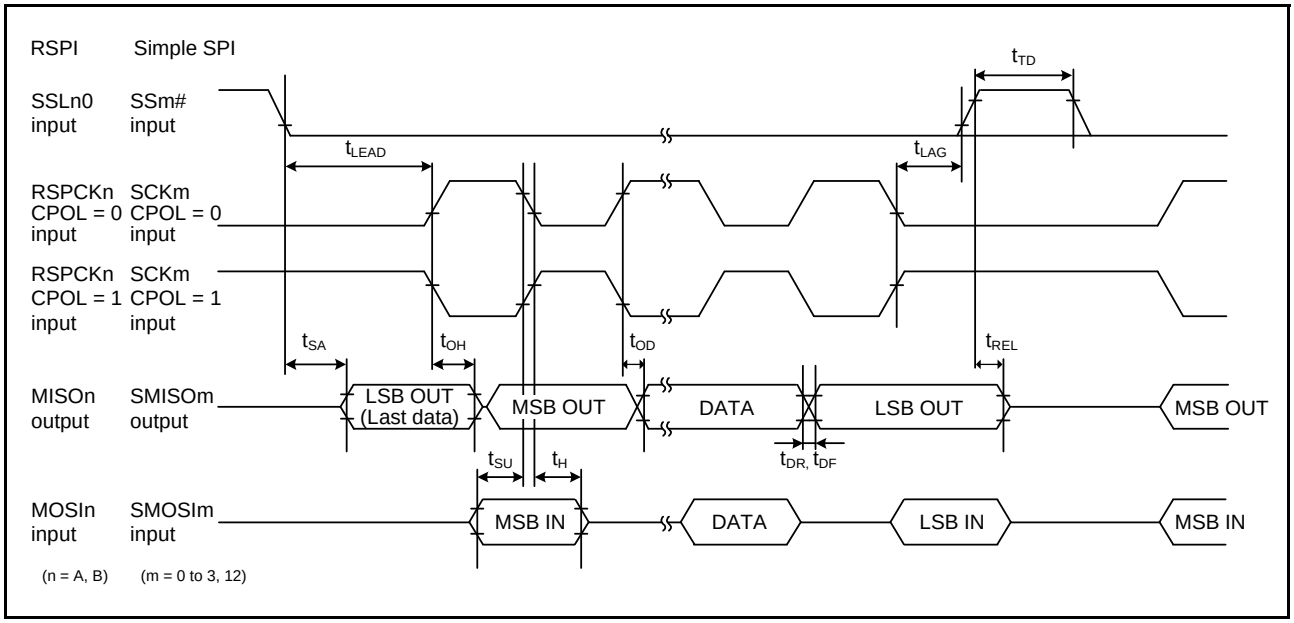
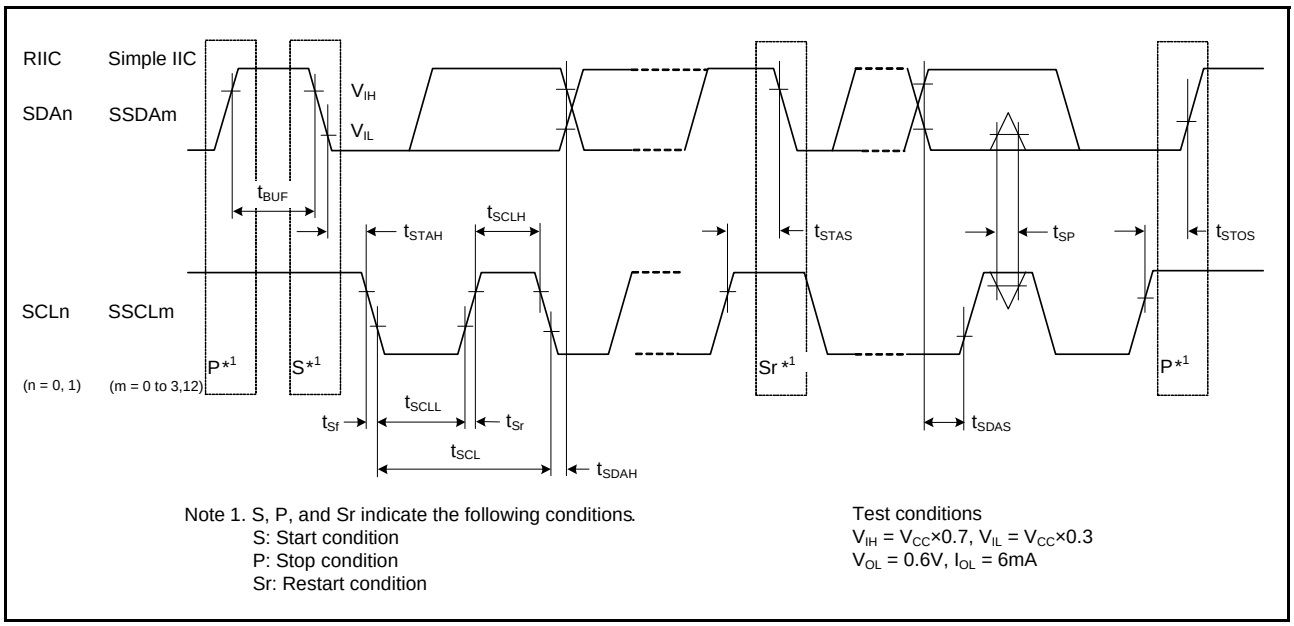


Figure 5.35 RSPI Timing (Slave, CPHA = 1) and Simple SPI Timing (Slave, CKPH = 0)



Note 1. S, P, and Sr indicate the following conditions.
S: Start condition
P: Stop condition
Sr: Restart condition

Test conditions
$V_{IH} = V_{CC} \times 0.7$, $V_{IL} = V_{CC} \times 0.3$
$V_{OL} = 0.6V$, $I_{OL} = 6mA$

Figure 5.36 RIIC Bus Interface Input/Output Timing and Simple IIC Bus Interface Input/Output Timing

5.7 Power-on Reset Circuit and Voltage Detection Circuit Characteristics

Table 5.26 Power-on Reset Circuit and Voltage Detection Circuit Characteristics (1)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” and “Condition 2” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. T_a is common to conditions 1 and 2.

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	V_{POR}	2.46	2.58	2.7	V	Figure 5.41
	Voltage detection circuit (LVD0)	V_{DET0}	2.7	2.82	2.94		Figure 5.42
	Voltage detection circuit (LVD1)*1	V_{DET1_8}	2.75	2.90	3.05		Figure 5.43
		V_{DET1_9}	2.70	2.85	3.00		
		V_{DET1_A}	2.73	2.88	3.03		
	Voltage detection circuit (LVD2)*2	V_{DET2_8}	2.75	2.9	3.05		Figure 5.44
		V_{DET2_9}	2.70	2.85	3.00		
		V_{DET2_A}	2.73	2.88	3.03		
Internal reset time	Power-on reset (POR)	t_{POR}		9.7		ms	Figure 5.41
	Voltage detection circuit (LVD0)	t_{LVD0}		9.7			Figure 5.42
	Voltage detection circuit (LVD1)	t_{LVD1}		0.9			Figure 5.43
	Voltage detection circuit (LVD2)	t_{LVD2}		0.9			Figure 5.44
Minimum VCC down time*3		t_{VOFF}	200	—	—	µs	Figure 5.41 and Figure 5.42
Response delay time		t_{DET}			200	µs	
LVD operation stabilization time (after LVD is enabled)		$Td_{(E-A)}$			3	µs	Figure 5.41 to Figure 5.44
Hysteresis width (LVD1 and LVD2)		V_{LVH}		80		mV	

Note 1. # in symbol $V_{DET1\_\#}$ indicates the value of the LVDLVLR.LVD1LVL[3:0] bits.
Note 2. # in symbol $V_{DET2\_\#}$ indicates the value of the LVDLVLR.LVD2LVL[3:0] bits.
Note 3. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{DET1}, and V_{DET2} for the POR/ LVD.

5.8 Oscillation Stop Detection Circuit Characteristics

Table 5.28 Oscillation Stop Detection Circuit Characteristics

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection time	t_{dr}	—	—	1.0	ms	Figure 5.43

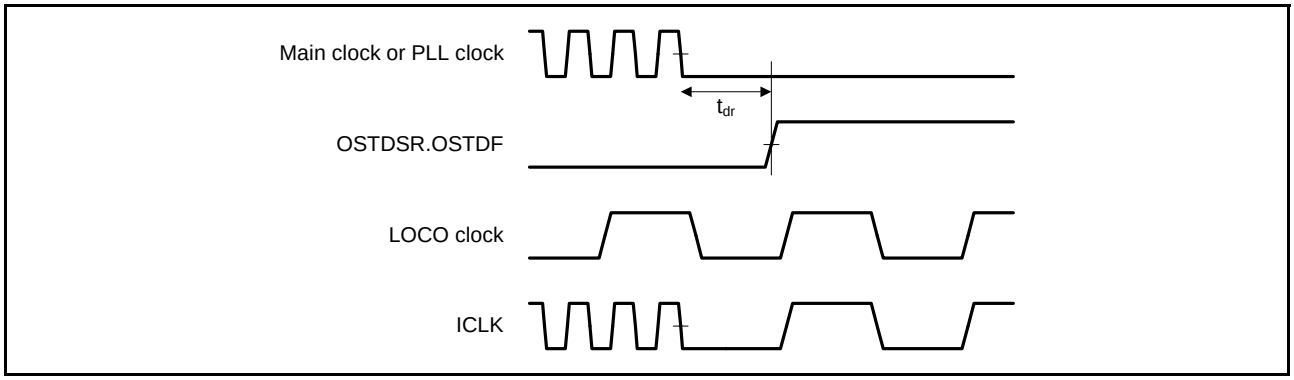


Figure 5.43 Oscillation Stop Detection Timing

Table 6.12 Timing of On-Chip Peripheral Modules (2)

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
RSPI	RSPCK clock cycle	Master	t_{SPcyc}	2	4096	t_{Pcyc}	Figure 6.20
		Slave		8	4096		
	RSPCK clock high pulse width	Master	t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2 - 3$	—	ns	
		Slave		$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2$	—		
	RSPCK clock low pulse width	Master	t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2 - 3$	—	ns	
		Slave		$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2$	—		
	RSPCK clock rise/fall time	Output	t_{SPCKR}, t_{SPCKF}	—	5	ns	
		Input		—	1	µs	
	Data input setup time	Master	t_{SU}	15	—	ns	Figure 6.21 to Figure 6.24
				20	—		
		Slave		$20 - t_{Pcyc}$	—		
	Data input hold time	Master	t_H	0	—	ns	
		Slave		$20 + 2 \times t_{Pcyc}$	—		
	SSL setup time	Master	t_{LEAD}	1	8	t_{SPcyc}	
		Slave		4	—	t_{Pcyc}	
	SSL hold time	Master	t_{LAG}	1	8	t_{SPcyc}	
		Slave		4	—	t_{Pcyc}	
	Data output delay time	Master	t_{OD}	—	18	ns	
		Slave		—	$3 \times t_{Pcyc} + 40$		
	Data output hold time	Master	t_{OH}	0	—	ns	
		Slave		0	—		
	Successive transmission delay time	Master	t_{TD}	$t_{SPcyc} + 2 \times t_{Pcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	ns	
		Slave		$4 \times t_{Pcyc}$	—		
	MOSI rise/fall time	Output	t_{MODR}, t_{MODF}	—	5	ns	
		Input		—	1	µs	
	MISO rise/fall time	Output	t_{MODR}, t_{MODF}	—	5	ns	
		Input		—	1	µs	
	SSL rise/fall time	Output	t_{SSLr}, t_{SSLf}	—	15	ns	
		Input		—	1	µs	
	Slave access time		t_{SA}	—	4	t_{Pcyc}	Figure 6.23 and Figure 6.24
	Slave output release time		t_{REL}	—	3	t_{Pcyc}	

Note 1. t_{Pcyc}: PCLK cycle

Table 6.14 Timing of On-Chip Peripheral Modules (4)

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item		Symbol	Min.	Max.	Unit	Test Conditions
RIIC (Standard-mode)	SCL input cycle time	t_{SCL}	6(12) × t_{IICcyc} + 1300	—	ns	Figure 6.25
	SCL input high pulse width	t_{SCLH}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA input rise time	t_{Sr}	—	1000	ns	
	SCL, SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	3(6) × t_{IICcyc} + 300	—	ns	
	Start condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Restart condition input setup time	t_{STAS}	1000	—	ns	
	Stop condition input setup time	t_{STOS}	1000	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
RIIC (Fast-mode)	SCL input cycle time	t_{SCL}	6(12) × t_{IICcyc} + 600	—	ns	
	SCL input high pulse width	t_{SCLH}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA input rise time	t_{Sr}	20 + 0.1C_b	300	ns	
	SCL, SDA input fall time	t_{Sf}	20 + 0.1C_b	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	3(6) × t_{IICcyc} + 300	—	ns	
	Start condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Restart condition input setup time	t_{STAS}	300	—	ns	
	Stop condition input setup time	t_{STOS}	300	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note 1. t_{IICcyc}: RIIC internal reference clock (IICϕ) Cycle
Note 2. The value within parentheses is applicable when the value of the ICMR3.NF[1:0] bits is 11b while the digital filter is enabled by the setting ICFER.NFE = 1.
Note 3. Cb is the total capacitance of the bus lines.

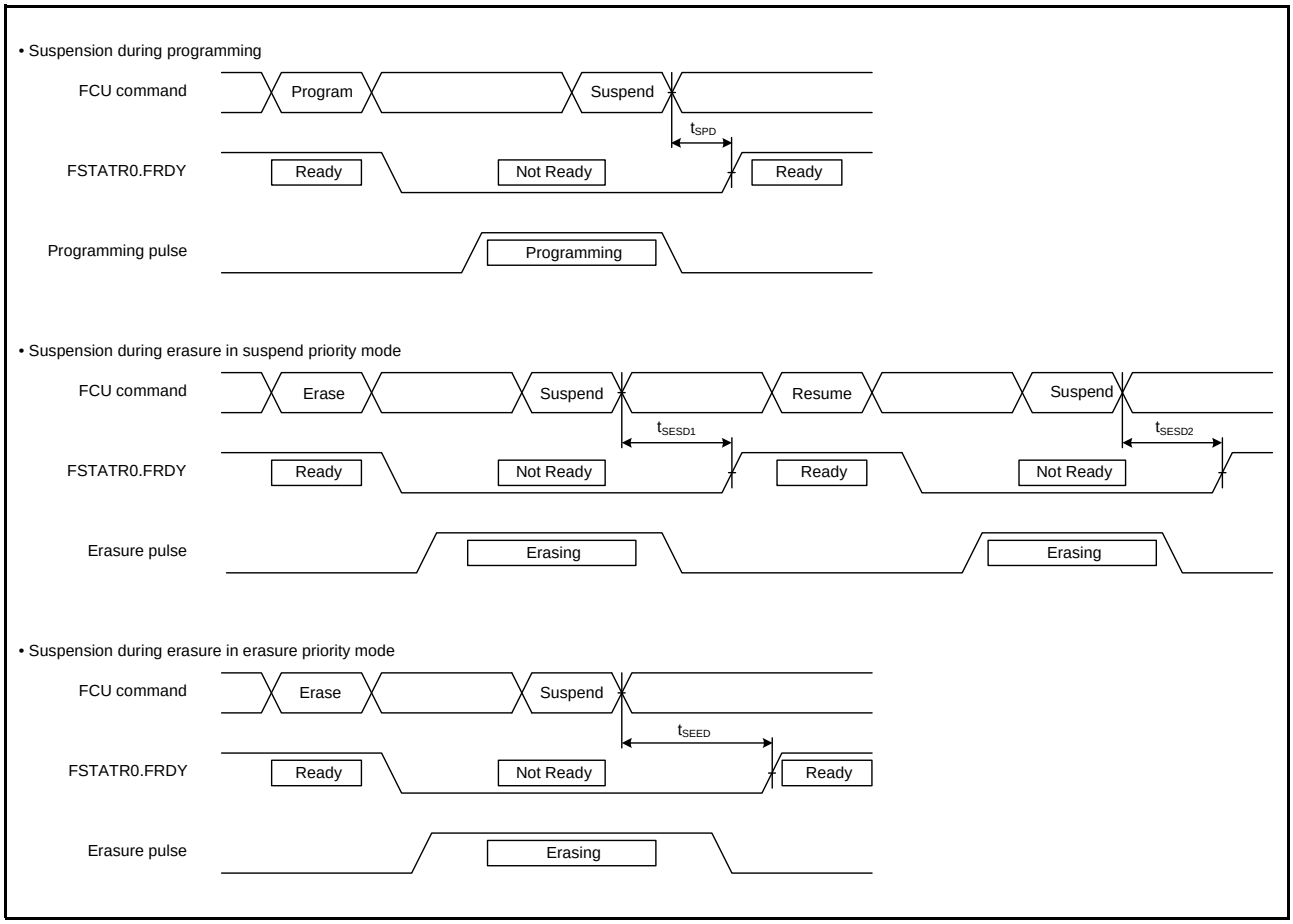
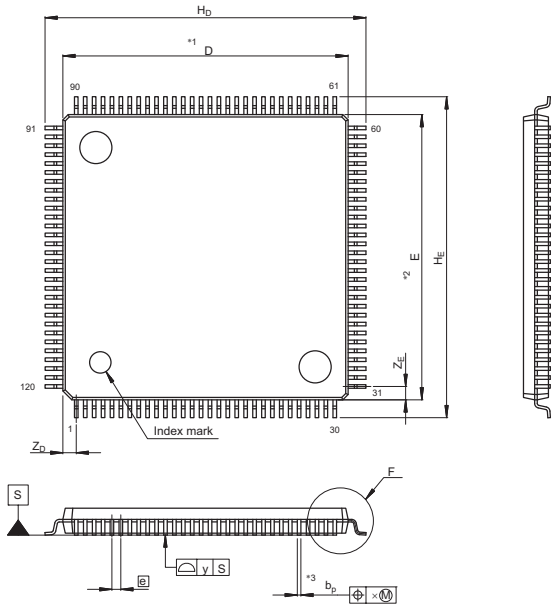
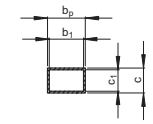


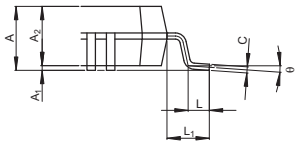
Figure 6.31 Flash Memory Program/Erase Suspend Timing

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP120-16x16-0.50	PLQP0120KA-A	—	0.9g





Terminal cross section



Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	15.9	16.0	16.1
E	15.9	16.0	16.1
A_2	—	1.4	—
H_D	17.8	18.0	18.2
H_E	17.8	18.0	18.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.17	0.22	0.27
b_1	—	0.20	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	0.75	—
Z_E	—	0.75	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure B 120-Pin LQFP (PLQP0120KA-A)