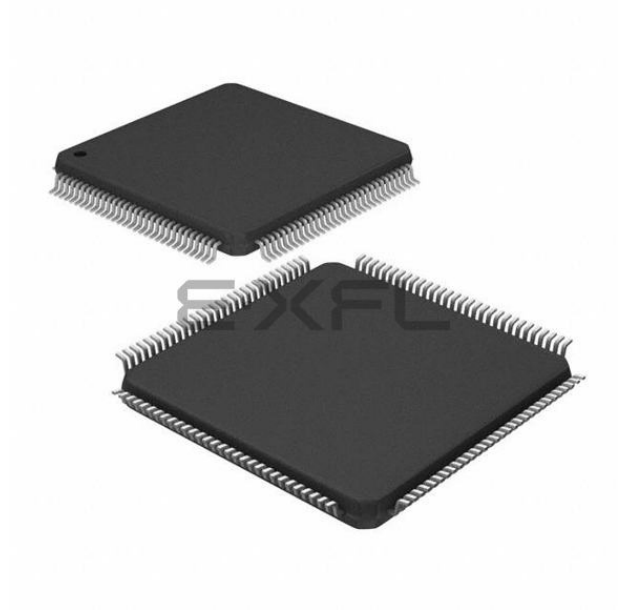
# Renesas Electronics America Inc - R5F563TEDDFA#V0 Datasheet



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## Applications of "Embedded - Microcontrollers"

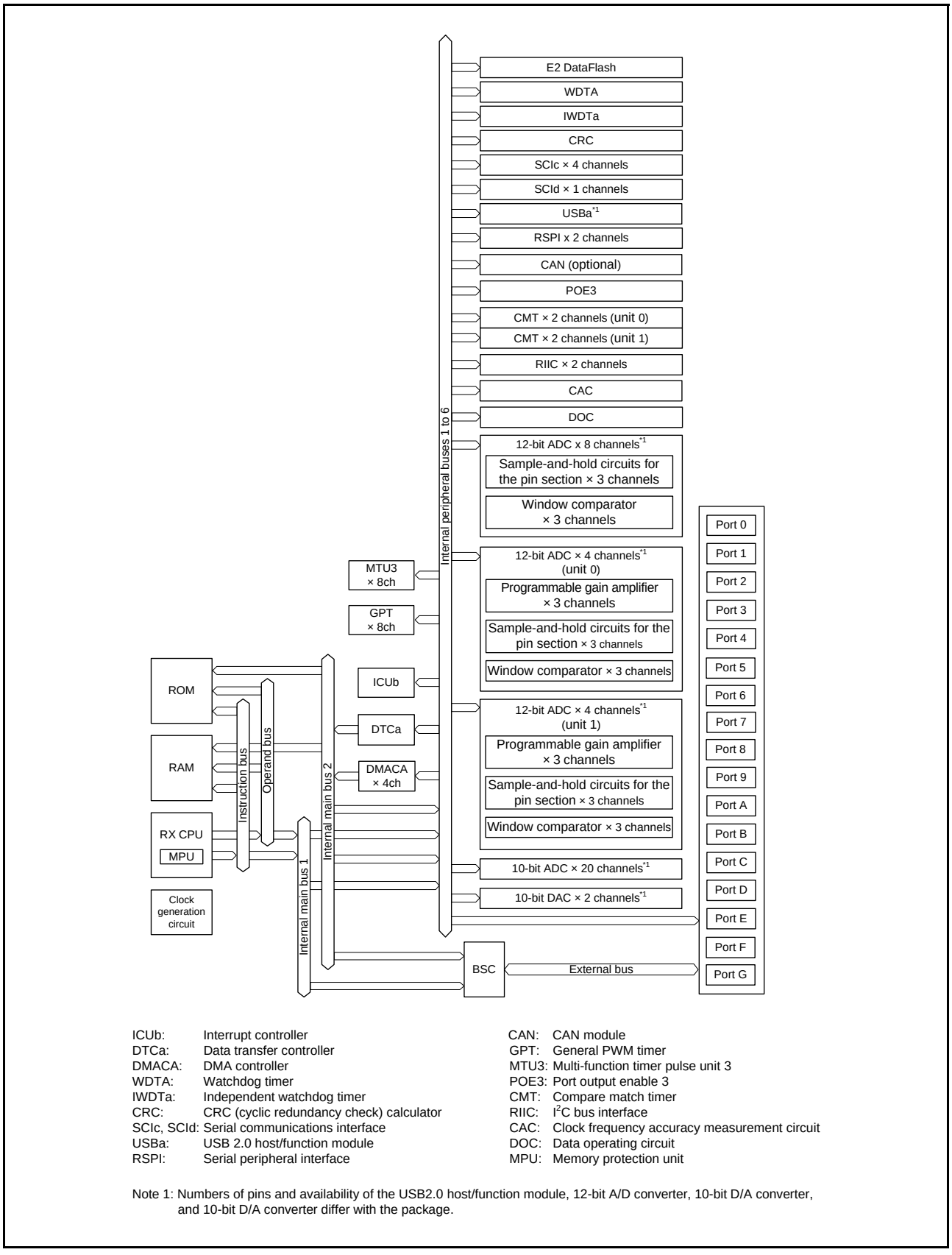
| Details | |
|---|---|
| Product Status | Not For New Designs |
| Core Processor | RX |
| Core Size | 32-Bit Single-Core |
| Speed | 100MHz |
| Connectivity | EBI/EMI, I²C, LINbus, SCI, SPI |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 72 |
| Program Memory Size | 512KB (512K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 32K x 8 |
| RAM Size | 48K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 5.5V |
| Data Converters | A/D 12x10b, 8x12b; D/A 2x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 120-LQFP |
| Supplier Device Package | 120-LQFP (16x16) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f563teddfa-v0 |

**Table 1.1 Outline of Specifications (3/7)**

| Classification | Module/Function | Description |
|---|---|---|
| I/O ports | General I/O ports | • 144-pin LQFP<br>I/O pins: 81<br>Input pins: 29<br>Open-drain outputs: 27<br>• 120-pin LQFP<br>I/O pins: 72<br>Input pin: 21<br>Open-drain outputs: 26<br>• 112-pin LQFP<br>I/O pins: 69<br>Input pins: 21<br>Open-drain outputs: 20<br>• 100-pin LQFP<br>I/O pins: 57<br>Input pins: 21<br>Open-drain outputs: 16<br>• 64-pin LQFP<br>I/O pins: 39<br>Input pins: 9<br>Open-drain outputs: 10<br>5-V tolerance: 39<br>• 48-pin LQFP<br>I/O pins: 25<br>Input pins: 7<br>Open-drain outputs: 8<br>5-V tolerance: 25 |
| Timers | Multi-function timer pulse unit 3 (MTU3) | • (16 bits × 8 channels)<br>• Maximum of 16 pulse-input/output and 3 pulse-input possible<br>• Select eight clocks from among ten count clocks (PCLKA/1, PCLKA/4, PCLKA/16, PCLKA/64, PCLKA/256, PCLKA/1024, MTCLKA, MTCLKB, MTCLKC, and MTCLKD) for each channel (seven clocks for channel 1, four clocks for channel 5, and six clocks for channel 6 or 7)<br>• 24 output compare/input capture registers<br>• Counter-clearing operation (simultaneous clearing on compare match or input capture)<br>• Simultaneous writing to multiple timer counters (TCNT)<br>• Simultaneous input and output to registers in synchronization with counter operations<br>• Buffer operation specifiable<br>• Capable of cascade-connected operation<br>• Interrupts: 38 sources<br>• Automatic transfer of register data<br>• Pulse output modes<br>Topple, PWM, complementary PWM, and reset-synchronous PWM modes<br>• Complementary PWM output mode<br>Outputs non-overlapping waveforms for controlling 3-phase inverters<br>Automatic specification of dead times<br>PWM duty cycle: Selectable as any value from 0% to 100%<br>Delay can be applied to requests for A/D conversion.<br>Non-generation of interrupt requests at peak or trough values of counters can be selected.<br>Double buffering<br>• Reset-synchronous PWM mode<br>Three PWM waveforms and corresponding inverse waveforms are output with the desired duty cycles.<br>• Phase-counting mode<br>• Counter functionality for dead-time compensation<br>• Generation of triggers for A/D converters<br>• Differential timing for initiation of A/D conversion |
| | Port output enable 3 (POE3) | • Control of the high-impedance state of the MTU3 and GPT's waveform output pins<br>• Six pins for input from signal sources: POE0, POE4, POE8, POE10, POE11, and POE12<br>• Initiation on detection of short-circuited outputs (detection of PWM outputs having simultaneously become an active level.)<br>• Initiation by comparator-detection, oscillation-stoppage detection, or software<br>• Software control of the states of pins for output control can also be added. |

## 1.3 Block Diagram

Figure 1.2 shows a block diagram.



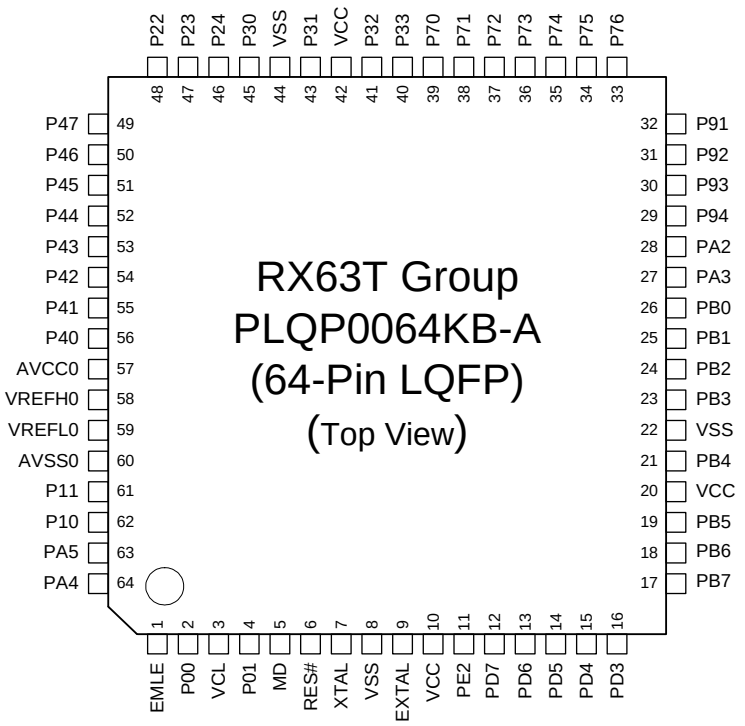

ICUb: Interrupt controller
DTCa: Data transfer controller
DMACA: DMA controller
WDTA: Watchdog timer
IWDTa: Independent watchdog timer
CRC: CRC (cyclic redundancy check) calculator
SCIc, SCId: Serial communications interface
USBa: USB 2.0 host/function module
RSPI: Serial peripheral interface
CAN: CAN module
GPT: General PWM timer
MTU3: Multi-function timer pulse unit 3
POE3: Port output enable 3
CMT: Compare match timer
RIIC: $I^2C$ bus interface
CAC: Clock frequency accuracy measurement circuit
DOC: Data operating circuit
MPU: Memory protection unit

Note 1: Numbers of pins and availability of the USB2.0 host/function module, 12-bit A/D converter, 10-bit D/A converter, and 10-bit D/A converter differ with the package.

**Figure 1.2 Block Diagram**

**Table 1.4 Pin Functions (4/5)**

| Classifications | Pin Name | I/O | Description |
|---|---|---|---|
| USB 2.0 host/function module | VCC_USB | Input | Power supply pin for USB |
| | VSS_USB | Input | Ground pin for USB |
| | USB0_DP | I/O | USB internal transceiver D + input and output pins |
| | USB0_DM | I/O | USB internal transceiver D - input and output pins |
| | USB0_EXICEN | Output | Low power control signal for OTG chip |
| | USB0_VBUSEN | Output | Supply enable signal of VBUS (5 V) to OTG chip |
| | USB0_ID | Input | Mini AB connector ID input pin for use in OTG operation |
| | USB0_DPRPD | Output | D+ signal pull-down control pin for use during host operation |
| | USB0_DRPD | Output | D- signal pull-down control pin for use during host operation |
| | USB0_DPUPE | Output | D+ signal pull-up control pin for use during function operation |
| | USB0_VBUS | Input | Pin for monitoring USB cable connection |
| | USB0_OVRCURA, USB0_OVRCURB | Input | Pin for detecting external over current |
| CAN module | CRX1 | Input | Input pins |
| | CTX1 | Output | Output pins |
| Serial peripheral interface | RSPCKA, RSPCKB | I/O | Clock input/output pins |
| | MOSIA, MOSIB | I/O | Inputs or outputs data output from the master |
| | MISOA, MISOB | I/O | Inputs or outputs data output from the slave |
| | SSLA0, SSLB0 | I/O | Input or output pins for slave selection |
| | SSLA1 to SSLA3<br>SSLB1 to SSLB3 | Output | Output pins for slave selection |
| 12-bit A/D converter | AN000 to AN007<br>AN100 to AN103 | Input | Input pins for the analog signals to be processed by the A/D converter |
| | ADTRG0#, ADTRG1# | Input | Input pins for the external trigger signals that start the A/D conversion |
| | CVREFH | Input | Input pin for the high-level reference voltage to the comparator |
| | CVREFL | Input | Input pin for the low-level reference voltage to the comparator |
| 10-bit A/D converter | AN0 to AN19 | Input | Input pins for the analog signals to be processed by the 10-bit A/D converter |
| | ADTRG# | Input | Input pins for the external trigger signals that start the A/D conversion |
| D/A converter | DA0, DA1 | Output | Output pins for the analog signals to be processed by the 10-bit A/D converter |
| Analog power supply | AVCC0 | — | Analog voltage supply pin for the 12-bit A/D converter. Connect this pin to VCC if the 12-bit A/D converter is not to be used |
| | AVSS0 | — | Analog ground pin for the 12-bit A/D converter. Connect this pin to VSS if the 12-bit A/D converter is not to be used |
| | VREFH0 | — | Reference voltage supply pin for the 12-bit A/D converter. Connect this pin to VCC if the 12-bit A/D converter is not to be used |
| | VREFL0 | — | Reference ground pin for the 12-bit A/D converter. Connect this pin to VSS if the 12-bit A/D converter is not to be used |
| | AVCC | — | Analog voltage supply pin for the 10-bit A/D converter and the 10-bit D/A converter. Connect this pin to the power supply of the system if the A/D converter and the D/A converter are not to be used. |
| | AVSS | — | Ground pin for the 10-bit A/D converter and 10-bit D/A converter. Connect this pin to the power-supply ground for the system (0 V). |
| | VREF | — | Reference-voltage input pin for the 10-bit A/D converter and the 10-bit D/A converter. Connect this pin to the power supply for the system if the A/D converter and the D/A converter are not to be used. |




Note: • This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.9, List of Pins and Pin Functions (64-Pin LQFP).

**Figure 1.7 Pin Assignment (64-Pin LQFP)**

**Table 1.6 List of Pins and Pin Functions (120-Pin LQFP) (4/4)**

| Pin Number 120-Pin LQFP | Power Supply Clock System Control | I/O Port | Bus | Timer (MTU3, GPT, POE3, CAC) | Communications (SCIc, SCId, RSPI, RIIC, CAN, USB) | Interrupt | S12ADB, AD, DA |
|---|---|---|---|---|---|---|---|
| 111 | | P82 | WAIT# | MTIC5U | SCK12 | IRQ3 | |
| 112 | | P81 | A8 | MTIC5V | TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12 | | |
| 113 | | P80 | A9 | MTIC5W | RXD12/SMISO12/ SSCL12/RXDX12 | IRQ5 | |
| 114 | | P12 | CS3# | | USB0_DPRPD | | |
| 115 | | P11 | ALE | MTCLKC | | IRQ1-DS | |
| 116 | | P10 | | MTCLKD | | IRQ0-DS | |
| 117 | | | | | USB0_DPUPE | | |
| 118 | VSS_USB | | | | | | |
| 119 | | | | | USB0_DM | | |
| 120 | | | | | USB0_DP | | |

**Table 1.7 List of Pins and Pin Functions (112-Pin LQFP) (2/4)**

| Pin Number 112-Pin LQFP | Power Supply Clock System Control | I/O Port | Bus | Timer (MTU3, GPT, POE3, CAC) | Communications (SCIc, SCId, RSPI, RIIC, CAN) | Interrupt | S12ADB, AD, DA |
|---|---|---|---|---|---|---|---|
| 38 | | PB0 | A14 | MTIOC0D | MOSIA/MOSIB | | |
| 39 | | PA5 | | MTIOC1A | RXD0/SMISO0/ SSCL0/ MISOA/MISOB | | ADTRG1# |
| 40 | | PA4 | | MTIOC1B | TXD0/SMOSI0/ SSDA0/RSPCKA/ RSPCKB | | ADTRG0# |
| 41 | | PA3 | | MTIOC2A | SCK0/SSLA0/SSLB0 | | |
| 42 | | PA2 | | MTIOC2B | RXD2/SMISO2/ SSCL2/ SSLA1/SSLB1 | | |
| 43 | | PA1 | | MTIOC6A | TXD2/SMOSI2/ SSDA2/SSLA2/SSLB2 | | |
| 44 | | PA0 | | MTIOC6C | SCK2/SSLA3/SSLB3 | | |
| 45 | VCC | | | | | | |
| 46 | | P96 | A13 | POE4# | RXD1/SMISO1/SSCL1 | IRQ4-DS | |
| 47 | VSS | | | | | | |
| 48 | | P95 | | MTIOC6B/ GTIOC4A | TXD1/SMOSI1/SSDA1 | | |
| 49 | | P94 | | MTIOC7A/ GTIOC5A | CTS1#/RTS1#/SS1# | | |
| 50 | | P93 | | MTIOC7B/ GTIOC6A | CTS2#/RTS2#/SS2# | | |
| 51 | | P92 | | MTIOC6D/GTIOC4B | | | |
| 52 | | P91 | | MTIOC7C/GTIOC5B | | | |
| 53 | | P90 | | MTIOC7D/GTIOC6B | | | |
| 54 | TRCLK | PG5 | | POE12# | SCK3 | | ADTRG# |
| 55 | TRDATA3 | PG4 | | GTIOC6B | RXD3/SMISO3/SSCL3 | IRQ6 | |
| 56 | TRDATA2 | PG3 | | GTIOC6A | TXD3/SMOSI3/SSDA3 | | |
| 57 | TRDATA1 | PG2 | | | SCK2 | IRQ2 | |
| 58 | TRDATA0 | PG1 | | GTIOC7B | RXD2/SMISO2/SSCL2 | IRQ1 | |
| 59 | TRSYNC | PG0 | | GTIOC7A | TXD2/SMOSI2/SSDA2 | IRQ0 | |
| 60 | | P76 | D0/[A0/D0] | MTIOC4D/GTIOC2B | | | |
| 61 | | P75 | D1/[A1/D1] | MTIOC4C/GTIOC1B | | | |
| 62 | | P74 | D2/[A2/D2] | MTIOC3D/GTIOC0B | | | |
| 63 | | P73 | D3/[A3/D3] | MTIOC4B/GTIOC2A | | | |
| 64 | | P72 | D4/[A4/D4] | MTIOC4A/GTIOC1A | | | |
| 65 | | P71 | D5/[A5/D5] | MTIOC3B/GTIOC0A | | | |
| 66 | | P70 | D6/[A6/D6] | POE0# | CTS1#/RTS1#/SS1# | IRQ5-DS | |
| 67 | | P33 | D7/[A7/D7] | MTIOC3A/MTCLKA | SSLA3/SSLB3 | | |
| 68 | | P32 | D8/[A8/D8] | MTIOC3C/MTCLKB | SSLA2/SSLB2 | | |
| 69 | VCC | | | | | | |
| 70 | | P31 | D9/[A9/D9] | MTIOC0A/MTCLKC | SSLA1/SSLB1 | | |
| 71 | VSS | | | | | | |
| 72 | | P30 | D10/[A10/ D10] | MTIOC0B/MTCLKD | SCK0/SSLA0/SSLB0 | | |
| 73 | | P24 | D11/[A11/D11] | | CTS0#/RTS0#/SS0#/ RSPCKA/RSPCKB | IRQ4 | |

## 2.1 General-Purpose Registers (R0 to R15)

This CPU has sixteen general-purpose registers (R0 to R15). R1 to R15 can be used as data registers or address registers. R0, a general-purpose register, also functions as the stack pointer (SP).
The stack pointer is switched to operate as the interrupt stack pointer (ISP) or user stack pointer (USP) by the value of the stack pointer select bit (U) in the processor status word (PSW).

## 2.2 Control Registers

### (1) Interrupt Stack Pointer (ISP)/User Stack Pointer (USP)

The stack pointer (SP) can be either of two types, the interrupt stack pointer (ISP) or the user stack pointer (USP). Whether the stack pointer operates as the ISP or USP depends on the value of the stack pointer select bit (U) in the processor status word (PSW).
Set the ISP or USP to a multiple of four, as this reduces the numbers of cycles required to execute interrupt sequences and instructions entailing stack manipulation.

### (2) Interrupt Table Register (INTB)

The interrupt table register (INTB) specifies the address where the relocatable vector table starts.

### (3) Program Counter (PC)

The program counter (PC) indicates the address of the instruction being executed.

### (4) Processor Status Word (PSW)

The processor status word (PSW) indicates the results of instruction execution or the state of the CPU.

### (5) Backup PC (BPC)

The backup PC (BPC) is provided to speed up response to interrupts.
After a fast interrupt has been generated, the contents of the program counter (PC) are saved in the BPC register.

### (6) Backup PSW (BPSW)

The backup PSW (BPSW) is provided to speed up response to interrupts.
After a fast interrupt has been generated, the contents of the processor status word (PSW) are saved in the BPSW. The allocation of bits in the BPSW corresponds to that in the PSW.

### (7) Fast Interrupt Vector Register (FINTV)

The fast interrupt vector register (FINTV) is provided to speed up response to interrupts.
The FINTV register specifies a branch destination address when a fast interrupt has been generated.

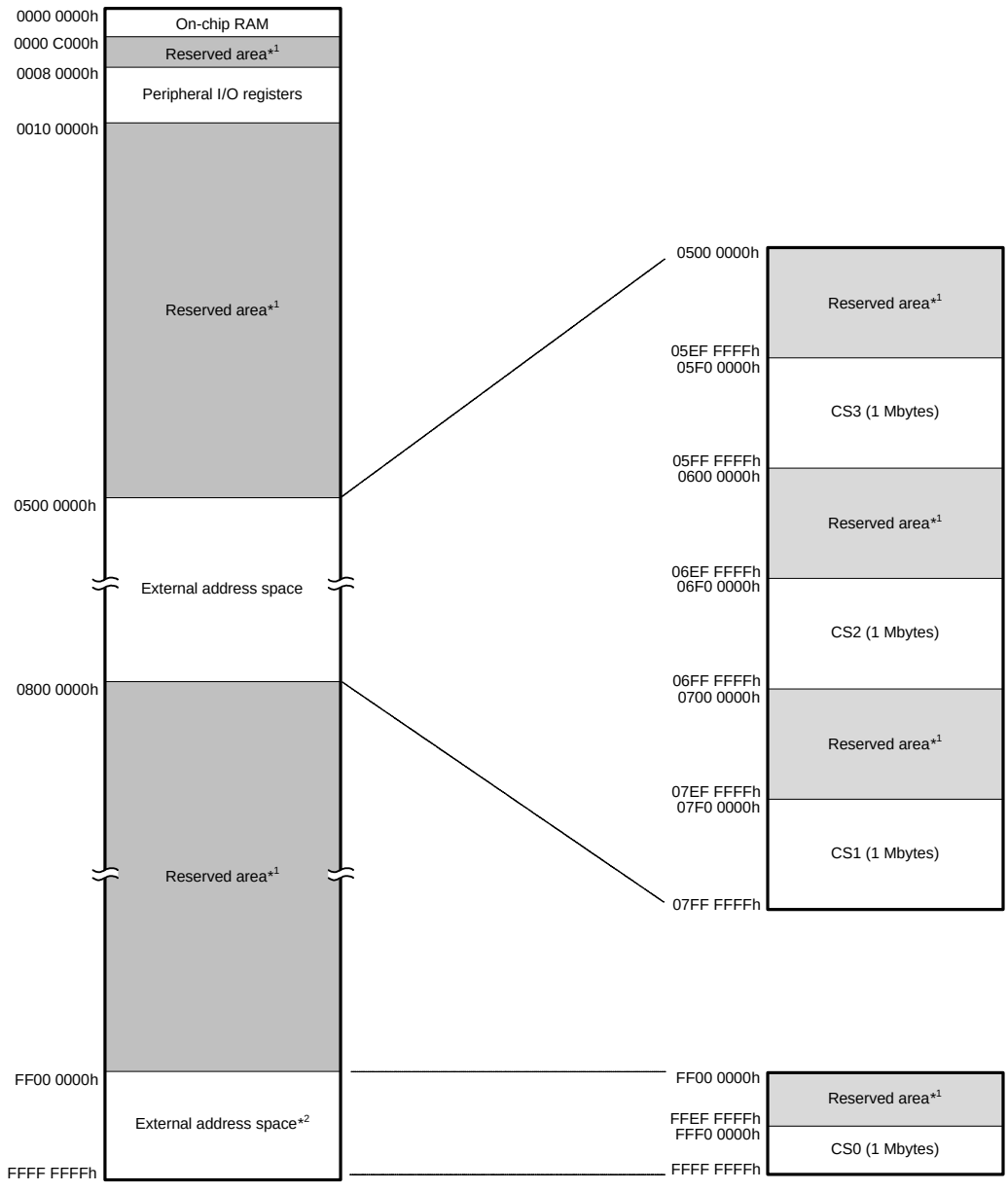
### (8) Floating-Point Status Word (FPSW)

The floating-point status word (FPSW) indicates the results of floating-point operations.
When an exception handling enable bit (Ej) enables the exception handling (Ej = 1), the exception cause can be identified by checking the corresponding Cj flag in the exception handling routine. If the exception handling is masked (Ej = 0), the occurrence of exception can be checked by reading the Fj flag at the end of a series of processing. Once the Fj flag has been set to 1, this value is retained until it is cleared to 0 by software (j = X, U, Z, O, or V).

## 3.2 External Address Space

The external address space is divided into up to four CS areas (CS0 to CS3), each corresponding to the CSn# signal output from a CSn# (n = 0 to 3) pin.

Figure 3.2 shows the address ranges corresponding to the individual CS areas (CS0 to CS3) in on-chip ROM disabled extended mode.




Note 1. Reserved areas should not be accessed.
Note 2. The CS0 area is disabled in on-chip ROM enabled extended mode.
In this mode, the address space for addresses above 0800 0000h is as shown in Figure 3.1, Memory Map in Each Operating Mode.

**Figure 3.2 Correspondence between External Address Spaces and CS Areas (In On-Chip ROM Disabled Extended Mode)**

**Table 4.1 List of I/O Registers (Address Order) (2/48)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Module Name | Remarks |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | | |
| 0008 201Fh | DMAC0 | DMA Activation Source Flag Control Register | DMCSL | 8 | 8 | 2 ICLK | | DMACA | |
| 0008 2040h | DMAC1 | DMA Source Address Register | DMSAR | 32 | 32 | 2 ICLK | | | |
| 0008 2044h | DMAC1 | DMA Destination Address Register | DMDAR | 32 | 32 | 2 ICLK | | | |
| 0008 2048h | DMAC1 | DMA Transfer Count Register | DMCRA | 32 | 32 | 2 ICLK | | | |
| 0008 204Ch | DMAC1 | DMA Block Transfer Count Register | DMCRB | 16 | 16 | 2 ICLK | | | |
| 0008 2050h | DMAC1 | DMA Transfer Mode Register | DMTMD | 16 | 16 | 2 ICLK | | | |
| 0008 2053h | DMAC1 | DMA Interrupt Setting Register | DMINT | 8 | 8 | 2 ICLK | | | |
| 0008 2054h | DMAC1 | DMA Address Mode Register | DMAMD | 16 | 16 | 2 ICLK | | | |
| 0008 205Ch | DMAC1 | DMA Transfer Enable Register | DMCNT | 8 | 8 | 2 ICLK | | | |
| 0008 205Dh | DMAC1 | DMA Software Start Register | DMREQ | 8 | 8 | 2 ICLK | | | |
| 0008 205Eh | DMAC1 | DMA Status Register | DMSTS | 8 | 8 | 2 ICLK | | | |
| 0008 205Fh | DMAC1 | DMA Activation Source Flag Control Register | DMCSL | 8 | 8 | 2 ICLK | | | |
| 0008 2080h | DMAC2 | DMA Source Address Register | DMSAR | 32 | 32 | 2 ICLK | | | |
| 0008 2084h | DMAC2 | DMA Destination Address Register | DMDAR | 32 | 32 | 2 ICLK | | | |
| 0008 2088h | DMAC2 | DMA Transfer Count Register | DMCRA | 32 | 32 | 2 ICLK | | | |
| 0008 208Ch | DMAC2 | DMA Block Transfer Count Register | DMCRB | 16 | 16 | 2 ICLK | | | |
| 0008 2090h | DMAC2 | DMA Transfer Mode Register | DMTMD | 16 | 16 | 2 ICLK | | | |
| 0008 2093h | DMAC2 | DMA Interrupt Setting Register | DMINT | 8 | 8 | 2 ICLK | | | |
| 0008 2094h | DMAC2 | DMA Address Mode Register | DMAMD | 16 | 16 | 2 ICLK | | | |
| 0008 209Ch | DMAC2 | DMA Transfer Enable Register | DMCNT | 8 | 8 | 2 ICLK | | | |
| 0008 209Dh | DMAC2 | DMA Software Start Register | DMREQ | 8 | 8 | 2 ICLK | | | |
| 0008 209Eh | DMAC2 | DMA Status Register | DMSTS | 8 | 8 | 2 ICLK | | | |
| 0008 209Fh | DMAC2 | DMA Activation Source Flag Control Register | DMCSL | 8 | 8 | 2 ICLK | | | |
| 0008 20C0h | DMAC3 | DMA Source Address Register | DMSAR | 32 | 32 | 2 ICLK | | | |
| 0008 20C4h | DMAC3 | DMA Destination Address Register | DMDAR | 32 | 32 | 2 ICLK | | | |
| 0008 20C8h | DMAC3 | DMA Transfer Count Register | DMCRA | 32 | 32 | 2 ICLK | | | |
| 0008 20CCh | DMAC3 | DMA Block Transfer Count Register | DMCRB | 16 | 16 | 2 ICLK | | | |
| 0008 20D0h | DMAC3 | DMA Transfer Mode Register | DMTMD | 16 | 16 | 2 ICLK | | | |
| 0008 20D3h | DMAC3 | DMA Interrupt Setting Register | DMINT | 8 | 8 | 2 ICLK | | | |
| 0008 20D4h | DMAC3 | DMA Address Mode Register | DMAMD | 16 | 16 | 2 ICLK | | | |
| 0008 20DCh | DMAC3 | DMA Transfer Enable Register | DMCNT | 8 | 8 | 2 ICLK | | | |
| 0008 20DDh | DMAC3 | DMA Software Start Register | DMREQ | 8 | 8 | 2 ICLK | | | |
| 0008 20DEh | DMAC3 | DMA Status Register | DMSTS | 8 | 8 | 2 ICLK | | | |
| 0008 20DFh | DMAC3 | DMA Activation Source Flag Control Register | DMCSL | 8 | 8 | 2 ICLK | | | |
| 0008 2200h | DMAC | DMACA Module Activation Register | DMAST | 8 | 8 | 2 ICLK | | | |
| 0008 2400h | DTC | DTC Control Register | DTCCR | 8 | 8 | 2ICLK | | DTCa | |
| 0008 2404h | DTC | DTC Vector Base Register | DTCVBR | 32 | 32 | 2ICLK | | | |
| 0008 2408h | DTC | DTC Address Mode Register | DTCADMOD | 8 | 8 | 2ICLK | | | |
| 0008 240Ch | DTC | DTC Module Start Register | DTCST | 8 | 8 | 2ICLK | | | |
| 0008 240Eh | DTC | DTC Status Register | DTCSTS | 16 | 16 | 2ICLK | | | |
| 0008 3002h | BSC | CS0 Mode Register | CS0MOD | 16 | 16 | 1, 2 BCLK | | Buses | Not present in versions with 64 or 48 pins. |
| 0008 3004h | BSC | CS0 Wait Control Register 1 | CS0WCR1 | 32 | 32 | 1, 2 BCLK | | | Not present in versions with 64 or 48 pins. |
| 0008 3008h | BSC | CS0 Wait Control Register 2 | CS0WCR2 | 32 | 32 | 1, 2 BCLK | | | Not present in versions with 64 or 48 pins. |
| 0008 3012h | BSC | CS1 Mode Register | CS1MOD | 16 | 16 | 1, 2 BCLK | | | Not present in versions with 64 or 48 pins. |
| 0008 3014h | BSC | CS1 Wait Control Register 1 | CS1WCR1 | 32 | 32 | 1, 2 BCLK | | | Not present in versions with 64 or 48 pins. |
| 0008 3018h | BSC | CS1 Wait Control Register 2 | CS1WCR2 | 32 | 32 | 1, 2 BCLK | | | Not present in versions with 64 or 48 pins. |
| 0008 3022h | BSC | CS2 Mode Register | CS2MOD | 16 | 16 | 1, 2 BCLK | | | Not present in versions with 64 or 48 pins. |

**Table 4.1 List of I/O Registers (Address Order) (5/48)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Module Name | Remarks |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | | |
| 0008 703Eh | ICU | Interrupt Request Register 062 | IR062 | 8 | 8 | 2 ICLK | | ICUb | Not present in versions with 64 or 48 pins. |
| 0008 7040h | ICU | Interrupt Request Register 064 | IR064 | 8 | 8 | 2 ICLK | | | |
| 0008 7041h | ICU | Interrupt Request Register 065 | IR065 | 8 | 8 | 2 ICLK | | | |
| 0008 7042h | ICU | Interrupt Request Register 066 | IR066 | 8 | 8 | 2 ICLK | | | |
| 0008 7043h | ICU | Interrupt Request Register 067 | IR067 | 8 | 8 | 2 ICLK | | | |
| 0008 7044h | ICU | Interrupt Request Register 068 | IR068 | 8 | 8 | 2 ICLK | | | |
| 0008 7045h | ICU | Interrupt Request Register 069 | IR069 | 8 | 8 | 2 ICLK | | | |
| 0008 7046h | ICU | Interrupt Request Register 070 | IR070 | 8 | 8 | 2 ICLK | | | Not present in versions with 64 or 48 pins. |
| 0008 7047h | ICU | Interrupt Request Register 071 | IR071 | 8 | 8 | 2 ICLK | | | Not present in versions with 64 or 48 pins. |
| 0008 705Ah | ICU | Interrupt Request Register 090 | IR090 | 8 | 8 | 2 ICLK | | | Not present in versions with 112, 100, 64 or 48 pins. |
| 0008 7062h | ICU | Interrupt Request Register 098 | IR098 | 8 | 8 | 2 ICLK | | | Not present in versions with 64 or 48 pins. |
| 0008 7066h | ICU | Interrupt Request Register 102 | IR102 | 8 | 8 | 2 ICLK | | | |
| 0008 7067h | ICU | Interrupt Request Register 103 | IR103 | 8 | 8 | 2 ICLK | | | |
| 0008 7068h | ICU | Interrupt Request Register 104 | IR104 | 8 | 8 | 2 ICLK | | | Not present in versions with 64 or 48 pins. |
| 0008 7069h | ICU | Interrupt Request Register 105 | IR105 | 8 | 8 | 2 ICLK | | | Not present in versions with 64 or 48 pins. |
| 0008 706Ah | ICU | Interrupt Request Register 106 | IR106 | 8 | 8 | 2 ICLK | | | Not present in versions with 64 or 48 pins. |
| 0008 7072h | ICU | Interrupt Request Register 114 | IR114 | 8 | 8 | 2 ICLK | | | |
| 0008 707Ah | ICU | Interrupt Request Register 122 | IR122 | 8 | 8 | 2 ICLK | | | |
| 0008 707Bh | ICU | Interrupt Request Register 123 | IR123 | 8 | 8 | 2 ICLK | | | |
| 0008 707Ch | ICU | Interrupt Request Register 124 | IR124 | 8 | 8 | 2 ICLK | | | |
| 0008 707Dh | ICU | Interrupt Request Register 125 | IR125 | 8 | 8 | 2 ICLK | | | |
| 0008 707Eh | ICU | Interrupt Request Register 126 | IR126 | 8 | 8 | 2 ICLK | | | |
| 0008 707Fh | ICU | Interrupt Request Register 127 | IR127 | 8 | 8 | 2 ICLK | | | |
| 0008 7080h | ICU | Interrupt Request Register 128 | IR128 | 8 | 8 | 2 ICLK | | | |
| 0008 7081h | ICU | Interrupt Request Register 129 | IR129 | 8 | 8 | 2 ICLK | | | |
| 0008 7082h | ICU | Interrupt Request Register 130 | IR130 | 8 | 8 | 2 ICLK | | | |
| 0008 7083h | ICU | Interrupt Request Register 131 | IR131 | 8 | 8 | 2 ICLK | | | |
| 0008 7084h | ICU | Interrupt Request Register 132 | IR132 | 8 | 8 | 2 ICLK | | | |
| 0008 7085h | ICU | Interrupt Request Register 133 | IR133 | 8 | 8 | 2 ICLK | | | |
| 0008 7086h | ICU | Interrupt Request Register 134 | IR134 | 8 | 8 | 2 ICLK | | | |
| 0008 7087h | ICU | Interrupt Request Register 135 | IR135 | 8 | 8 | 2 ICLK | | | |
| 0008 7088h | ICU | Interrupt Request Register 136 | IR136 | 8 | 8 | 2 ICLK | | | |
| 0008 7089h | ICU | Interrupt Request Register 137 | IR137 | 8 | 8 | 2 ICLK | | | |
| 0008 708Ah | ICU | Interrupt Request Register 138 | IR138 | 8 | 8 | 2 ICLK | | | |
| 0008 708Bh | ICU | Interrupt Request Register 139 | IR139 | 8 | 8 | 2 ICLK | | | |
| 0008 708Ch | ICU | Interrupt Request Register 140 | IR140 | 8 | 8 | 2 ICLK | | | |
| 0008 708Dh | ICU | Interrupt Request Register 141 | IR141 | 8 | 8 | 2 ICLK | | | |
| 0008 708Eh | ICU | Interrupt Request Register 142 | IR142 | 8 | 8 | 2 ICLK | | | |
| 0008 708Fh | ICU | Interrupt Request Register 143 | IR143 | 8 | 8 | 2 ICLK | | | |
| 0008 7090h | ICU | Interrupt Request Register 144 | IR144 | 8 | 8 | 2 ICLK | | | |
| 0008 7091h | ICU | Interrupt Request Register 145 | IR145 | 8 | 8 | 2 ICLK | | | |
| 0008 7092h | ICU | Interrupt Request Register 146 | IR146 | 8 | 8 | 2 ICLK | | | |
| 0008 7093h | ICU | Interrupt Request Register 147 | IR147 | 8 | 8 | 2 ICLK | | | |
| 0008 7094h | ICU | Interrupt Request Register 148 | IR148 | 8 | 8 | 2 ICLK | | | |
| 0008 7095h | ICU | Interrupt Request Register 149 | IR149 | 8 | 8 | 2 ICLK | | | |
| 0008 7096h | ICU | Interrupt Request Register 150 | IR150 | 8 | 8 | 2 ICLK | | | |
| 0008 7097h | ICU | Interrupt Request Register 151 | IR151 | 8 | 8 | 2 ICLK | | | |

**Table 4.1 List of I/O Registers (Address Order) (42/48)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Module Name | Remarks |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | | |
| 000C 2884h | GPTB | LOCO Count Value Register | LCNT | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | GPT | Not present in versions with 64, or 48 pins. |
| 000C 2886h | GPTB | LOCO Count Result Average Register | LCNTA | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64, or 48 pins. |
| 000C 2888h | GPTB | LOCO Count Result Register 0 | LCNT00 | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64, or 48 pins. |
| 000C 288Ah | GPTB | LOCO Count Result Register 1 | LCNT01 | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64, or 48 pins. |
| 000C 288Ch | GPTB | LOCO Count Result Register 2 | LCNT02 | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 288Eh | GPTB | LOCO Count Result Register 3 | LCNT03 | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 2890h | GPTB | LOCO Count Result Register 4 | LCNT04 | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 2892h | GPTB | LOCO Count Result Register 5 | LCNT05 | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 2894h | GPTB | LOCO Count Result Register 6 | LCNT06 | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 2896h | GPTB | LOCO Count Result Register 7 | LCNT07 | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 2898h | GPTB | LOCO Count Result Register 8 | LCNT08 | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 289Ah | GPTB | LOCO Count Result Register 9 | LCNT09 | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 289Ch | GPTB | LOCO Count Result Register 10 | LCNT10 | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 289Eh | GPTB | LOCO Count Result Register 11 | LCNT11 | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 28A0h | GPTB | LOCO Count Result Register 12 | LCNT12 | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 28A2h | GPTB | LOCO Count Result Register 13 | LCNT13 | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 28A4h | GPTB | LOCO Count Result Register 14 | LCNT14 | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 28A6h | GPTB | LOCO Count Result Register 15 | LCNT15 | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 28A8h | GPTB | LOCO Count Upper Permissible Deviation Register | LCNTDU | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 28AAh | GPTB | LOCO Count Lower Permissible Deviation Register | LCNTDL | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 2900h | GPT4 | General PWM Timer I/O Control Register | GTIOR | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 2902h | GPT4 | General PWM Timer Interrupt Output Setting Register | GTINTAD | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 2904h | GPT4 | General PWM Timer Control Register | GTCR | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 2906h | GPT4 | General PWM Timer Buffer Enable Register | GTBER | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 2908h | GPT4 | General PWM Timer Count Direction Register | GTUDC | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 290Ah | GPT4 | General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register | GTITC | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 290Ch | GPT4 | General PWM Timer Status Register | GTST | 16 | 8, 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 290Eh | GPT4 | General PWM Timer Counter | GTCNT | 16 | 16 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 2910h | GPT4 | General PWM Timer Compare Capture Register A | GTCCRA | 16 | 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 2912h | GPT4 | General PWM Timer Compare Capture Register B | GTCCRB | 16 | 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 2914h | GPT4 | General PWM Timer Compare Capture Register C | GTCCRC | 16 | 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 2916h | GPT4 | General PWM Timer Compare Capture Register D | GTCCRD | 16 | 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |
| 000C 2918h | GPT4 | General PWM Timer Compare Capture Register E | GTCCRE | 16 | 16, 32 | 2 to 5 PCLKA | 2, 3 ICLK | | Not present in versions with 64 or 48 pins. |

## 5.3.1 Reset Timing

**Table 5.8 Reset Timing**

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. $T_a$ is common to conditions 1 to 3.

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| RES# pulse width | Power-on | $t_{RESWP}$ | 2 | — | — | ms | Figure 5.1 |
| | Deep software standby mode | $t_{RESWD}$ | 1 | — | — | ms | Figure 5.2 |
| | Software standby mode | $t_{RESWS}$ | 1 | — | — | ms | |
| | Programming or erasure of the ROM or E2 DataFlash memory or blank checking of the E2 DataFlash memory | $t_{RESWF}$ | 200 | — | — | µs | |
| | Other than above | $t_{RESW}$ | 200 | — | — | µs | |
| Wait time after RES# cancellation | | $t_{RESWT}$ | 59 | — | 60 | $t_{cyc}$ | |
| Internal reset time (independent watchdog timer reset, watchdog timer reset, software reset) | | $t_{RESW2}$ | 112 | — | 120 | $t_{cyc}$ | |

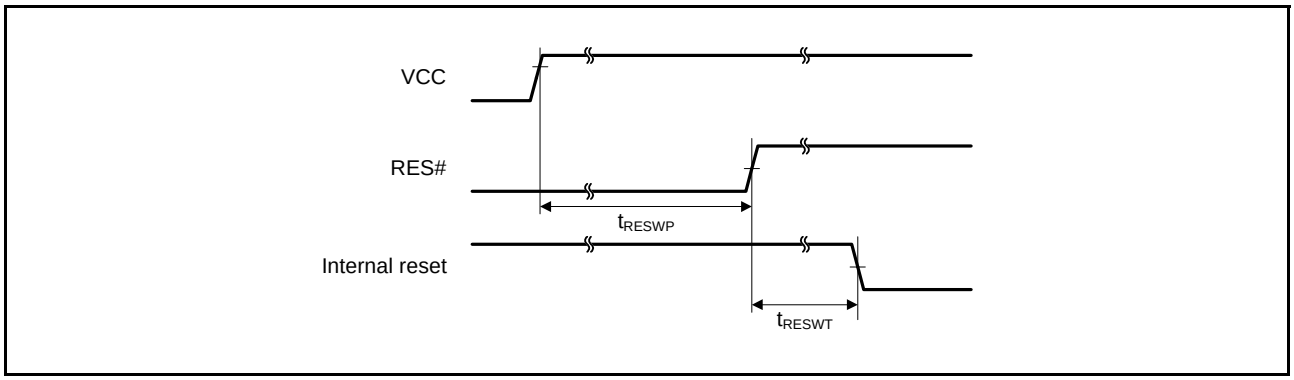



**Figure 5.1 Reset Input Timing at Power-On**

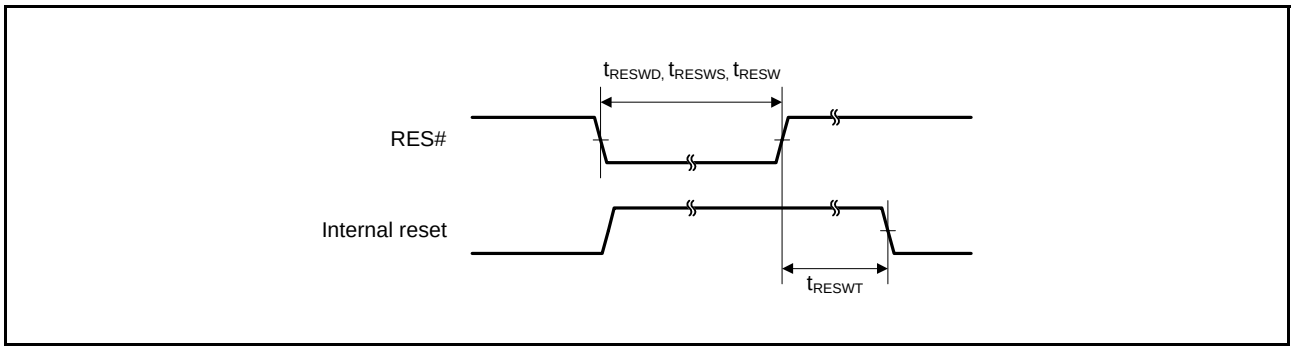



**Figure 5.2 Reset Input Timing**

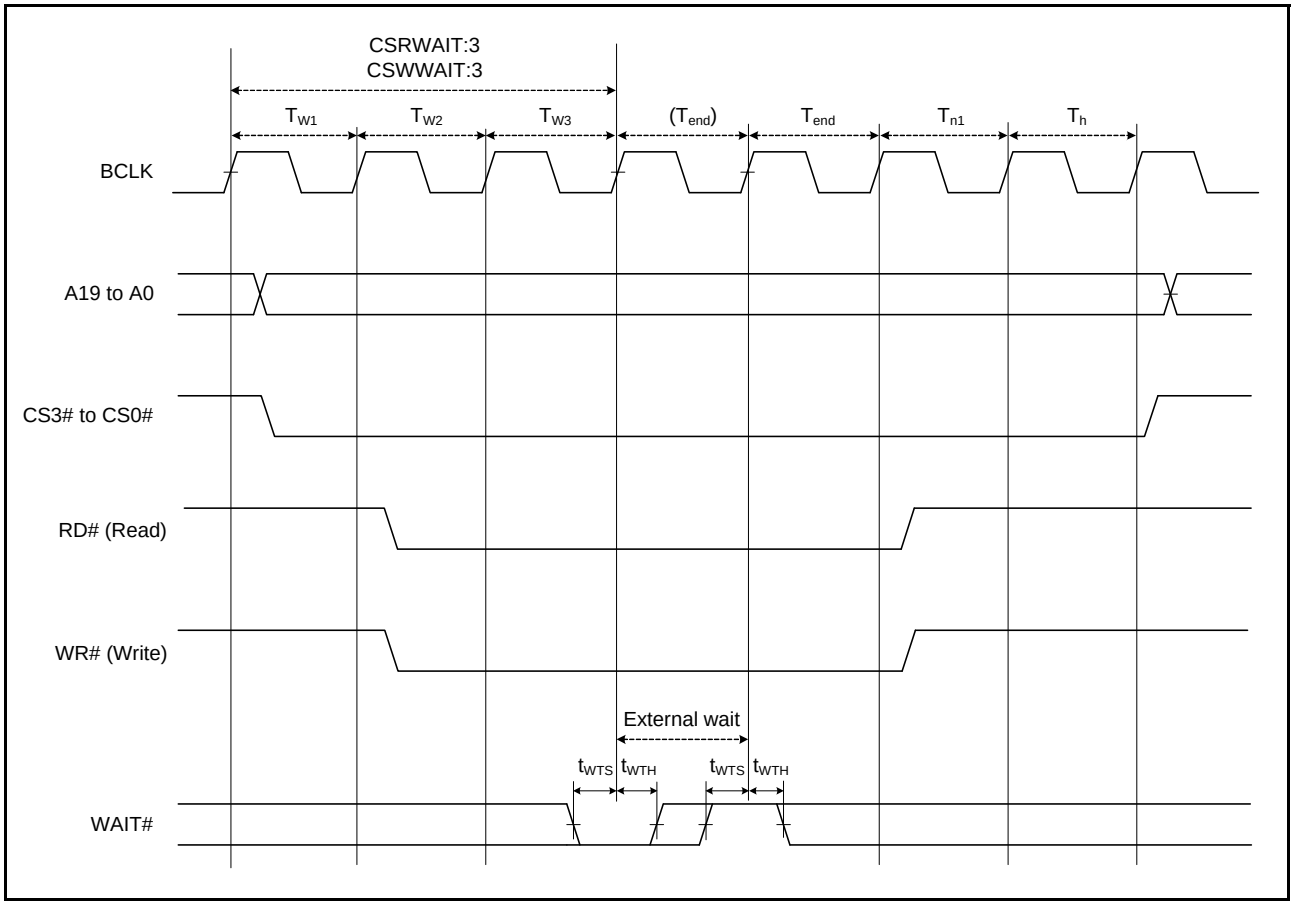



**Figure 5.17 External Bus Timing/External Wait Control**

**Table 5.14 Bus Timing (Multiplexed Bus) (3)**

Condition: PLLVCC = VCC_USB = AVCC0 = AVCC = VREF = 3.0 to 3.6 V
VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V, VREFH0 = 3.0 V to AVCC0
$T_a = T_{opr}$
Output load conditions: $V_{OH}$ = VCC x 0.5, $V_{OL}$ = VCC x 0.5, $I_{OH}$ = –1.0 mA, $I_{OL}$ = 1.0 mA, C = 30 pF

| Item | Symbol | Min. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|
| Address delay time | $t_{AD}$ | — | 35 | ns | Figure 5.18, Figure 5.19 |
| Byte control delay time | $t_{BCD}$ | — | 30 | ns | |
| CS# delay time | $t_{CSD}$ | — | 30 | ns | |
| RD# delay time | $t_{RSD}$ | — | 30 | ns | |
| ALE delay time | $t_{ALED}$ | — | 30 | ns | |
| Read data setup time | $t_{RDS}$ | 20 | — | ns | |
| Read data hold time | $t_{RDH}$ | 0 | — | ns | |
| WR# delay time | $t_{WRD}$ | — | 30 | ns | |
| Write data delay time | $t_{WDD}$ | — | 35 | ns | |
| Write data hold time | $t_{WDH}$ | 0 | — | ns | |
| WAIT# setup time | $t_{WTS}$ | 20 | — | ns | Figure 5.17 |
| WAIT# hold time | $t_{WTH}$ | 0.0 | — | ns | |

### Table 5.16 Timing of On-Chip Peripheral Modules (2)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. $T_a$ is common to conditions 1 to 3.

| Item | | | Symbol | Min. | Max. | Unit*1 | Test Conditions |
|---|---|---|---|---|---|---|---|
| SCI | Input clock cycle | Asynchronous | $t_{Scyc}$ | 4 | — | $t_{Pcyc}$ | C = 30 pF<br>Figure 5.29 |
| | | Clock synchronous | | 6 | — | | |
| | Input clock pulse width | | $t_{SCKW}$ | 0.4 | 0.6 | $t_{Scyc}$ | |
| | Input clock rise time | | $t_{SCKr}$ | — | 20 | ns | |
| | Input clock fall time | | $t_{SCKf}$ | — | 20 | ns | |
| | Output clock cycle | Asynchronous | $t_{Scyc}$ | 16 | — | $t_{Pcyc}$ | |
| | | Clock synchronous | | 4 | — | | |
| | Output clock pulse width | | $t_{SCKW}$ | 0.4 | 0.6 | $t_{Scyc}$ | |
| | Output clock rise time | | $t_{SCKr}$ | — | 20 | ns | |
| | Output clock fall time | | $t_{SCKf}$ | — | 20 | ns | |
| | Transmit data delay time | Clock synchronous | $t_{TXD}$ | — | 40 | ns | Figure 5.30 |
| | Receive data setup time | Clock synchronous | $t_{RXS}$ | 40 | — | ns | |
| | Receive data hold time | Clock synchronous | $t_{RXH}$ | 40 | — | ns | |
| | Receive data fall time | | $t_{TICTF}$ | — | 0.1 | µs/V | When Noise Cancellation Function is not used. |
| A/D converter | 10-bit A/D converter trigger input pulse width | | $t_{TRGW}$ | 1.5 | — | $t_{Pcyc}$ | Figure 5.31 |
| | 12-bit A/D converter trigger input pulse width | | | 1.5 | — | | |
| CAC | CACREF input pulse width | $t_{Pcyc} \leq t_{cac}$*2 | $t_{CACREF}$ | 4.5 $t_{cac}$ + 3 $t_{Pcyc}$ | — | ns | |
| | | $t_{Pcyc} > t_{cac}$*2 | | 5 $t_{cac}$ + 6.5 $t_{Pcyc}$ | — | ns | |
| | CACREF input fall time | | $t_{CACREFTF}$ | — | 0.1 | µs/V | |

Note 1. $t_{Pcyc}$: PCLK cycle, $t_{PAcye}$: PCLKA cycle
Note 2. $t_{cac}$: CAC count clock source cycle.

### Table 5.16 Timing of On-Chip Peripheral Modules (4)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. $T_a$ is common to conditions 1 to 3.

| Item | | Symbol | Min. | Max. | Unit*1 | Test Conditions |
|---|---|---|---|---|---|---|
| Simple SPI | SCK clock cycle output (master) | $t_{SPcyc}$ | 4 | 65536 | $t_{Pcyc}$ | C = 30 pF, Figure 5.30 |
| | SCK clock cycle input (slave) | | 8 | 65536 | | |
| | SCK clock high pulse width | $t_{SPCKWH}$ | 0.4 | 0.6 | $t_{SPcyc}$ | |
| | SCK clock low pulse width | $t_{SPCKWL}$ | 0.4 | 0.6 | $t_{SPcyc}$ | |
| | SCK clock rise/fall time | $t_{SPCKR}$, $t_{SPCKF}$ | — | 20 | ns | |
| | Data input setup time | $t_{SU}$ | 40 | — | ns | C = 30 pF, Figure 5.31 to Figure 5.38 |
| | Data input hold time | $t_H$ | 40 | — | ns | |
| | SS input setup time | $t_{LEAD}$ | 6 | — | $t_{Pcyc}$ | |
| | SS input hold time | $t_{LAG}$ | 6 | — | $t_{Pcyc}$ | |
| | Data output delay time | $t_{OD}$ | — | 40 | ns | |
| | Data output hold time | $t_{OH}$ | –10 | — | ns | |
| | Data rise/fall time | $t_{DR}$, $t_{DF}$ | — | 20 | ns | |
| | SS input rise/fall time | $t_{SSLr}$, $t_{SSLf}$ | — | 20 | ns | |
| | Slave access time | $t_{SA}$ | — | 5 | $t_{Pcyc}$ | C = 30 pF, Figure 5.37 and Figure 5.38 |
| | Slave output release time | $t_{REL}$ | — | 5 | $t_{Pcyc}$ | |

Note 1. $t_{Pcyc}$: PCLK cycle

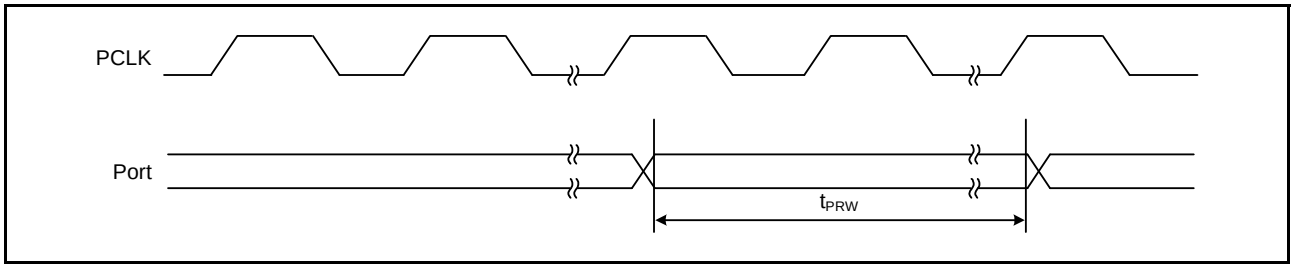



**Figure 5.20 I/O port Input Timing**

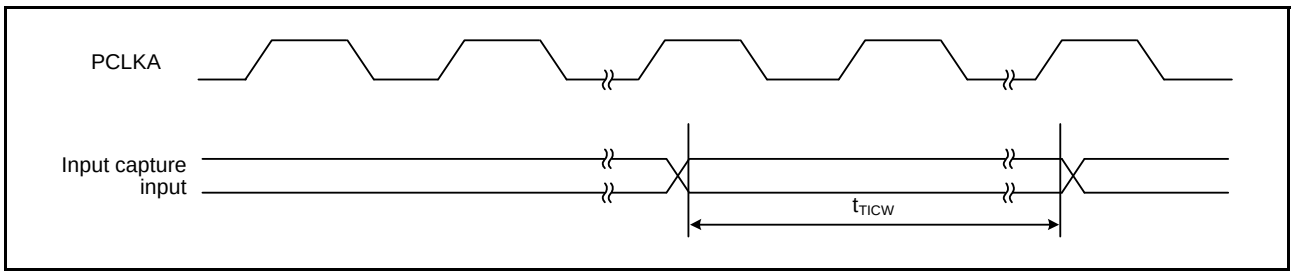



**Figure 5.21 MTU3 Input/Output Timing**

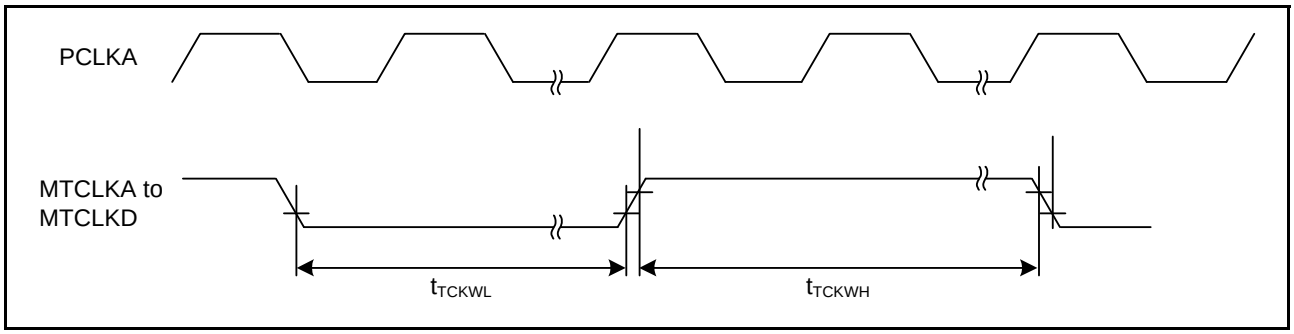



**Figure 5.22 MTU3 Clock Input Timing**

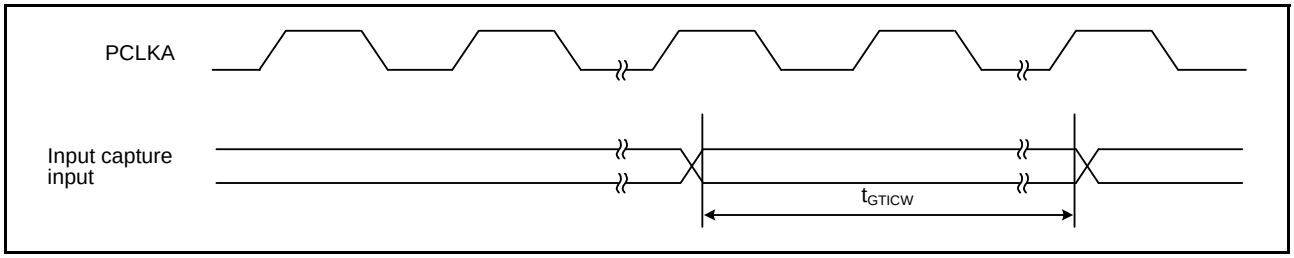



**Figure 5.23 GPT Input Capture Input Timing**

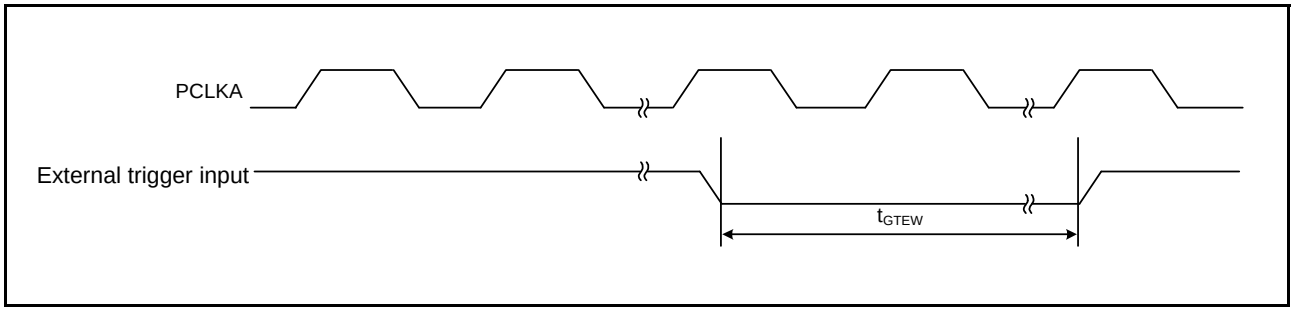



**Figure 5.24 GPT External Trigger Input Timing**

**Table 6.15 Timing of On-Chip Peripheral Modules (5)**

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = $T_{opr}$

| Item | | Symbol | Min.*1, *2 | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Simple IIC (Standard-mode) | SCL, SDAinput rise time | $t_{Sr}$ | — | 1000 | ns | Figure 6.25 |
| | SCL, SDA input fall time | $t_{Sf}$ | — | 300 | ns | |
| | SCL, SDA input spike pulse removal time | $t_{SP}$ | 0 | 4 × $t_{IICcyc}$ | ns | |
| | Data input setup time | $t_{SDAS}$ | 250 | — | ns | |
| | Data input hold time | $t_{SDAH}$ | 0 | — | ns | |
| | SCL, SDA capacitive load | $C_b$ | — | 400 | pF | |
| Simple IIC (Fast-mode) | SCL, SDA input rise time | $t_{Sr}$ | 20 + 0.1$C_b$ | 300 | ns | |
| | SCL, SDA input fall time | $t_{Sf}$ | 20 + 0.1$C_b$ | 300 | ns | |
| | SCL, SDA input spike pulse removal time | $t_{SP}$ | 0 | 4 × $t_{IICcyc}$ | ns | |
| | Data input setup time | $t_{SDAS}$ | 100 | — | ns | |
| | Data input hold time | $t_{SDAH}$ | 0 | — | ns | |
| | SCL, SDA capacitive load | $C_b$ | — | 400 | pF | |

Note 1. The value in parentheses is used when ICMR3.NF[1:0] are set to 11b while a digital filter is enabled with ICFER.NFE = 1.
Note 2. Cb indicates the total capacity of the bus line.

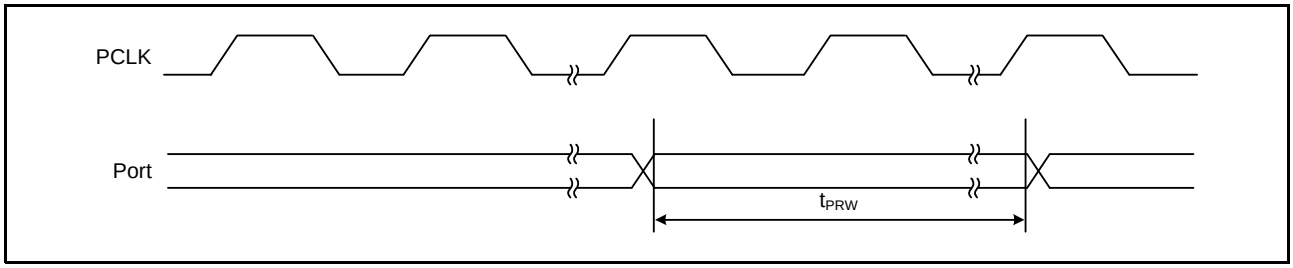



**Figure 6.12 I/O port Input Timing**

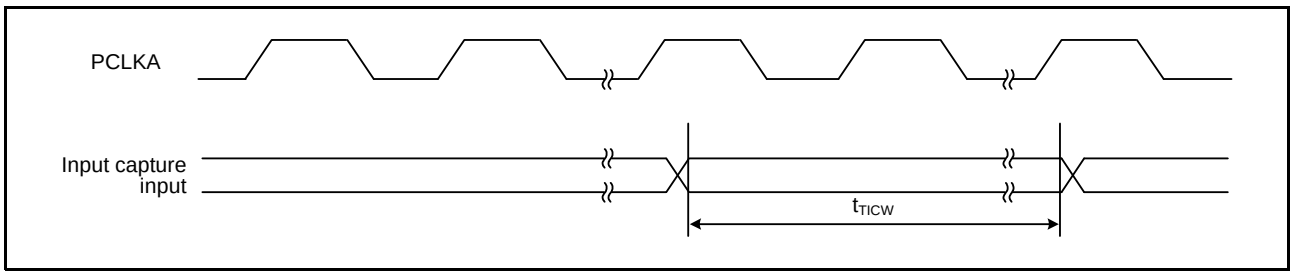



**Figure 6.13 MTU3 Input/Output Timing**

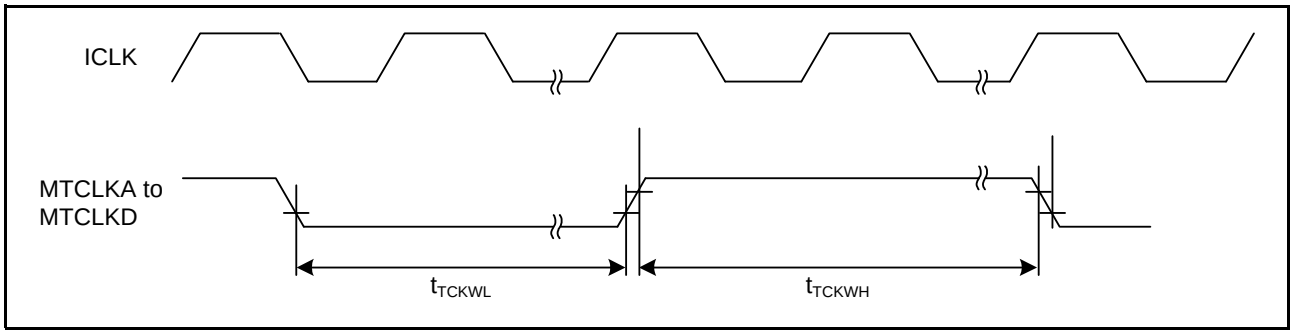



**Figure 6.14 MTU3 Clock Input Timing**

## 6.4 A/D Conversion Characteristics

### Table 6.16 12-Bit A/D Conversion Characteristics

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = $T_{opr}$

| Item | | min | typ | max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Resolution | | 12 | 12 | 12 | Bit | |
| Conversion time *1 (ADCLK = 50 MHz) | When the sample-and-hold circuit is in use per pin | 1.6 | — | — | µs | Sampling by the sample-and-hold circuit in 30 states.<br>Sampling by the A/D converter in 20 states. |
| | When the sample-and-hold circuit is not in use per pin | 1.0 | — | — | µs | Sampling by the A/D converter in 20 states. |
| Analog input capacitance | | — | — | 6 | pF | |
| Integral nonlinearity error | | — | — | ±4.0 | LSB | |
| Offset error | | — | — | ±7.5 | LSB | |
| Full-scale error | | — | — | ±7.5 | LSB | |
| Quantization error | | — | ±0.5 | — | LSB | |
| Absolute accuracy | Sample and hold circuit in use | — | — | ±8.0 | LSB | AVin = 0.25 to $AV_{REFH}$–0.25 |
| | Sample and hold circuit not in use | — | — | ±8.0 | LSB | AVin = $AV_{REFL}$ to $AV_{REFH}$ |
| Permissible signal source impedance | | — | — | 3.0 | kΩ | |

Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

### Table 6.17 Comparator Characteristics

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = $T_{opr}$

| Item | Symbol | Min | Typ | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Analog input capacitance | Cin | — | — | 6 | pF | |
| REFH pin offset voltage | Voff | — | — | 5 | mV | |
| REFL pin offset voltage | | — | — | 5 | mV | |
| REFH input voltage range | Vin | 1.7 | — | AVcc – 0.3 | V | |
| REFL input voltage range | | 0.3 | — | AVcc – 1.7 | V | |
| REFH reply time | tCR | — | — | 0.5 | µs | |
| REFL reply time | tCF | — | — | 0.5 | µs | |

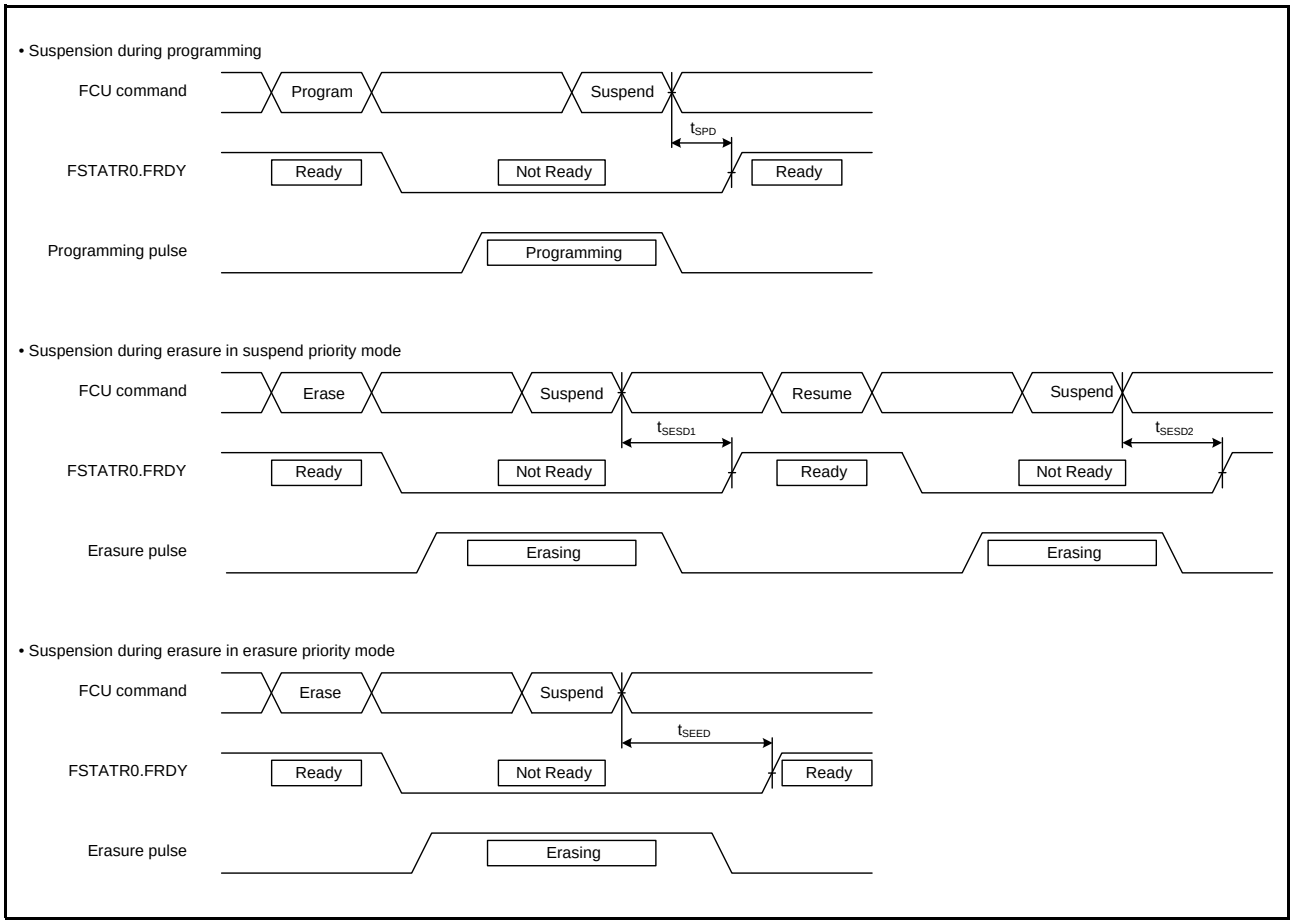



**Figure 6.31 Flash Memory Program/Erase Suspend Timing**

# REVISION HISTORY — RX63T Group Datasheet

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 1.00 | Aug 28, 2012 | — | First Edition issued |
| 2.00 | Mar 11, 2013 | Features | |
| | | 1 | Changed |
| | | 1. Overview | |
| | | 2 | 1.1 Outline of Specifications, description changed |
| | | 2 to 8 | Table 1.1 Outline of Specifications, changed |
| | | 9 | Table 1.2 Comparison of Functions for Different Packages, changed |
| | | 10 to 12 | Table 1.3 List of Products, changed |
| | | 12 | Figure 1.1 How to Read the Product Part Number, changed |
| | | 13 | Figure 1.2 Block Diagram, changed |
| | | 14 to 18 | Table 1.4 Pin Functions, changed |
| | | 19 | Figure 1.3 Pin Assignment (144-Pin LQFP), added |
| | | 20 | Figure 1.4 Pin Assignment (120-Pin LQFP), added |
| | | 21 | Figure 1.5 Pin Assignment (112-Pin LQFP), added |
| | | 22 | Figure 1.6 Pin Assignment (100-Pin LQFP), added |
| | | 23 | Figure 1.7 Pin Assignment (64-Pin LQFP), notes changed |
| | | 24 | Figure 1.8 Pin Assignment (48-Pin LQFP), notes changed |
| | | 25 to 28 | Table 1.5 List of Pins and Pin Functions (144-Pin LQFP), added |
| | | 29 to 32 | Table 1.6 List of Pins and Pin Functions (120-Pin LQFP), added |
| | | 33 to 36 | Table 1.7 List of Pins and Pin Functions (112-Pin LQFP), added |
| | | 37 to 39 | Table 1.8 List of Pins and Pin Functions (100-Pin LQFP), added |
| | | 3. Address Space | |
| | | 49 | Figure 3.1 Memory Map in Each Operating Mode, changed |
| | | 50 | 3.2 External Address Space, added |
| | | 4. I/O Registers | |
| | | 52 | (3) Number of Access Cycles to I/O Registers, description changed |
| | | 53 to 103 | Table 4.1 List of I/O Registers (Address Order), changed |
| | | 5. Electrical Characteristics [144-, 120-, 112- and 100-Pin Versions] | |
| | | 104 to 148 | Added |
| | | 6. Electrical Characteristics [64- and 48-Pin Versions] | |
| | | 149 | Title changed |
| | | 152 | Table 6.6 Clock Timing, changed |
| | | 158 | Table 6.10 Timing of On-Chip Peripheral Modules (1), changed |
| | | 160 | Table 6.12 Timing of On-Chip Peripheral Modules (3), changed |
| | | 170 | 6.6 Oscillation Stop Detection Circuit Characteristics, title changed |
| | | 170 | Table 6.18 Oscillation Stop Detection Circuit Characteristics, title changed |
| | | 171 | Table 6.19 ROM (Flash Memory for Code Storage) Characteristics (1), added |
| | | 171 | Table 6.20 ROM (Flash Memory for Code Storage) Characteristics (2), title and description changed |
| | | 172 | Table 6.21 DataFlash (Flash Memory for Data Storage) Characteristics (1), added |
| | | 172 | Table 6.22 DataFlash (Flash Memory for Data Storage) Characteristics (2), title and description changed |
| | | Appendix 1. Package Dimensions | |
| | | 174 to 177 | Figure A 144-Pin LQFP (PLQP0144KA-A) to Figure D 100-Pin LQFP (PLQP0100KB-A), added |
| 2.10 | Sep 26, 2013 | The RX63T Group and RX63T changed to this MCU | |
| | | Features | |
| | | 1 | Changed |
| | | 1. Overview | |
| | | 2 to 8 | Table 1.1 Outline of Specifications, changed, Note 1, added. |
| | | 9 | Table 1.2 Comparison of Functions for Different Packages, changed, Note 2, added. |
| | | 10 to 14 | Table 1.3 List of Products, changed, Note 1, added |
| | | 15 | Figure 1.1 How to Read the Product Part Number, changed |
| | | 28 to 31 | Table 1.5 List of Pins and Pin Functions (144-Pin LQFP), changed |
| | | 32 to 35 | Table 1.6 List of Pins and Pin Functions (120-Pin LQFP), changed |