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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	EBI/EMI, I ² C, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	69
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 12x10b, 8x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f563teedfh-v0

Table 1.2 Comparison of Functions for Different Packages

Functions			RX63T Group								
Package			144 Pins	120 Pins	112 Pins	100 Pins	64 Pins	48 Pins			
External bus			16 bits				—				
External address space			1 Mbyte × 4 areas				—				
DMA	DMA controller (DMACA)		Ch. 0 to 3								
	Data transfer controller (DTCa)		Supported								
Interrupt controller (ICUb)	NMI pin		Supported								
	IRQ pin		Supported (x 8)				Supported (x 6)				
Timers	Multi-function timer pulse unit 3 (MTU3)* ¹		Ch. 0 to 7								
	General PWM timer (GPT)* ¹	Generation of delays in PWM, not supported	Ch. 0 to 7				Ch. 0 to 3				
		Generation of delays in PWM, supported	Ch. 0 to 3				—				
	Port output enable 3 (POE3)		Supported (POE pins × 6)			Supported (POE pins × 5)	Supported (POE pins × 4)				
	Compare match timer (CMT)		Ch. 0 to 3								
	Watchdog timer (WDTA)		Supported								
	Independent watchdog timer (IWDTa)		Supported								
	Communication function	USB2.0 host/function module (USBa)		Ch. 0		—					
Serial communications interfaces (SClc)		Ch. 0 to 3			Ch. 0 to 2	Ch. 0, 1					
Serial communications interfaces (SCld)		Ch. 12									
I ² C bus interfaces (RIIC)		Ch. 0, 1		Ch. 0							
Serial peripheral interfaces (RSPI)		Ch. 0, 1				Ch. 0					
CAN module (CAN) (as an optional function)* ¹		Ch. 0				—					
12-bit A/D converter (S12ADB)			4 channels × 2 units				8 channels × 1 unit (AN000 to 007)	8 channels × 1 unit (AN000 to 004, 007)			
			Three-channel simultaneous sampling function				2 units			1 unit	
			Programmable gain amplifier				3 channels × 2 units			—	
			Window comparator				3 channels × 2 units			3 channels × 1 unit	
10-bit A/D converter (ADA)			20 channels	12 channels			—				
D/A converter (DAa)			Ch. 0, 1				—				
Clock Frequency Accuracy Measurement Circuit			Supported								
Digital power supply controller (DPC)* ²			Supported				Not supported				

Note 1. For the MTU3 and GPT, the number of pins will differ with the package. See the list of pins and pin functions for details.

In addition, the CAN module is an optional function. For details, see Table 1.3.

Note 2. Not provided for the product ID code O.

Table 1.6 List of Pins and Pin Functions (120-Pin LQFP) (3/4)

Pin Number 120-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3, GPT, POE3, CAC)	Communications (SClC, SClD, RSPI, RIIC, CAN, USB)	Interrupt	S12ADB, AD, DA
75	VSS						
76		P30	D10/[A10/ D10]	MTIOC0B/MTCLKD	SCK0/SSLA0/SSLB0		
77		P26	CS0#		TXD1/SMOSI1/ SSDA1/SDA1		
78		P25	CS1#		SCK1/SCL1		
79		P24	D11/[A11/D11]		CTS0#/RTS0#/SS0#/ RSPCKA/RSPCKB	IRQ4	
80		P23	D12/[A12/ D12]	CACREF	TXD0/SMOSI0/ SSDA0/MOSIA/ MOSIB/CTX1		
81		P22	D13/[A13/ D13]		RXD0/SMISO0/ SSCL0/MISOA/ MISOB/CRX1		ADTRG#
82		P21	D14/[A14/ D14]	MTCLKA		IRQ6-DS	ADTRG1#
83		P20	D15/[A15/ D15]	MTCLKB		IRQ7-DS	ADTRG0#
84		P65	A0/BC0#				AN5
85		P64	A1				AN4
86	AVCC						
87	VREF						
88	AVSS						
89		P63	A2				AN3
90		P62	A3				AN2
91		P61	A4				AN1
92		P60	A5				AN0
93		P55					AN11/DA1
94		P54					AN10/ DA0
95		P53	A6				AN9
96		P52	A7				AN8
97		P51					AN7
98		P50					AN6
99		P47					AN103/ CVREFH
100		P46					AN102
101		P45					AN101
102		P44					AN100
103		P43					AN003/ CVREFL
104		P42					AN002
105		P41					AN001
106		P40					AN000
107	AVCC0						
108	VREFH0						
109	VREFL0						
110	AVSS0						

Table 4.1 List of I/O Registers (Address Order) (5/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 703Eh	ICU	Interrupt Request Register 062	IR062	8	8	2 ICLK		ICUB	Not present in versions with 64 or 48 pins.
0008 7040h	ICU	Interrupt Request Register 064	IR064	8	8	2 ICLK			
0008 7041h	ICU	Interrupt Request Register 065	IR065	8	8	2 ICLK			
0008 7042h	ICU	Interrupt Request Register 066	IR066	8	8	2 ICLK			
0008 7043h	ICU	Interrupt Request Register 067	IR067	8	8	2 ICLK			
0008 7044h	ICU	Interrupt Request Register 068	IR068	8	8	2 ICLK			
0008 7045h	ICU	Interrupt Request Register 069	IR069	8	8	2 ICLK			
0008 7046h	ICU	Interrupt Request Register 070	IR070	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7047h	ICU	Interrupt Request Register 071	IR071	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 705Ah	ICU	Interrupt Request Register 090	IR090	8	8	2 ICLK			Not present in versions with 112, 100, 64 or 48 pins.
0008 7062h	ICU	Interrupt Request Register 098	IR098	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7066h	ICU	Interrupt Request Register 102	IR102	8	8	2 ICLK			
0008 7067h	ICU	Interrupt Request Register 103	IR103	8	8	2 ICLK			
0008 7068h	ICU	Interrupt Request Register 104	IR104	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7069h	ICU	Interrupt Request Register 105	IR105	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 706Ah	ICU	Interrupt Request Register 106	IR106	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 7072h	ICU	Interrupt Request Register 114	IR114	8	8	2 ICLK			
0008 707Ah	ICU	Interrupt Request Register 122	IR122	8	8	2 ICLK			
0008 707Bh	ICU	Interrupt Request Register 123	IR123	8	8	2 ICLK			
0008 707Ch	ICU	Interrupt Request Register 124	IR124	8	8	2 ICLK			
0008 707Dh	ICU	Interrupt Request Register 125	IR125	8	8	2 ICLK			
0008 707Eh	ICU	Interrupt Request Register 126	IR126	8	8	2 ICLK			
0008 707Fh	ICU	Interrupt Request Register 127	IR127	8	8	2 ICLK			
0008 7080h	ICU	Interrupt Request Register 128	IR128	8	8	2 ICLK			
0008 7081h	ICU	Interrupt Request Register 129	IR129	8	8	2 ICLK			
0008 7082h	ICU	Interrupt Request Register 130	IR130	8	8	2 ICLK			
0008 7083h	ICU	Interrupt Request Register 131	IR131	8	8	2 ICLK			
0008 7084h	ICU	Interrupt Request Register 132	IR132	8	8	2 ICLK			
0008 7085h	ICU	Interrupt Request Register 133	IR133	8	8	2 ICLK			
0008 7086h	ICU	Interrupt Request Register 134	IR134	8	8	2 ICLK			
0008 7087h	ICU	Interrupt Request Register 135	IR135	8	8	2 ICLK			
0008 7088h	ICU	Interrupt Request Register 136	IR136	8	8	2 ICLK			
0008 7089h	ICU	Interrupt Request Register 137	IR137	8	8	2 ICLK			
0008 708Ah	ICU	Interrupt Request Register 138	IR138	8	8	2 ICLK			
0008 708Bh	ICU	Interrupt Request Register 139	IR139	8	8	2 ICLK			
0008 708Ch	ICU	Interrupt Request Register 140	IR140	8	8	2 ICLK			
0008 708Dh	ICU	Interrupt Request Register 141	IR141	8	8	2 ICLK			
0008 708Eh	ICU	Interrupt Request Register 142	IR142	8	8	2 ICLK			
0008 708Fh	ICU	Interrupt Request Register 143	IR143	8	8	2 ICLK			
0008 7090h	ICU	Interrupt Request Register 144	IR144	8	8	2 ICLK			
0008 7091h	ICU	Interrupt Request Register 145	IR145	8	8	2 ICLK			
0008 7092h	ICU	Interrupt Request Register 146	IR146	8	8	2 ICLK			
0008 7093h	ICU	Interrupt Request Register 147	IR147	8	8	2 ICLK			
0008 7094h	ICU	Interrupt Request Register 148	IR148	8	8	2 ICLK			
0008 7095h	ICU	Interrupt Request Register 149	IR149	8	8	2 ICLK			
0008 7096h	ICU	Interrupt Request Register 150	IR150	8	8	2 ICLK			
0008 7097h	ICU	Interrupt Request Register 151	IR151	8	8	2 ICLK			

Table 4.1 List of I/O Registers (Address Order) (7/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 70C0h	ICU	Interrupt Request Register 192	IR192	8	8	2 ICLK		ICUb	Not present in versions with 112, 100, 64 or 48 pins.
0008 70C1h	ICU	Interrupt Request Register 193	IR193	8	8	2 ICLK			Not present in versions with 112, 100, 64 or 48 pins.
0008 70C2h	ICU	Interrupt Request Register 194	IR194	8	8	2 ICLK			
0008 70C3h	ICU	Interrupt Request Register 195	IR195	8	8	2 ICLK			
0008 70C4h	ICU	Interrupt Request Register 196	IR196	8	8	2 ICLK			
0008 70C5h	ICU	Interrupt Request Register 197	IR197	8	8	2 ICLK			
0008 70C6h	ICU	Interrupt Request Register 198	IR198	8	8	2 ICLK			
0008 70C7h	ICU	Interrupt Request Register 199	IR199	8	8	2 ICLK			
0008 70C8h	ICU	Interrupt Request Register 200	IR200	8	8	2 ICLK			
0008 70C9h	ICU	Interrupt Request Register 201	IR201	8	8	2 ICLK			
0008 70D6h	ICU	Interrupt Request Register 214	IR214	8	8	2 ICLK			
0008 70D7h	ICU	Interrupt Request Register 215	IR215	8	8	2 ICLK			
0008 70D8h	ICU	Interrupt Request Register 216	IR216	8	8	2 ICLK			
0008 70D9h	ICU	Interrupt Request Register 217	IR217	8	8	2 ICLK			
0008 70DAh	ICU	Interrupt Request Register 218	IR218	8	8	2 ICLK			
0008 70DBh	ICU	Interrupt Request Register 219	IR219	8	8	2 ICLK			
0008 70DCh	ICU	Interrupt Request Register 220	IR220	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70DDh	ICU	Interrupt Request Register 221	IR221	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70DEh	ICU	Interrupt Request Register 222	IR222	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 70DFh	ICU	Interrupt Request Register 223	IR223	8	8	2 ICLK			Not present in versions with 100, 64 or 48 pins.
0008 70E0h	ICU	Interrupt Request Register 224	IR224	8	8	2 ICLK			Not present in versions with 100, 64 or 48 pins.
0008 70E1h	ICU	Interrupt Request Register 225	IR225	8	8	2 ICLK			Not present in versions with 100, 64 or 48 pins.
0008 70E2h	ICU	Interrupt Request Register 226	IR226	8	8	2 ICLK			
0008 70E3h	ICU	Interrupt Request Register 227	IR227	8	8	2 ICLK			
0008 70E4h	ICU	Interrupt Request Register 228	IR228	8	8	2 ICLK			
0008 70E5h	ICU	Interrupt Request Register 229	IR229	8	8	2 ICLK			
0008 70E6h	ICU	Interrupt Request Register 230	IR230	8	8	2 ICLK			
0008 70E7h	ICU	Interrupt Request Register 231	IR231	8	8	2 ICLK			
0008 70E8h	ICU	Interrupt Request Register 232	IR232	8	8	2 ICLK			
0008 70E9h	ICU	Interrupt Request Register 233	IR233	8	8	2 ICLK			
0008 70EAh	ICU	Interrupt Request Register 234	IR234	8	8	2 ICLK			
0008 70EBh	ICU	Interrupt Request Register 235	IR235	8	8	2 ICLK			
0008 70ECh	ICU	Interrupt Request Register 236	IR236	8	8	2 ICLK			
0008 70EEh	ICU	Interrupt Request Register 238	IR238	8	8	2 ICLK			
0008 70EFh	ICU	Interrupt Request Register 239	IR239	8	8	2 ICLK			
0008 70F0h	ICU	Interrupt Request Register 240	IR240	8	8	2 ICLK			
0008 70F1h	ICU	Interrupt Request Register 241	IR241	8	8	2 ICLK			
0008 70F2h	ICU	Interrupt Request Register 242	IR242	8	8	2 ICLK			
0008 70F4h	ICU	Interrupt Request Register 244	IR244	8	8	2 ICLK			
0008 70F5h	ICU	Interrupt Request Register 245	IR245	8	8	2 ICLK			
0008 70F6h	ICU	Interrupt Request Register 246	IR246	8	8	2 ICLK			
0008 70F7h	ICU	Interrupt Request Register 247	IR247	8	8	2 ICLK			
0008 70F8h	ICU	Interrupt Request Register 248	IR248	8	8	2 ICLK			
0008 70FAh	ICU	Interrupt Request Register 250	IR250	8	8	2 ICLK			
0008 70FBh	ICU	Interrupt Request Register 251	IR251	8	8	2 ICLK			
0008 70FCh	ICU	Interrupt Request Register 252	IR252	8	8	2 ICLK			

Table 4.1 List of I/O Registers (Address Order) (18/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 90E0h	S12AD	Comparator Operating Mode Selection Register 0	ADCMPPMD0	16	16	2, 3 PCLKB	2 ICLK	S12ADB	
0008 90E2h	S12AD	Comparator Operating-Mode Selection Register 1	ADCMPPMD1	16	16	2, 3 PCLKB	2 ICLK		
0008 90E4h	S12AD	Comparator Filter-Mode Register	ADCMPPNR0	16	16	2, 3 PCLKB	2 ICLK		
0008 90E8h	S12AD	Comparator Detection Flag Register	ADCMPPFR	8	8	2, 3 PCLKB	2 ICLK		
0008 90EAh	S12AD	Comparator Interrupt Selection Register	ADCMPPSEL	16	16	2, 3 PCLKB	2 ICLK		
0008 90FCh	S12AD	A/D Group Scan Priority Control Register	ADGSPMR	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9100h	S12AD1	A/D Control Register	ADCSR	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9104h	S12AD1	A/D Channel Select Register A	ADANSA	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9108h	S12AD1	A/D-Converted Value Addition Mode Select Register (ADADS)	ADADS	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 910Ch	S12AD1	A/D-Converted Value Addition Count Select Register	ADADC	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 910Eh	S12AD1	A/D Control Extended Register	ADCER	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9110h	S12AD1	A/D Start Trigger Select Register	ADSTRGR	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9114h	S12AD1	A/D Channel Select Register B	ADANSB	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9118h	S12AD1	A/D Data-Doubling Register	ADDBLDR	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 911Eh	S12AD1	A/D Self-Diagnosis Data Register	ADRD	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9120h	S12AD1	A/D Data Register 0	ADDR0	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9122h	S12AD1	A/D Data Register 1	ADDR1	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9124h	S12AD1	A/D Data Register 2	ADDR2	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9126h	S12AD1	A/D Data Register 3	ADDR3	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9160h	S12AD1	A/D Sampling State Register 0	ADSSTR0	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9166h	S12AD1	A/D Sample and Hold Circuit Control Register	ADSHCR	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9173h	S12AD1	A/D Sampling State Register 1	ADSSTR1	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9174h	S12AD1	A/D Sampling State Register 2	ADSSTR2	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9175h	S12AD1	A/D Sampling State Register 3	ADSSTR3	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9180h	S12AD1	A/D Group Scan Priority Control Register	ADGSPCR	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9184h	S12AD1	A/D Data-Doubling Register A	ADDBLDRA	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9186h	S12AD1	A/D Data-Doubling Register B	ADDBLDRB	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 918Ah	S12AD1	A/D Programmable Gain Amplifier Register	ADPG	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 91E0h	S12AD1	Comparator Operating Mode Selection Register 0	ADCMPPMD0	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 91E2h	S12AD1	Comparator Operating-Mode Selection Register 1	ADCMPPMD1	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 91E4h	S12AD1	Comparator Filter-Mode Register	ADCMPPNR0	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 91E8h	S12AD1	Comparator Detection Flag Register	ADCMPPFR	8	8	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 91EAh	S12AD1	Comparator Interrupt Selection Register	ADCMPPSEL	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.
0008 9800h	AD	A/D Control Register	ADCSR	16	16	2, 3 PCLKB	2 ICLK		Not present in versions with 64 or 48 pins.

Table 4.1 List of I/O Registers (Address Order) (43/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
000C 291Ah	GPT4	General PWM Timer Compare Capture Register F	GTCCRF	16	16, 32	2 to 5 PCLKA	2, 3 ICLK	GPT	Not present in versions with 64 or 48 pins.
000C 291Ch	GPT4	General PWM Timer Cycle Setting Register	GTPR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 291Eh	GPT4	General PWM Timer Cycle Setting Buffer Register	GTPBR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2920h	GPT4	General PWM Timer Cycle Setting Double-Buffer Register	GTPDBR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2924h	GPT4	A/D Converter Start Request Timing Register A	GTADTRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2926h	GPT4	A/D Converter Start Request Timing Buffer Register A	GTADTBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2928h	GPT4	A/D Converter Start Request Timing Double-Buffer Register A	GTADTDBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 292Ch	GPT4	A/D Converter Start Request Timing Register B	GTADTRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 292Eh	GPT4	A/D Converter Start Request Timing Buffer Register B	GTADTBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2930h	GPT4	A/D Converter Start Request Timing Double-Buffer Register B	GTADTDBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2934h	GPT4	General PWM Timer Output Negate Control Register	GTONCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2936h	GPT4	General PWM Timer Dead Time Control Register	GTDTCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2938h	GPT4	General PWM Timer Dead Time Value Register U	GTDVU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 293Ah	GPT4	General PWM Timer Dead Time Value Register D	GTDVD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 293Ch	GPT4	General PWM Timer Dead Time Buffer Register U	GTDBU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 293Eh	GPT4	General PWM Timer Dead Time Buffer Register D	GTDBD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2940h	GPT4	General PWM Timer Output Protection Function Status Register	GTSOS	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2942h	GPT4	General PWM Timer Output Protection Function Temporary Release Register	GTSOTR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2980h	GPT5	General PWM Timer I/O Control Register	GTIOR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2982h	GPT5	General PWM Timer Interrupt Output Setting Register	GTINTAD	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2984h	GPT5	General PWM Timer Control Register	GTCR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2986h	GPT5	General PWM Timer Buffer Enable Register	GTBER	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2988h	GPT5	General PWM Timer Count Direction Register	GTUDC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 298Ah	GPT5	General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register	GTITC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 298Ch	GPT5	General PWM Timer Status Register	GTST	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 298Eh	GPT5	General PWM Timer Counter	GTCNT	16	16	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2990h	GPT5	General PWM Timer Compare Capture Register A	GTCCRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2992h	GPT5	General PWM Timer Compare Capture Register B	GTCCRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2994h	GPT5	General PWM Timer Compare Capture Register C	GTCCRC	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2996h	GPT5	General PWM Timer Compare Capture Register D	GTCCRD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2998h	GPT5	General PWM Timer Compare Capture Register E	GTCCRE	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 299Ah	GPT5	General PWM Timer Compare Capture Register F	GTCCRF	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 299Ch	GPT5	General PWM Timer Cycle Setting Register	GTPR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.

Table 4.1 List of I/O Registers (Address Order) (44/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK $\geq$ PCLK	ICLK $<$ PCLK		
000C 299Eh	GPT5	General PWM Timer Cycle Setting Buffer Register	GTPBR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK	GPT	Not present in versions with 64 or 48 pins.
000C 29A0h	GPT5	General PWM Timer Cycle Setting Double-Buffer Register	GTPDBR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 29A4h	GPT5	A/D Converter Start Request Timing Register A	GTADTRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 29A6h	GPT5	A/D Converter Start Request Timing Buffer Register A	GTADTBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 29A8h	GPT5	A/D Converter Start Request Timing Double-Buffer Register A	GTADTDBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 29ACh	GPT5	A/D Converter Start Request Timing Register B	GTADTRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 29AEh	GPT5	A/D Converter Start Request Timing Buffer Register B	GTADTBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 29B0h	GPT5	A/D Converter Start Request Timing Double-Buffer Register B	GTADTDBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 29B4h	GPT5	General PWM Timer Output Negate Control Register	GTONCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 29B6h	GPT5	General PWM Timer Dead Time Control Register	GTDTCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 29B8h	GPT5	General PWM Timer Dead Time Value Register U	GTDVU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 29BAh	GPT5	General PWM Timer Dead Time Value Register D	GTDVD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 29BCh	GPT5	General PWM Timer Dead Time Buffer Register U	GTDBU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 29BEh	GPT5	General PWM Timer Dead Time Buffer Register D	GTDBD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 29C0h	GPT5	General PWM Timer Output Protection Function Status Register	GTSOS	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 29C2h	GPT5	General PWM Timer Output Protection Function Temporary Release Register	GTSOTR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A00h	GPT6	General PWM Timer I/O Control Register	GTIOR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A02h	GPT6	General PWM Timer Interrupt Output Setting Register	GTINTAD	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A04h	GPT6	General PWM Timer Control Register	GTCR	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A06h	GPT6	General PWM Timer Buffer Enable Register	GTBER	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A08h	GPT6	General PWM Timer Count Direction Register	GTUDC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A0Ah	GPT6	General PWM Timer Interrupt, A/D Converter Start Request Skipping Setting Register	GTITC	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A0Ch	GPT6	General PWM Timer Status Register	GTST	16	8, 16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A0Eh	GPT6	General PWM Timer Counter	GTCNT	16	16	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A10h	GPT6	General PWM Timer Compare Capture Register A	GTCCRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A12h	GPT6	General PWM Timer Compare Capture Register B	GTCCRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A14h	GPT6	General PWM Timer Compare Capture Register C	GTCCRC	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A16h	GPT6	General PWM Timer Compare Capture Register D	GTCCRD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A18h	GPT6	General PWM Timer Compare Capture Register E	GTCCRE	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A1Ah	GPT6	General PWM Timer Compare Capture Register F	GTCCRF	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A1Ch	GPT6	General PWM Timer Cycle Setting Register	GTPR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A1Eh	GPT6	General PWM Timer Cycle Setting Buffer Register	GTPBR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2A20h	GPT6	General PWM Timer Cycle Setting Double-Buffer Register	GTPDBR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.

Table 4.1 List of I/O Registers (Address Order) (46/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK $\geq$ PCLK	ICLK $<$ PCLK		
000C 2AA8h	GPT7	A/D Converter Start Request Timing Double-Buffer Register A	GTADTDBRA	16	16, 32	2 to 5 PCLKA	2, 3 ICLK	GPT	Not present in versions with 64 or 48 pins.
000C 2AACh	GPT7	A/D Converter Start Request Timing Register B	GTADTRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2AAEh	GPT7	A/D Converter Start Request Timing Buffer Register B	GTADTBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2AB0h	GPT7	A/D Converter Start Request Timing Double-Buffer Register B	GTADTDBRB	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2AB4h	GPT7	General PWM Timer Output Negate Control Register	GTONCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2AB6h	GPT7	General PWM Timer Dead Time Control Register	GTDTCR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2AB8h	GPT7	General PWM Timer Dead Time Value Register U	GTDVU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2ABAh	GPT7	General PWM Timer Dead Time Value Register D	GTDVD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2ABCh	GPT7	General PWM Timer Dead Time Buffer Register U	GTDBU	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2ABEh	GPT7	General PWM Timer Dead Time Buffer Register D	GTDBD	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2AC0h	GPT7	General PWM Timer Output Protection Function Status Register	GTSOS	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C 2AC2h	GPT7	General PWM Timer Output Protection Function Temporary Release Register	GTSOTR	16	16, 32	2 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3002h	DPC	Software Start Setting Register 0	SOFTSTART 0	16	16	3 to 5 PCLKA	2, 3 ICLK	DPC	Not present in versions with 64 or 48 pins.
000C3006h	DPC	Software Start Setting Register 1	SOFTSTART 1	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C300Ah	DPC	Software Start Setting Register 2	SOFTSTART 2	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C300Eh	DPC	Software Start Setting Register 3	SOFTSTART 3	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3012h	DPC	Reference Value Setting Register 0	VOTARGET 0	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3016h	DPC	Reference Value Setting Register 1	VOTARGET 1	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C301Ah	DPC	Reference Value Setting Register 2	VOTARGET 2	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C301Eh	DPC	Reference Value Setting Register 3	VOTARGET 3	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3022h	DPC	Reference Value Select Register	REFSEL	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3026h	DPC	PWM Channel Setting Register	CHLSEL	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C302Ah	DPC	Control Enable Setting Register	ENABLE	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C302Eh	DPC	Control Calculation Parameter Setting Register KP0	PARAMKP0	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3032h	DPC	Control Calculation Parameter Setting Register KI0	PARAMKI0	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3036h	DPC	Control Calculation Parameter Setting Register KQ0	PARAMKQ0	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C303Ah	DPC	Control Calculation Parameter Setting Register KF0	PARAMKF0	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C303Eh	DPC	Control Calculation Parameter Setting Register KP1	PARAMKP1	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3042h	DPC	Control Calculation Parameter Setting Register KI1	PARAMKI1	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3046h	DPC	Control Calculation Parameter Setting Register KQ1	PARAMKQ1	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C304Ah	DPC	Control Calculation Parameter Setting Register KF1	PARAMKF1	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C304Eh	DPC	Control Calculation Parameter Setting Register KP2	PARAMKP2	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.
000C3052h	DPC	Control Calculation Parameter Setting Register KI2	PARAMKI2	16	16	3 to 5 PCLKA	2, 3 ICLK		Not present in versions with 64 or 48 pins.

Table 5.3 DC Characteristics (2)

Note: Common standard values for conditions not given in the table are listed as "Condition 1" to "Condition 3" below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

The following relation applies when the USB is in use under condition 1 or condition 2: Vcc = PLLVcc = Vcc_USB = 3.0 to 3.6 V.

T_a = T_{opr}. T_a is common to conditions 1 to 3.

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output high voltage	All output pins (except for P52, P53, P60 to P65, P71 to P76, P90 to P95, and USB0_DPUPE)	V _{OH}	VCC – 0.5	—	—	V	I _{OH} = –1 mA
	P52, P53, and P60 to P65		AVCC – 0.5	—	—		I _{OH} = –1 mA
	USB0_DPUPE		VCC_USB – 0.5				I _{OH} = –1 mA
	P71 to P76, and P90 to P95		VCC – 1.0	—	—		I _{OH} = –5 mA
Output low voltage	All output pins (except for P71 to P76, P90 to P95, and RIIC pins)	V _{OL}	—	—	0.5	V	I _{OL} = 1.0 mA
	P71 to P76, and P90 to P95		—	—	1.1		I _{OL} = 15 mA
	RIIC pins		—	—	0.4		I _{OL} = 3 mA
			—	—	0.6		I _{OL} = 6 mA
Input leakage current	RES#, MD pin, EMLE, Port 4, Ports P50, P51, P54 to P57, and Port C	I _{in}	—	—	1.0	μA	V _{in} = 0 V, V _{in} = VCC
Three-state leakage current (off state)	Port 0, Port 1, Ports P20 to P24, Port 3, Ports P52, P53, Ports 6 to A, Ports PB0, PB3 to PB7, and Ports D to G	I _{TSI}	—	—	1.0	μA	V _{in} = 0 V, V _{in} = VCC
	Ports P25, P26, PB1, and PB2		—	—	5.0		
Input capacitance	All output pins (except for P25, P26, PB1, and PB2)	C _{in}	—	—	15	pF	V _{in} = 0 V, f = 1 MHz, T _a = 25 °C
	Ports P25, P26, PB1, and PB2		—	—	30		

Table 5.5 Permissible Output Currents

Note: Common standard values for conditions not given in the table are listed as "Condition 1" to "Condition 3" below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

The following relation applies when the USB is in use under condition 1 or condition 2: Vcc = PLLVcc = Vcc_USB = 3.0 to 3.6 V.

T_a = T_{opr} T_a is common to conditions 1 to 3.

Item		Symbol	Min.	Typ.	Max.	Unit
Permissible output low current (average value per pin)	All output pins (except for P71 to P76, P90 to P95, and RIIC pins)*1	I _{OL}	—	—	2.0	mA
	RIIC pins	I _{OL}	—	—	6.0	mA
	P71 to P76, and P90 to P95*2	I _{OL}	—	—	15.0	mA
Permissible output low current (max. value per pin)	All output pins (except for P71 to P76, P90 to P95, and RIIC pins)*1	I _{OL}	—	—	4.0	mA
	RIIC pins	I _{OL}	—	—	6.0	mA
	P71 to P76, and P90 to P95*2	I _{OL}	—	—	15.0	mA
Permissible output low current (total)	Total of output pins	ΣI _{OL}	—	—	110	mA
Permissible output high current (average value per pin)	All output pins (except for P71 to P76, P90 to P95, and USB0_DPUPE pin)*1	−I _{OH}	—	—	2.0	mA
	USB0_DPUPE pin	−I _{OH}	—	—	3.0	mA
	P71 to P76, and P90 to P95*2	−I _{OH}	—	—	5.0	mA
Permissible output high current (max. value per pin)	All output pins (except for P71 to P76, P90 to P95)*1	−I _{OH}	—	—	4.0	mA
	P71 to P76, and P90 to P95*2	−I _{OH}	—	—	5.0	mA
Permissible output high current (total)		Σ−I _{OH}	—	—	35	mA

Note 1. USB0_DP and USB0_DM are not included.

Note 2. For pins P71 to P76 and P90 to P95, I_{OL} = 15 mA (max.) and −I_{OH} = 5 mA (max.). However, if several of the pins are to supply I_{OL} and −I_{OH} of more than 2.0 mA at the same time, the number of pins should be six or less.

Caution: To protect the MCU's reliability, the output current values should not exceed the values in this table.

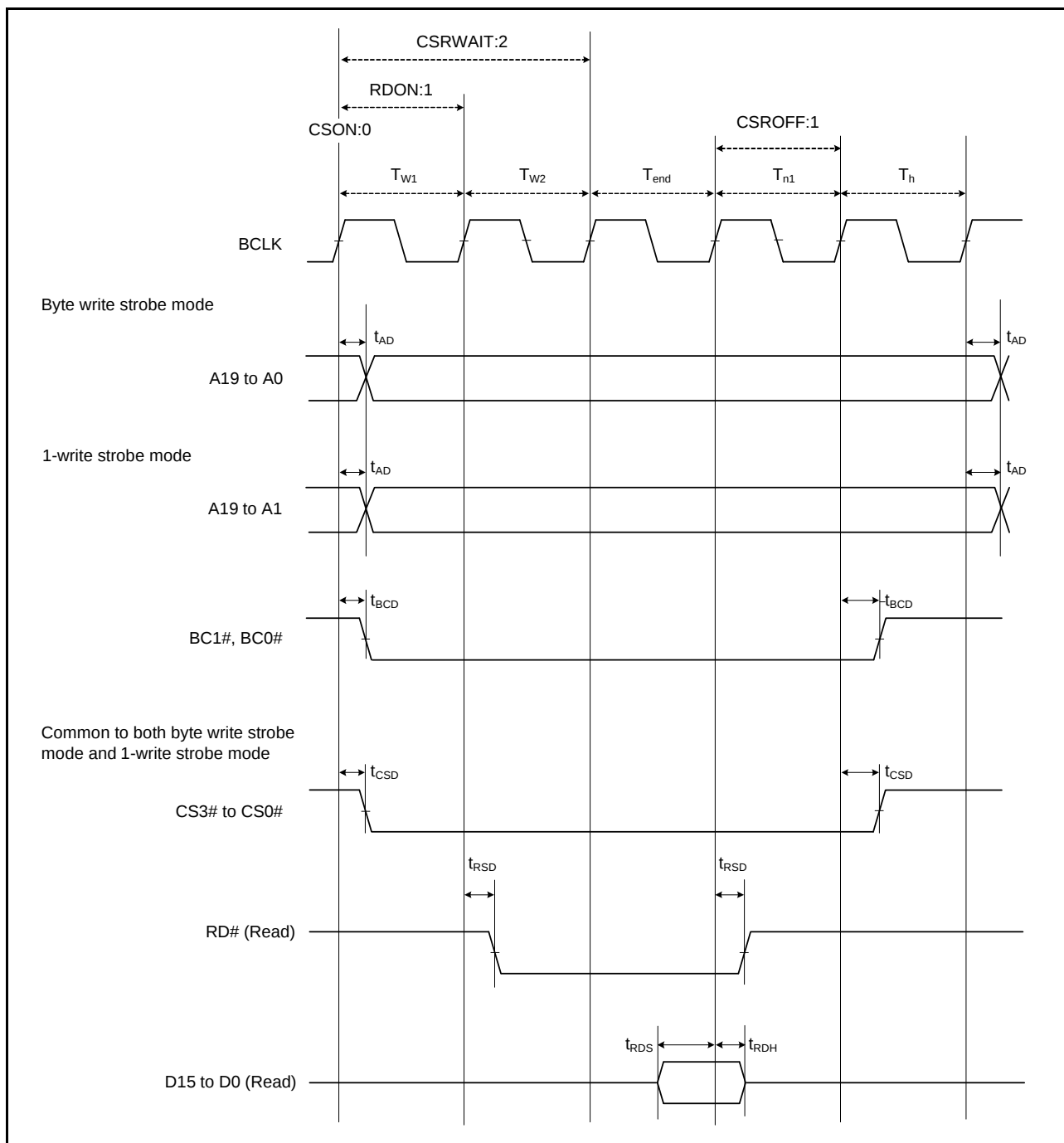


Figure 5.13 External Bus Timing/Normal Read Cycle (Bus Clock Synchronized)

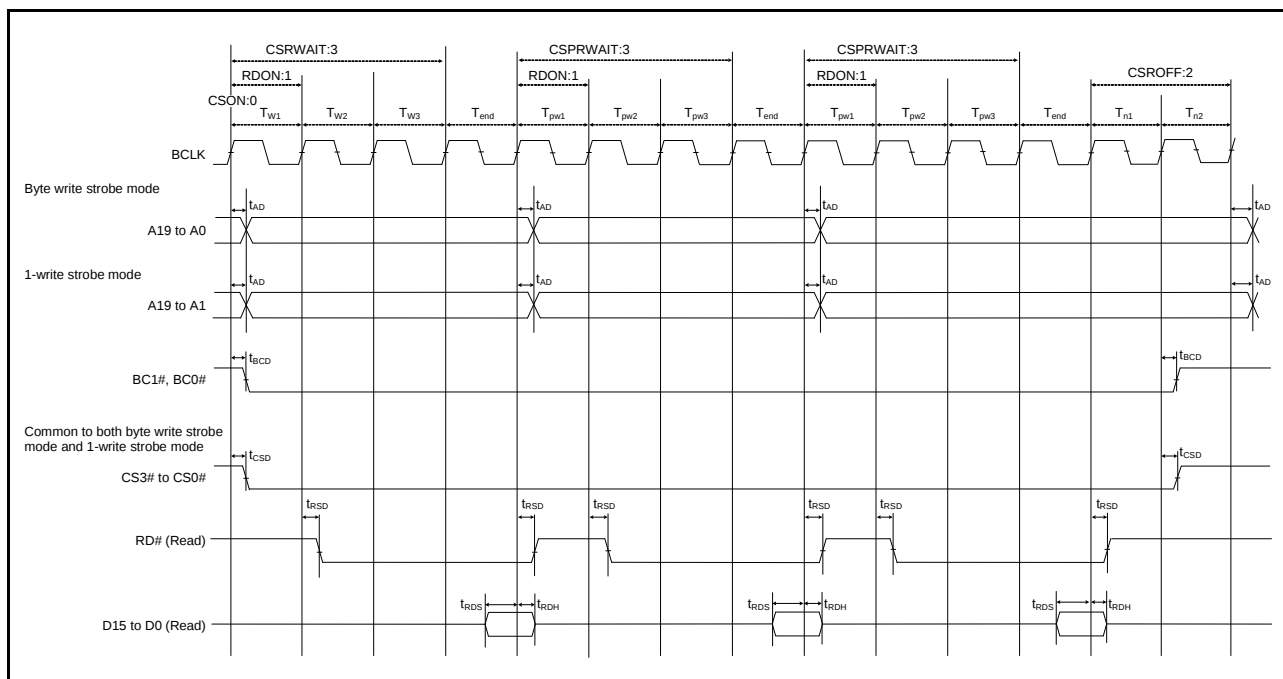


Figure 5.15 External Bus Timing/Page Read Cycle (Bus Clock Synchronized)

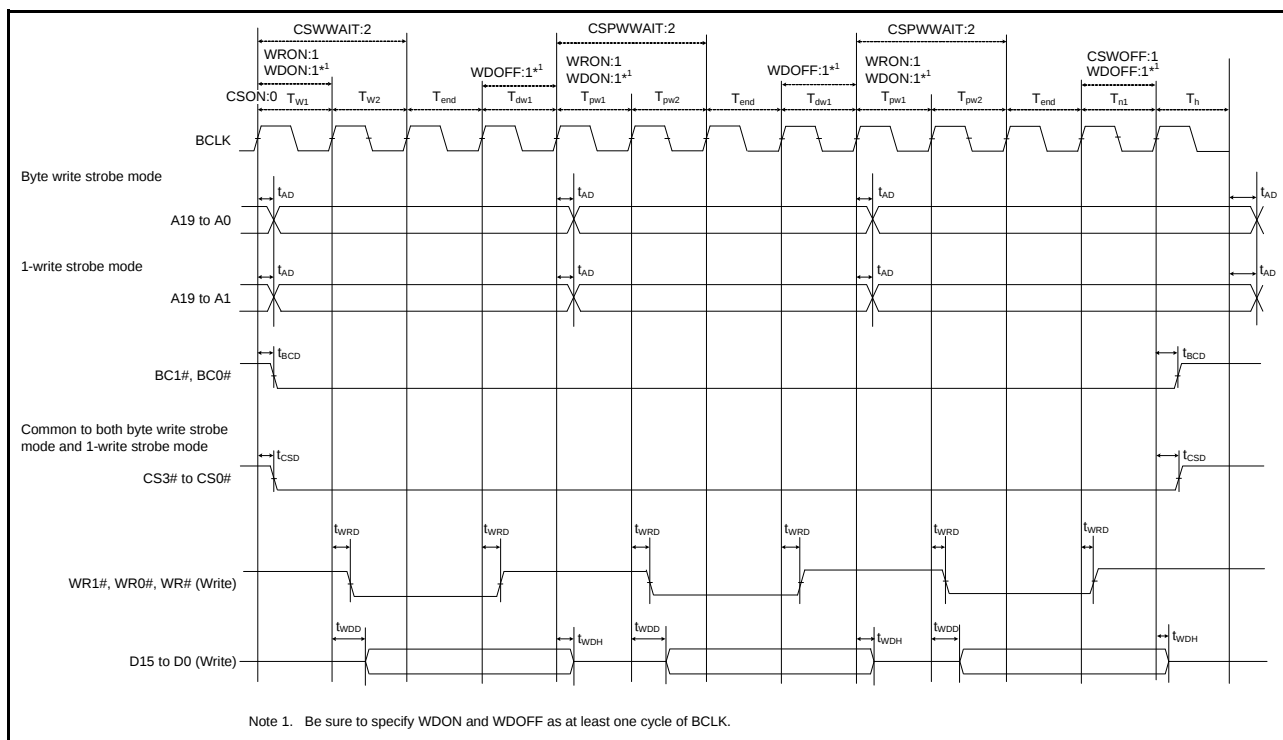


Figure 5.16 External Bus Timing/Page Write Cycle (Bus Clock Synchronized)

Table 5.16 Timing of On-Chip Peripheral Modules (6)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

T_a = T_{opr}. T_a is common to conditions 1 to 3.

Item		Symbol	Min.*1, *2	Max.	Unit	Test Conditions
Simple IIC (Standard-mode)	SCL, SDA input rise time	t _{Sr}	—	1000	ns	Figure 5.36
	SCL, SDA input fall time	t _{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t _{SP}	0	4 × t _{Pcy}	ns	
	Data input setup time	t _{SDAS}	250	—	ns	
	Data input hold time	t _{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C _b	—	400	pF	
Simple IIC (Fast-mode)	SCL, SDA input rise time	t _{Sr}	20 + 0.1C _b	300	ns	
	SCL, SDA input fall time	t _{Sf}	20 + 0.1C _b	300	ns	
	SCL, SDA input spike pulse removal time	t _{SP}	0	4 × t _{Pcy}	ns	
	Data input setup time	t _{SDAS}	100	—	ns	
	Data input hold time	t _{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C _b	—	400	pF	

Note 1. The value in parentheses is used when ICMR3.NF[1:0] are set to 11b while a digital filter is enabled with ICFER.NFE = 1.

Note 2. C_b indicates the total capacity of the bus line.

Note 3. t_{Pcy}: PCLK cycle

5.3.7 Timing of PWM Delay Generation Circuit

Table 5.17 Timing of the PWM Delay Generation Circuit

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

T_a = T_{opr}. T_a is common to conditions 1 to 3.

Item	Symbol	Typ.	Max.	Unit	Test Conditions
Resolution	—	312.5	—	ps	PCLKA = 100 MHz
DNL*1	—	±2.0	—	LSB	

Note 1. This value is correct when the difference between each code and the next is a resolution of one bit (1 LSB).

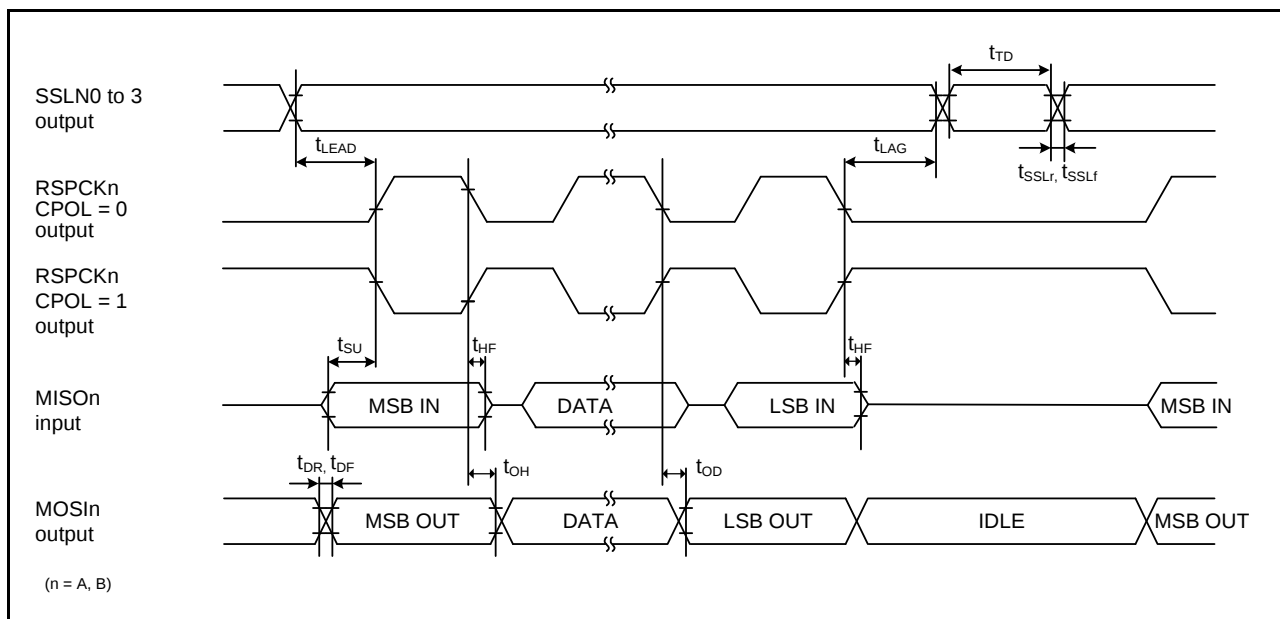


Figure 5.31 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKB Division Ratio Set to 1/2)

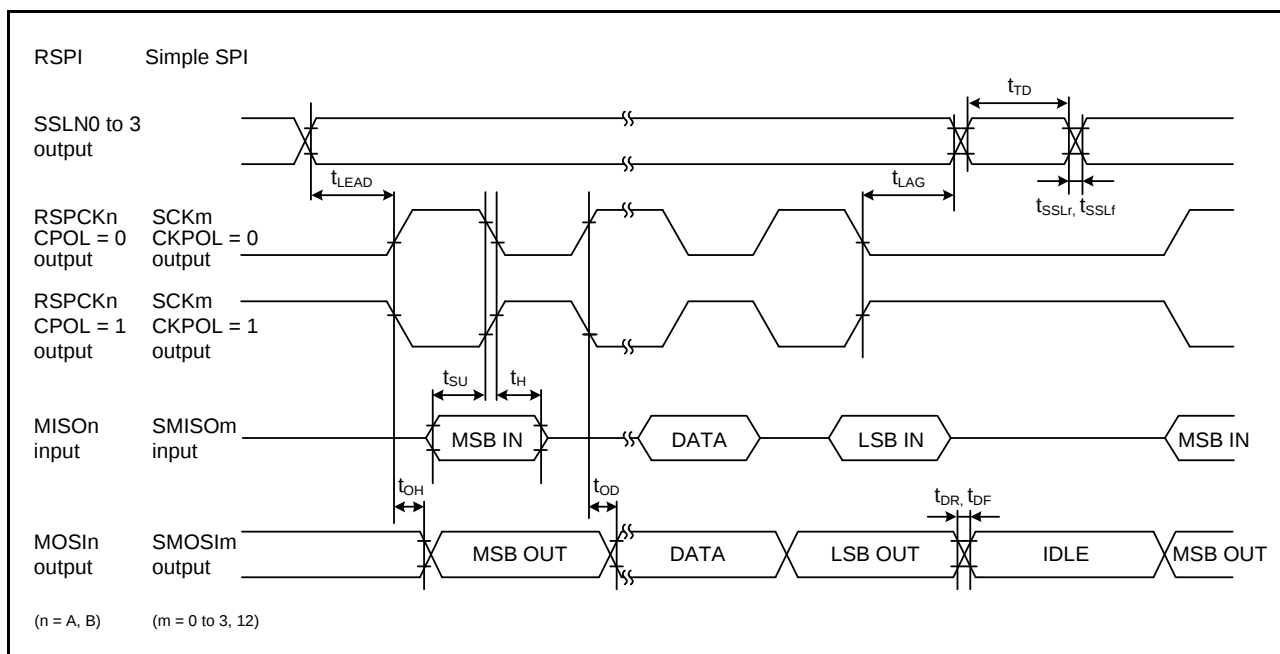


Figure 5.32 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKB Division Ratio Set to a Value Other Than 1/2) and Simple SPI Timing (Master, CKPH = 0)

5.7 Power-on Reset Circuit and Voltage Detection Circuit Characteristics

Table 5.26 Power-on Reset Circuit and Voltage Detection Circuit Characteristics (1)

Note: Common standard values for conditions not given in the table are listed as "Condition 1" and "Condition 2" below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

T_a = T_{opr}, T_a is common to conditions 1 and 2.

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	V _{POR}	2.46	2.58	2.7	V	Figure 5.41
	Voltage detection circuit (LVD0)	V _{DET0}	2.7	2.82	2.94		Figure 5.42
	Voltage detection circuit (LVD1)*1	V _{DET1_8}	2.75	2.90	3.05		Figure 5.43
		V _{DET1_9}	2.70	2.85	3.00		
		V _{DET1_A}	2.73	2.88	3.03		
	Voltage detection circuit (LVD2)*2	V _{DET2_8}	2.75	2.9	3.05		Figure 5.44
		V _{DET2_9}	2.70	2.85	3.00		
		V _{DET2_A}	2.73	2.88	3.03		
Internal reset time	Power-on reset (POR)	t _{POR}		9.7		ms	Figure 5.41
	Voltage detection circuit (LVD0)	t _{LVD0}		9.7			Figure 5.42
	Voltage detection circuit (LVD1)	t _{LVD1}		0.9			Figure 5.43
	Voltage detection circuit (LVD2)	t _{LVD2}		0.9			Figure 5.44
Minimum VCC down time*3		t _{VOFF}	200	—	—	μs	Figure 5.41 and Figure 5.42
Response delay time		t _{DET}			200	μs	
LVD operation stabilization time (after LVD is enabled)		T _{d(E-A)}			3	μs	Figure 5.41 to Figure 5.44
Hysteresis width (LVD1 and LVD2)		V _{LVH}		80		mV	

Note 1. # in symbol V_{DET1_#} indicates the value of the LVDLVLR.LVD1LVL[3:0] bits.

Note 2. # in symbol V_{DET2_#} indicates the value of the LVDLVLR.LVD2LVL[3:0] bits.

Note 3. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{DET1}, and V_{DET2} for the POR/ LVD.

5.9 ROM (Flash Memory for Code Storage) Characteristics

Table 5.29 ROM (Flash Memory for Code Storage) Characteristics (1)

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Temperature range for the programming/erasure operation: $T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Reprogram/erase cycle*1	N_{pec}	1000	—	—	Times	
Data hold time	t_{DRP}	30*2	—	—	Year	$T_a = +85^\circ\text{C}$

Note 1. Definition of reprogram/erase cycle:

The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times ($n = 1000$), erasing can be performed n times for each block. For instance, when 128-byte programming is performed 16 times for different addresses in 2-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. The value is obtained from the reliability test.

Table 5.30 ROM (Flash Memory for Code Storage) Characteristics (2)

Note: Common standard values for conditions not given in the table are listed as "Condition 1" to "Condition 3" below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Temperature range for the programming/erasure operation: $T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time $N_{PEC} \leq 100$ times	128 bytes	t_{P128}	—	2.8	28	—	1	10	ms
	4 Kbytes	t_{P4K}	—	63	140	—	23	50	ms
	16 Kbytes	t_{P16K}	—	252	560	—	90	200	ms
Programming time $N_{PEC} > 100$ times	128 bytes	t_{P128}	—	3.4	33.6	—	1.2	12	ms
	4 Kbytes	t_{P4K}	—	75.6	168	—	27.6	60	ms
	16 Kbytes	t_{P16K}	—	302.4	672	—	108	240	ms
Erasure time $N_{PEC} \leq 100$ times	4 Kbytes	t_{E4K}	—	50	120	—	25	60	ms
	16 Kbytes	t_{E16K}	—	200	480	—	100	240	ms
Erasure time $N_{PEC} > 100$ times	4 Kbytes	t_{E4K}	—	60	144	—	30	72	ms
	16 Kbytes	t_{E16K}	—	240	576	—	120	288	ms
Suspend delay time during programming		t_{SPD}	—	—	400	—	—	120	μs
First suspend delay time during erasing (in suspend priority mode)		t_{SESD1}	—	—	300	—	—	120	μs
Second suspend delay time during erasing (in suspend priority mode)		t_{SESD2}	—	—	1.7	—	—	1.7	ms
Suspend delay time during erasing (in erasure priority mode)		t_{SEED}	—	—	1.7	—	—	1.7	ms
FCU reset time		t_{FCUR}	35	—	—	35	—	—	μs

6.2 DC Characteristics

Table 6.2 DC Characteristics (1)

Conditions: $V_{CC} = 2.7$ to 3.6 V, $V_{SS} = AVSS0 = VREFL0 = 0$ V,
 $AVCC0 = 3.0$ to 3.6 V, $VREFH0 = 3.0$ V to $AVCC0$,
 $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	IRQ input pin	V_{IH}	$V_{CC} \times 0.8$	—	$V_{CC} + 0.3$	V
	MTU3 input pin	V_{IL}	-0.3	—	$V_{CC} \times 0.2$	
	POE3 input pin	ΔV_T	$V_{CC} \times 0.06$	—	—	
	SCI input pin					
	A/D trigger input pin					
	GPT input pin					
	RES#, NMI					
	RIIC input pin (IICBus operating)	V_{IH}	$V_{CC} \times 0.7$	—	5.8	
		V_{IL}	-0.3	—	$V_{CC} \times 0.3$	
		ΔV_T	$V_{CC} \times 0.05$	—	—	
	Port 4 (also used as an analog port)	V_{IH}	$AVCC0 \times 0.8$	—	$AVCC0 + 0.3$	
		V_{IL}	-0.3	—	$AVCC0 \times 0.2$	
	Ports for 5 V tolerant*1	V_{IH}	$V_{CC} \times 0.8$	—	5.8	
		V_{IL}	-0.3	—	$V_{CC} \times 0.2$	
Input high voltage (except for Schmitt trigger input pin)	MD pin, EMLE	V_{IH}	$V_{CC} \times 0.9$	—	$V_{CC} + 0.3$	V
	EXTAL, TCK, RSPI input pin		$V_{CC} \times 0.8$	—	$V_{CC} + 0.3$	
	RIIC input pin (SMBus operating)		2.1	—	$V_{CC} + 0.3$	
Input low voltage (except for Schmitt trigger input pin)	MD pin, EMLE	V_{IL}	-0.3	—	$V_{CC} \times 0.1$	
	EXTAL, TCK, RSPI input pin		-0.3	—	$V_{CC} \times 0.2$	
	RIIC input pin (SMBus operating)		-0.3	—	0.8	
Output high voltage	All output pins	V_{OH}	$V_{CC} - 0.5$	—	—	$I_{OH} = -1$ mA
Output low voltage	All output pins (except for RIIC pins)	V_{OL}	—	—	0.5	$I_{OL} = 1.0$ mA
			—	—	0.4	$I_{OL} = 3$ mA
	RIIC pins		—	—	0.6	$I_{OL} = 6$ mA
Input leakage current	RES#, MD pin, EMLE, Ports 4 and PE2	$ I_{in} $	—	—	1.0	μA , $V_{in} = 0V$, $V_{in} = V_{CC}$
Three-state leakage current (off state)	Ports for 5V tolerant	$ I_{TSI} $	—	—	1.0	μA , $V_{in} = 0V$, $V_{in} = 5.5$ V
			—	—	5.0	
Input capacitance	All input pins (except for ports PB1 and PB2)	C_{in}	—	—	15	pF , $V_{in} = 0V$, $f = 1$ MHz, $T_a = 25^\circ C$
	Ports PB1 and PB2		—	—	30	

Note 1. Ports 0, 1, 2, 3, 7, 9, A, B, and D are 5 V tolerant.

6.3.3 Timing of Recovery from Low Power Consumption Modes

Table 6.9 Timing of Recovery from Low Power Consumption Modes

Conditions: $V_{CC} = 2.7$ to 3.6 V, $V_{SS} = AV_{SS0} = V_{REFL0} = 0$ V,
 $AV_{CC0} = 3.0$ to 3.6 V, $V_{REFH0} = 3.0$ V to AV_{CC0} ,
 $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time after cancellation of software standby mode	Crystal resonator connected to main clock oscillator operating	t_{SBYMC}	10	—	—	ms
	Main clock oscillator and PLL circuit operating	t_{SBYPC}	10	—	—	ms
	External clock input to main clock oscillator operating	t_{SBYEX}	1	—	—	ms
	Main clock oscillator and PLL circuit operating	t_{SBYPE}	1	—	—	ms
	Low-speed clock oscillator or IWDG-specific low-speed clock oscillator operating	t_{SBYLO}	—	—	800	μ s
Recovery time after cancellation of deep software standby mode	t_{DSBY}	—	—	1	ms	Figure 6.9
Wait time after cancellation of deep software standby mode	t_{DSBYWT}	45	—	46	t_{cyc}	

Note: • The wait time varies depending on the state in which each oscillator was when the WAIT instruction was executed. The recovery time when multiple oscillators are operating is the same period as that when the oscillator, which takes the longest time for recovery among the operating oscillators, is operating alone.

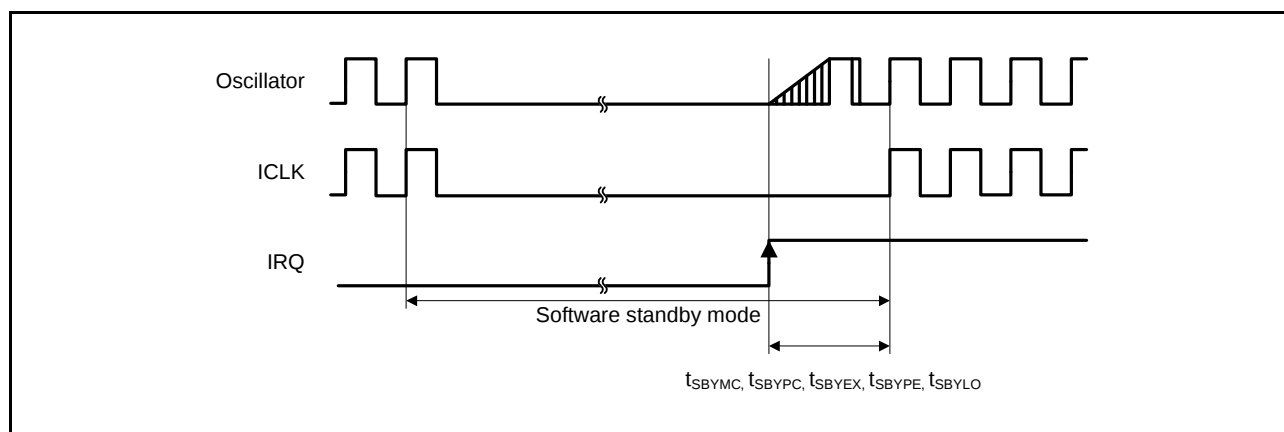


Figure 6.8 Software Standby Mode Cancellation Timing

6.3.5 Timing of On-Chip Peripheral Modules

Table 6.11 Timing of On-Chip Peripheral Modules (1)

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
I/O ports	Input data pulse width		t _{PRW}	1.5	—	t _{Pcyc}	Figure 6.12
MTU3	Input capture input pulse width	Single-edge setting	t _{TICW}	3	—	t _{PAcyc}	Figure 6.13
		Both-edge setting		5	—		
	Timer clock pulse width	Single-edge setting	t _{TCKWH} , t _{TCKWL}	3	—	t _{PAcyc}	Figure 6.14
		Both-edge setting		5	—		
		Phase counting mode		5	—		
POE3	POE# input pulse width		t _{POEW}	1.5	—	t _{Pcyc}	Figure 6.16
GPT	Input capture input pulse width	Single-edge setting	t _{GTICW}	3	—	t _{PAcyc}	Figure 6.15
		Both-edge setting		5	—		
	External trigger input pulse width	Single-edge setting	t _{OTETW}	3	—	t _{PAcyc}	Figure 6.18
		Both-edge setting		5	—		
SCI	Input clock cycle	Asynchronous	t _{Scyc}	4	—	t _{Pcyc}	Figure 6.17
		Clock synchronous		6	—		
	Input clock pulse width		t _{SCKW}	0.4	0.6	t _{Scyc}	
	Input clock rise time		t _{SCKr}	—	20	ns	
	Input clock fall time		t _{SCKf}	—	20	ns	
	Output clock cycle	Asynchronous	t _{Scyc}	16	—	t _{Pcyc}	
		Clock synchronous		4	—		
	Output clock pulse width		t _{SCKW}	0.4	0.6	t _{Scyc}	
	Output clock rise time		t _{SCKr}	—	20	ns	
	Output clock fall time		t _{SCKf}	—	20	ns	
	Transmit data delay time	Clock synchronous	t _{TXD}	—	40	ns	Figure 6.18
	Receive data setup time	Clock synchronous	t _{RXS}	40	—	ns	
	Receive data hold time	Clock synchronous	t _{RXH}	40	—	ns	
A/D converter	12-bit A/D converter trigger input pulse width		t _{TRGW}	1.5	—	t _{Pcyc}	Figure 6.19

Note 1. t_{Pcyc}: PCLK cycle, t_{PAcyc}: PCLKA cycle

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