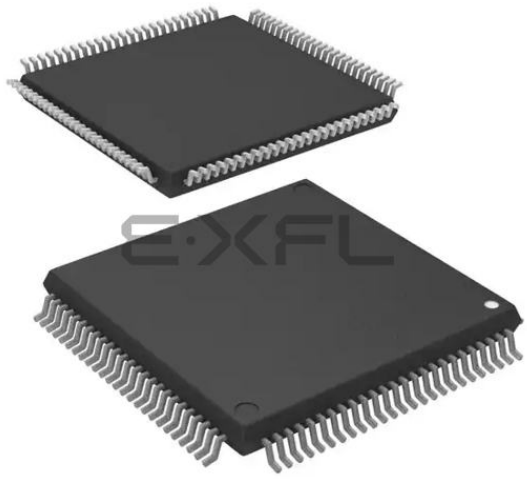
Renesas Electronics America Inc - R5F563TEEDFP#V0 Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	EBI/EMI, I²C, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	57
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 12x10b, 8x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f563teedfp-v0

Table 1.1 Outline of Specifications (6/7)

Classification Module/Function	Description
12-bit A/D converter (S12ADB) [64- and 48-pin versions]	• 12 bits (8 channels x 1 unit) • 12-bit resolution • Conversion time 1.0 µs per channel (S12ADB clock: PCLKD (A/D conversion clock: ADCLK) = 50 MHz • Operating modes Scan mode (single scan mode / continuous scan mode / group scan mode) Group A priority control (group scan mode only) • Sample-and-hold function A common sample-and-hold circuit for units is included Separate sample-and-hold circuits are also included (three channels per unit) • Self-diagnosis function Three analog input voltages (VREFL0, VREFH0 × 1/2, VREFH0) can be generated internally by the self-diagnosis function. • Double trigger mode (double the results of A/D conversion) • Three ways to start A/D conversion Conversion can be started by software, a conversion start trigger from a timer (MTU3 or GPT), or an external trigger signal. • Window comparators (three channels per unit)
10-bit A/D converter (ADA)	10 bits (20 channels × 1 unit) • 10-bit resolution • Conversion time 0.5 µs per channel (A/D conversion clock ADCLK = 100 MHz) • Two operating modes Single mode, scan mode • Scan mode Single-cycle scan mode Continuous scan mode • Sample-and-hold function A common sample-and-hold circuit for units is included • Three ways to start A/D conversion Conversion can be started by software, a conversion start trigger from a timer (MTU3 or GPT), or an external trigger signal. • 8-bit precision output 2-bit right shifting for output of conversion results is selectable. • Self-diagnostic function The self-diagnostic function internally generates three analog input voltages (AVSS, VREF x 1/2, VREF)
D/A converter (DAa)	• 2 channels • 10-bit resolution • Output voltage: 0 V to VREF
CRC calculator (CRC)	• CRC code generation for arbitrary amounts of data in 8-bit units • Select any of three generating polynomials: $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$. • Generation of CRC codes for use with LSB-first or MSB-first communications is selectable
Data operating circuit (DOC)	• Comparison, addition, and subtraction of 16-bit data
Digital power supply controller (DPC)	• Control parameters calculation unit of the digital switch-mode power supply systems. • Adopt robust control algorithm with high control stability • Results of measurement by the 10-bit A/D converter can be used in calculating the control parameters.
Operating frequency	Up to 100 MHz
Power supply voltage [144-, 120-, 112- and 100-pin versions]	• 3-V product VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V AVCC0 = AVCC = VREF = 3.0 to 3.6 V, or 4.0 to 5.5 V VREFH0 = 3.0 to AVCC0, or 4.0 to AVCC0 • 5-V product VCC = PLLVCC = 4.0 to 5.5 V VCC_USB = 3.0 to 3.6 V AVCC0 = AVCC = VREF = 4.0 to 5.5 V VREFH0 = 4.0 to AVCC0
Power supply voltage [64- and 48-pin versions]	VCC = 2.7 to 3.6 V, AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Table 1.3 List of Products (3/4)

Group	Part No.	Order Part No.	Package	On-chip ROM Capacity	On-chip RAM Capacity	Option	Operating Voltage	Operating Temperature
RX63T	R5F563TBBDFP	R5F563TBBDFP#V0	PLQP0100KB-A	256 Kbytes	24 Kbytes	CAN module included	VCC/ PLLVCC/ VCC_USB 2.7 to 3.6V AVCC/ AVCC0 3.0 to 3.6V or 4.0 to 5.5V	-40 to +85°C (D Version)
	R5F563TBBDFP	R5F563TBBDFP#V1	PLQP0100KB-A	256 Kbytes	24 Kbytes	CAN module included		
	R5F563TEEDFB	R5F563TEEDFB#V0	PLQP0144KA-A	512 Kbytes	48 Kbytes	CAN module not included		
	R5F563TEEDFA	R5F563TEEDFA#V0	PLQP0120KA-A	512 Kbytes	48 Kbytes	CAN module not included		
	R5F563TEEDFH	R5F563TEEDFH#V0	PLQP0112JA-A	512 Kbytes	48 Kbytes	CAN module not included		
	R5F563TEEDFP	R5F563TEEDFP#V0	PLQP0100KB-A	512 Kbytes	48 Kbytes	CAN module not included		
	R5F563TCEDFB	R5F563TCEDFB#V0	PLQP0144KA-A	384 Kbytes	32 Kbytes	CAN module not included		
	R5F563TCEDFA	R5F563TCEDFA#V0	PLQP0120KA-A	384 Kbytes	32 Kbytes	CAN module not included		
	R5F563TCEDFH	R5F563TCEDFH#V0	PLQP0112JA-A	384 Kbytes	32 Kbytes	CAN module not included		
	R5F563TCEDFP	R5F563TCEDFP#V0	PLQP0100KB-A	384 Kbytes	32 Kbytes	CAN module not included		
	R5F563TBEDFB	R5F563TBEDFB#V0	PLQP0144KA-A	256 Kbytes	24 Kbytes	CAN module not included		
	R5F563TBEDFA	R5F563TBEDFA#V0	PLQP0120KA-A	256 Kbytes	24 Kbytes	CAN module not included		
	R5F563TBEDFH	R5F563TBEDFH#V0	PLQP0112JA-A	256 Kbytes	24 Kbytes	CAN module not included		
	R5F563TBEDFP	R5F563TBEDFP#V0	PLQP0100KB-A	256 Kbytes	24 Kbytes	CAN module not included		
	R5F563T6EDFM	R5F563T6EDFM#V0	PLQP0064KB-A	64 Kbytes	8 Kbytes	CAN module not included	VCC/ PLLVCC 2.7 to 3.6V AVCC0 3.0 to 3.6V	
	R5F563T5EDFM	R5F563T5EDFM#V0	PLQP0064KB-A	48 Kbytes	8 Kbytes	CAN module not included		
	R5F563T4EDFM	R5F563T4EDFM#V0	PLQP0064KB-A	32 Kbytes	8 Kbytes	CAN module not included		
	R5F563T6EDFL	R5F563T6EDFL#V0	PLQP0048KB-A	64 Kbytes	8 Kbytes	CAN module not included		
	R5F563T5EDFL	R5F563T5EDFL#V0	PLQP0048KB-A	48 Kbytes	8 Kbytes	CAN module not included		
	R5F563T4EDFL	R5F563T4EDFL#V0	PLQP0048KB-A	32 Kbytes	8 Kbytes	CAN module not included		
	R5F563TEAGFB	R5F563TEAGFB#V1	PLQP0144KA-A	512 Kbytes	48 Kbytes	CAN module included	VCC/ PLLVCC 4.0 to 5.5V VCC_USB 3.0 to 3.6V AVCC/ AVCC0 4.0 to 5.5V	-40 to +105°C (G Version)*1
	R5F563TEAGFA	R5F563TEAGFA#V1	PLQP0120KA-A	512 Kbytes	48 Kbytes	CAN module included		
	R5F563TEAGFH	R5F563TEAGFH#V1	PLQP0112JA-A	512 Kbytes	48 Kbytes	CAN module included		
	R5F563TEAGFP	R5F563TEAGFP#V1	PLQP0100KB-A	512 Kbytes	48 Kbytes	CAN module included		
	R5F563TCAGFB	R5F563TCAGFB#V1	PLQP0144KA-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TCAGFA	R5F563TCAGFA#V1	PLQP0120KA-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TCAGFH	R5F563TCAGFH#V1	PLQP0112JA-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TCAGFP	R5F563TCAGFP#V1	PLQP0100KB-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TBAGFB	R5F563TBAGFB#V1	PLQP0144KA-A	256 Kbytes	24 Kbytes	CAN module included		

Table 1.3 List of Products (4/4)

Group	Part No.	Order Part No.	Package	On-chip ROM Capacity	On-chip RAM Capacity	Option	Operating Voltage	Operating Temperature
RX63T	R5F563TBAGFA	R5F563TBAGFA#V1	PLQP0120KA-A	256 Kbytes	24 Kbytes	CAN module included	VCC/ PLLVCC 4.0 to 5.5V VCC_USB 3.0 to 3.6V AVCC/ AVCC0 4.0 to 5.5V	-40 to +105°C (G Version)*1
	R5F563TBAGFH	R5F563TBAGFH#V1	PLQP0112JA-A	256 Kbytes	24 Kbytes	CAN module included		
	R5F563TBAGFP	R5F563TBAGFP#V1	PLQP0100KB-A	256 Kbytes	24 Kbytes	CAN module included		
	R5F563TEBGFB	R5F563TEBGFB#V1	PLQP0144KA-A	512 Kbytes	48 Kbytes	CAN module included	VCC/ PLLVCC/ VCC_USB 2.7 to 3.6V AVCC/ AVCC0 3.0 to 3.6V or 4.0 to 5.5V	
	R5F563TEBGFA	R5F563TEBGFA#V1	PLQP0120KA-A	512 Kbytes	48 Kbytes	CAN module included		
	R5F563TEBGFH	R5F563TEBGFH#V1	PLQP0112JA-A	512 Kbytes	48 Kbytes	CAN module included		
	R5F563TEBGFP	R5F563TEBGFP#V1	PLQP0100KB-A	512 Kbytes	48 Kbytes	CAN module included		
	R5F563TCBGFB	R5F563TCBGFB#V1	PLQP0144KA-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TCBGFA	R5F563TCBGFA#V1	PLQP0120KA-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TCBGFH	R5F563TCBGFH#V1	PLQP0112JA-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TCBGFP	R5F563TCBGFP#V1	PLQP0100KB-A	384 Kbytes	32 Kbytes	CAN module included		
	R5F563TBBGFB	R5F563TBBGFB#V1	PLQP0144KA-A	256 Kbytes	24 Kbytes	CAN module included		
	R5F563TBBGFA	R5F563TBBGFA#V1	PLQP0120KA-A	256 Kbytes	24 Kbytes	CAN module included		
	R5F563TBBGFH	R5F563TBBGFH#V1	PLQP0112JA-A	256 Kbytes	24 Kbytes	CAN module included		
	R5F563TBBGFP	R5F563TBBGFP#V1	PLQP0100KB-A	256 Kbytes	24 Kbytes	CAN module included		
	R5F563T6EGFM	R5F563T6EGFM#V0	PLQP0064KB-A	64 Kbytes	8 Kbytes	CAN module not included	VCC/ PLLVCC 2.7 to 3.6V AVCC0 3.0 to 3.6V	
	R5F563T5EGFM	R5F563T5EGFM#V0	PLQP0064KB-A	48 Kbytes	8 Kbytes	CAN module not included		
	R5F563T4EGFM	R5F563T4EGFM#V0	PLQP0064KB-A	32 Kbytes	8 Kbytes	CAN module not included		
	R5F563T6EGFL	R5F563T6EGFL#V0	PLQP0048KB-A	64 Kbytes	8 Kbytes	CAN module not included		
	R5F563T5EGFL	R5F563T5EGFL#V0	PLQP0048KB-A	48 Kbytes	8 Kbytes	CAN module not included		
	R5F563T4EGFL	R5F563T4EGFL#V0	PLQP0048KB-A	32 Kbytes	8 Kbytes	CAN module not included		

Note: • Orderable part numbers are current as of when this manual was published. Please make sure to refer to the relevant product page on the Renesas website for the latest part numbers.

Note: • The products with the product ID code 1 (ex. R5F563TEADFB#V1) are the revised version to the specification constraints of technical update TX-RX*-A84A / E described.

Note 1. Please contact Renesas Electronics sales office for derating of operation under Ta = +85°C to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.

Table 1.6 List of Pins and Pin Functions (120-Pin LQFP) (3/4)

Pin Number 120-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3, GPT, POE3, CAC)	Communications (SCIc, SCId, RSPI, RIIC, CAN, USB)	Interrupt	S12ADB, AD, DA
75	VSS						
76		P30	D10/[A10/D10]	MTIOC0B/MTCLKD	SCK0/SSLA0/SSLB0		
77		P26	CS0#		TXD1/SMOSI1/SSDA1/SDA1		
78		P25	CS1#		SCK1/SCL1		
79		P24	D11/[A11/D11]		CTS0#/RTS0#/SS0#/RSPCKA/RSPCKB	IRQ4	
80		P23	D12/[A12/D12]	CACREF	TXD0/SMOSI0/SSDA0/MOSIA/MOSIB/CTX1		
81		P22	D13/[A13/D13]		RXD0/SMISO0/SSCL0/MISOA/MISOB/CRX1		ADTRG#
82		P21	D14/[A14/D14]	MTCLKA		IRQ6-DS	ADTRG1#
83		P20	D15/[A15/D15]	MTCLKB		IRQ7-DS	ADTRG0#
84		P65	A0/BC0#				AN5
85		P64	A1				AN4
86	AVCC						
87	VREF						
88	AVSS						
89		P63	A2				AN3
90		P62	A3				AN2
91		P61	A4				AN1
92		P60	A5				AN0
93		P55					AN11/DA1
94		P54					AN10/DA0
95		P53	A6				AN9
96		P52	A7				AN8
97		P51					AN7
98		P50					AN6
99		P47					AN103/CVREFH
100		P46					AN102
101		P45					AN101
102		P44					AN100
103		P43					AN003/CVREFL
104		P42					AN002
105		P41					AN001
106		P40					AN000
107	AVCC0						
108	VREFH0						
109	VREFL0						
110	AVSS0						

Table 1.6 List of Pins and Pin Functions (120-Pin LQFP) (4/4)

Pin Number 120-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3, GPT, POE3, CAC)	Communications (SCIc, SCId, RSPI, RIIC, CAN, USB)	Interrupt	S12ADB, AD, DA
111		P82	WAIT#	MTIC5U	SCK12	IRQ3	
112		P81	A8	MTIC5V	TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12		
113		P80	A9	MTIC5W	RXD12/SMISO12/ SSCL12/RXDX12	IRQ5	
114		P12	CS3#		USB0_DPRPD		
115		P11	ALE	MTCLKC		IRQ1-DS	
116		P10		MTCLKD		IRQ0-DS	
117					USB0_DPUPE		
118	VSS_USB						
119					USB0_DM		
120					USB0_DP		

Table 1.8 List of Pins and Pin Functions (100-Pin LQFP) (1/3)

Pin Number 100-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3, GPT, POE3, CAC)	Communications (SCIc, SCId, RSPI, RIIC, CAN)	Interrupt	S12ADB, AD, DA
1		PE5	BCLK			IRQ0	
2	EMLE						
3	VSS						
4		P01	RD#		CTS0#/RTS0#/SS0#		
5	VCL						
6		P00	CS1#	CACREF			
7	MD/FINED						
8		PE4	A10	POE10#/MTCLKC		IRQ1	
9		PE3	A11	POE11#/MTCLKD		IRQ2-DS	
10	RES#						
11	XTAL						
12	VSS						
13	EXTAL						
14	VCC						
15		PE2		POE10#		NMI	
16		PE1	WR0#/WR#		CTS12#/RTS12#/ SS12#/SSLA3/SSLB3		
17		PE0	WR1#/BC1#/ WAIT#		SSLA2/SSLB2/CRX1	IRQ7	
18	TRST#	PD7		GTIOC0A	CTS0#/RTS0#/SS0#/ SSLA1/SSLB1/CTX1		
19	TMS	PD6		GTIOC0B	SSLA0/SSLB0		
20	TDI	PD5		GTIOC1A	RXD1/SMISO1/SSCL1	IRQ6	
21	TCK/FINEC	PD4		GTIOC1B	SCK1		
22	TDO	PD3		GTIOC2A	TXD1/SMOSI1/SSDA1		
23		PD2	CS2#	GTIOC2B	MOSIA/MOSIB		
24		PD1	CS0#	GTIOC3A	MISOA/MISOB		
25		PD0	A12	GTIOC3B	RSPCKA/RSPCKB		
26		PB7	A19		SCK12		
27		PB6	A18		RXD12/SMISO12/ SSCL12/RXDX12/ CRX1	IRQ2	
28		PB5	A17		TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/CTX1		
29	PLLVCC						
30		PB4	A16	POE8#/GTETRG0		IRQ3-DS	
31	PLLVSS						
32		PB3	A15	MTIOC0A/CACREF	SCK0		
33		PB2		MTIOC0B	TXD0/SMOSI0/ SSDA0/SDA0		
34		PB1		MTIOC0C	RXD0/SMISO0/ SSCL0/SCL0	IRQ4	
35		PB0	A14	MTIOC0D	MOSIA/MOSIB		
36		PA5		MTIOC1A	RXD0/SMISO0/ SSCL0/ MISOA/MISOB		ADTRG1#

Table 1.8 List of Pins and Pin Functions (100-Pin LQFP) (2/3)

Pin Number 100-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3, GPT, POE3, CAC)	Communications (SCIc, SCId, RSPI, RIIC, CAN)	Interrupt	S12ADB, AD, DA
37		PA4		MTIOC1B	TXD0/SMOSI0/ SSDA0/ RSPCKA/RSPCKB		ADTRG0#
38		PA3		MTIOC2A	SCK0/SSLA0/SSLB0		
39		PA2		MTIOC2B	RXD2/SMISO2/ SSCL2/ SSLA1/SSLB1		
40		PA1		MTIOC6A	TXD2/SMOSI2/ SSDA2/ SSLA2/SSLB2		
41		PA0		MTIOC6C	SCK2/SSLA3/SSLB3		
42	VCC						
43		P96	A13	POE4#	RXD1/SMISO1/SSCL1	IRQ4-DS	
44	VSS						
45		P95		MTIOC6B/GTIOC4A	TXD1/SMOSI1/SSDA1		
46		P94		MTIOC7A/GTIOC5A	CTS1#/RTS1#/SS1#		
47		P93		MTIOC7B/GTIOC6A	CTS2#/RTS2#/SS2#		
48		P92		MTIOC6D/GTIOC4B			
49		P91		MTIOC7C/GTIOC5B			
50		P90		MTIOC7D/GTIOC6B			
51		P76	D0/[A0/D0]	MTIOC4D/GTIOC2B			
52		P75	D1/[A1/D1]	MTIOC4C/GTIOC1B			
53		P74	D2/[A2/D2]	MTIOC3D/GTIOC0B			
54		P73	D3/[A3/D3]	MTIOC4B/GTIOC2A			
55		P72	D4/[A4/D4]	MTIOC4A/GTIOC1A			
56		P71	D5/[A5/D5]	MTIOC3B/GTIOC0A			
57		P70	D6/[A6/D6]	POE0#	CTS1#/RTS1#/SS1#	IRQ5-DS	
58		P33	D7/[A7/D7]	MTIOC3A/MTCLKA	SSLA3/SSLB3		
59		P32	D8/[A8/D8]	MTIOC3C/MTCLKB	SSLA2/SSLB2		
60	VCC						
61		P31	D9/[A9/D9]	MTIOC0A/MTCLKC	SSLA1/SSLB1		
62	VSS						
63		P30	D10/[A10/ D10]	MTIOC0B/MTCLKD	SCK0/SSLA0/SSLB0		
64		P24	D11/[A11/D11]		CTS0#/RTS0#/SS0#/ RSPCKA/RSPCKB	IRQ4	
65		P23	D12/[A12/ D12]	CACREF	TXD0/SMOSI0/ SSDA0/MOSIA/ MOSIB/CTX1		
66		P22	D13/[A13/ D13]		RXD0/SMISO0/ SSCL0/MISOA/ MISOB/CRX1		ADTRG#
67		P21	D14/[A14/ D14]	MTCLKA		IRQ6-DS	ADTRG1#
68		P20	D15/[A15/ D15]	MTCLKB		IRQ7-DS	ADTRG0#
69		P65	A0/BC0#				AN5
70		P64	A1				AN4

Table 1.10 List of Pins and Pin Functions (48-Pin LQFP) (1/2)

Pin Number 64-Pin LQFP	Power Supply Clock System Control	I/O Port	POE3	Timer (MTU3, GPT, CAC)	Communications		Interrupt	S12ADB
					(SCIc, SCId)	(RSPI, RIIC)		
1	MD FINED							
2	RES#							
3	XTAL							
4	VSS							
5	EXTAL							
6	VCC							
7		PE2	POE10#				NMI	
8	TRST#	PD7		GTIOC0A	CTS0# RTS0# SS0#			
9	TMS	PD6		GTIOC0B				
10	TDI	PD5		GTIOC1A	RXD1 SMISO1 SSCL1			
11	TCK FINEC	PD4		GTIOC1B	SCK1			
12	TDO	PD3		GTIOC2A	TXD1 SMOSI1 SSDA1			
13		PB6		GTIOC2B	RXD12 SMISO12 SSCL12 RXDX12			
14		PB5	POE11#		TXD12 SMOSI12 SSDA12 TXDX12 SIOX12		IRQ0	
15	VCC							
16		PB4	POE8#	GTETRG	CTS12# RTS12# SS12#		IRQ3-DS	
17	VSS							
18		PB3		MTIOC0A MTCLKA CACREF	SCK0			
19		PB2		MTIOC0B MTCLKB	TXD0 SMOSI0 SSDA0	SDA		
20		PB1		MTIOC0C	RXD0 SMISO0 SSCL0	SCL		
21		PB0		MTIOC0D		MOSIA		
22		PA3		MTIOC2A		SSLA0		
23		PA2		MTIOC2B		SSLA1		
24		P76		MTIOC4D GTIOC2B MTIOC7D				
25		P75		MTIOC4C GTIOC1B MTIOC7C				

Table 4.1 List of I/O Registers (Address Order) (3/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 3024h	BSC	CS2 Wait Control Register 1	CS2WCR1	32	32	1, 2 BCLK		Buses	Not present in versions with 64 or 48 pins.
0008 3028h	BSC	CS2 Wait Control Register 2	CS2WCR2	32	32	1, 2 BCLK			Not present in versions with 64 or 48 pins.
0008 3032h	BSC	CS3 Mode Register	CS3MOD	16	16	1, 2 BCLK			Not present in versions with 64 or 48 pins.
0008 3034h	BSC	CS3 Wait Control Register 1	CS3WCR1	32	32	1, 2 BCLK			Not present in versions with 64 or 48 pins.
0008 3038h	BSC	CS3 Wait Control Register 2	CS3WCR2	32	32	1, 2 BCLK			Not present in versions with 64 or 48 pins.
0008 3802h	BSC	CS0 Control Register	CS0CR	16	16	1, 2 BCLK			Not present in versions with 64 or 48 pins.
0008 380Ah	BSC	CS0 Recovery Cycle Register	CS0REC	16	16	1, 2 BCLK			Not present in versions with 64 or 48 pins.
0008 3812h	BSC	CS1 Control Register	CS1CR	16	16	1, 2 BCLK			Not present in versions with 64 or 48 pins.
0008 381Ah	BSC	CS1 Recovery Cycle Register	CS1REC	16	16	1, 2 BCLK			Not present in versions with 64 or 48 pins.
0008 3822h	BSC	CS2 Control Register	CS2CR	16	16	1, 2 BCLK			Not present in versions with 64 or 48 pins.
0008 382Ah	BSC	CS2 Recovery Cycle Register	CS2REC	16	16	1, 2 BCLK			Not present in versions with 64 or 48 pins.
0008 3832h	BSC	CS3 Control Register	CS3CR	16	16	1, 2 BCLK			Not present in versions with 64 or 48 pins.
0008 383Ah	BSC	CS3 Recovery Cycle Register	CS3REC	16	16	1, 2 BCLK			Not present in versions with 64 or 48 pins.
0008 3880h	BSC	CS Recovery Cycle Insertion Enable Register	CSRECEN	16	16	1, 2 BCLK			Not present in versions with 64 or 48 pins.
0008 6400h	MPU	Region-0 Start Page Number Register	RSPAGE0	32	32	1 ICLK		MPU	
0008 6404h	MPU	Region-0 End Page Number Register	REPAGE0	32	32	1 ICLK			
0008 6408h	MPU	Region-1 Start Page Number Register	RSPAGE1	32	32	1 ICLK			
0008 640Ch	MPU	Region-1 End Page Number Register	REPAGE1	32	32	1 ICLK			
0008 6410h	MPU	Region-2 Start Page Number Register	RSPAGE2	32	32	1 ICLK			
0008 6414h	MPU	Region-2 End Page Number Register	REPAGE2	32	32	1 ICLK			
0008 6418h	MPU	Region-3 Start Page Number Register	RSPAGE3	32	32	1 ICLK			
0008 641Ch	MPU	Region-3 End Page Number Register	REPAGE3	32	32	1 ICLK			
0008 6420h	MPU	Region-4 Start Page Number Register	RSPAGE4	32	32	1 ICLK			
0008 6424h	MPU	Region-4 End Page Number Register	REPAGE4	32	32	1 ICLK			
0008 6428h	MPU	Region-5 Start Page Number Register	RSPAGE5	32	32	1 ICLK			
0008 642Ch	MPU	Region-5 End Page Number Register	REPAGE5	32	32	1 ICLK			
0008 6430h	MPU	Region-6 Start Page Number Register	RSPAGE6	32	32	1 ICLK			
0008 6434h	MPU	Region-6 End Page Number Register	REPAGE6	32	32	1 ICLK			
0008 6438h	MPU	Region-7 Start Page Number Register	RSPAGE7	32	32	1 ICLK			
0008 643Ch	MPU	Region-7 End Page Number Register	REPAGE7	32	32	1 ICLK			
0008 6500h	MPU	Memory-Protection Enable Register	MPEN	32	32	1 ICLK			
0008 6504h	MPU	Background Access Control Register	MPBAC	32	32	1 ICLK			
0008 6508h	MPU	Memory-Protection Error Status-Clearing Register	MPECLR	32	32	1 ICLK			
0008 650Ch	MPU	Memory-Protection Error Status Register	MPESTS	32	32	1 ICLK			
0008 6514h	MPU	Data Memory-Protection Error Address Register	MPDEA	32	32	1 ICLK			
0008 6520h	MPU	Region Search Address Register	MPSA	32	32	1 ICLK			
0008 6524h	MPU	Region Search Operation Register	MPOPS	16	16	1 ICLK			
0008 6526h	MPU	Region Invalidation Operation Register	MPOPI	16	16	1 ICLK			
0008 6528h	MPU	Instruction-Hit Region Register	MHITI	32	32	1 ICLK			
0008 652Ch	MPU	Data-Hit Region Register	MHITD	32	32	1 ICLK			

Table 4.1 List of I/O Registers (Address Order) (9/48)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Module Name	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 717Fh	ICU	DTC Activation Enable Register 127	DTCER127	8	8	2 ICLK		ICUb	
0008 7180h	ICU	DTC Activation Enable Register 128	DTCER128	8	8	2 ICLK			
0008 7181h	ICU	DTC Activation Enable Register 129	DTCER129	8	8	2 ICLK			
0008 7185h	ICU	DTC Activation Enable Register 133	DTCER133	8	8	2 ICLK			
0008 7186h	ICU	DTC Activation Enable Register 134	DTCER134	8	8	2 ICLK			
0008 7189h	ICU	DTC Activation Enable Register 137	DTCER137	8	8	2 ICLK			
0008 718Ah	ICU	DTC Activation Enable Register 138	DTCER138	8	8	2 ICLK			
0008 718Dh	ICU	DTC Activation Enable Register 141	DTCER141	8	8	2 ICLK			
0008 718Eh	ICU	DTC Activation Enable Register 142	DTCER142	8	8	2 ICLK			
0008 718Fh	ICU	DTC Activation Enable Register 143	DTCER143	8	8	2 ICLK			
0008 7190h	ICU	DTC Activation Enable Register 144	DTCER144	8	8	2 ICLK			
0008 7192h	ICU	DTC Activation Enable Register 146	DTCER146	8	8	2 ICLK			
0008 7193h	ICU	DTC Activation Enable Register 147	DTCER147	8	8	2 ICLK			
0008 7194h	ICU	DTC Activation Enable Register 148	DTCER148	8	8	2 ICLK			
0008 7195h	ICU	DTC Activation Enable Register 149	DTCER149	8	8	2 ICLK			
0008 7196h	ICU	DTC Activation Enable Register 150	DTCER150	8	8	2 ICLK			
0008 7197h	ICU	DTC Activation Enable Register 151	DTCER151	8	8	2 ICLK			
0008 7198h	ICU	DTC Activation Enable Register 152	DTCER152	8	8	2 ICLK			
0008 7199h	ICU	DTC Activation Enable Register 153	DTCER153	8	8	2 ICLK			
0008 719Ah	ICU	DTC Activation Enable Register 154	DTCER154	8	8	2 ICLK			
0008 719Bh	ICU	DTC Activation Enable Register 155	DTCER155	8	8	2 ICLK			
0008 719Ch	ICU	DTC Activation Enable Register 156	DTCER156	8	8	2 ICLK			
0008 719Dh	ICU	DTC Activation Enable Register 157	DTCER157	8	8	2 ICLK			
0008 71A1h	ICU	DTC Activation Enable Register 161	DTCER161	8	8	2 ICLK			
0008 71A2h	ICU	DTC Activation Enable Register 162	DTCER162	8	8	2 ICLK			
0008 71A3h	ICU	DTC Activation Enable Register 163	DTCER163	8	8	2 ICLK			
0008 71A4h	ICU	DTC Activation Enable Register 164	DTCER164	8	8	2 ICLK			
0008 71A5h	ICU	DTC Activation Enable Register 165	DTCER165	8	8	2 ICLK			
0008 71ABh	ICU	DTC Activation Enable Register 171	DTCER171	8	8	2 ICLK			
0008 71ACh	ICU	DTC Activation Enable Register 172	DTCER172	8	8	2 ICLK			
0008 71ADh	ICU	DTC Activation Enable Register 173	DTCER173	8	8	2 ICLK			
0008 71AEh	ICU	DTC Activation Enable Register 174	DTCER174	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 71AFh	ICU	DTC Activation Enable Register 175	DTCER175	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 71B0h	ICU	DTC Activation Enable Register 176	DTCER176	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 71B1h	ICU	DTC Activation Enable Register 177	DTCER177	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 71B2h	ICU	DTC Activation Enable Register 178	DTCER178	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 71B3h	ICU	DTC Activation Enable Register 179	DTCER179	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 71B4h	ICU	DTC Activation Enable Register 180	DTCER180	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 71B5h	ICU	DTC Activation Enable Register 181	DTCER181	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 71B6h	ICU	DTC Activation Enable Register 182	DTCER182	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 71B7h	ICU	DTC Activation Enable Register 183	DTCER183	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 71B8h	ICU	DTC Activation Enable Register 184	DTCER184	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 71B9h	ICU	DTC Activation Enable Register 185	DTCER185	8	8	2 ICLK			Not present in versions with 64 or 48 pins.
0008 71BAh	ICU	DTC Activation Enable Register 186	DTCER186	8	8	2 ICLK			Not present in versions with 64 or 48 pins.

Table 5.4 DC Characteristics (3)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

The following relation applies when the USB is in use under condition 1 or condition 2: Vcc = PLLVcc = Vcc_USB = 3.0 to 3.6 V.

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Supply current *1	During operation	Max. *2	I_{CC}*3	—	—	70	mA	ICLK = 100 MHz PCLKA = 100 MHz PCLKB = 50 MHz PCLKC = 100 MHz PCLKD = 50 MHz FCLK = 50 MHz
		Normal *4		—	40	—		
		Increased by BGO operation *5		—	15	—		
	Sleep mode				40	55		
	All-module-clock-stop mode *6				20	30		
	During standby	Software standby mode		—	0.10	3	mA	
		Deep software standby mode		—	20	60	µA	
Analog power supply current	During 12-bit A/D conversion (per unit)		AI_{CC0}	—	1.5	4.2	mA	
	Programmable gain amplifier (per channel)			—	1	1.5	mA	
	Window comparator (per channel)			—	0.5	0.7	mA	
	Waiting for 12-bit A/D conversion (all units)			—	0.1	8	µA	
	During 10-bit A/D conversion (per channel)		AI_{CC}	—	0.9	1.4	mA	
	During D/A conversion (per unit)				0.1	4	µA	
	Waiting for 10-bit A/D, D/A conversion (all units)			—	0.1	4	µA	
Reference power supply current	During 12-bit A/D conversion (per unit)		AI_{REFH0}	—	1.6	2.5	mA	
	Waiting for 12-bit A/D conversion (all units)			—	0.1	1.5	µA	
	During 10-bit A/D conversion (per channel)		AI_{REF}	—	0.2	0.3	mA	
	During D/A conversion (per unit)				1	1.5	mA	
	Waiting for 10-bit A/D, D/A conversion (all units)			—	0.1	1.2	µA	
VCC rising gradient			SV_{CC}	—	—	20	ms/V	

Note 1. Supply current values are with all output pins unloaded.
Note 2. Measured with clocks supplied to the peripheral functions. This does not include the BGO operation.
Note 3. I_{CC} depends on f (ICLK) as follows. (ICLK: PCLK = 8:4)
I_{CC} max = 0.6 × f + 10 (max)
I_{CC} typ = 0.3 × f + 10 (normal)
I_{CC} max = 0.45 × f + 10 (sleep mode)
Note 4. Measured with clocks not supplied to the peripheral functions. This does not include the BGO operation.
Note 5. Incremented if data is written to or erased from the on-chip ROM or on-chip data-flash memory for data storage during the program execution.
Note 6. The values are for reference.

Table 5.5 Permissible Output Currents

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

The following relation applies when the USB is in use under condition 1 or condition 2: Vcc = PLLVcc = Vcc_USB = 3.0 to 3.6 V.

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item		Symbol	Min.	Typ.	Max.	Unit
Permissible output low current (average value per pin)	All output pins (except for P71 to P76, P90 to P95, and RIIC pins)*1	I_{OL}	—	—	2.0	mA
	RIIC pins	I_{OL}	—	—	6.0	mA
	P71 to P76, and P90 to P95*2	I_{OL}	—	—	15.0	mA
Permissible output low current (max. value per pin)	All output pins (except for P71 to P76, P90 to P95, and RIIC pins)*1	I_{OL}	—	—	4.0	mA
	RIIC pins	I_{OL}	—	—	6.0	mA
	P71 to P76, and P90 to P95*2	I_{OL}	—	—	15.0	mA
Permissible output low current (total)	Total of output pins	ΣI_{OL}	—	—	110	mA
Permissible output high current (average value per pin)	All output pins (except for P71 to P76, P90 to P95, and USB0_DPUPE pin)*1	$-I_{OH}$	—	—	2.0	mA
	USB0_DPUPE pin	$-I_{OH}$	—	—	3.0	mA
	P71 to P76, and P90 to P95*2	$-I_{OH}$	—	—	5.0	mA
Permissible output high current (max. value per pin)	All output pins (except for P71 to P76, P90 to P95)*1	$-I_{OH}$	—	—	4.0	mA
	P71 to P76, and P90 to P95*2	$-I_{OH}$	—	—	5.0	mA
Permissible output high current (total)		$\Sigma-I_{OH}$	—	—	35	mA

Note 1. USB0_DP and USB0_DM are not included.

Note 2. For pins P71 to P76 and P90 to P95, I_{OL} = 15 mA (max.) and $-I_{OH}$ = 5 mA (max.). However, if several of the pins are to supply I_{OL} and $-I_{OH}$ of more than 2.0 mA at the same time, the number of pins should be six or less.

Caution: To protect the MCU’s reliability, the output current values should not exceed the values in this table.

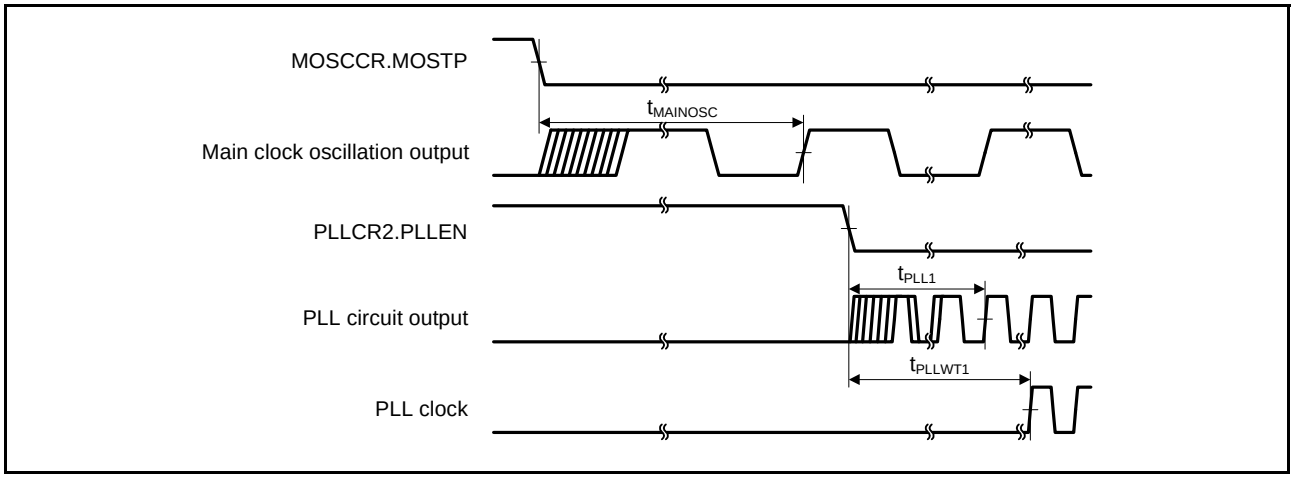


Figure 5.7 PLL Clock Oscillation Start Timing (PLL is Operated after Main Clock Oscillation Has Settled)

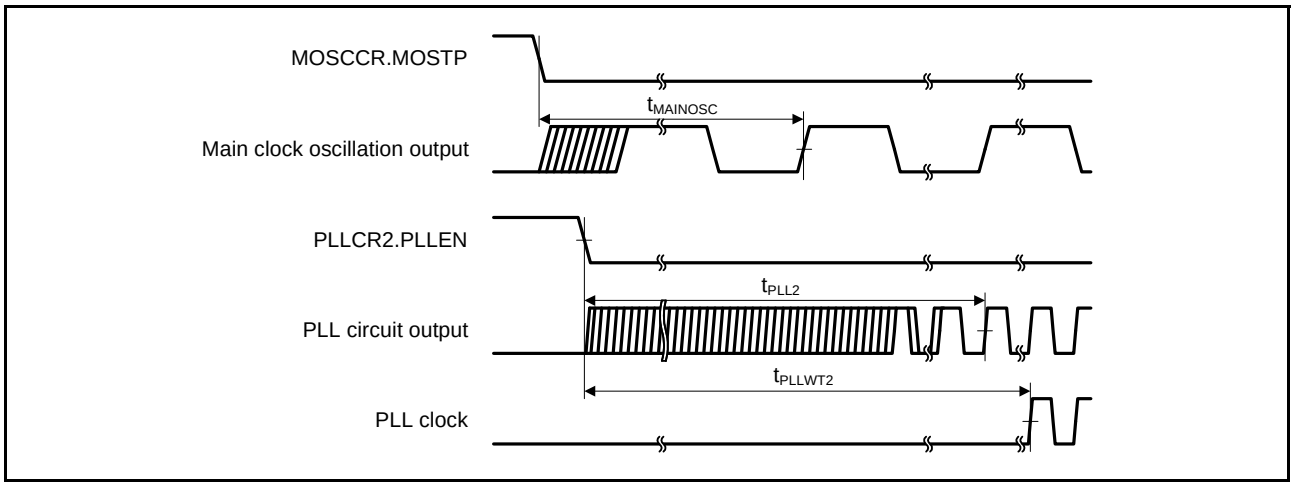


Figure 5.8 PLL Clock Oscillation Start Timing (PLL is Operated before Main Clock Oscillation Has Settled)

5.4 USB Characteristics

Table 5.18 On-Chip USB Full-Speed Characteristics (DP and DM Pin Characteristics)

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item		Symbol	Min.	Max.	Unit	Test Conditions	
Input characteristics	Input high level voltage	V_{IH}	2.0	—	V		Figure 5.37 Figure 5.38
	Input low level voltage	V_{IL}	—	0.8	V		
	Differential input sensitivity	V_{DI}	0.2	—	V	| DP – DM |	
	Differential common mode range	V_{CM}	0.8	2.5	V		
Output characteristics	Output high level voltage	V_{OH}	2.8	3.6	V	I_{OH} = –200 µA	
	Output low level voltage	V_{OL}	0.0	0.3	V	I_{OL} = 2 mA	
	Cross-over voltage	V_{CRS}	1.3	2.0	V		
	Rise time	t_{Lr}	4	20	ns		
	Fall time	t_{Lf}	4	20	ns		
	Rise/fall time ratio	t_{Lr} / t_{Lf}	90	111.11	%	t_{Lr} / t_{Lf}	
	Output resistance	Z_{DRV}	28	44	Ω	Rs = 24 Ω included	

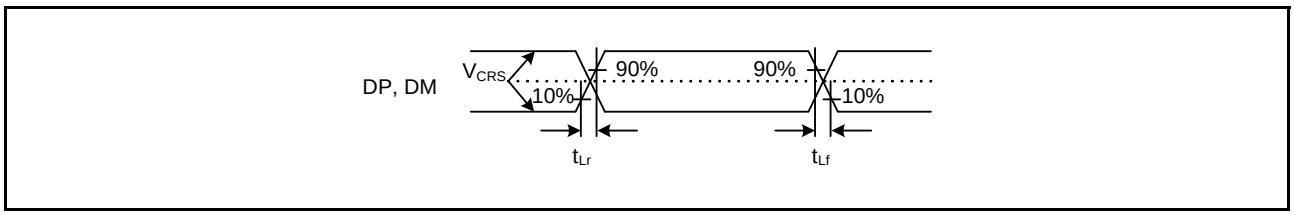


Figure 5.37 DP and DM Output Timing (Full-Speed)

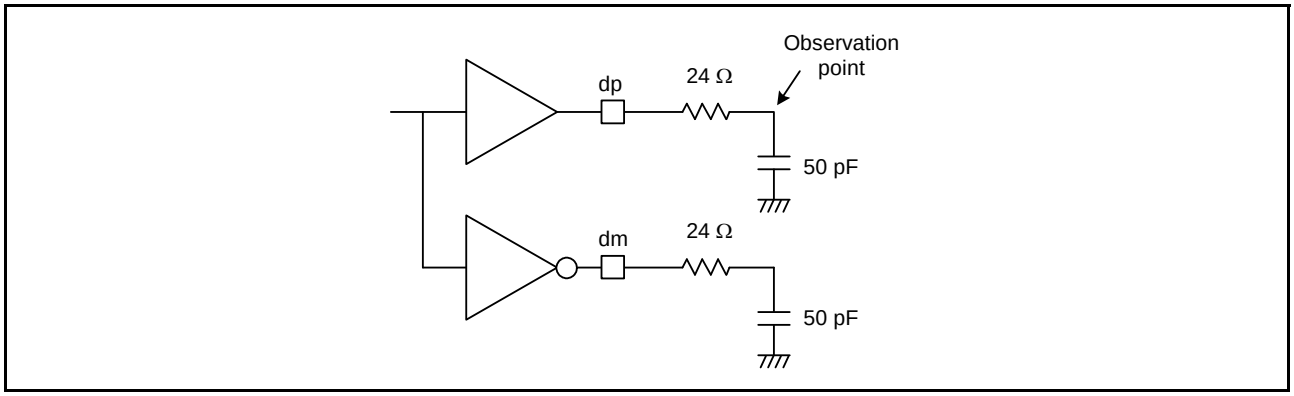


Figure 5.38 Test Circuit (Full-Speed)

Table 5.24 Comparator Characteristics

Note: Common standard values for conditions not given in the table are listed as “Condition 1” to “Condition 3” below.

Condition 1: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0

Condition 2: VCC = PLLVCC = VCC_USB = 2.7 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VCC_USB = 3.0 to 3.6 V, VSS = PLLVSS = VSS_USB = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = VREF = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0

$T_a = T_{opr}$. T_a is common to conditions 1 to 3.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Analog input capacitance	C_{in}	—	—	8	pF	
REFH pin offset voltage	V_{off}	—	—	5	mV	
REFL pin offset voltage		—	—	5	mV	
REFH input voltage range	V_{in}	1.7	—	AVcc – 0.3	V	
REFL input voltage range		0.3	—	AVcc – 1.7	V	
REFH reply time	t_{CR}	—	—	500	ns	VI = VREF±25mV
REFL reply time	t_{CF}	—	—	500	ns	

6.3.3 Timing of Recovery from Low Power Consumption Modes

Table 6.9 Timing of Recovery from Low Power Consumption Modes

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time after cancellation of software standby mode	Crystal resonator connected to main clock oscillator	Main clock oscillator operating	t_{SBYMC}	10	—	—	ms	Figure 6.8
		Main clock oscillator and PLL circuit operating	t_{SBYPC}	10	—	—	ms	
	External clock input to main clock oscillator	Main clock oscillator operating	t_{SBYEX}	1	—	—	ms	
		Main clock oscillator and PLL circuit operating	t_{SBYPE}	1	—	—	ms	
	Low-speed clock oscillator or IWDT-specific low-speed clock oscillator operating		t_{SBYLO}	—	—	800	µs	
Recovery time after cancellation of deep software standby mode			t_{DSBY}	—	—	1	ms	Figure 6.9
Wait time after cancellation of deep software standby mode			t_{DSBYWT}	45	—	46	t_{cyc}	

Note: • The wait time varies depending on the state in which each oscillator was when the WAIT instruction was executed. The recovery time when multiple oscillators are operating is the same period as that when the oscillator, which takes the longest time for recovery among the operating oscillators, is operating alone.

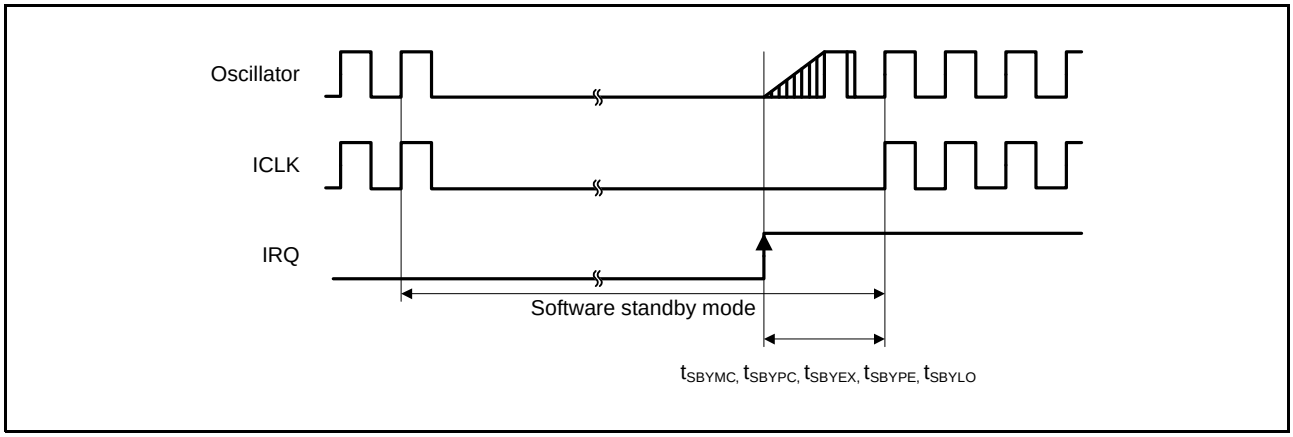


Figure 6.8 Software Standby Mode Cancellation Timing

Table 6.13 Timing of On-Chip Peripheral Modules (3)

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item		Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI	SCK clock cycle output (master)	t_{SPcyc}	4	65536	t_{Pcyc}	Figure 6.20
	SCK clock cycle input (slave)		8	65536		
	SCK clock high pulse width	t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width	t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise/fall time	t_{SPCKR}, t_{SPCKF}	—	20	ns	
	Data input setup time	t_{SU}	40	—	ns	Figure 6.21 to Figure 6.24
	Data input hold time	t_{H}	40	—	ns	
	SS input setup time	t_{LEAD}	6	—	t_{Pcyc}	
	SS input hold time	t_{LAG}	6	—	t_{Pcyc}	
	Data output delay time	t_{OD}	—	40	ns	
	Data output hold time	t_{OH}	–10	—	ns	
	Data rise/fall time	t_{DR}, t_{DF}	—	20	ns	
	SS input rise/fall time	t_{SSLr}, t_{SSLf}	—	20	ns	
	Slave access time	t_{SA}	—	5	t_{Pcyc}	Figure 6.23 and Figure 6.24
	Slave output release time	t_{REL}	—	5	t_{Pcyc}	

Note 1. t_{Pcyc}: PCLK cycle

6.4 A/D Conversion Characteristics

Table 6.16 12-Bit A/D Conversion Characteristics

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item		min	typ	max	Unit	Test Conditions
Resolution		12	12	12	Bit	
Conversion time *1 (ADCLK = 50 MHz)	When the sample-and-hold circuit is in use per pin	1.6	—	—	µs	Sampling by the sample-and-hold circuit in 30 states. Sampling by the A/D converter in 20 states.
	When the sample-and-hold circuit is not in use per pin	1.0	—	—	µs	Sampling by the A/D converter in 20 states.
Analog input capacitance		—	—	6	pF	
Integral nonlinearity error		—	—	±4.0	LSB	
Offset error		—	—	±7.5	LSB	
Full-scale error		—	—	±7.5	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy	Sample and hold circuit in use	—	—	±8.0	LSB	AVin = 0.25 to AV_{REFH}–0.25
	Sample and hold circuit not in use	—	—	±8.0	LSB	AVin = AV_{REFL} to AV_{REFH}
Permissible signal source impedance		—	—	3.0	kΩ	

Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Table 6.17 Comparator Characteristics

Conditions: VCC = 2.7 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V,
AVCC0 = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0,
Ta = T_{opr}

Item	Symbol	Min	Typ	Max.	Unit	Test Conditions
Analog input capacitance	Cin	—	—	6	pF	
REFH pin offset voltage	Voff	—	—	5	mV	
REFL pin offset voltage		—	—	5	mV	
REFH input voltage range	Vin	1.7	—	AVcc – 0.3	V	
REFL input voltage range		0.3	—	AVcc – 1.7	V	
REFH reply time	tCR	—	—	0.5	µs	
REFL reply time	tCF	—	—	0.5	µs	

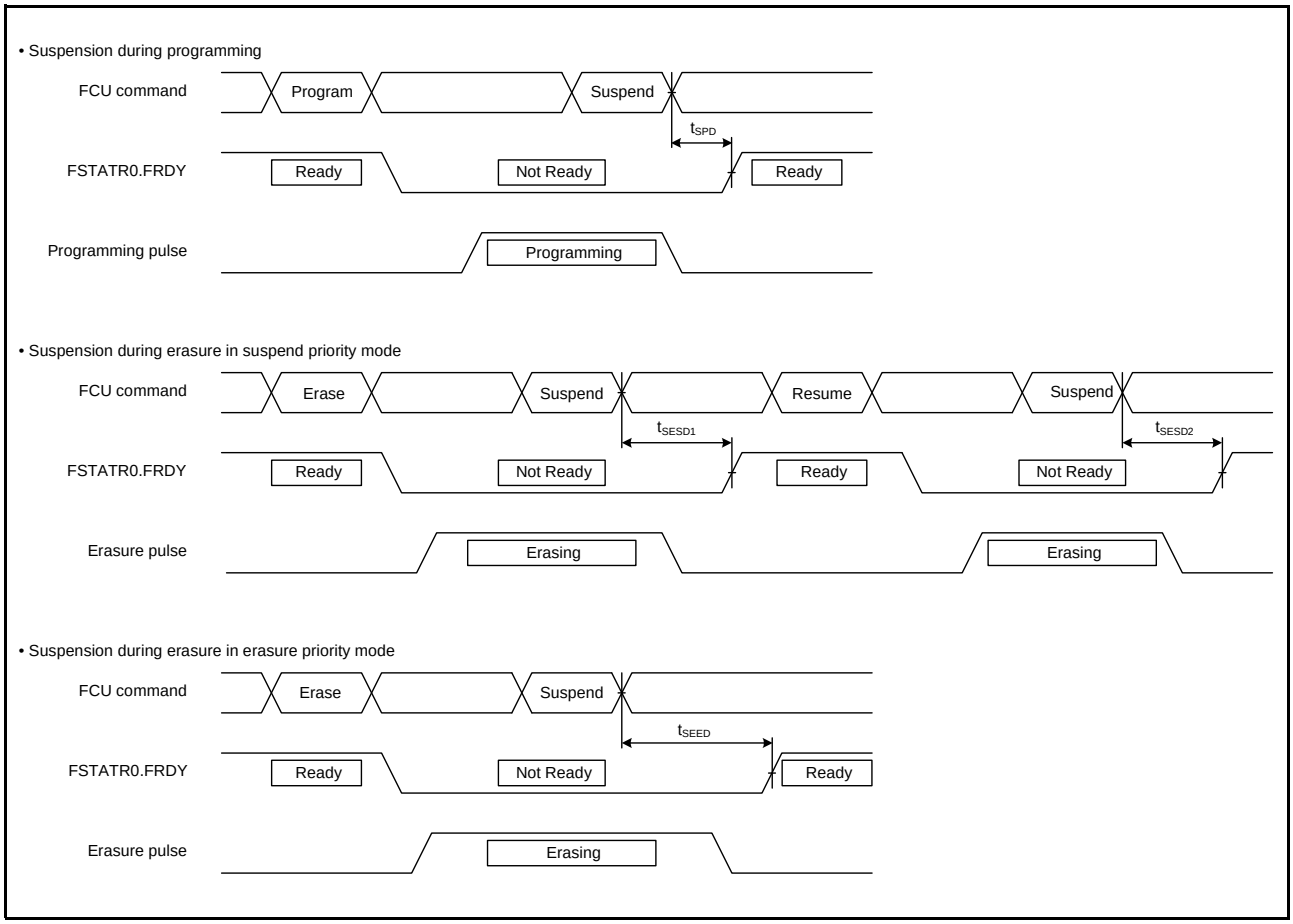
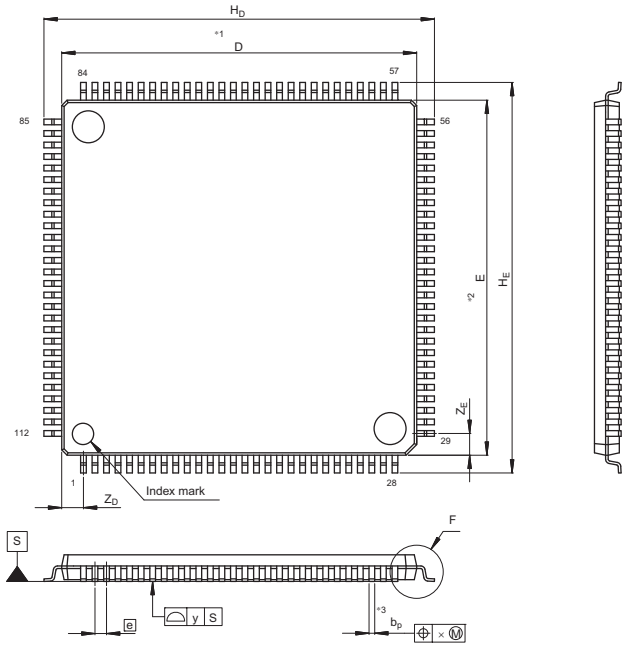
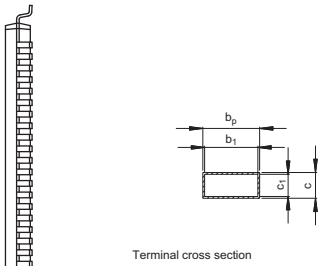
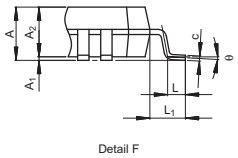


Figure 6.31 Flash Memory Program/Erase Suspend Timing

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP112-20x20-0.65	PLQP0112JA-A	FP-112E/FP-112EV	1.2g







NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	19.9	20.0	20.1
E	19.9	20.0	20.1
A_2	—	1.4	—
H_D	21.8	22.0	22.2
H_E	21.8	22.0	22.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.27	0.32	0.37
b_1	—	0.30	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z_D	—	1.225	—
Z_E	—	1.225	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure C 112-Pin LQFP (PLQP0112JA-A)