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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	XCore
Core Size	32-Bit 32-Core
Speed	4000MIPS
Connectivity	USB
Peripherals	-
Number of I/O	176
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	0.95V ~ 3.6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	374-LFBGA
Supplier Device Package	374-FBGA (18x18)
Purchase URL	https://www.e-xfl.com/product-detail/xmos/xuf232-512-fb374-i40

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on events generated by hardware resources such as the I/O pins, communication channels and timers. Once triggered, a core runs independently and concurrently to other cores, until it pauses to wait for more events. Section 6.2

- Channels and channel ends Tasks running on logical cores communicate using channels formed between two channel ends. Data can be passed synchronously or asynchronously between the channel ends assigned to the communicating tasks. Section 6.5
- xCONNECT Switch and Links Between tiles, channel communications are implemented over a high performance network of xCONNECT Links and routed through a hardware xCONNECT Switch. Section 6.6
- ▶ **Ports** The I/O pins are connected to the processing cores by Hardware Response ports. The port logic can drive its pins high and low, or it can sample the value on its pins optionally waiting for a particular condition. Section 6.3
- Clock blocks xCORE devices include a set of programmable clock blocks that can be used to govern the rate at which ports execute. Section 6.4
- Memory Each xCORE Tile integrates a bank of SRAM for instructions and data, and a block of one-time programmable (OTP) memory that can be configured for system wide security features. Section 9
- PLL The PLL is used to create a high-speed processor clock given a low speed external oscillator. Section 7
- ▶ **USB** The USB PHY provides High-Speed and Full-Speed, device, host, and on-thego functionality. Data is communicated through ports on the digital node. A library is provided to implement USB device functionality. Section 10
- ▶ Flash The device has a built-in 2MBflash. Section 8
- JTAG The JTAG module can be used for loading programs, boundary scan testing, in-circuit source-level debugging and programming the OTP memory. Section 11

1.1 Software

Devices are programmed using C, C++ or xC (C with multicore extensions). XMOS provides tested and proven software libraries, which allow you to quickly add interface and processor functionality such as USB, Ethernet, PWM, graphics driver, and audio EQ to your applications.

1.2 xTIMEcomposer Studio

The xTIMEcomposer Studio development environment provides all the tools you need to write and debug your programs, profile your application, and write images into flash memory or OTP memory on the device. Because xCORE devices operate deterministically, they can be simulated like hardware within xTIMEcomposer: uniquely in the embedded world, xTIMEcomposer Studio therefore includes a static timing analyzer, cycle-accurate simulator, and high-speed in-circuit instrumentation.

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Figure 7 also lists the values of OD, F and R, which are the registers that define the ratio of the tile frequency to the oscillator frequency:

$$F_{core} = F_{osc} \times \frac{F+1}{2} \times \frac{1}{R+1} \times \frac{1}{OD+1}$$

OD, *F* and *R* must be chosen so that $0 \le R \le 63$, $0 \le F \le 4095$, $0 \le OD \le 7$, and $260MHz \le F_{osc} \times \frac{F+1}{2} \times \frac{1}{R+1} \le 1.3GHz$. The *OD*, *F*, and *R* values can be modified by writing to the digital node PLL configuration register.

The MODE pins must be held at a static value during and after deassertion of the system reset. If the USB PHY is used, then either a 24 MHz or 12 MHz oscillator must be used.

If a different tile frequency is required (eg, 500 MHz), then the PLL must be reprogrammed after boot to provide the required tile frequency. The XMOS tools perform this operation by default. Further details on configuring the clock can be found in the xCORE-200 Clock Frequency Control document.

8 Boot Procedure

The device is kept in reset by driving RST_N low. When in reset, all GPIO pins have a pull-down enabled. The processor must be held in reset until VDDIOL is in spec for at least 1 ms. When the device is taken out of reset by releasing RST_N the processor starts its internal reset process. After 15-150 μ s (depending on the input clock) the processor boots.

Pin X2D06 must be pulled high with an external pull-up whilst the chip comes out of reset, to ensure that tile 2 will boot from link. X2D04, X2D05, and X2D07 should be kept low whilst the chip comes out of reset.

The device boots from a QSPI flash (IS25LQ016B) that is embedded in the device. The QSPI flash is connected to the ports on Tile 0 as shown in Figure 8. An external 1K resistor must connect X0D01 to VDDIOL. X0D10 should ideally not be connected. If X0D10 is connected, then a 150 ohm series resistor close to the device is recommended. X0D04..X0D07 should be not connected.



Feature	Bit	Description
Disable JTAG	0	The JTAG interface is disabled, making it impossible for the tile state or memory content to be accessed via the JTAG interface.
Disable Link access	1	Other tiles are forbidden access to the processor state via the system switch. Disabling both JTAG and Link access transforms an xCORE Tile into a "secure island" with other tiles free for non-secure user application code.
Secure Boot	5	The xCORE Tile is forced to boot from address 0 of the OTP, allowing the xCORE Tile boot ROM to be bypassed (see \S 8).
Redundant rows	7	Enables redundant rows in OTP.
Sector Lock 0	8	Disable programming of OTP sector 0.
Sector Lock 1	9	Disable programming of OTP sector 1.
Sector Lock 2	10	Disable programming of OTP sector 2.
Sector Lock 3	11	Disable programming of OTP sector 3.
OTP Master Lock	12	Disable OTP programming completely: disables up- dates to all sectors and security register.
Disable JTAG-OTP	13	Disable all (read & write) access from the JTAG inter- face to this OTP.
Disable Global Debug	14	Disables access to the DEBUG_N pin.
	2115	General purpose software accessable security register available to end-users.
	3122	General purpose user programmable JTAG UserID code extension.

Figure 10: Security register features

implement secure bootloaders and store encryption keys. Data for the security register is loaded from the OTP on power up. All additional data in OTP is copied from the OTP to SRAM and executed first on the processor.

The OTP memory is programmed using three special I/O ports: the OTP address port is a 16-bit port with resource ID 0x100200, the OTP data is written via a 32-bit port with resource ID 0x200100, and the OTP control is on a 16-bit port with ID 0x100300. Programming is performed through libotp and xburn.

9.2 SRAM

Each xCORE Tile integrates a single 128KBSRAM bank for both instructions and data. All internal memory is 32 bits wide, and instructions are either 16-bit or 32-bit. Byte (8-bit), half-word (16-bit) or word (32-bit) accesses are supported and are executed within one tile clock cycle. There is no dedicated external memory interface, although data memory can be expanded through appropriate use of the ports.

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	Symbol	Parameter	MIN	ТҮР	MAX	UNITS	Notes
5' 24	T(XOVALID)	Input data valid window	8			ns	
Figure 24: I/O AC char- acteristics	T(XOINVALID)	Output data invalid window	9			ns	
	T(XIFMAX)	Rate at which data can be sampled with respect to an external clock			60	MHz	

13.7	xCORE	Tile	I/0	\mathbf{AC}	Characteristics
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The input valid window parameter relates to the capability of the device to capture data input to the chip with respect to an external clock source. It is calculated as the sum of the input setup time and input hold time with respect to the external clock as measured at the pins. The output invalid window specifies the time for which an output is invalid with respect to the external clock. Note that these parameters are specified as a window rather than absolute numbers since the device provides functionality to delay the incoming clock with respect to the incoming data.

Information on interfacing to high-speed synchronous interfaces can be found in the XS1 Port I/O Timing document, X5821.

13.8 xConnect Link Performance

	Symbol	Parameter	MIN	ТҮР	MAX	UNITS	Notes
	B(2blinkP)	2b link bandwidth (packetized)			87	MBit/s	А, В
Figure 25:	B(5blinkP)	5b link bandwidth (packetized)			217	MBit/s	А, В
Link	B(2blinkS)	2b link bandwidth (streaming)			100	MBit/s	В
erformance	B(5blinkS)	5b link bandwidth (streaming)			250	MBit/s	В

perform

A Assumes 32-byte packet in 3-byte header mode. Actual performance depends on size of the header and payload.

B 7.5 ns symbol time.

The asynchronous nature of links means that the relative phasing of CLK clocks is not important in a multi-clock system, providing each meets the required stability criteria.

_			
1	3.9	ITAG	Timina
-	0.0	J . / . C	

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
f(TCK_D)	TCK frequency (debug)			18	MHz	
f(TCK_B)	TCK frequency (boundary scan)			10	MHz	
T(SETUP)	TDO to TCK setup time	5			ns	А
T(HOLD)	TDO to TCK hold time	5			ns	А
T(DELAY)	TCK to output delay			15	ns	В

Figure 26 JTAG timing

A Timing applies to TMS and TDI inputs.

B Timing applies to TDO output from negative edge of TCK.

All JTAG operations are synchronous to TCK apart from the global asynchronous reset TRST_N.

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14.1 Part Marking



15 Ordering Information

Figure 28:	Product Code	Marking	Qualification	Speed Grade
Orderable part numbers	XUF232-512-FB374-C40	U13292C40	Commercial	2000 MIPS
	XUF232-512-FB374-I40	U13292I40	Industrial	2000 MIPS



0x12: Debug SSP	Bits	Perm	Init	Description
	31:0	DRW		Value.

B.15 DGETREG operand 1: 0x13

The resource ID of the logical core whose state is to be read.

0x13	Bits	Perm	Init	Description
DGETREG operand 1	31:8	RO	-	Reserved
	7:0	DRW		Thread number to be read

B.16 DGETREG operand 2: 0x14

Register number to be read by DGETREG

0x14: DGETREG operand 2

Bits	Perm	Init	Description
31:5	RO	-	Reserved
4:0	DRW		Register number to be read

B.17 Debug interrupt type: 0x15

Register that specifies what activated the debug interrupt.

Bits	Perm	Init	Description
31:18	RO	-	Reserved
17:16	DRW		Number of the hardware breakpoint/watchpoint which caused the interrupt (always 0 for =HOST= and =DCALL=). If multiple breakpoints/watchpoints trigger at once, the lowest number is taken.
15:8	DRW		Number of thread which caused the debug interrupt (always 0 in the case of =HOST=).
7:3	RO	-	Reserved
2:0	DRW	0	Indicates the cause of the debug interrupt 1: Host initiated a debug interrupt through JTAG 2: Program executed a DCALL instruction 3: Instruction breakpoint 4: Data watch point 5: Resource watch point

0x15: Debug interrupt type



B.25 Data breakpoint control register: 0x70 ... 0x73

This set of registers controls each of the four data watchpoints.

	Bits	Perm	Init	Description
	31:24	RO	-	Reserved
	23:16	DRW	0	A bit for each thread in the machine allowing the breakpoint to be enabled individually for each thread.
:	15:3	RO	-	Reserved
	2	DRW	0	When 1 the breakpoints will be be triggered on loads.
	1	DRW	0	Determines the break condition: $0 = A AND B$, $1 = A OR B$.
	0	DRW	0	When 1 the instruction breakpoint is enabled.

0x70 .. 0x73: Data breakpoint control register

B.26 Resources breakpoint mask: 0x80 .. 0x83

This set of registers contains the mask for the four resource watchpoints.

0x80 .. 0x83: Resources breakpoint mask

urces point	Bits	Perm	Init	Description
mask	31:0	DRW		Value.

B.27 Resources breakpoint value: 0x90 .. 0x93

This set of registers contains the value for the four resource watchpoints.

0x90 .. 0x93: Resources breakpoint value

ces oint	Bits	Perm	Init	Description
ເlue	31:0	DRW		Value.

B.28 Resources breakpoint control register: 0x9C .. 0x9F

This set of registers controls each of the four resource watchpoints.

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XS2-UF32A-512-FB374

C Tile Configuration

The xCORE Tile control registers can be accessed using configuration reads and writes (use write_tile_config_reg(tileref, ...) and read_tile_config_reg(tileref, \rightarrow ...) for reads and writes).

Number	Perm	Description
0x00	CRO	Device identification
0x01	CRO	xCORE Tile description 1
0x02	CRO	xCORE Tile description 2
0x04	CRW	Control PSwitch permissions to debug registers
0x05	CRW	Cause debug interrupts
0x06	CRW	xCORE Tile clock divider
0x07	CRO	Security configuration
0x20 0x27	CRW	Debug scratch
0x40	CRO	PC of logical core 0
0x41	CRO	PC of logical core 1
0x42	CRO	PC of logical core 2
0x43	CRO	PC of logical core 3
0x44	CRO	PC of logical core 4
0x45	CRO	PC of logical core 5
0x46	CRO	PC of logical core 6
0x47	CRO	PC of logical core 7
0x60	CRO	SR of logical core 0
0x61	CRO	SR of logical core 1
0x62	CRO	SR of logical core 2
0x63	CRO	SR of logical core 3
0x64	CRO	SR of logical core 4
0x65	CRO	SR of logical core 5
0x66	CRO	SR of logical core 6
0x67	CRO	SR of logical core 7

Figure 31: Summary

C.1 Device identification: 0x00

This register identifies the xCORE Tile

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	Bits	Perm	Init	Description
	31:24	CRO		Processor ID of this XCore.
0×00:	23:16	CRO		Number of the node in which this XCore is located.
Device	15:8	CRO		XCore revision.
identification	7:0	CRO		XCore version.

C.2 xCORE Tile description 1: 0x01

This register describes the number of logical cores, synchronisers, locks and channel ends available on this xCORE tile.

Bits	Perm	Init	Description
31:24	CRO		Number of channel ends.
23:16	CRO		Number of the locks.
15:8	CRO		Number of synchronisers.
7:0	RO	-	Reserved

C.3 xCORE Tile description 2: 0x02

This register describes the number of timers and clock blocks available on this xCORE tile.

0x02: xCORE Tile description 2

0x01: xCORE Tile description 1

	Bits	Perm	Init	Description
02.	31:16	RO	-	Reserved
īle	15:8	CRO		Number of clock blocks.
n 2	7:0	CRO		Number of timers.

C.4 Control PSwitch permissions to debug registers: 0x04

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This register can be used to control whether the debug registers (marked with permission CRW) are accessible through the tile configuration registers. When this bit is set, write -access to those registers is disabled, preventing debugging of the xCORE tile over the interconnect.



0x04: Control PSwitch permissions to debug registers

Bits	Perm	Init	Description
31	CRW	0	When 1 the PSwitch is restricted to RO access to all CRW registers from SSwitch, XCore(PS_DBG_Scratch) and JTAG
30:1	RO	-	Reserved
0	CRW	0	When 1 the PSwitch is restricted to RO access to all CRW registers from SSwitch

C.5 Cause debug interrupts: 0x05

This register can be used to raise a debug interrupt in this xCORE tile.

0x05: Cause debug interrupts

Bits	Perm	Init	Description
31:2	RO	-	Reserved
1	CRW	0	1 when the processor is in debug mode.
0	CRW	0	Request a debug interrupt on the processor.

C.6 xCORE Tile clock divider: 0x06

This register contains the value used to divide the PLL clock to create the xCORE tile clock. The divider is enabled under control of the tile control register

0x06: xCORE Tile clock divider

Bits	Perm	Init	Description
31	CRW	0	Clock disable. Writing '1' will remove the clock to the tile.
30:16	RO	-	Reserved
15:0	CRW	0	Clock divider.

C.7 Security configuration: 0x07

Copy of the security register as read from OTP.

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0x41: PC of logical core 1

Bits	Perm	Init	Description
31:0	CRO		Value.

C.11 PC of logical core 2: 0x42

Value of the PC of logical core 2.

0x42: PC of logical core 2

Bits	Perm	Init	Description
31:0	CRO		Value.

C.12 PC of logical core 3: 0x43

Value of the PC of logical core 3.

0v43				
PC of logical	Bits	Perm	Init	Description
core 3	31:0	CRO		Value.

C.13 PC of logical core 4: 0x44

Value of the PC of logical core 4.

0x44 PC of logical core 4

9x44: gical	Bits	Perm	Init	Description
ore 4	31:0	CRO		Value.

C.14 PC of logical core 5: 0x45

Value of the PC of logical core 5.

0x45: PC of logical core 5

Bits	Perm	Init	Description
31:0	CRO		Value.

D.2 System switch description: 0x01

This register specifies the number of processors and links that are connected to this switch.

0x01 System switch description

	Bits	Perm	Init	Description
•	31:24	RO	-	Reserved
:	23:16	RO		Number of SLinks on the SSwitch.
	15:8	RO		Number of processors on the SSwitch.
•	7:0	RO		Number of processors on the device.

D.3 Switch configuration: 0x04

This register enables the setting of two security modes (that disable updates to the PLL or any other registers) and the header-mode.

Bits	Perm	Init	Description
31	RW	0	0 = SSCTL registers have write access. $1 = SSCTL$ registers can not be written to.
30:9	RO	-	Reserved
8	RW	0	0 = PLL_CTL_REG has write access. 1 = PLL_CTL_REG can not be written to.
7:1	RO	-	Reserved
0	RW	0	0 = 2-byte headers, $1 = 1$ -byte headers (reset as 0).

0x04: Switch configuration

D.4 Switch node identifier: 0x05

This register contains the node identifier.

0x05 Switch node identifier

15.	Bits	Perm	Init	Description
de.	31:16	RO	-	Reserved
er	15:0	RW	0	The unique ID of this node.

D.5 PLL settings: 0x06

An on-chip PLL multiplies the input clock up to a higher frequency clock, used to clock the I/O, processor, and switch, see Oscillator. Note: a write to this register will cause the tile to be reset.

Bits	Perm	Init	Description
31	RW		If set to 1, the chip will not be reset
30	RW		If set to 1, the chip will not wait for the PLL to re-lock. Only use this if a gradual change is made to the PLL
29	DW		If set to 1, set the PLL to be bypassed
28	DW		If set to 1, set the boot mode to boot from JTAG
27:26	RO	-	Reserved
25:23	RW		Output divider value range from 1 (8'h0) to 250 (8'hF9). P value.
22:21	RO	-	Reserved
20:8	RW		Feedback multiplication ratio, range from 1 (8'h0) to 255 (8'hFE). M value.
7	RO	-	Reserved
6:0	RW		Oscilator input divider value range from 1 (8'h0) to 32 (8'h0F). N value.

0x06: PLL settings

D.6 System switch clock divider: 0x07

Sets the ratio of the PLL clock and the switch clock.

0x07 System switch clock divider

7:	Bits	Perm	Init	Description
k	31:16	RO	-	Reserved
r	15:0	RW	0	SSwitch clock generation

D.7 Reference clock: 0x08

Sets the ratio of the PLL clock and the reference clock used by the node.

0,08.	Bits	Perm	Init	Description
Reference	31:16	RO	-	Reserved
clock	15:0	RW	3	Software ref. clock divider

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D.8 System JTAG device ID register: 0x09

0x09: System JTAG device ID register

	Bits	Perm	Init	Description
•	31:28	RO		
	27:12	RO		
)	11:1	RO		
	0	RO		

D.9 System USERCODE register: 0x0A

0x0A System USERCODE register

:	Bits	Perm	Init	Description
Ē	31:18	RO		JTAG USERCODE value programmed into OTP SR
r	17:0	RO		metal fixable ID code

D.10 Directions 0-7: 0x0C

This register contains eight directions, for packets with a mismatch in bits 7..0 of the node-identifier. The direction in which a packet will be routed is goverened by the most significant mismatching bit.

Bits	Perm	Init	Description
31:28	RW	0	The direction for packets whose dimension is 7.
27:24	RW	0	The direction for packets whose dimension is 6.
23:20	RW	0	The direction for packets whose dimension is 5.
19:16	RW	0	The direction for packets whose dimension is 4.
15:12	RW	0	The direction for packets whose dimension is 3.
11:8	RW	0	The direction for packets whose dimension is 2.
7:4	RW	0	The direction for packets whose dimension is 1.
3:0	RW	0	The direction for packets whose dimension is 0.

0x0C: Directions 0-7

D.11 Directions 8-15: 0x0D

This register contains eight directions, for packets with a mismatch in bits 15..8 of the node-identifier. The direction in which a packet will be routed is goverened by the most significant mismatching bit.

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E USB Node Configuration

The USB node control registers can be accessed using configuration reads and writes (use write_node_config_reg(device, ...) and read_node_config_reg(device, \rightarrow ...) for reads and writes).

Number	Perm	Description		
0x00	RO	Device identification register		
0x04	RW	Node configuration register		
0x05	RW	Node identifier		
0x51	RW	RW System clock frequency		
0x80	80 RW Link Control and Status			

Figure 33: Summary

E.1 Device identification register: 0x00

This register contains version information, and information on power-on behavior.

0x00: Device identification register

Bits	Perm	Init	Description	
31:24	RO	0x0F	Chip identifier	
23:16	RO	-	Reserved	
15:8	RO	0x02	Revision number of the USB block	
7:0	RO	0x00	Version number of the USB block	

E.2 Node configuration register: 0x04

This register is used to set the communication model to use (1 or 3 byte headers), and to prevent any further updates.

	Bits	Perm	Init	Description
0x04: Node guration	31	RW	0	Set to 1 to disable further updates to the node configuration and link control and status registers.
	30:1	RO	-	Reserved
register	0	RW	0	Header mode. 0: 3-byte headers; 1: 1-byte headers.

config

Bits	Perm	Init	Description		
31:8	RO	-	Reserved		
7	RW	0	Set to 1 to enable XEVACKMODE mode.		
6	RW	0	Set to 1 to enable SOFISTOKEN mode.		
5	RW	0	Set to 1 to enable UIFM power signalling mode.		
4	RW	0	Set to 1 to enable IF timing mode.		
3	RO	-	Reserved		
2	RW	0	Set to 1 to enable UIFM linestate decoder.		
1	RW	0	Set to 1 to enable UIFM CHECKTOKENS mode.		
0	RW	0	Set to 1 to enable UIFM DOTOKENS mode.		

0x04: UIFM IFM control

F.3 UIFM Device Address: 0x08

The device address whose packets should be received. 0 until enumeration, it should be set to the assigned value after enumeration.

0x08: UIFM Device Address

Bits	Perm	Init	Description
31:7	RO	-	Reserved
6:0	RW	0	The enumerated USB device address must be stored here. Only packets to this address are passed on.

F.4 UIFM functional control: 0x0C

0x0C: UIFM functional control

Bits	Perm	Init	Description
31:5	RO	-	Reserved
4:2	RW	1	Set to 0 to disable UIFM to UTMI+ OPMODE mode.
1	RW	1	Set to 1 to switch UIFM to UTMI+ TERMSELECT mode.
0	RW	1	Set to 1 to switch UIFM to UTMI+ XCVRSELECT mode.

F.5 UIFM on-the-go control: 0x10

This register is used to negotiate an on-the-go connection.

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	Dits
0x2C:	31:4
UIFM PID	3.0

Bits	Perm	Init	Description
31:4	RO	-	Reserved
3:0	RO	0	Value of the last received PID.

F.13 UIFM Endpoint: 0x30

The last endpoint seen

0x30 UIFM Endpoint

	Bits	Perm	Init	Description
	31:5	RO	-	Reserved
•	4	RO	0	1 if endpoint contains a valid value.
1	3:0	RO	0	A copy of the last received endpoint.

F.14 UIFM Endpoint match: 0x34

This register can be used to mark UIFM endpoints as special.

0x34: UIFM Endpoint match

Bits	Perm	Init	Description
31:16	RO	-	Reserved
15:0	RW	0	This register contains a bit for each endpoint. If its bit is set, the endpoint will be supplied on the RX port when ORed with $0x10$.

F.15 OTG Flags mask: 0x38

0x38 OTG Flags mask

ags	Bits	Perm	Init	Description
ask	31:0	RW	0	Data

F.16 UIFM power signalling: 0x3C

	Bits	Perm	Init	Description
0x2C:	31:9	RO	-	Reserved
UIFM power	8	RW	0	Valid
signalling	7:0	RW	0	Data

F.17	UIFM PHY	control: 0x40	
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Bits	Perm	Init	Description
31:19	RO	-	Reserved
18	RW	0	Set to 1 to disable pulldowns on ports 8A and 8B.
17:14	RO	-	Reserved
13	RW	0	After an auto-resume, this bit is set to indicate that the resume signalling was for reset (se0). Set to 0 to clear.
12	RW	0	After an auto-resume, this bit is set to indicate that the resume signalling was for resume (K). Set to 0 to clear.
11:8	RW	0	Log-2 number of clocks before any linestate change is propa- gated.
7	RW	0	Set to 1 to use the suspend controller handle to resume from suspend. Otherwise, the program has to poll the linestate_filt field in phy_teststatus.
6:4	RW	0	Control the the conf1,2,3 input pins of the PHY.
3:0	RO	-	Reserved

0x40: UIFM PHY control

I PCB Layout Design Check List

✓ This section is a checklist for use by PCB designers using the XS2-UF32A-512-FB374. Each of the following sections contains items to check for each design.

I.1 Ground Plane

- \Box Each ground ball has a via to minimize impedance and conduct heat away from the device. (Section 12.4)
- Other than ground vias, there are no (or only a few) vias underneath or closely around the device. This create a good, solid, ground plane.

I.2 Power supply decoupling

- \Box The decoupling capacitors are all placed close to a supply pin (Section 12).
- \Box The decoupling capacitors are spaced around the device (Section 12).
- □ The ground side of each decoupling capacitor has a direct path back to the center ground of the device.

I.3 PLL_AVDD

The PLL_AVDD filter (especially the capacitor) is placed close to the PLL_AVDD pin (Section 12).

J Associated Design Documentation

Document Title	Information	Document Number
Estimating Power Consumption For XS1-UF Devices	Power consumption	
Programming XC on XMOS Devices	Timers, ports, clocks, cores and channels	X9577
xTIMEcomposer User Guide	Compilers, assembler and linker/mapper	X3766
	Timing analyzer, xScope, debugger	
	Flash and OTP programming utilities	

K Related Documentation

Document Title	Information	Document Number
The XMOS XS1 Architecture	ISA manual	X7879
XS1 Port I/O Timing	Port timings	X5821
xCONNECT Architecture	Link, switch and system information	X4249
XS1-UF Link Performance and Design Guidelines	Link timings	
XS1-UF Clock Frequency Control	Advanced clock control	