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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	30MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, Cap Sense, DMA, POR, PWM, WDT
Number of I/O	54
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	External, Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc844m201jbd64e

7. Pinning information

7.1 Pinning

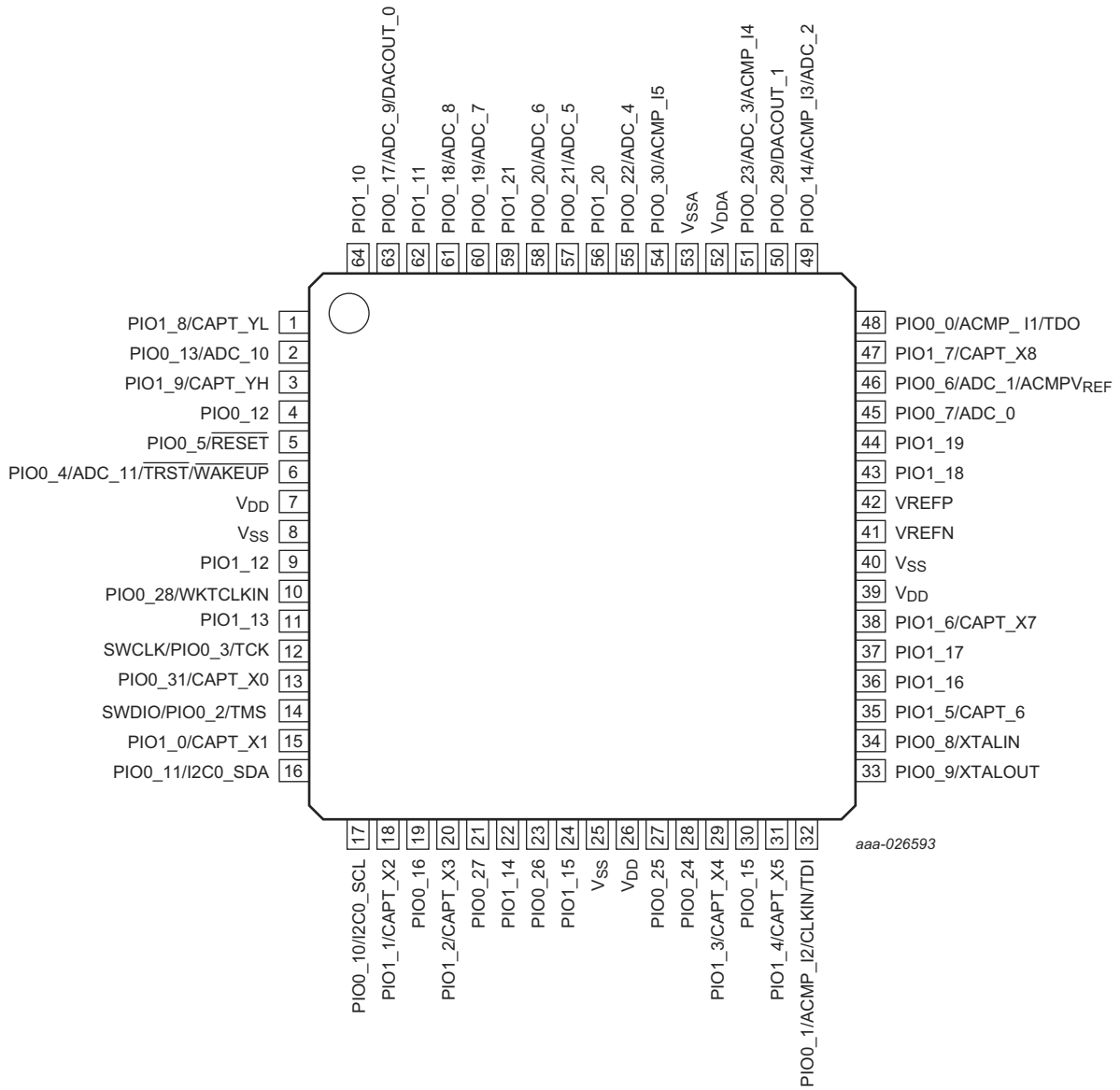


Fig 4. Pin configuration LQFP64 package

Table 4. Pin description

Symbol	LQFP64	LQFP48	HVQFN48	HVQFN33		Reset state[1]	Type	Description
PIO0_31/CAPT_X0	13	9	9	-	[5]	I; PU	IO	**PIO0_31 —** General-purpose port 0 input/output 31.
								CAPT_X0 — Capacitive Touch X sensor 0.
PIO1_0/CAPT_X1	15	11	11	-	[5]	I; PU	IO	**PIO1_0 —** General-purpose port 1 input/output 0.
								CAPT_X1 — Capacitive Touch X sensor 1.
PIO1_1/CAPT_X2	18	14	14	-	[5]	I; PU	IO	**PIO1_1 —** General-purpose port 1 input/output 1.
								CAPT_X2 — Capacitive Touch X sensor 2.
PIO1_2/CAPT_X3	20	16	16	-	[5]	I; PU	IO	**PIO1_2 —** General-purpose port 1 input/output 2.
								CAPT_X3 — Capacitive Touch X sensor 3.
PIO1_3/CAPT_X4	29	21	21	-	[5]	I; PU	IO	**PIO1_3 —** General-purpose port 1 input/output 3.
								CAPT_X4 — Capacitive Touch X sensor 4.
PIO1_4/CAPT_X5	31	23	23	-	[5]	I; PU	IO	**PIO1_4 —** General-purpose port 1 input/output 4.
								CAPT_X5 — Capacitive Touch X sensor 5.
PIO1_5/CAPT_X6	35	27	27	-	[5]	I; PU	IO	**PIO1_5 —** General-purpose port 1 input/output 5.
								CAPT_X6 — Capacitive Touch X sensor 6.
PIO1_6/CAPT_X7	38	28	28	-	[5]	I; PU	IO	**PIO1_6 —** General-purpose port 1 input/output 6.
								CAPT_X7 — Capacitive Touch X sensor 7.
PIO1_7/CAPT_X8	47	35	35	-	[5]	I; PU	IO	**PIO1_7 —** General-purpose port 1 input/output 7.
								CAPT_X8 — Capacitive Touch X sensor 8.
PIO1_8/CAPT_YL	1	1	1	-	[5]	I; PU	IO	**PIO1_8 —** General-purpose port 1 input/output 8.
								CAPT_YL — Capacitive Touch Y Low.
PIO1_9/CAPT_YH	3	3	3	-	[5]	I; PU	IO	**PIO1_9 —** General-purpose port 1 input/output 9.
								CAPT_YH — Capacitive Touch Y High.
PIO1_10	64	-	-	-	[5]	I; PU	IO	**PIO1_10 —** General-purpose port 1 input/output 10.
PIO1_11	62	-	-	-	[5]	I; PU	IO	**PIO1_11 —** General-purpose port 1 input/output 11.
PIO1_12	9	-	-	-	[5]	I; PU	IO	**PIO1_12 —** General-purpose port 1 input/output 12.
PIO1_13	11	-	-	-	[5]	I; PU	IO	**PIO1_13 —** General-purpose port 1 input/output 13.
PIO1_14	22	-	-	-	[5]	I; PU	IO	**PIO1_14 —** General-purpose port 1 input/output 14.
PIO1_15	24	-	-	-	[5]	I; PU	IO	**PIO1_15 —** General-purpose port 1 input/output 15.
PIO1_16	36	-	-	-	[5]	I; PU	IO	**PIO1_16 —** General-purpose port 1 input/output 16.
PIO1_17	37	-	-	-	[5]	I; PU	IO	**PIO1_17 —** General-purpose port 1 input/output 17.
PIO1_18	43	-	-	-	[5]	I; PU	IO	**PIO1_18 —** General-purpose port 1 input/output 18.
PIO1_19	44	-	-	-	[5]	I; PU	IO	**PIO1_19 —** General-purpose port 1 input/output 19.
PIO1_20	56	-	-	-	[5]	I; PU	IO	**PIO1_20 —** General-purpose port 1 input/output 20.
PIO1_21	59	-	-	-	[5]	I; PU	IO	**PIO1_21 —** General-purpose port 1 input/output 21.
V_{DD}	7;26;39	29	29	19		-	-	Supply voltage for the I/O pad ring, the and core voltage regulator.
V_{DDA}	52	40	40					Analog supply voltage.
V_{SS}	8;25;40	30	30	33[11]		-	-	Ground.

8.7 Nested Vectored Interrupt Controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is part of the Cortex-M0+. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

8.7.1 Features

- Nested Vectored Interrupt Controller is a part of the Arm Cortex-M0+.
- Tightly coupled interrupt controller provides low interrupt latency.
- Controls system exceptions and peripheral interrupts.
- Supports 32 vectored interrupts.
- In the LPC84x, the NVIC supports vectored interrupts for each of the peripherals and the eight pin interrupts.
- Four programmable interrupt priority levels with hardware priority level masking.
- Software interrupt generation using the Arm exceptions SVCall and PendSV.
- Supports NMI.

8.7.2 Interrupt sources

Each peripheral device has at least one interrupt line connected to the NVIC but can have several interrupt flags. Individual interrupt flags can also represent more than one interrupt source.

8.8 System tick timer

The Arm Cortex-M0+ includes a 24-bit system tick timer (SysTick) that is intended to generate a dedicated SysTick exception at a fixed time interval (typically 10 ms).

8.9 I/O configuration

The IOCON block controls the configuration of the I/O pins. Each digital or mixed digital/analog pin with the PIO0_n designator (except the true open-drain pins PIO0_10 and PIO0_11) in Table 4 can be configured as follows:

- Enable or disable the weak internal pull-up and pull-down resistors.
- Select a pseudo open-drain mode. The input cannot be pulled up above V_{DD}. The pins are not 5 V tolerant when V_{DD} is grounded.
- Program the input glitch filter with different filter constants using one of the IOCON divided clock signals (IOCONCLKCDIV, see Figure 11 “LPC84x clock generation”). You can also bypass the glitch filter.
- Invert the input signal.
- Hysteresis can be enabled or disabled.
- For pins PIO0_10 and PIO0_11, select the I2C-mode and output driver for standard digital operation, for I2C standard and fast modes, or for I2C Fast mode+.
- The switch matrix setting enables the analog input mode on pins with analog and digital functions. Enabling the analog mode disconnects the digital functionality.

Remark: The functionality of each I/O pin is flexible and is determined entirely through the switch matrix. See Section 8.10 for details.

- Reset timer on match with optional interrupt generation.
- Shadow registers are added for glitch-free PWM output.

- For each timer, up to four external outputs corresponding to match registers with the following capabilities (the number of match outputs for each timer that are actually available on device pins can vary by device):
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.
- Up to two match registers can be used to generate timed DMA requests.
- The timer and prescaler may be configured to be cleared on a designated capture event. This feature permits easy pulse width measurement by clearing the timer on the leading edge of an input pulse and capturing the timer value on the trailing edge.
- Up to four match registers can be configured for PWM operation, allowing up to three single edged controlled PWM outputs. (The number of match outputs for each timer that are actually available on device pins can vary by device.)

8.20 Multi-Rate Timer (MRT)

The Multi-Rate Timer (MRT) provides a repetitive interrupt timer with four channels. Each channel can be programmed with an independent time interval, and each channel operates independently from the other channels.

8.20.1 Features

- 31-bit interrupt timer
- Four channels independently counting down from individually set values
- Bus stall, repeat and one-shot interrupt modes

8.21 Windowed WatchDog Timer (WWDT)

The watchdog timer resets the controller if software fails to service the watchdog timer periodically within a programmable time window.

8.21.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.
- Optional warning interrupt can be generated at a programmable time prior to watchdog time-out.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect feed sequence causes reset or interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.

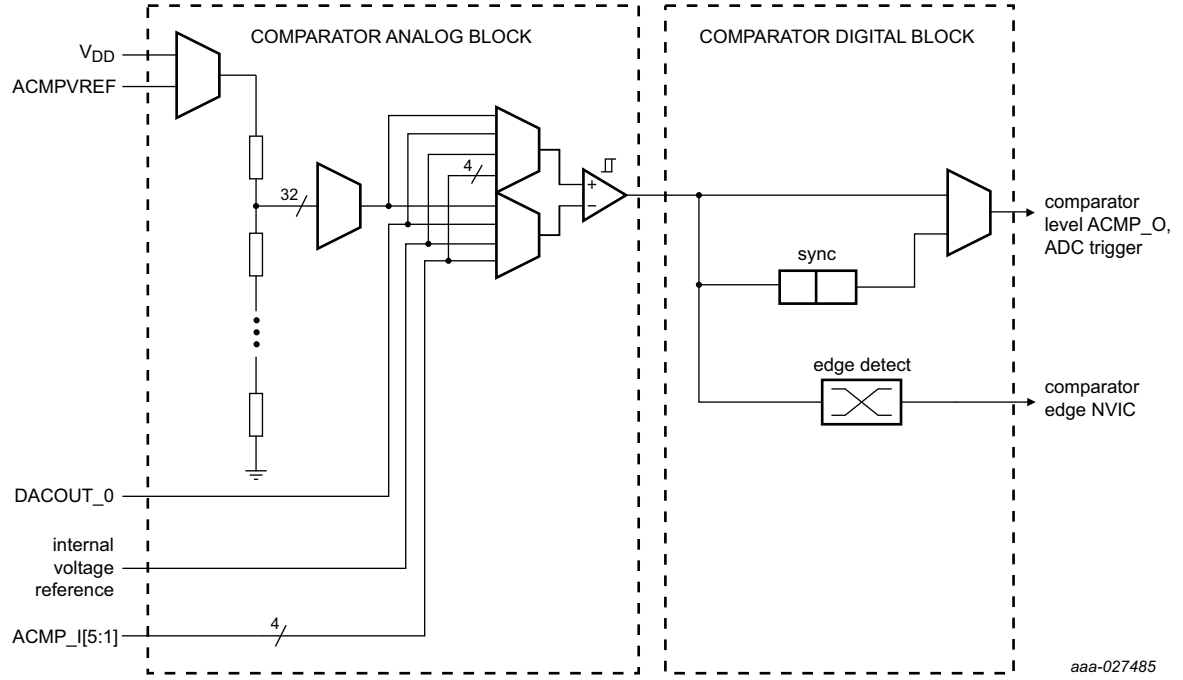


Fig 10. Comparator block diagram

8.23.1 Features

- Selectable 0 mV, 10 mV (± 5 mV), and 20 mV (± 10 mV), 40 mV (± 20 mV) input hysteresis.
- Two selectable external voltages (V_{DD} or $ACMPV_{REF}$); fully configurable on either positive or negative input channel.
- Internal voltage reference from band gap selectable on either positive or negative input channel.
- 32-stage voltage ladder with the internal reference voltage selectable on either the positive or the negative input channel.
- Voltage ladder source voltage is selectable from an external pin or the main 3.3 V supply voltage rail.
- Voltage ladder can be separately powered down for applications only requiring the comparator function.
- Interrupt output is connected to NVIC.
- Comparator level output is connected to output pin ACMP_O.
- One comparator output is internally collected to the ADC trigger input multiplexer.

8.24 Analog-to-Digital Converter (ADC)

The ADC supports a resolution of 12 bit and fast conversion rates of up to 1.2 MSamples/s. Sequences of analog-to-digital conversions can be triggered by multiple sources. Possible trigger sources are the pin triggers, the SCT output SCT_OUT3, the analog comparator output, and the Arm TXEV.

- Supports CPU PIO or DMA back-to-back transfer.
- Accept any size of data width per write: 8, 16 or 32-bit.
  - 8-bit write: 1-cycle operation.
  - 16-bit write: 2-cycle operation (8-bit x 2-cycle).
  - 32-bit write: 4-cycle operation (8-bit x 4-cycle).

8.27 Clocking and power control

8.27.1 Crystal and internal oscillators

The LPC84x include four independent oscillators:

1. The crystal oscillator (SysOsc) operating at frequencies between 1 MHz and 25 MHz.
2. Free Running Oscillator.
3. Watchdog Oscillator
4. Low Power Oscillator

Each oscillator, except the low-frequency oscillator, can be used for more than one purpose as required in a particular application.

Following reset, the LPC84x operates from the FRO until switched by software allowing the part to run without any external crystal and the bootloader code to operate at a known frequency.

See Figure 11 for an overview of the LPC84x clock generation.

8.27.1.1 Free Running Oscillator (FRO)

The FRO oscillator provides the default clock at reset and provides a clean system clock shortly after the supply pins reach operating voltage.

- This oscillator provides a selectable 18 MHz, 24 MHz, and 30 MHz outputs that can be used as a system clock. Also, these outputs can be divided down to 1.125 MHz, 1.5 MHz, 1.875 MHz, 9 MHz, 12 MHz, and 15 MHz for system clock.
- The FRO is trimmed to ±1 % accuracy over the entire voltage and temperature range of 0 C to 70 C.
- By default, the fro_oscout is 24 MHz and is divided by 2 to provide a default system (CPU) clock frequency of 12 MHz.

8.27.1.2 Crystal Oscillator (SysOsc)

The crystal oscillator can be used as the clock source for the CPU, with or without using the PLL.

The SysOsc operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the system PLL.

8.27.1.3 Internal Low-power Oscillator and Watchdog Oscillator (WDOsc)

The nominal frequency of the WDOsc is programmable between 9.4 kHz and 2.3 MHz. The frequency spread over silicon process variations is ± 40%.

The WDOsc is a dedicated oscillator for the windowed WWDT.

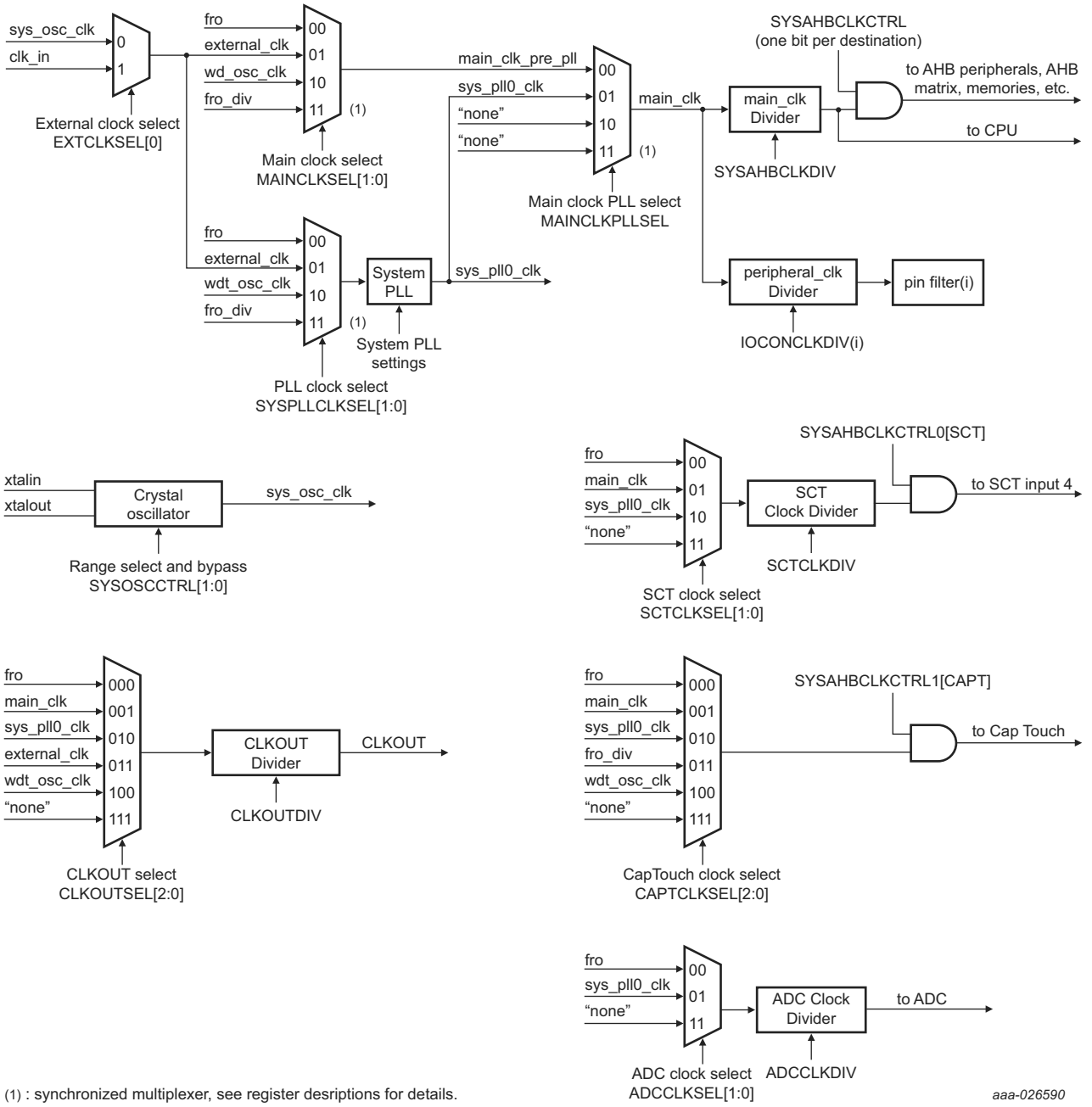


Fig 11. LPC84x clock generation

8.29 Emulation and debugging

Debug functions are integrated into the Arm Cortex-M0+. Serial wire debug functions are supported in addition to a standard JTAG boundary scan. The Arm Cortex-M0+ is configured to support up to four breakpoints and two watch points.

The Micro Trace Buffer is implemented on the LPC84x.

The $\overline{\text{RESET}}$ pin selects between the JTAG boundary scan ($\overline{\text{RESET}}$ = LOW) and the Arm SWD debug ($\overline{\text{RESET}}$ = HIGH). The Arm SWD debug port is disabled while the LPC84x is in reset. The JTAG boundary scan pins are selected by hardware when the part is in boundary scan mode (see Table 4).

To perform boundary scan testing, follow these steps:

1. Erase any user code residing in flash.
2. Power up the part with the $\overline{\text{RESET}}$ pin pulled HIGH externally.
3. Wait for at least 250 μs.
4. Pull the $\overline{\text{RESET}}$ pin LOW externally.
5. Perform boundary scan operations.
6. Once the boundary scan operations are completed, assert the $\overline{\text{TRST}}$ pin to enable the SWD debug mode, and release the $\overline{\text{RESET}}$ pin (pull HIGH).

Remark: The JTAG interface cannot be used for debug purposes.

11.4 Peripheral power consumption

The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled in the SYSAHBCLKCFG and PDRUNCFG (for analog blocks) registers. All other blocks are disabled in both registers and no code accessing the peripheral is executed. Measured on a typical sample at T_{amb} = 25 °C.

The supply currents are shown for FRO clock frequencies of 12 MHz and 30 MHz.

Table 14. Power consumption for individual analog and digital blocks

Peripheral	Typical supply current in µA			Notes
	System clock frequency =			
	n/a	12 MHz	30 MHz	
FRO	89	-	-	System oscillator running; PLL off; independent of main clock frequency; FRO = 24 MHz. FRO output disabled.
System oscillator at 12 MHz	243	-	-	FRO running; PLL off; independent of main clock frequency.
Watchdog oscillator	1	-	-	FRO; PLL off; independent of main clock frequency.
BOD	42	-	-	Independent of main clock frequency.
Flash	273	-	-	-
Main PLL	156	-	-	FRO (24 MHz) running; Main clock running at fro_div (12 MHz)
CLKOUT	-	25	61	Main clock divided by 4 in the CLKOUTDIV register. Not connected to pin.
ROM	-	35	86	-
GPIO + pin interrupt/pattern match	-	159	384	GPIO pins configured as outputs and set to LOW. Direction and pin state are maintained if the GPIO is disabled in the SYSAHBCLKCFG register.
SWM	-	85	206	-
IOCON	-	80	193	-
SCTimer/PWM	-	172	419	-
CTimer		51	123	
MRT	-	102	245	-
WWDT	-	28	70	-
I2C0	-	54	131	-
I2C1	-	47	115	-
I2C2	-	44	106	-
I2C3	-	60	145	-
SPI0	-	43	106	-
SPI1	-	44	107	-
USART0	-	53	128	-
USART1	-	53	130	-
USART2	-	46	90	-

11.5 Pin characteristics

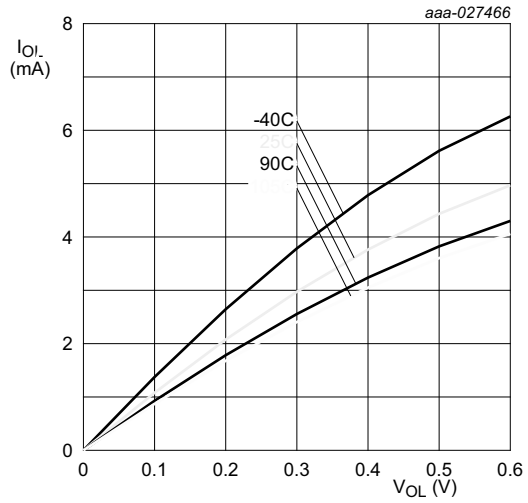
Table 15. Static characteristics, pin characteristics

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

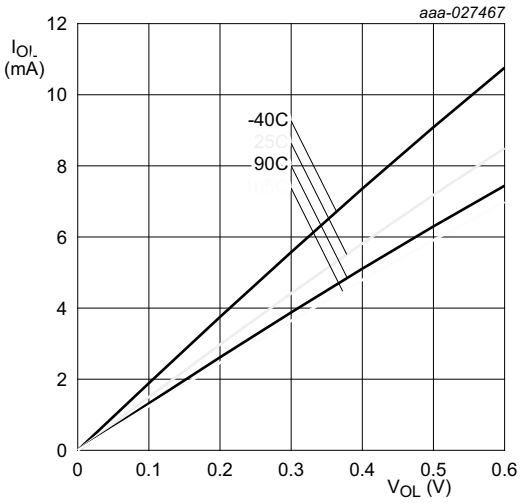
Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
Standard port pins configured as digital pins, RESET							
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled		-	0.5	10[2]	nA
I_{IH}	HIGH-level input current	$V_I = V_{DD}$; on-chip pull-down resistor disabled		-	0.5	10[2]	nA
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD}$; on-chip pull-up/down resistors disabled		-	0.5	10[2]	nA
V_I	input voltage	$V_{DD} \geq$ 1.8 V; 5 V tolerant pins except PIO0_6		0	-	5	V
		V_{DD} = 0 V		0	-	3.6	V
V_O	output voltage	output active		0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD}$	V
V_{hys}	hysteresis voltage			-	0.4	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = 4 mA; 2.5 V <= V_{DD} <= 3.6 V		$V_{DD} - 0.4$	-	-	V
		I_{OH} = 3 mA; 1.8 V <= V_{DD} < 2.5 V		$V_{DD} - 0.5$	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA; 2.5 V <= V_{DD} <= 3.6 V		-	-	0.5	V
		I_{OL} = 3 mA; 1.8 V <= V_{DD} < 2.5 V		-	-	0.5	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD} - 0.4$ V; 2.5 V ≤ V_{DD} ≤ 3.6 V		4	-	-	mA
		$V_{OH} = V_{DD} - 0.5$ V; 1.8 V ≤ V_{DD} < 2.5 V		3	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.5 V 2.5 V ≤ V_{DD} ≤ 3.6 V		4	-	-	mA
		1.8 V ≤ V_{DD} < 2.5 V		3	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V	[5]	-	-	45	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DD}$	[5]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V	[6]	10	50	150	µA
I_{pu}	pull-up current	V_I = 0 V; 2.0 V ≤ V_{DD} ≤ 3.6 V	[6]	15	50	85	µA
		1.8 V ≤ V_{DD} < 2.0 V		10	50	85	
		$V_{DD} < V_I$ < 5 V		0	0	0	µA
High-drive output pin configured as digital pin (PIO0_2, PIO0_3, PIO0_12, and PIO0_16)							
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled		-	0.5	10[2]	nA
I_{IH}	HIGH-level input current	$V_I = V_{DD}$; on-chip pull-down resistor disabled		-	0.5	10[2]	nA

Table 15. Static characteristics, pin characteristics *...continued*
T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{OZ}	OFF-state output current	V_O = 0 V; V_O = V_{DD}; on-chip pull-up/down resistors disabled		-	0.5	10[2]	nA
V_I	input voltage	$V_{DD} \geq$ 1.8 V		0	-	5.0	V
		V_{DD} = 0 V		0	-	3.6	V
V_O	output voltage	output active		0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage			0.7V_{DD}	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.3V_{DD}	V
V_{hys}	hysteresis voltage			-	0.4	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = 20 mA; 2.5 V <= V_{DD} < 3.6 V		V_{DD} − 0.5	-	-	V
		I_{OH} = 12 mA; 1.8 V <= V_{DD} < 2.5 V		V_{DD} − 0.5	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA 2.5 V <= V_{DD} < 3.6 V		-	-	0.5	V
		I_{OL} = 3 mA 1.8 V <= V_{DD} < 2.5 V		-	-	0.5	V
I_{OH}	HIGH-level output current	V_{OH} = V_{DD} − 0.5 V; 2.5 V <= V_{DD} < 3.6 V		20	-	-	mA
		V_{OH} = V_{DD} − 0.5 V; 1.8 V <= V_{DD} < 2.5 V		12	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.5 V 2.5 V ≤ V_{DD} ≤ 3.6 V		4	-	-	mA
		1.8 V ≤ V_{DD} < 2.5 V		3	-	-	mA
I_{OLS}	LOW-level short-circuit output current	V_{OL} = V_{DD}	[5]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V	[6]	10	50	150	µA
I_{pu}	pull-up current	V_I = 0 V	[6]	−10	−50	−85	µA
		V_{DD} < V_I < 5 V		0	0	0	µA
I^2C-bus pins (PIO0_10 and PIO0_11)							
V_{IH}	HIGH-level input voltage			0.7V_{DD}	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.3V_{DD}	V
V_{hys}	hysteresis voltage			-	0.05V_{DD}	-	V
I_{OL}	LOW-level output current	V_{OL} = 0.5 V; I^2C-bus pins configured as standard mode pins 2.5 V <= V_{DD} < 3.6 V		3.5	-	-	mA
		1.8 V <= V_{DD} < 2.5 V		3	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.5 V; I^2C-bus pins configured as Fast-mode Plus pins; 2.5 V <= V_{DD} < 3.6 V		20	-	-	mA
		1.8 V <= V_{DD} < 2.5 V		16	-	-	mA

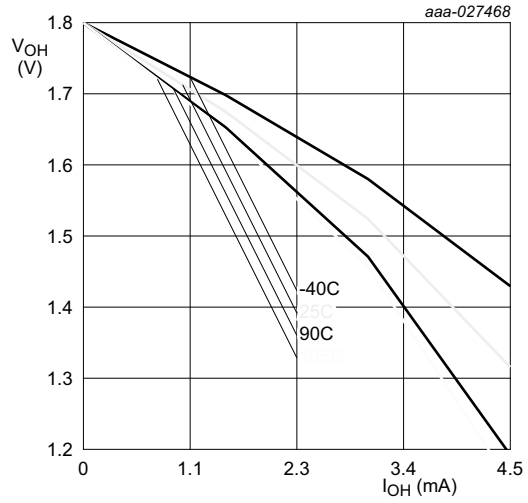


Conditions: V_{DD} = 1.8 V; standard port pins and high-drive pin PIO0_12.

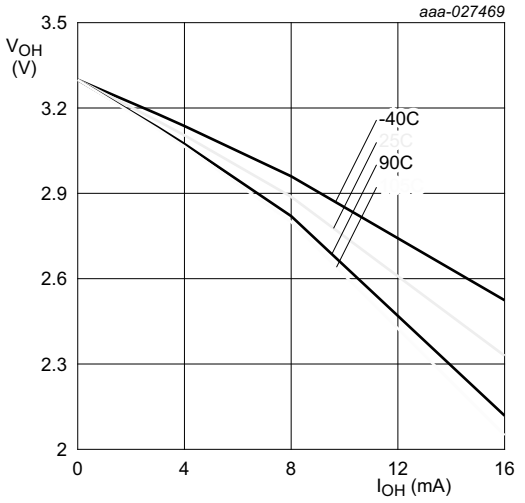


Conditions: V_{DD} = 3.3 V; standard port pins and high-drive pin PIO0_12.

Fig 25. Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}



Conditions: V_{DD} = 1.8 V; standard port pins.



Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 26. Typical HIGH-level output voltage V_{OH} versus HIGH-level output source current I_{OH}

12. Dynamic characteristics

12.1 Flash memory

Table 16. Flash characteristics

T_{amb} = −40 °C to +105 °C. Based on JEDEC NVM qualification. Failure rate < 10 ppm for parts as specified below.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
N_{endu}	endurance		[1]	10000	100000	-	cycles
t_{ret}	retention time	powered		10	20	-	years
		not powered		20	40	-	years
t_{er}	erase time	page or multiple consecutive pages, sector or multiple consecutive sectors		95	100	105	ms
t_{prog}	programming time		[2]	0.95	1	1.05	ms

[1] Number of program/erase cycles.

[2] Programming times are given for writing 64 bytes to the flash. T_{amb} <= +85 °C. Flash programming with IAP calls (see *LPC84x user manual*).

12.2 FRO

Table 17. Dynamic characteristic: FRO

T_{amb} = −40 °C to +105 °C; 1.8 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Min	Typ[1]	Max	Unit
FRO clock frequency; Condition: 0 °C ≤ T_{amb} ≤ 70 °C				
$f_{osc(RC)}$	18 -1 %	18	18 +1 %	MHz
$f_{osc(RC)}$	24 -1 %	24	24 +1 %	MHz
$f_{osc(RC)}$	30 -1 %	30	30 +1 %	MHz
FRO clock frequency; Condition: −20 °C ≤ T_{amb} ≤ 70 °C				
$f_{osc(RC)}$	18 -2 %	18	18 +1 %	MHz
$f_{osc(RC)}$	24 -2 %	24	24 +1 %	MHz
$f_{osc(RC)}$	30 -2 %	30	30 +1 %	MHz
FRO clock frequency; Condition: −40 °C ≤ T_{amb} ≤ 105 °C				
$f_{osc(RC)}$	18 -3.5 %	18	18 +2.5 %	MHz
$f_{osc(RC)}$	24 -3.5 %	24	24 +2.5 %	MHz
$f_{osc(RC)}$	30 -3.5 %	30	30 +2.5 %	MHz

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

12.8 USART interface

The actual USART bit rate depends on the delays introduced by the external trace, the external device, system clock (CCLK), and capacitive loading. Excluding delays introduced by external device and PCB, the maximum supported bit rate for USART master synchronous mode is 10 Mbit/s, and the maximum supported bit rate for USART slave synchronous mode is 10 Mbit/s.

Remark: USART functions can be assigned to all digital pins. The characteristics are valid for all digital pins except the open-drain pins PIO0_10 and PIO0_11.

Table 24. USART dynamic characteristics

T_{amb} = −40 °C to 105 °C; 1.8 V <= V_{DD} <= 3.6 V unless noted otherwise; C_L = 10 pF; input slew = 10 ns. Simulated parameters sampled at the 30 %/70 % level of the falling or rising edge; values guaranteed by design.

Symbol	Parameter	Conditions	Min	Max	Unit
USART master (in synchronous mode)					
$t_{su(D)}$	data input set-up time	3.0 V <= V_{DD} <= 3.6 V	31	-	ns
		1.8 V <= V_{DD} < 3.0 V	42		
$t_{h(D)}$	data input hold time		0	-	ns
$t_{v(Q)}$	data output valid time		0	7	ns
USART slave (in synchronous mode)					
$t_{su(D)}$	data input set-up time		5	-	ns
$t_{h(D)}$	data input hold time		5	-	ns
$t_{v(Q)}$	data output valid time	3.0 V <= V_{DD} <= 3.6 V	0	35	ns
		1.8 V <= V_{DD} < 3.0 V	0	46	ns

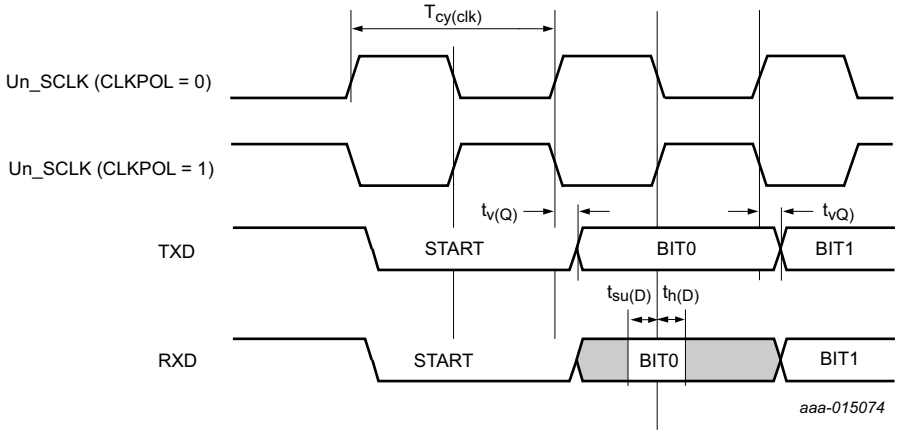


Fig 32. USART timing

13. Characteristics of analog peripherals

13.1 BOD

Table 26. BOD static characteristics[1]
T_{amb} = 25 °C.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{th}	threshold voltage	interrupt level 1					
		assertion		-	2.25	-	V
		de-assertion		-	2.38	-	V
		interrupt level 2					
		assertion		-	2.55	-	V
		de-assertion		-	2.66	-	V
		interrupt level 3					
		assertion		-	2.84	-	V
		de-assertion		-	2.92	-	V
		reset level 0					
		assertion		-	1.84	-	V
		de-assertion		-	1.97	-	V
		reset level 1					
		assertion		-	2.05	-	V
		de-assertion		-	2.18	-	V
		reset level 2					
		assertion		-	2.35	-	V
		de-assertion		-	2.47	-	V
		reset level 3					
		assertion		-	2.63	-	V
		de-assertion		-	2.76	-	V

[1] Interrupt levels are selected by writing the level value to the BOD control register BODCTRL, see *the* LPC84x *user manual*. Interrupt level 0 is reserved.

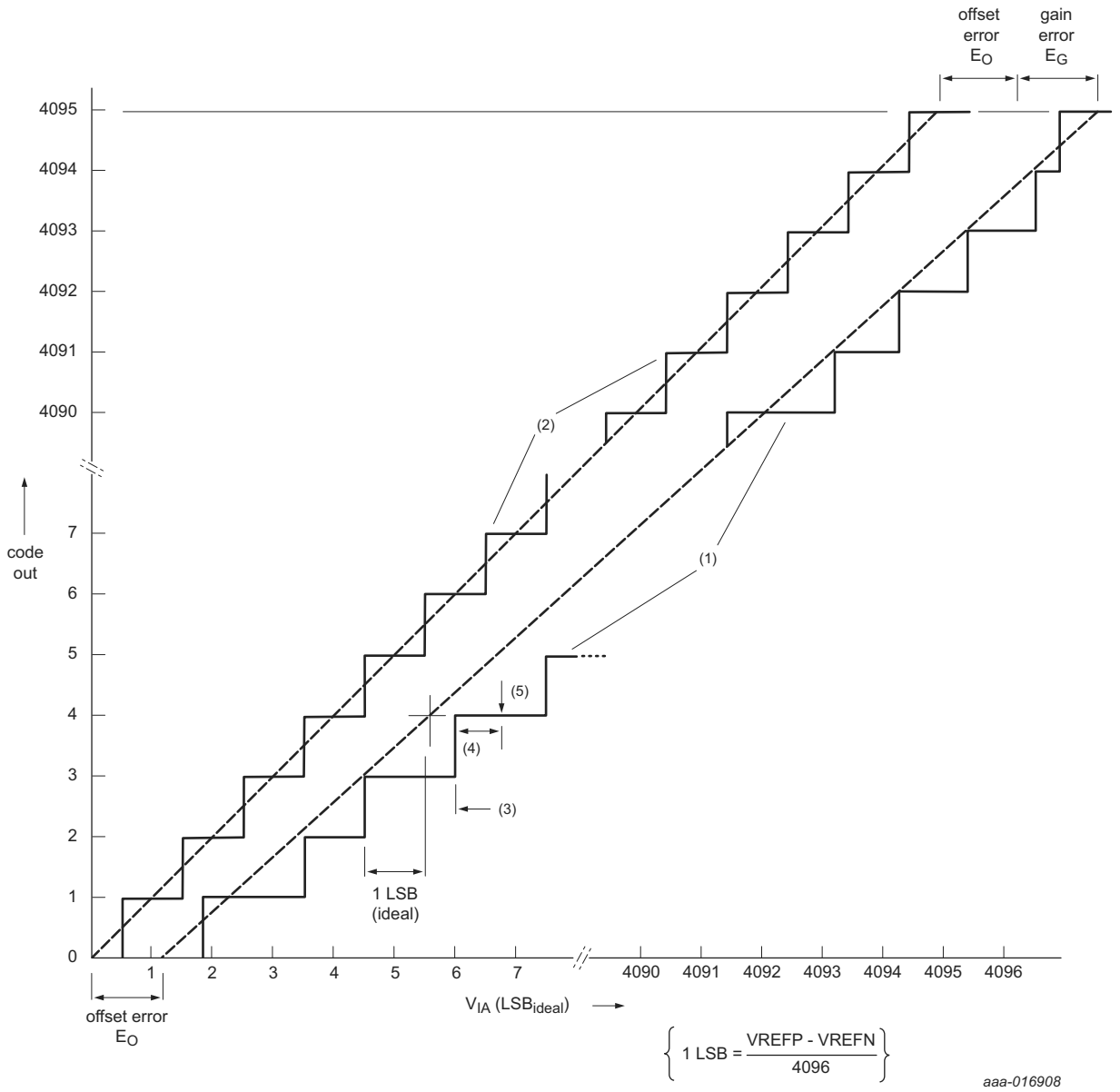
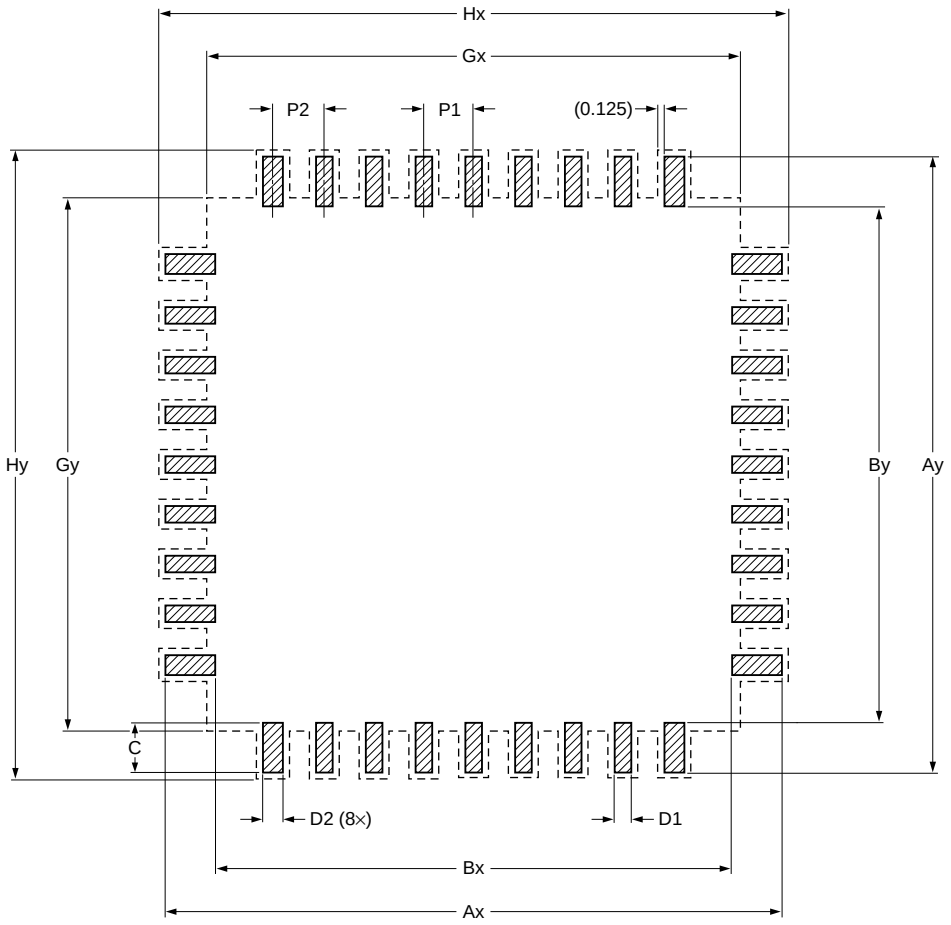


Fig 33. 12-bit ADC characteristics

Footprint information for reflow soldering of LQFP64 package **SOT314-2**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

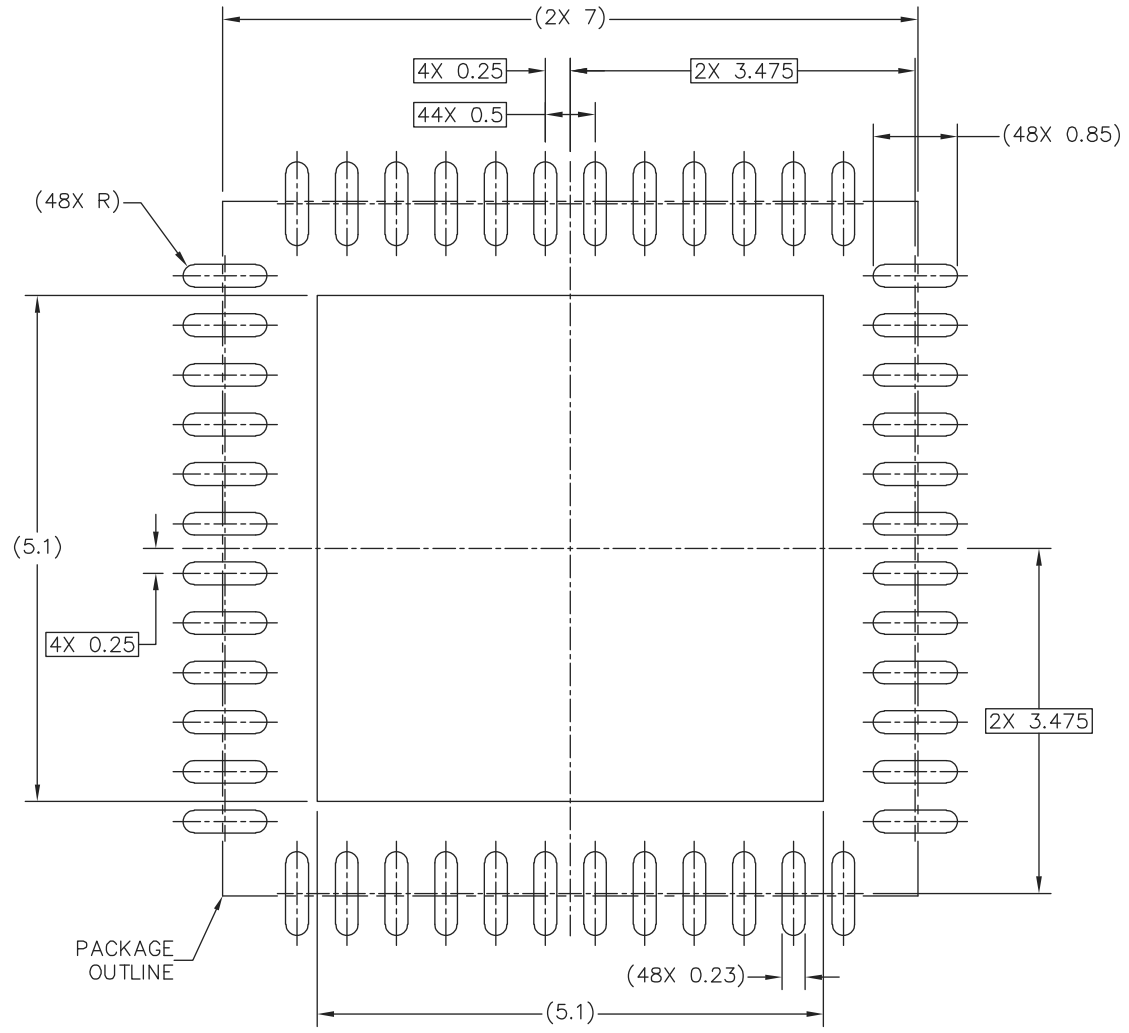
occupied area

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	13.300	13.300	10.300	10.300	1.500	0.280	0.400	10.500	10.500	13.550	13.550

sot314-2_fr

Fig 45. Reflow soldering for the LQFP64 package



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 DATE: 13 DEC 2017

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: SOT619–1	REVISION: 0	

Fig 47. Reflow soldering of the HVQFN48 package (7x7) 2 of 3

20. Legal information

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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