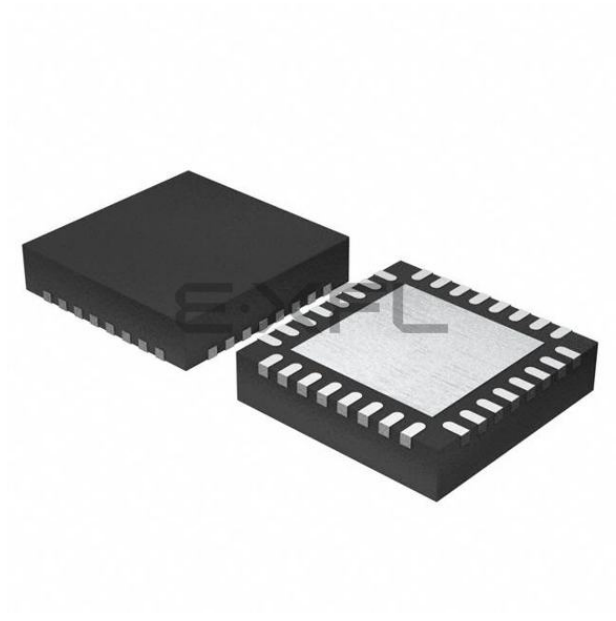

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	30MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, Cap Sense, DMA, POR, PWM, WDT
Number of I/O	29
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	External, Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-HVQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc844m201jhi33e

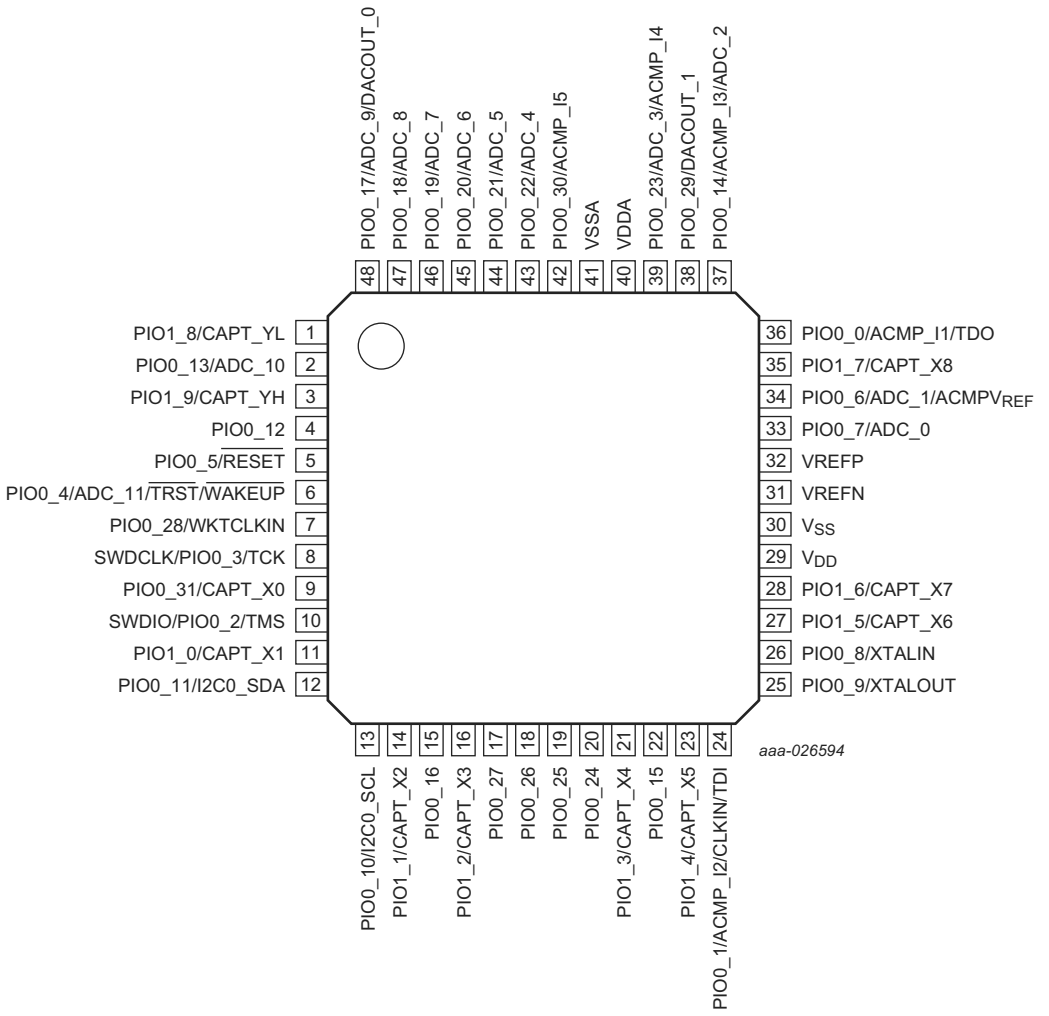


Fig 5. Pin configuration LQFP48 package

Table 4. Pin description

Symbol	LQFP64	LQFP48	HVQFN48	HVQFN33		Reset state[1]	Type	Description
PIO0_14/ ACMP_I3/ADC_2	49	37	37	25	[2]	I; PU	IO	**PIO0_14 —** General-purpose port 0 input/output 14.
							A	**ACMP_I3 —** Analog comparator common input 3.
							A	**ADC_2 —** ADC input 2.
PIO0_15	30	22	22	15	[5]	I; PU	IO	**PIO0_15 —** General-purpose port 0 input/output 15.
PIO0_16	19	15	15	10	[4]	I; PU	IO	**PIO0_16 —** General-purpose port 0 input/output 16.
PIO0_17/ADC_9/ DACOUT_0	63	48	48	32	[2]	I; PU	IO	**PIO0_17 —** General-purpose port 0 input/output 17.
							A	**ADC_9 —** ADC input 9.
							A	**DACOUT_0 —** DAC Output 0.
PIO0_18/ADC_8	61	47	47	31	[2]	I; PU	IO	**PIO0_18 —** General-purpose port 0 input/output 18.
							A	**ADC_8 —** ADC input 8.
PIO0_19/ADC_7	60	46	46	30	[2]	I; PU	IO	**PIO0_19 —** General-purpose port 0 input/output 19.
							A	**ADC_7 —** ADC input 7.
PIO0_20/ADC_6	58	45	45	29	[2]	I; PU	IO	**PIO0_20 —** General-purpose port 0 input/output 20.
							A	**ADC_6 —** ADC input 6.
PIO0_21/ADC_5	57	44	44	28	[2]	I; PU	IO	**PIO0_21 —** General-purpose port 0 input/output 21.
							A	**ADC_5 —** ADC input 5.
PIO0_22/ADC_4	55	43	43	27	[2]	I; PU	IO	**PIO0_22 —** General-purpose port 0 input/output 22.
							A	**ADC_4 —** ADC input 4.
PIO0_23/ADC_3/ ACMP_I4	51	39	39	26	[2]	I; PU	IO	**PIO0_23 —** General-purpose port 0 input/output 23.
							A	**ADC_3 —** ADC input 3.
							A	**ACMP_I4 —** Analog comparator common input 4.
PIO0_24	28	20	20	14	[5]	I; PU	IO	**PIO0_24 —** General-purpose port 0 input/output 24. In ISP mode, this is the U0_RXD pin.
PIO0_25	27	19	19	13	[5]	I; PU	IO	**PIO0_25 —** General-purpose port 0 input/output 25. In ISP mode, this pin is the U0_TXD pin.
PIO0_26	23	18	18	12	[5]	I; PU	IO	**PIO0_26 —** General-purpose port 0 input/output 26.
PIO0_27	21	17	17	11	[5]	I; PU	IO	**PIO0_27 —** General-purpose port 0 input/output 27.
PIO0_28/ WKTCLKIN	10	7	7	5	[3]	I; PU	IO	**PIO0_28 —** General-purpose port 0 input/output 28. This pin can host an external clock for the self-wake-up timer. To use the pin as a self-wake-up timer clock input, select the external clock in the wake-up timer CTRL register. The external clock input is active in all power modes, including deep power-down.
PIO0_29/ DACOUT_1	50	38	38	-	[5]	I; PU	IO	**PIO0_29 —** General-purpose port 0 input/output 29.
							A	**DACOUT_1 —** DAC output 1.
PIO0_30/ACMP_I5	54	42	42	-	[5]	I; PU	IO	**PIO0_30 —** General-purpose port 0 input/output 30.
							A	**ACMP_I5 —** Analog comparator common input 5.

Table 4. Pin description

Symbol	LQFP64	LQFP48	HVQFN48	HVQFN33		Reset state[1]	Type	Description
PIO0_31/CAPT_X0	13	9	9	-	[5]	I; PU	IO	**PIO0_31 —** General-purpose port 0 input/output 31.
								CAPT_X0 — Capacitive Touch X sensor 0.
PIO1_0/CAPT_X1	15	11	11	-	[5]	I; PU	IO	**PIO1_0 —** General-purpose port 1 input/output 0.
								CAPT_X1 — Capacitive Touch X sensor 1.
PIO1_1/CAPT_X2	18	14	14	-	[5]	I; PU	IO	**PIO1_1 —** General-purpose port 1 input/output 1.
								CAPT_X2 — Capacitive Touch X sensor 2.
PIO1_2/CAPT_X3	20	16	16	-	[5]	I; PU	IO	**PIO1_2 —** General-purpose port 1 input/output 2.
								CAPT_X3 — Capacitive Touch X sensor 3.
PIO1_3/CAPT_X4	29	21	21	-	[5]	I; PU	IO	**PIO1_3 —** General-purpose port 1 input/output 3.
								CAPT_X4 — Capacitive Touch X sensor 4.
PIO1_4/CAPT_X5	31	23	23	-	[5]	I; PU	IO	**PIO1_4 —** General-purpose port 1 input/output 4.
								CAPT_X5 — Capacitive Touch X sensor 5.
PIO1_5/CAPT_X6	35	27	27	-	[5]	I; PU	IO	**PIO1_5 —** General-purpose port 1 input/output 5.
								CAPT_X6 — Capacitive Touch X sensor 6.
PIO1_6/CAPT_X7	38	28	28	-	[5]	I; PU	IO	**PIO1_6 —** General-purpose port 1 input/output 6.
								CAPT_X7 — Capacitive Touch X sensor 7.
PIO1_7/CAPT_X8	47	35	35	-	[5]	I; PU	IO	**PIO1_7 —** General-purpose port 1 input/output 7.
								CAPT_X8 — Capacitive Touch X sensor 8.
PIO1_8/CAPT_YL	1	1	1	-	[5]	I; PU	IO	**PIO1_8 —** General-purpose port 1 input/output 8.
								CAPT_YL — Capacitive Touch Y Low.
PIO1_9/CAPT_YH	3	3	3	-	[5]	I; PU	IO	**PIO1_9 —** General-purpose port 1 input/output 9.
								CAPT_YH — Capacitive Touch Y High.
PIO1_10	64	-	-	-	[5]	I; PU	IO	**PIO1_10 —** General-purpose port 1 input/output 10.
PIO1_11	62	-	-	-	[5]	I; PU	IO	**PIO1_11 —** General-purpose port 1 input/output 11.
PIO1_12	9	-	-	-	[5]	I; PU	IO	**PIO1_12 —** General-purpose port 1 input/output 12.
PIO1_13	11	-	-	-	[5]	I; PU	IO	**PIO1_13 —** General-purpose port 1 input/output 13.
PIO1_14	22	-	-	-	[5]	I; PU	IO	**PIO1_14 —** General-purpose port 1 input/output 14.
PIO1_15	24	-	-	-	[5]	I; PU	IO	**PIO1_15 —** General-purpose port 1 input/output 15.
PIO1_16	36	-	-	-	[5]	I; PU	IO	**PIO1_16 —** General-purpose port 1 input/output 16.
PIO1_17	37	-	-	-	[5]	I; PU	IO	**PIO1_17 —** General-purpose port 1 input/output 17.
PIO1_18	43	-	-	-	[5]	I; PU	IO	**PIO1_18 —** General-purpose port 1 input/output 18.
PIO1_19	44	-	-	-	[5]	I; PU	IO	**PIO1_19 —** General-purpose port 1 input/output 19.
PIO1_20	56	-	-	-	[5]	I; PU	IO	**PIO1_20 —** General-purpose port 1 input/output 20.
PIO1_21	59	-	-	-	[5]	I; PU	IO	**PIO1_21 —** General-purpose port 1 input/output 21.
V_{DD}	7;26;39	29	29	19		-	-	Supply voltage for the I/O pad ring, the and core voltage regulator.
V_{DDA}	52	40	40					Analog supply voltage.
V_{SS}	8;25;40	30	30	33[11]		-	-	Ground.

8.7 Nested Vectored Interrupt Controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is part of the Cortex-M0+. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

8.7.1 Features

- Nested Vectored Interrupt Controller is a part of the Arm Cortex-M0+.
- Tightly coupled interrupt controller provides low interrupt latency.
- Controls system exceptions and peripheral interrupts.
- Supports 32 vectored interrupts.
- In the LPC84x, the NVIC supports vectored interrupts for each of the peripherals and the eight pin interrupts.
- Four programmable interrupt priority levels with hardware priority level masking.
- Software interrupt generation using the Arm exceptions SVCall and PendSV.
- Supports NMI.

8.7.2 Interrupt sources

Each peripheral device has at least one interrupt line connected to the NVIC but can have several interrupt flags. Individual interrupt flags can also represent more than one interrupt source.

8.8 System tick timer

The Arm Cortex-M0+ includes a 24-bit system tick timer (SysTick) that is intended to generate a dedicated SysTick exception at a fixed time interval (typically 10 ms).

8.9 I/O configuration

The IOCON block controls the configuration of the I/O pins. Each digital or mixed digital/analog pin with the PIO0_n designator (except the true open-drain pins PIO0_10 and PIO0_11) in Table 4 can be configured as follows:

- Enable or disable the weak internal pull-up and pull-down resistors.
- Select a pseudo open-drain mode. The input cannot be pulled up above V_{DD}. The pins are not 5 V tolerant when V_{DD} is grounded.
- Program the input glitch filter with different filter constants using one of the IOCON divided clock signals (IOCONCLKCDIV, see Figure 11 “LPC84x clock generation”). You can also bypass the glitch filter.
- Invert the input signal.
- Hysteresis can be enabled or disabled.
- For pins PIO0_10 and PIO0_11, select the I2C-mode and output driver for standard digital operation, for I2C standard and fast modes, or for I2C Fast mode+.
- The switch matrix setting enables the analog input mode on pins with analog and digital functions. Enabling the analog mode disconnects the digital functionality.

Remark: The functionality of each I/O pin is flexible and is determined entirely through the switch matrix. See Section 8.10 for details.

8.13.2 DMA trigger input MUX (TRIGMUX)

Each DMA trigger is connected to a programmable multiplexer which connects the trigger input to one of multiple trigger sources. Each multiplexer supports the same trigger sources: the ADC sequence interrupts, the SCT DMA request lines, and pin interrupts PININT0 and PININT1, and the outputs of the DMA triggers 0 and 1 for chaining DMA triggers.

8.14 USART0/1/2/3/4

All USART functions are movable functions and are assigned to pins through the switch matrix.

8.14.1 Features

- Maximum bit rates of 1.875 Mbit/s in asynchronous mode and 10 Mbit/s in synchronous mode for USART functions connected to all digital pins except the open-drain pins.
- 7, 8, or 9 data bits and 1 or 2 stop bits
- Synchronous mode with master or slave operation. Includes data phase selection and continuous clock option.
- Multiprocessor/multidrop (9-bit) mode with software address compare. (RS-485 possible with software address detection and transceiver direction control.)
- Parity generation and checking: odd, even, or none.
- One transmit and one receive data buffer.
- RTS/CTS for hardware signaling for automatic flow control. Software flow control can be performed using Delta CTS detect, Transmit Disable control, and any GPIO as an RTS output.
- Received data and status can optionally be read from a single register
- Break generation and detection.
- Receive data is 2 of 3 sample "voting". Status flag set when one sample differs.
- Built-in Baud Rate Generator.
- A fractional rate divider is shared among all UARTs.
- Interrupts available for Receiver Ready, Transmitter Ready, Receiver Idle, change in receiver break detect, Framing error, Parity error, Overrun, Underrun, Delta CTS detect, and receiver sample noise detected.
- Separate data and flow control loopback modes for testing.
- Baud rate clock can also be output in asynchronous mode.

8.15 SPI0/1

All SPI functions are movable functions and are assigned to pins through the switch matrix.

8.15.1 Features

- Maximum data rates of up to 30 Mbit/s in master mode and up to 18 Mbit/s in slave mode for SPI functions connected to all digital pins except the open-drain pins.

- The following conditions define an event: a counter match condition, an input (or output) condition such as a rising or falling edge or level, a combination of match and/or input/output condition.
- Selected events can limit, halt, start, or stop a counter or change its direction.
- Events trigger state changes, output toggles, interrupts, and DMA transactions.
- Match register 0 can be used as an automatic limit.
- In bidirectional mode, events can be enabled based on the count direction.
- Match events can be held until another qualifying event occurs.

- State control features:
  - A state is defined by events that can happen in the state while the counter is running.
  - A state changes into another state as a result of an event.
  - Each event can be assigned to one or more states.
  - State variable allows sequencing across multiple counter cycles.
- One SCTimer match output can be selected as ADC hardware trigger input.

8.18.2 SCTimer/PWM input MUX (INPUT MUX)

Each input of the SCTimer/PWM is connected to a programmable multiplexer which allows to connect one of multiple internal or external sources to the input. The available sources are the same for each SCTimer/PWM input and can be selected from four pins configured through the switch matrix, the ADC threshold compare interrupt, the comparator output, and the Arm core signals Arm_TXEV and DEBUG_HALTED.

8.19 CTIMER

8.19.1 General-purpose 32-bit timers/external event counter

The LPC84x has one general-purpose 32-bit timer/counter.

The timer/counter is designed to count cycles of the system derived clock or an externally-supplied clock. It can optionally generate interrupts, generate timed DMA requests, or perform other actions at specified timer values, based on four match registers. Each timer/counter also includes two capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt.

8.19.2 Features

- A 32-bit timer/counter with a programmable 32-bit prescaler.
- Counter or timer operation.
- Up to three 32-bit captures can take a snapshot of the timer value when an input signal transitions. A capture event may also optionally generate an interrupt. The number of capture inputs for each timer that are actually available on device pins can vary by device.
- Four 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.

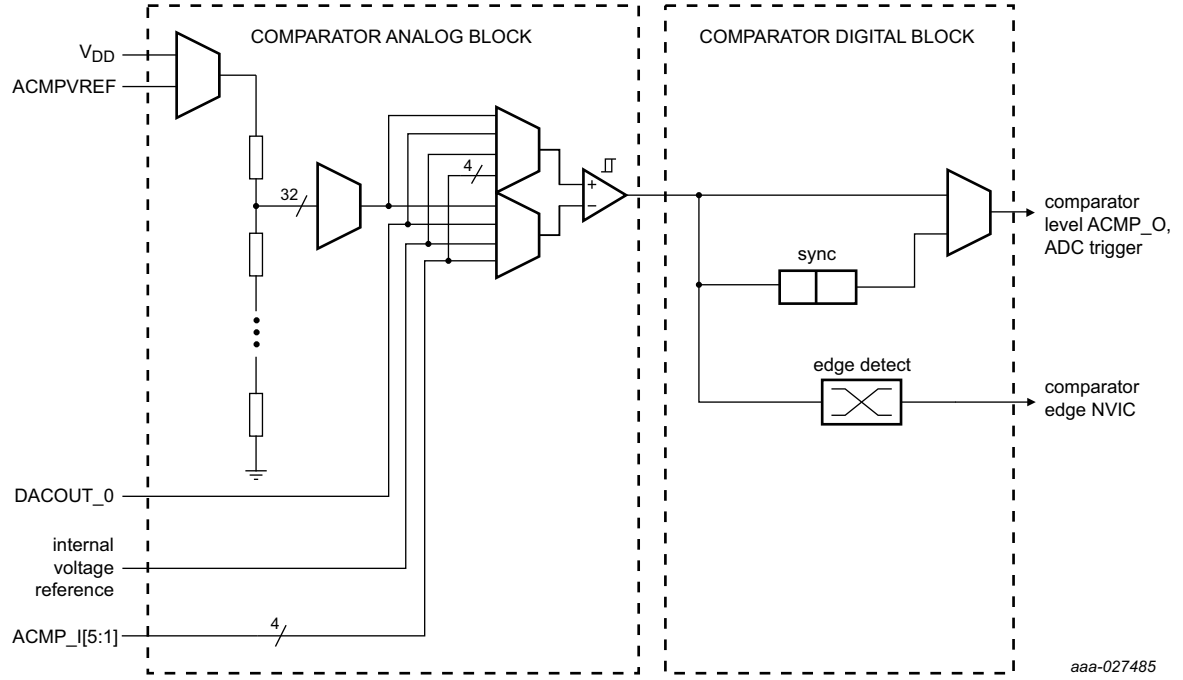


Fig 10. Comparator block diagram

8.23.1 Features

- Selectable 0 mV, 10 mV (± 5 mV), and 20 mV (± 10 mV), 40 mV (± 20 mV) input hysteresis.
- Two selectable external voltages (V_{DD} or $ACMPV_{REF}$); fully configurable on either positive or negative input channel.
- Internal voltage reference from band gap selectable on either positive or negative input channel.
- 32-stage voltage ladder with the internal reference voltage selectable on either the positive or the negative input channel.
- Voltage ladder source voltage is selectable from an external pin or the main 3.3 V supply voltage rail.
- Voltage ladder can be separately powered down for applications only requiring the comparator function.
- Interrupt output is connected to NVIC.
- Comparator level output is connected to output pin ACMP_O.
- One comparator output is internally collected to the ADC trigger input multiplexer.

8.24 Analog-to-Digital Converter (ADC)

The ADC supports a resolution of 12 bit and fast conversion rates of up to 1.2 MSamples/s. Sequences of analog-to-digital conversions can be triggered by multiple sources. Possible trigger sources are the pin triggers, the SCT output SCT_OUT3, the analog comparator output, and the Arm TXEV.

- Supports CPU PIO or DMA back-to-back transfer.
- Accept any size of data width per write: 8, 16 or 32-bit.
  - 8-bit write: 1-cycle operation.
  - 16-bit write: 2-cycle operation (8-bit x 2-cycle).
  - 32-bit write: 4-cycle operation (8-bit x 4-cycle).

8.27 Clocking and power control

8.27.1 Crystal and internal oscillators

The LPC84x include four independent oscillators:

1. The crystal oscillator (SysOsc) operating at frequencies between 1 MHz and 25 MHz.
2. Free Running Oscillator.
3. Watchdog Oscillator
4. Low Power Oscillator

Each oscillator, except the low-frequency oscillator, can be used for more than one purpose as required in a particular application.

Following reset, the LPC84x operates from the FRO until switched by software allowing the part to run without any external crystal and the bootloader code to operate at a known frequency.

See Figure 11 for an overview of the LPC84x clock generation.

8.27.1.1 Free Running Oscillator (FRO)

The FRO oscillator provides the default clock at reset and provides a clean system clock shortly after the supply pins reach operating voltage.

- This oscillator provides a selectable 18 MHz, 24 MHz, and 30 MHz outputs that can be used as a system clock. Also, these outputs can be divided down to 1.125 MHz, 1.5 MHz, 1.875 MHz, 9 MHz, 12 MHz, and 15 MHz for system clock.
- The FRO is trimmed to ±1 % accuracy over the entire voltage and temperature range of 0 C to 70 C.
- By default, the fro_oscout is 24 MHz and is divided by 2 to provide a default system (CPU) clock frequency of 12 MHz.

8.27.1.2 Crystal Oscillator (SysOsc)

The crystal oscillator can be used as the clock source for the CPU, with or without using the PLL.

The SysOsc operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the system PLL.

8.27.1.3 Internal Low-power Oscillator and Watchdog Oscillator (WDOsc)

The nominal frequency of the WDOsc is programmable between 9.4 kHz and 2.3 MHz. The frequency spread over silicon process variations is ± 40%.

The WDOsc is a dedicated oscillator for the windowed WWDT.

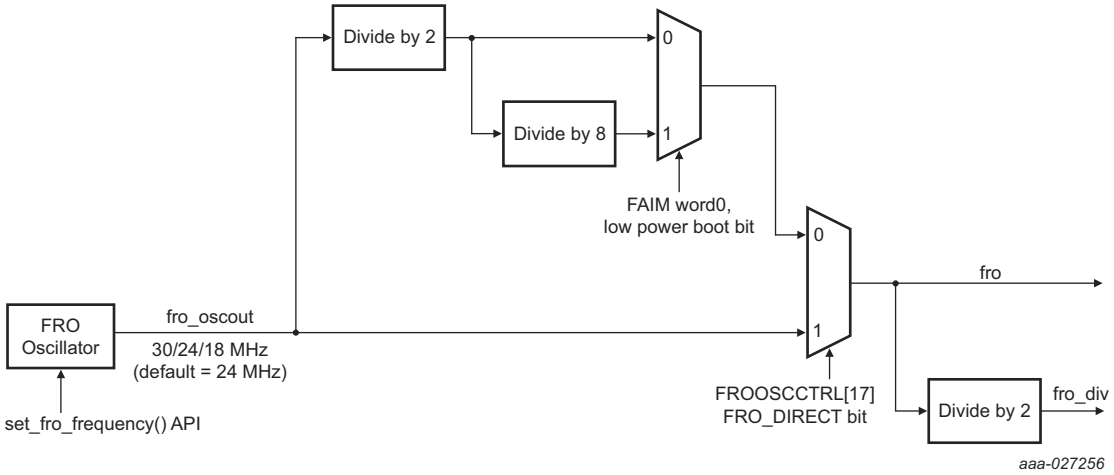


Fig 13. LPC84x FRO subsystem

Table 6. Clocking diagram signal name descriptions

Name	Description
sys_osc_clk	This is the internal clock that comes from external crystal oscillator through dedicated pins.
frg_clk	The output of the Fractional Rate Generator. The FRG and its source selection are shown in Figure 12 “LPC84x clock generation (continued)”.
fro	The output of the currently selected on-chip FRO oscillator. See UM11029 User manual.
fro_div	The FRO output. This may be either 15 MH, 12 MHz, or 9 MHz. See UM11029 User manual.
main_clk	The main clock used by the CPU and AHB bus, and potentially many others. The main clock and its source selection are shown in Figure 11 “LPC84x clock generation”.
“none”	A tied-off source that should be selected to save power when the output of the related multiplexer is not used.
sys_pll0_clk	The output of the System PLL. The System PLL and its source selection are shown in Figure 11 “LPC84x clock generation”.
wdt_osc_clk	The output of the watchdog oscillator, which has a selectable target frequency. It must also be enabled in the PDRINCFG0 register. See UM11029 User manual.
xtalin	Input of the main oscillator. If used, this is connected to an external crystal and load capacitor.
xtalout	Output of the main oscillator. If used, this is connected to an external crystal and load capacitor.
clk_in	This is the internal clock that comes from the main CLK_IN pin function. Connect that function to the pin by selecting it in the IOCON block.
external_clk	This is the internal clock that comes from the external crystal oscillator or the CLK_IN pin.

8.27.5 Power control

The LPC84x supports the Arm Cortex-M0+ sleep mode. The CPU clock rate may also be controlled as needed by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value. This allows a trade-off of power versus processing speed based on application requirements. In addition, a register is provided for shutting down the clocks to individual on-chip peripherals, allowing to fine-tune power consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Selected peripherals have their own clock divider which provides even better power control.

8.28.3 Code security (Code Read Protection - CRP)

CRP provides different levels of security in the system so that access to the on-chip flash and use of the Serial Wire Debugger (SWD) and In-System Programming (ISP) can be restricted. Programming a specific pattern into a dedicated flash location invokes CRP. IAP commands are not affected by the CRP.

In addition, ISP entry via the ISP entry pin can be disabled without enabling CRP. For details, see the *LPC84x user manual*.

There are three levels of Code Read Protection:

1. CRP1 disables access to the chip via the SWD and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors cannot be erased.
2. CRP2 disables access to the chip via the SWD and only allows full flash erase and update using a reduced set of the ISP commands.
3. Running an application with level CRP3 selected, fully disables any access to the chip via the SWD pins and the ISP. This mode effectively disables ISP override using the ISP entry pin as well. If necessary, the application must provide a flash update mechanism using IAP calls or using a call to the reinvoke ISP command to enable flash update via the USART.

CAUTION	
	If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

In addition to the three CRP levels, sampling of the ISP entry pin for valid user code can be disabled. For details, see the *LPC84x user manual*.

8.28.4 APB interface

The APB peripherals are located on one APB bus.

8.28.5 AHBLite

The AHBLite connects the CPU bus of the Arm Cortex-M0+ to the flash memory, the main static RAM, the CRC, the DMA, the ROM, and the APB peripherals.

Table 9. Limiting values *…continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
$P_{tot(pack)}$	total power dissipation (per package)	LQFP64, based on package heat transfer, not device power consumption	[12]	-	0.66	W
		LQFP64, based on package heat transfer, not device power consumption	[13]	-	0.48	W
		LQFP48, based on package heat transfer, not device power consumption	[12]	-	0.48	W
		LQFP48, based on package heat transfer, not device power consumption	[13]	-	0.34	W
		HVQFN48, based on package heat transfer, not device power consumption	[12]	-	1.12	W
		HVQFN48, based on package heat transfer, not device power consumption	[13]	-	0.46	W
		HVQFN33, based on package heat transfer, not device power consumption	[12]	-	0.98	W
		HVQFN33, based on package heat transfer, not device power consumption	[13]	-	0.34	W
V_{esd}	electrostatic discharge voltage	human body model; all pins		-	2000	V

[1] The following applies to the limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Maximum/minimum voltage above the maximum operating voltage (see Table 13) and below ground that can be applied for a short time (< 10 ms) to a device without leading to irrecoverable failure. Failure includes the loss of reliability and shorter lifetime of the device.

[3] Applies to all 5 V tolerant I/O pins except true open-drain pins PIO0_10 and PIO0_11 and except the 3 V tolerant pin PIO0_6.

[4] Including the voltage on outputs in 3-state mode.

[5] V_{DD} present or not present. Compliant with the I^2C-bus standard. 5.5 V can be applied to this pin when V_{DD} is powered down.

[6] V_{DD} present or not present.

[7] An ADC input voltage above 3.6 V can be applied for a short time without leading to immediate, unrecoverable failure. Accumulated exposure to elevated voltages at 4.6 V must be less than 10^6 s total over the lifetime of the device. Applying an elevated voltage to the ADC inputs for a long time affects the reliability of the device and reduces its lifetime.

[8] If the comparator is configured with the common mode input $V_{IC} = V_{DD}$, the other comparator input can be up to 0.2 V above or below V_{DD} without affecting the hysteresis range of the comparator function.

[9] It is recommended to connect an overvoltage protection diode between the analog input pin and the voltage supply pin.

[10] Dependent on package type.

[11] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

[12] JEDEC (4.5 in × 4 in); still air.

[13] Single layer (4.5 in × 3 in); still air.

11. Static characteristics

11.1 General operating conditions

Table 11. General operating conditions

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
f_{clk}	clock frequency	internal CPU/system clock		-	-	30	MHz
V_{DD}	supply voltage (core and external rail)		[3]	1.8	-	3.6	V
		FAIM programming only		3.0	-	3.6	V
		For ADC operations		2.4	-	3.6	V
		For DAC operations		2.7	-	3.6	V
V_{DDA}	analog supply voltage	For ADC operations		2.4	-	3.6	V
		For DAC operations		2.7	-	3.6	V
V_{ref}	ADC positive reference voltage	on pin VREFP		2.4	-	V_{DDA}	V
Oscillator pins							
$V_{i(xtal)}$	crystal input voltage	on pin XTALIN		−0.5	1.8	1.95	V
$V_{o(xtal)}$	crystal output voltage	on pin XTALOUT		−0.5	1.8	1.95	V
Pin capacitance							
C_{io}	input/output capacitance	pins with analog and digital functions	[2]	-	-	7.1	pF
		I^2C-bus pins	[2]	-	-	2.5	pF
		pins with digital functions only	[2]	-	-	2.8	pF

[1] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), nominal supply voltages.

[2] Including bonding pad capacitance. Based on simulation, not tested in production.

[3] The V_{DD} supply voltage must be 1.9 V or above when connecting an external crystal oscillator to the system oscillator. If the V_{DD} supply voltage is below 1.9 V, an external clock source can be fed to the XTALIN by bypassing the system oscillator or the other clock sources mentioned above can be used.

Table 14. Power consumption for individual analog and digital blocks *…continued*

Peripheral	Typical supply current in µA			Notes
	System clock frequency =			
	n/a	12 MHz	30 MHz	
USART3	-	58	142	-
USART4	-	56	137	-
Comparator ACMP	-	79	144	-
ADC	-	78	190	Digital controller only. Analog portion of the ADC disabled in the PDRUNCFG register.
	-	78	190	Combined analog and digital logic. ADC enabled in the PDRUNCFG register and LPWRMODE bit set to 1 in the ADC CTRL register (ADC in low-power mode).
	-	79	190	Combined analog and digital logic. ADC enabled in the PDRUNCFG register and LPWRMODE bit set to 0 in the ADC CTRL register (ADC powered).
DAC 0	-	46	107	-
DAC 1	-	36	88	-
Capacitive Touch	-	49	117	-
DMA	-	355	858	-
CRC	-	36	83	-

12. Dynamic characteristics

12.1 Flash memory

Table 16. Flash characteristics

T_{amb} = −40 °C to +105 °C. Based on JEDEC NVM qualification. Failure rate < 10 ppm for parts as specified below.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
N_{endu}	endurance		[1]	10000	100000	-	cycles
t_{ret}	retention time	powered		10	20	-	years
		not powered		20	40	-	years
t_{er}	erase time	page or multiple consecutive pages, sector or multiple consecutive sectors		95	100	105	ms
t_{prog}	programming time		[2]	0.95	1	1.05	ms

[1] Number of program/erase cycles.

[2] Programming times are given for writing 64 bytes to the flash. T_{amb} <= +85 °C. Flash programming with IAP calls (see *LPC84x user manual*).

12.2 FRO

Table 17. Dynamic characteristic: FRO

T_{amb} = −40 °C to +105 °C; 1.8 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Min	Typ[1]	Max	Unit
FRO clock frequency; Condition: 0 °C ≤ T_{amb} ≤ 70 °C				
$f_{osc(RC)}$	18 -1 %	18	18 +1 %	MHz
$f_{osc(RC)}$	24 -1 %	24	24 +1 %	MHz
$f_{osc(RC)}$	30 -1 %	30	30 +1 %	MHz
FRO clock frequency; Condition: −20 °C ≤ T_{amb} ≤ 70 °C				
$f_{osc(RC)}$	18 -2 %	18	18 +1 %	MHz
$f_{osc(RC)}$	24 -2 %	24	24 +1 %	MHz
$f_{osc(RC)}$	30 -2 %	30	30 +1 %	MHz
FRO clock frequency; Condition: −40 °C ≤ T_{amb} ≤ 105 °C				
$f_{osc(RC)}$	18 -3.5 %	18	18 +2.5 %	MHz
$f_{osc(RC)}$	24 -3.5 %	24	24 +2.5 %	MHz
$f_{osc(RC)}$	30 -3.5 %	30	30 +2.5 %	MHz

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

12.8 USART interface

The actual USART bit rate depends on the delays introduced by the external trace, the external device, system clock (CCLK), and capacitive loading. Excluding delays introduced by external device and PCB, the maximum supported bit rate for USART master synchronous mode is 10 Mbit/s, and the maximum supported bit rate for USART slave synchronous mode is 10 Mbit/s.

Remark: USART functions can be assigned to all digital pins. The characteristics are valid for all digital pins except the open-drain pins PIO0_10 and PIO0_11.

Table 24. USART dynamic characteristics

T_{amb} = −40 °C to 105 °C; 1.8 V <= V_{DD} <= 3.6 V unless noted otherwise; C_L = 10 pF; input slew = 10 ns. Simulated parameters sampled at the 30 %/70 % level of the falling or rising edge; values guaranteed by design.

Symbol	Parameter	Conditions	Min	Max	Unit
USART master (in synchronous mode)					
$t_{su(D)}$	data input set-up time	3.0 V <= V_{DD} <= 3.6 V	31	-	ns
		1.8 V <= V_{DD} < 3.0 V	42		
$t_{h(D)}$	data input hold time		0	-	ns
$t_{v(Q)}$	data output valid time		0	7	ns
USART slave (in synchronous mode)					
$t_{su(D)}$	data input set-up time		5	-	ns
$t_{h(D)}$	data input hold time		5	-	ns
$t_{v(Q)}$	data output valid time	3.0 V <= V_{DD} <= 3.6 V	0	35	ns
		1.8 V <= V_{DD} < 3.0 V	0	46	ns

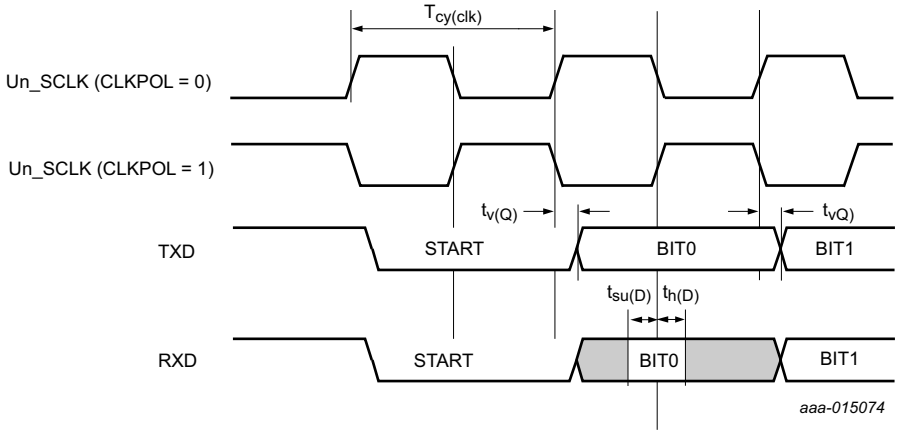


Fig 32. USART timing

14. Application information

14.1 Start-up behavior

Figure 36 shows the start-up timing after reset. The FRO 12 MHz oscillator provides the default clock at Reset and provides a clean system clock shortly after the supply pins reach operating voltage.

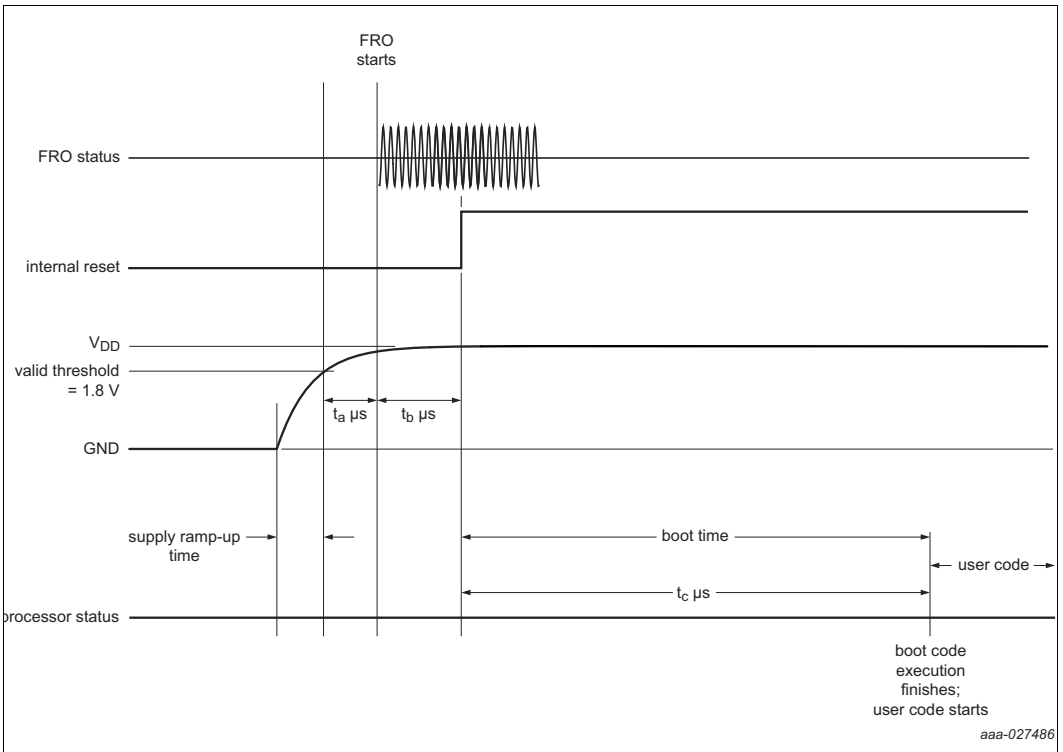


Fig 36. Start-up timing

Table 33. Typical start-up timing parameters

Parameter	Description	Value
t_a	FRO start time	≤ 26 µs
t_b	Internal reset de-asserted	101 µs
t_c	Boot time	51 µs

14.4 I/O power consumption

I/O pins are contributing to the overall dynamic and static power consumption of the part. If pins are configured as digital inputs, a static current can flow depending on the voltage level at the pin and the setting of the internal pull-up and pull-down resistors. This current can be calculated using the parameters R_{pu} and R_{pd} given in Table 15 for a given input voltage V_I. For pins set to output, the current drive strength is given by parameters I_{OH} and I_{OL} in Table 15, but for calculating the total static current, you also need to consider any external loads connected to the pin.

I/O pins also contribute to the dynamic power consumption when the pins are switching because the V_{DD} supply provides the current to charge and discharge all internal and external capacitive loads connected to the pin in addition to powering the I/O circuitry.

The contribution from the I/O switching current I_{sw} can be calculated as follows for any given switching frequency f_{sw} if the external capacitive load (C_{ext}) is known (see Table 15 for the internal I/O capacitance):

$$I_{sw} = V_{DD} \times f_{sw} \times (C_{io} + C_{ext})$$

14.5 Termination of unused pins

Table 34 shows how to terminate pins that are **not** used in the application. In many cases, unused pins may should be connected externally or configured correctly by software to minimize the overall power consumption of the part.

Unused pins with GPIO function should be configured as outputs set to LOW with their internal pull-up disabled. To configure a GPIO pin as output and drive it LOW, select the GPIO function in the IOCON register, select output in the GPIO DIR register, and write a 0 to the GPIO PORT register for that pin. Disable the pull-up in the pin's IOCON register.

In addition, it is recommended to configure all GPIO pins that are not bonded out on smaller packages as outputs driven LOW with their internal pull-up disabled.

Table 34. Termination of unused pins

Pin	Default state[1]	Recommended termination of unused pins
$\overline{\text{RESET}}$/PIO0_5	I; PU	In an application that does not use the $\overline{\text{RESET}}$ pin or its GPIO function, the termination of this pin depends on whether deep power-down mode is used: • Deep power-down used: Connect an external pull-up resistor and keep pin in default state (input, pull-up enabled) during all other power modes. • Deep power-down not used and no external pull-up connected: can be left unconnected if internal pull-up is disabled and pin is driven LOW and configured as output by software.
all PIOn_m (not open-drain)	I; PU	Can be left unconnected if driven LOW and configured as GPIO output with pull-up disabled by software.
PIOn_m (I2C open-drain)	IA	Can be left unconnected if driven LOW and configured as GPIO output by software.
VREFP	-	Tie to VDD.
VREFN	-	Tie to VSS.

[1] I = Input, O = Output, IA = Inactive (no pull-up/pull-down enabled), F = floating, PU = Pull-Up.

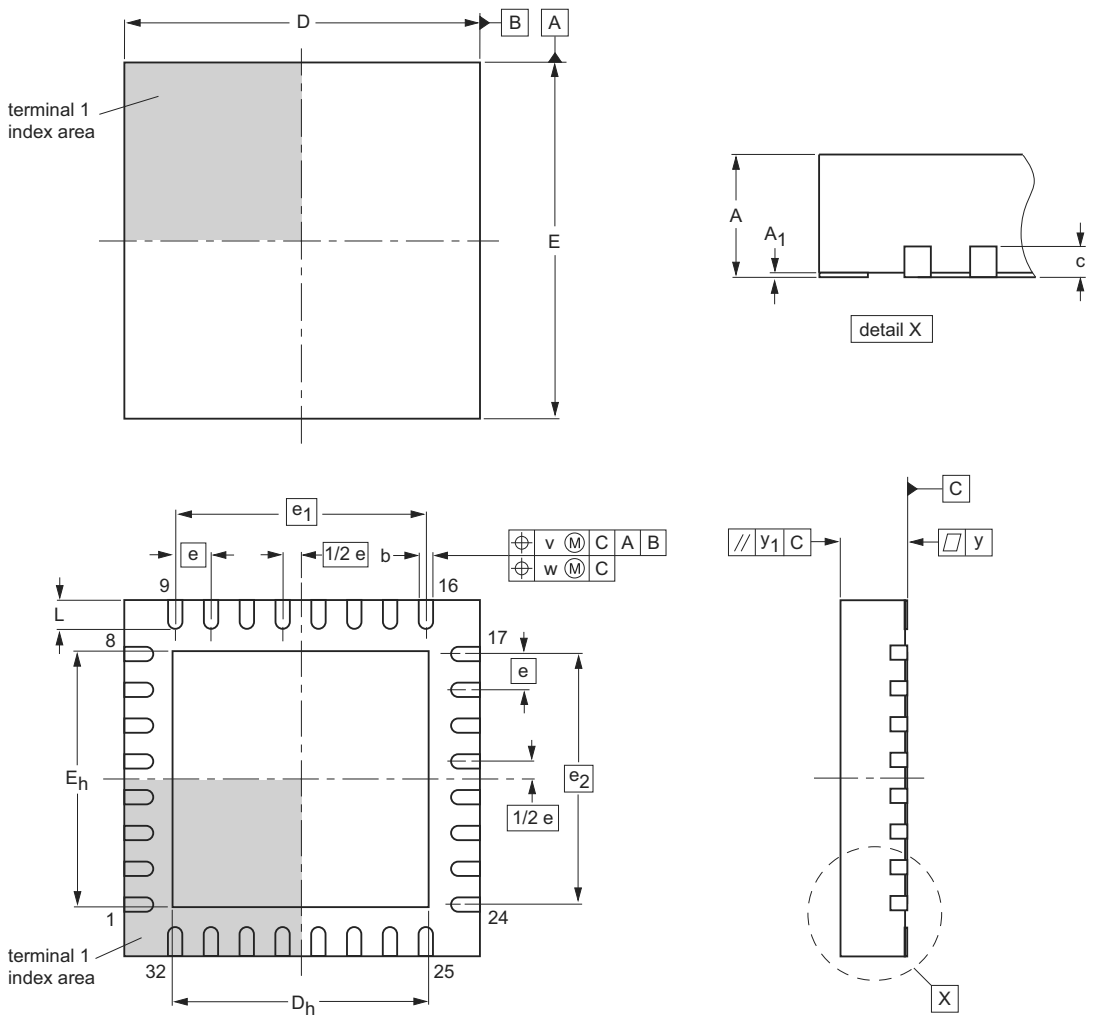
14.6 Pin states in different power modes

Table 35. Pin states in different power modes

Pin	Active	Sleep	Deep-sleep/power-down	Deep power-down
PIOn_m pins (not I2C)	As configured in the IOCON[1]. Default: internal pull-up enabled.			Floating.
Open-drain I2C-bus pins	As configured in the IOCON[1].			Floating.
$\overline{\text{RESET}}$	Reset function enabled. Default: input, internal pull-up enabled.			Reset function disabled; floating; if the part is in deep power-down mode, the $\overline{\text{RESET}}$ pin needs an external pull-up to reduce power consumption.
$\overline{\text{WAKEUP}}$	As configured in the IOCON[1]. $\overline{\text{WAKEUP}}$ function inactive.			Wake-up function enabled; can be disabled by software.

[1] Default and programmed pin states are retained in sleep, deep-sleep, and power-down modes.

HVQFN33: plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 x 5 x 0.85 mm



Dimensions (mm are the original dimensions)

Unit[1]		A[1]	A_1	b	c	D[1]	D_h	E[1]	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	max		0.05	0.30		5.1	3.75	5.1	3.75				0.5				
	nom	0.85			0.2					0.5	3.5	3.5		0.1	0.05	0.05	0.1
	min		0.00	0.18		4.9	3.45	4.9	3.45				0.3				

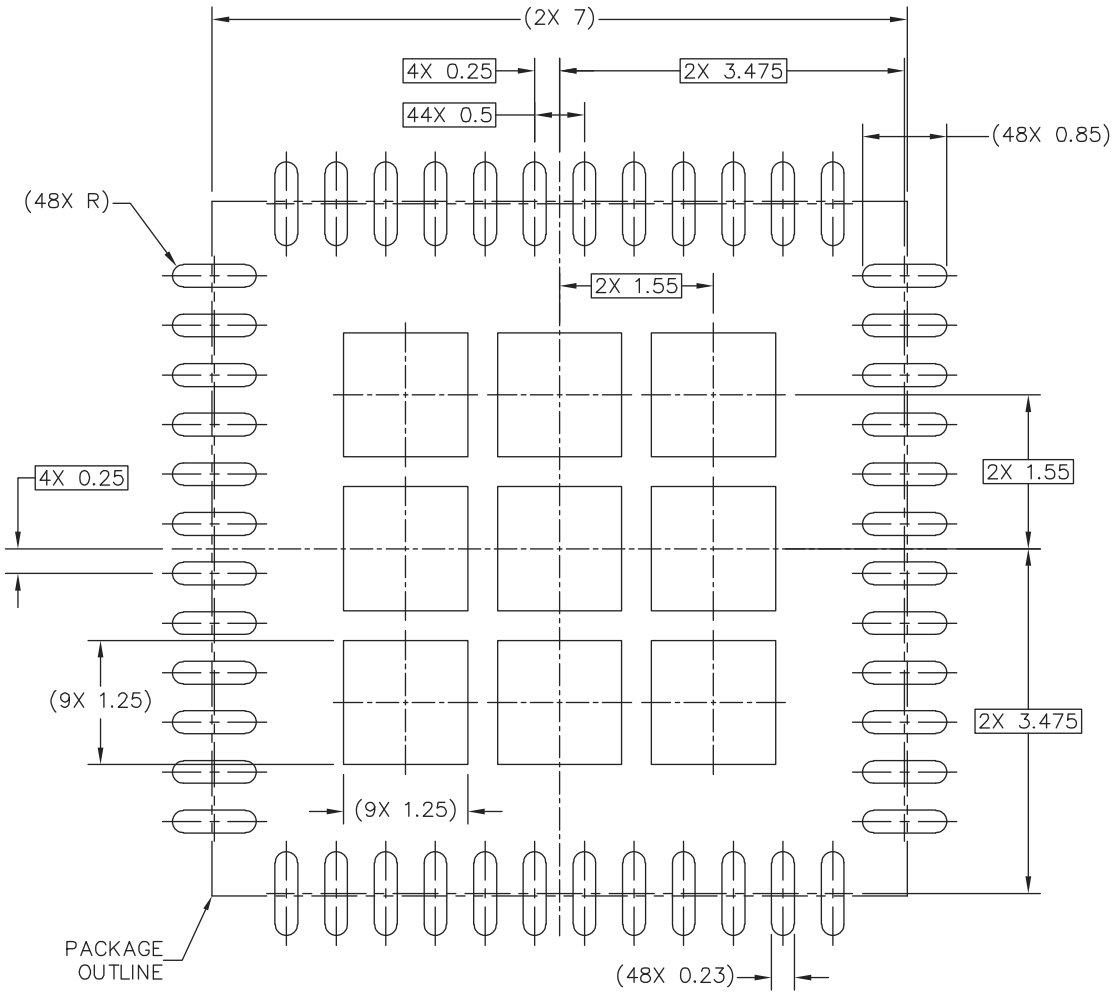
Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

hvqfn33f_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
		MO-220				~~11-10-11~~ 11-10-17

Fig 42. Package outline HVQFN33 (5 x 5 x 0.85 mm)



RECOMMENDED STENCIL THICKNESS 0.125

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

 DATE: 13 DEC 2017

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: SOT619–1	REVISION: 0	

Fig 48. Reflow soldering of the HVQFN48 package (7x7) 3 of 3