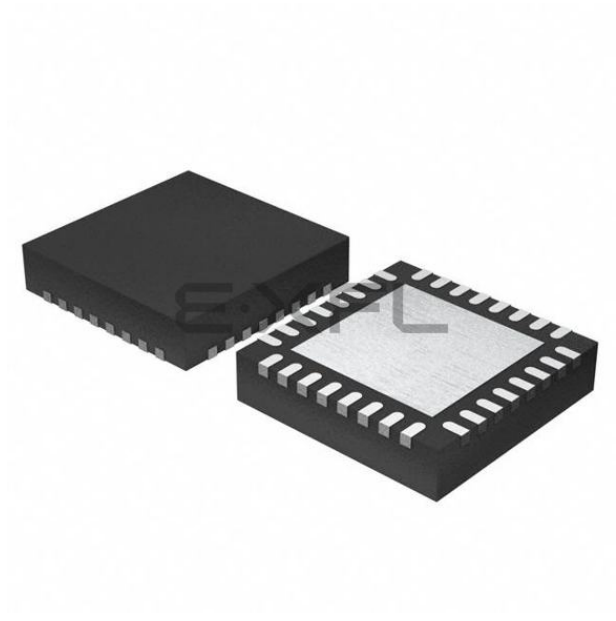

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	30MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, Cap Sense, DMA, POR, PWM, WDT
Number of I/O	29
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	External, Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-HVQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc844m201jhi33y

- Supports In-System Programming (ISP) through USART, SPI, and I^2C.
- FAIM API.
- FRO API.
- On-chip ROM APIs for integer divide.

- Digital peripherals:
  - High-speed GPIO interface connected to the Arm Cortex-M0+ I/O bus with up to 54 General-Purpose I/O (GPIO) pins with configurable pull-up/pull-down resistors, programmable open-drain mode, input inverter, and digital filter. GPIO direction control supports independent set/clear/toggle of individual bits.
  - High-current source output driver (20 mA) on four pins.
  - High-current sink driver (20 mA) on two true open-drain pins.
  - GPIO interrupt generation capability with boolean pattern-matching feature on eight GPIO inputs.
  - Switch matrix for flexible configuration of each I/O pin function.
  - CRC engine.
  - DMA with 25 channels and 13 trigger inputs.
  - Capacitive Touch Interface.
- Timers:
  - One SCTimer/PWM with five input and seven output functions (including capture and match) for timing and PWM applications. Inputs and outputs can be routed to or from external pins and internally to or from selected peripherals. Internally, the SCTimer/PWM supports 8 match/captures, 8 events, and 8 states.
  - One 32-bit general purpose counter/timer, with four match outputs and three capture inputs. Supports PWM mode, external count, and DMA.
  - Four channel Multi-Rate Timer (MRT) for repetitive interrupt generation at up to four programmable, fixed rates.
  - Self-Wake-up Timer (WKT) clocked from either Free Running Oscillator (FRO), a low-power, low-frequency internal oscillator, or an external clock input in the always-on power domain.
  - Windowed Watchdog timer (WWDT).
- Analog peripherals:
  - One 12-bit ADC with up to 12 input channels with multiple internal and external trigger inputs and with sample rates of up to 1.2 Msamples/s. The ADC supports two independent conversion sequences.
  - Comparator with five input pins and external or internal reference voltage.
  - Two 10-bit DACs.
- Serial peripherals:
  - Five USART interfaces with pin functions assigned through the switch matrix and two fractional baud rate generators.
  - Two SPI controllers with pin functions assigned through the switch matrix.
  - Four I^2C-bus interfaces. One I^2C supports Fast-mode Plus with 1 Mbit/s data rates on two true open-drain pins and listen mode. Three I^2Cs support data rates up to 400 kbit/s on standard digital pins.
- Clock generation:

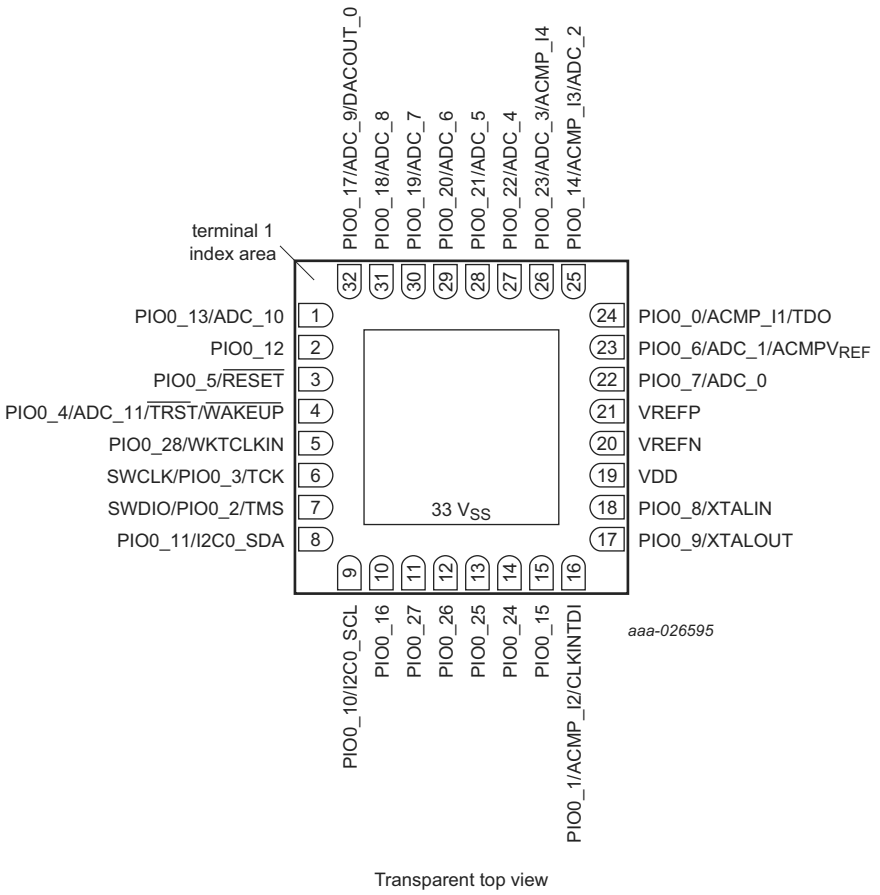


Fig 7. Pin configuration HVQFN33 package

7.2 Pin description

The pin description table shows the pin functions that are fixed to specific pins on each package. See Table 4. These fixed-pin functions are selectable through the switch matrix between GPIO and the comparator, ADC, SWD, RESET, and the XTAL pins. By default, the GPIO function is selected except on pins PIO0_2, PIO0_3, and PIO0_5. JTAG functions are available in boundary scan mode only.

Movable functions for the I^2C, USART, SPI, CTimer, SCT pins, and other peripherals can be assigned through the switch matrix to any pin that is not power or ground in place of the pin's fixed functions.

The following exceptions apply:

Do not assign more than one output to any pin. However, an output and/or one or more inputs can be assigned to a pin. Once any function is assigned to a pin, the pin's GPIO functionality is disabled.

Pin PIO0_4 triggers a wake-up from deep power-down mode. If the part must wake up from deep power-down mode via an external pin, do not assign any movable function to this pin.

The ADC includes a hardware threshold compare function with zero-crossing detection.

Remark: For best performance, select VREFP and VREFN at the same voltage levels as V_{DD} and V_{SS}. When selecting VREFP and VREFN different from VDD and VSS, ensure that the voltage midpoints are the same:

(VREFP-VREFN)/2 + VREFN = V_{DD}/2

8.24.1 Features

- 12-bit successive approximation analog to digital converter.
- 12-bit conversion rate of up to 1.2 MSamples/s.
- Two configurable conversion sequences with independent triggers.
- Optional automatic high/low threshold comparison and zero-crossing detection.
- Power-down mode and low-power operating mode.
- Measurement range VREFN to VREFP (not to exceed V_{DD} voltage level).
- Burst conversion mode for single or multiple inputs.
- Hardware calibration mode.

8.25 Digital-to-Analog Converter (DAC)

The DAC supports a resolution of 10 bits. Conversions can be triggered by an external pin input or an internal timer.

The DAC includes an optional automatic hardware shut-off feature which forces the DAC output voltage to zero while a HIGH level on the external DAC_SHUTOFF pin is detected.

8.25.1 Features

- 10-bit digital-to-analog converter.
- Supports DMA.
- Internal timer or pin external trigger for staged, jitter-free DAC conversion sequencing.
- Automatic hardware shut-off triggered by an external pin.

8.26 CRC engine

The Cyclic Redundancy Check (CRC) generator with programmable polynomial settings supports several CRC standards commonly used. To save system power and bus bandwidth, the CRC engine supports DMA transfers.

8.26.1 Features

- Supports three common polynomials CRC-CCITT, CRC-16, and CRC-32.
  - CRC-CCITT: $x^{16} + x^{12} + x^5 + 1$
  - CRC-16: $x^{16} + x^{15} + x^2 + 1$
  - CRC-32: $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$
- Bit order reverse and 1’s complement programmable setting for input data and CRC sum.
- Programmable seed number setting.

The internal low-power 10 kHz (± 40% accuracy) oscillator serves as the clock input to the WKT. This oscillator can be configured to run in all low-power modes.

8.27.2 Clock input

An external clock source can be supplied on the selected CLKIN pin directly to the PLL input. When selecting a clock signal for the CLKIN pin, follow the specifications for digital I/O pins in Table 13 “Static characteristics, supply pins” and Table 19 “Dynamic characteristics: I/O pins[1]”.

An 1.8 V external clock source can be supplied on the XTALIN pins to the system oscillator limiting the voltage of this signal (see Section 14.2 “XTAL oscillator”).

The maximum frequency for both clock signals is 25 MHz.

8.27.3 System PLL

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32. The CCO operates in the range of 156 MHz to 320 MHz, so there is an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider may be set to divide by 2, 4, 8, or 16 to produce the output clock. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip reset and may be enabled by software. The program must configure and activate the PLL, wait for the PLL to lock, and then connect to the PLL as a clock source. The PLL settling time is nominally 100 μs.

8.27.4 Clock output

The LPC84x features a clock output function that routes the FRO, the SysOsc, the watchdog oscillator, or the main clock to the CLKOUT function. The CLKOUT function can be connected to any digital pin through the switch matrix.

The LPC84x can be prevented from entering deep power-down mode by setting a lock bit in the PMU block. Locking out deep power-down mode enables the application to keep the watchdog timer or the BOD running at all times.

If the part must wake up from deep power-down mode via the $\overline{\text{WAKEUP}}$ pin or $\overline{\text{RESET}}$ pin, do not assign any movable function to this pin and must be externally pulled HIGH before entering deep power-down mode.

Table 7. Peripheral configuration in reduced power modes

Peripheral	Sleep mode	Deep-sleep mode	Power-down mode	Deep power-down mode
FRO	software configurable	on	off	off
FRO output	software configurable	off	off	off
Flash	software configurable	on	off	off
BOD	software configurable	software configurable	software configurable	off
PLL	software configurable	off	off	off
SysOsc	software configurable	off	off	off
WDosc/WWDT	software configurable	software configurable	software configurable	off
Digital peripherals	software configurable	off	off	off
WKT/low-power oscillator	software configurable	software configurable	software configurable	software configurable
ADC	software configurable	off	off	off
DAC0/1	software configurable	off	off	off
Capacitive Touch	software configurable	software configurable	software configurable	off
Comparator	software configurable	off	off	off

8.29 Emulation and debugging

Debug functions are integrated into the Arm Cortex-M0+. Serial wire debug functions are supported in addition to a standard JTAG boundary scan. The Arm Cortex-M0+ is configured to support up to four breakpoints and two watch points.

The Micro Trace Buffer is implemented on the LPC84x.

The $\overline{\text{RESET}}$ pin selects between the JTAG boundary scan ($\overline{\text{RESET}}$ = LOW) and the Arm SWD debug ($\overline{\text{RESET}}$ = HIGH). The Arm SWD debug port is disabled while the LPC84x is in reset. The JTAG boundary scan pins are selected by hardware when the part is in boundary scan mode (see Table 4).

To perform boundary scan testing, follow these steps:

1. Erase any user code residing in flash.
2. Power up the part with the $\overline{\text{RESET}}$ pin pulled HIGH externally.
3. Wait for at least 250 μs.
4. Pull the $\overline{\text{RESET}}$ pin LOW externally.
5. Perform boundary scan operations.
6. Once the boundary scan operations are completed, assert the $\overline{\text{TRST}}$ pin to enable the SWD debug mode, and release the $\overline{\text{RESET}}$ pin (pull HIGH).

Remark: The JTAG interface cannot be used for debug purposes.

11. Static characteristics

11.1 General operating conditions

Table 11. General operating conditions

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
f_{clk}	clock frequency	internal CPU/system clock		-	-	30	MHz
V_{DD}	supply voltage (core and external rail)		[3]	1.8	-	3.6	V
		FAIM programming only		3.0	-	3.6	V
		For ADC operations		2.4	-	3.6	V
		For DAC operations		2.7	-	3.6	V
V_{DDA}	analog supply voltage	For ADC operations		2.4	-	3.6	V
		For DAC operations		2.7	-	3.6	V
V_{ref}	ADC positive reference voltage	on pin VREFP		2.4	-	V_{DDA}	V
Oscillator pins							
$V_{i(xtal)}$	crystal input voltage	on pin XTALIN		−0.5	1.8	1.95	V
$V_{o(xtal)}$	crystal output voltage	on pin XTALOUT		−0.5	1.8	1.95	V
Pin capacitance							
C_{io}	input/output capacitance	pins with analog and digital functions	[2]	-	-	7.1	pF
		I^2C-bus pins	[2]	-	-	2.5	pF
		pins with digital functions only	[2]	-	-	2.8	pF

[1] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), nominal supply voltages.

[2] Including bonding pad capacitance. Based on simulation, not tested in production.

[3] The V_{DD} supply voltage must be 1.9 V or above when connecting an external crystal oscillator to the system oscillator. If the V_{DD} supply voltage is below 1.9 V, an external clock source can be fed to the XTALIN by bypassing the system oscillator or the other clock sources mentioned above can be used.

11.2 Power-up ramp conditions

Table 12. Power-up characteristics[1]

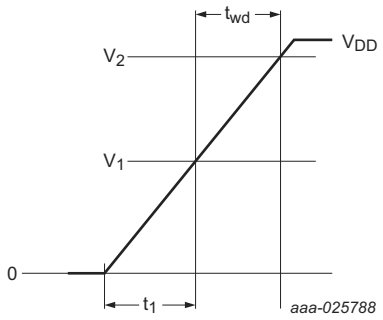
T_{amb} = −40 °C to +105 °C.

Symbol	Parameter		Min	Typ	Max	Unit
t_{wd}	Window duration (time where $V_1<V_{DD}<V_2$)		-	-	8	ms
V_1	Window low voltage	[2]	1.4	-	-	V
V_2	Window high voltage	[3]	-	-	1.8	V

[1] Assert the external reset pin until V_{DD} is > 1.8 V if the power-up characteristic specification cannot be implemented.

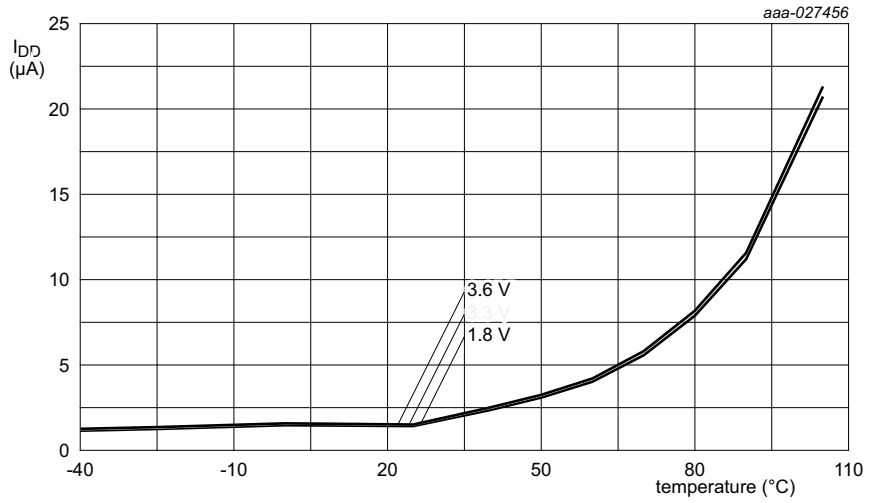
[2] V_{DD} to stay above V_1 for the entire duration t_{wd}.

[3] V_{DD} to stay below V_2 for the minimum duration of t_{wd}.



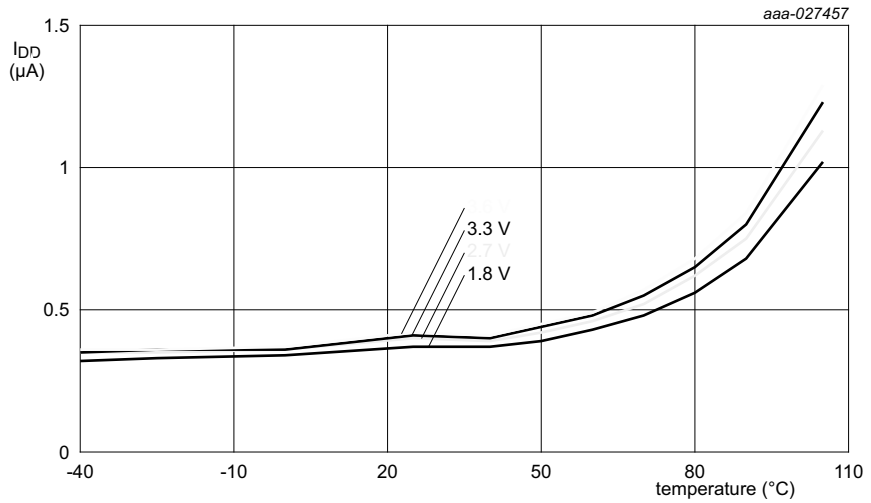
t_1: The time when there is no restriction on the ramp rate.

Fig 15. Power-up ramp



Conditions: BOD disabled; all oscillators and analog blocks disabled in the PDSLEEPCFG register (PDSLEEPCFG = 0x0000 18FF).

Fig 17. Power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}

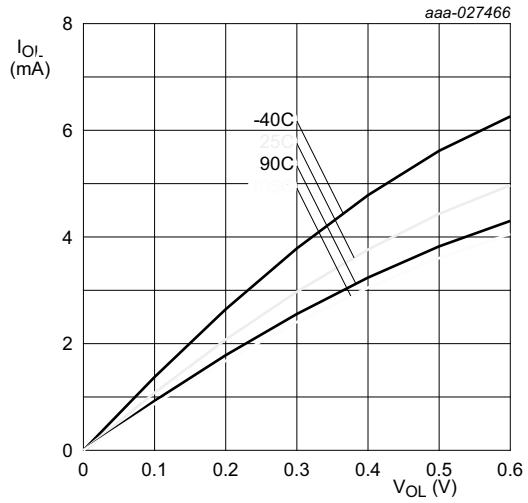


WKT not running.

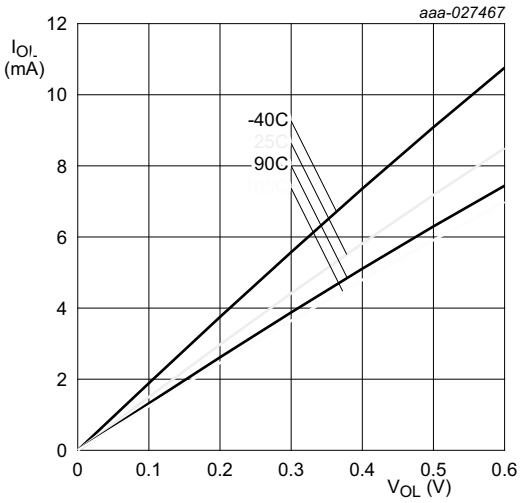
Fig 18. Deep power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}

Table 15. Static characteristics, pin characteristics *...continued*
T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{OZ}	OFF-state output current	V_O = 0 V; V_O = V_{DD}; on-chip pull-up/down resistors disabled		-	0.5	10[2]	nA
V_I	input voltage	$V_{DD} \geq$ 1.8 V		0	-	5.0	V
		V_{DD} = 0 V		0	-	3.6	V
V_O	output voltage	output active		0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage			0.7V_{DD}	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.3V_{DD}	V
V_{hys}	hysteresis voltage			-	0.4	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = 20 mA; 2.5 V <= V_{DD} < 3.6 V		V_{DD} − 0.5	-	-	V
		I_{OH} = 12 mA; 1.8 V <= V_{DD} < 2.5 V		V_{DD} − 0.5	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA 2.5 V <= V_{DD} < 3.6 V		-	-	0.5	V
		I_{OL} = 3 mA 1.8 V <= V_{DD} < 2.5 V		-	-	0.5	V
I_{OH}	HIGH-level output current	V_{OH} = V_{DD} − 0.5 V; 2.5 V <= V_{DD} < 3.6 V		20	-	-	mA
		V_{OH} = V_{DD} − 0.5 V; 1.8 V <= V_{DD} < 2.5 V		12	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.5 V 2.5 V ≤ V_{DD} ≤ 3.6 V		4	-	-	mA
		1.8 V ≤ V_{DD} < 2.5 V		3	-	-	mA
I_{OLS}	LOW-level short-circuit output current	V_{OL} = V_{DD}	[5]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V	[6]	10	50	150	µA
I_{pu}	pull-up current	V_I = 0 V	[6]	−10	−50	−85	µA
		V_{DD} < V_I < 5 V		0	0	0	µA
I^2C-bus pins (PIO0_10 and PIO0_11)							
V_{IH}	HIGH-level input voltage			0.7V_{DD}	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.3V_{DD}	V
V_{hys}	hysteresis voltage			-	0.05V_{DD}	-	V
I_{OL}	LOW-level output current	V_{OL} = 0.5 V; I^2C-bus pins configured as standard mode pins 2.5 V <= V_{DD} < 3.6 V		3.5	-	-	mA
		1.8 V <= V_{DD} < 2.5 V		3	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.5 V; I^2C-bus pins configured as Fast-mode Plus pins; 2.5 V <= V_{DD} < 3.6 V		20	-	-	mA
		1.8 V <= V_{DD} < 2.5 V		16	-	-	mA

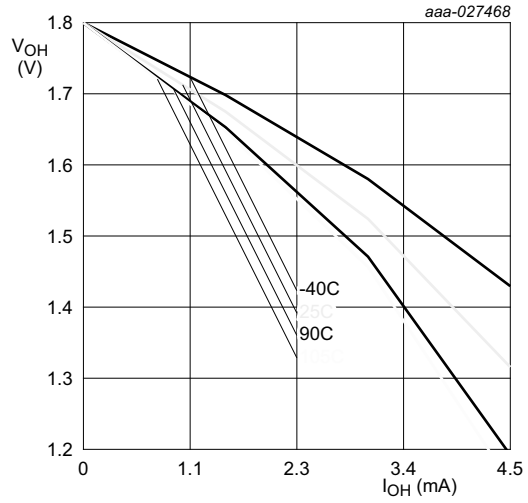


Conditions: V_{DD} = 1.8 V; standard port pins and high-drive pin PIO0_12.

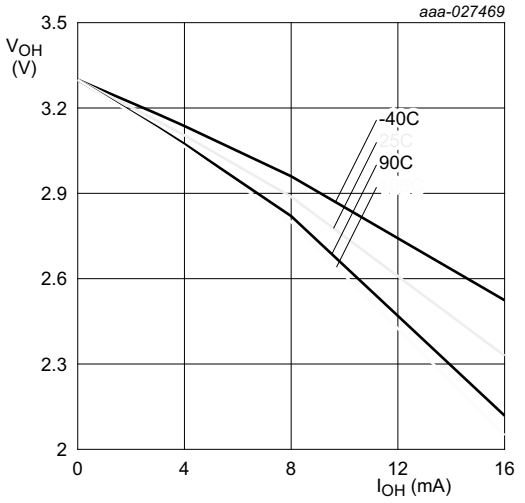


Conditions: V_{DD} = 3.3 V; standard port pins and high-drive pin PIO0_12.

Fig 25. Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}

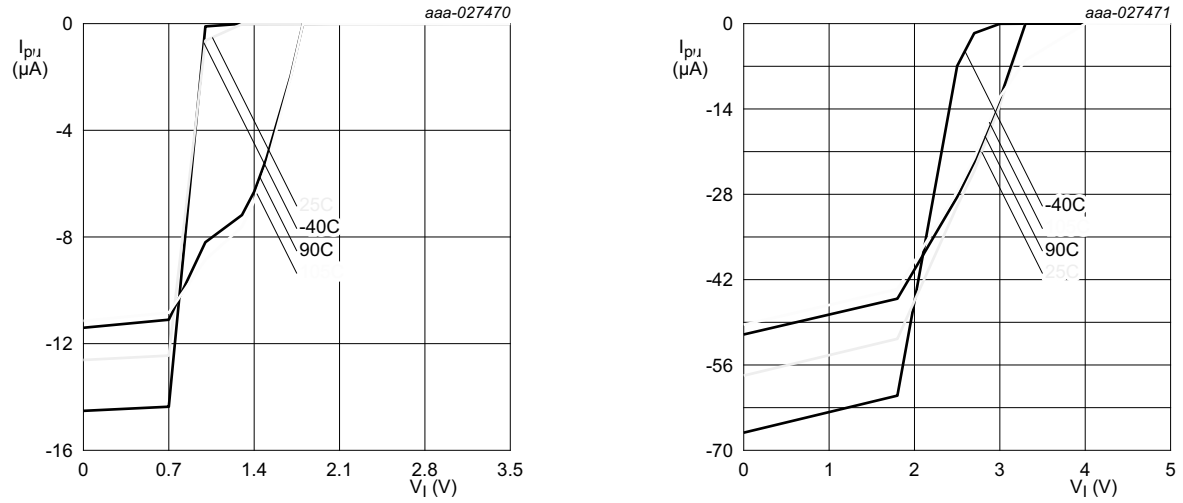


Conditions: V_{DD} = 1.8 V; standard port pins.



Conditions: V_{DD} = 3.3 V; standard port pins.

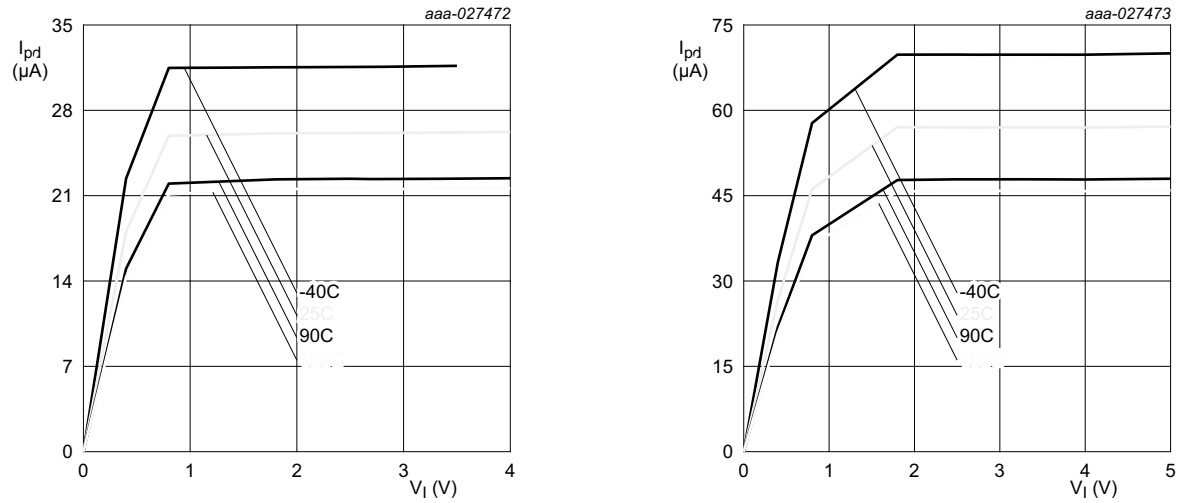
Fig 26. Typical HIGH-level output voltage V_{OH} versus HIGH-level output source current I_{OH}



Conditions: V_{DD} = 1.8 V; standard port pins.

Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 27. Typical pull-up current I_{PU} versus input voltage V_I



Conditions: V_{DD} = 1.8 V; standard port pins.

Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 28. Typical pull-down current I_{PD} versus input voltage V_I

13. Characteristics of analog peripherals

13.1 BOD

Table 26. BOD static characteristics[1]
T_{amb} = 25 °C.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{th}	threshold voltage	interrupt level 1					
		assertion		-	2.25	-	V
		de-assertion		-	2.38	-	V
		interrupt level 2					
		assertion		-	2.55	-	V
		de-assertion		-	2.66	-	V
		interrupt level 3					
		assertion		-	2.84	-	V
		de-assertion		-	2.92	-	V
		reset level 0					
		assertion		-	1.84	-	V
		de-assertion		-	1.97	-	V
		reset level 1					
		assertion		-	2.05	-	V
		de-assertion		-	2.18	-	V
		reset level 2					
		assertion		-	2.35	-	V
		de-assertion		-	2.47	-	V
		reset level 3					
		assertion		-	2.63	-	V
		de-assertion		-	2.76	-	V

[1] Interrupt levels are selected by writing the level value to the BOD control register BODCTRL, see *the* LPC84x *user manual*. Interrupt level 0 is reserved.

Table 29. Comparator characteristics *...continued*

T_{amb} = −40 °C to +105 °C unless noted otherwise; V_{DD} = 1.8 V to 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{PD}	propagation delay	HIGH to LOW; V_{DD} = 3.0 V; T_{amb} = 105 °C			150		
		V_{IC} = 0.1 V; 100 mV overdrive input	[1][2][4]	-		-	ns
		V_{IC} = 0.1 V; rail-to-rail input	[1][2]	-	250	-	ns
		V_{IC} = 1.5 V; 100 mV overdrive input	[1][2][4]	-	150	-	ns
		V_{IC} = 1.5 V; rail-to-rail input	[1][2]	-	170	-	ns
		V_{IC} = 2.9 V; 100 mV overdrive input	[1][2][4]	-	180	-	ns
		V_{IC} = 2.9 V; rail-to-rail input	[1][2]	-	70	-	ns
t_{PD}	propagation delay	LOW to HIGH; V_{DD} = 3.0 V; T_{amb} = 105 °C			260		
		V_{IC} = 0.1 V; 100 mV overdrive input	[1][2][4]	-		-	ns
		V_{IC} = 0.1 V; rail-to-rail input	[1][2]	-	90	-	ns
		V_{IC} = 1.5 V; 100 mV overdrive input	[1][2][4]	-	270	-	ns
		V_{IC} = 1.5 V; rail-to-rail input	[1][2]	-	220	-	ns
		V_{IC} = 2.9 V; 100 mV overdrive input	[1][2][4]	-	190	-	ns
		V_{IC} = 2.9 V; rail-to-rail input	[1][2]	-	700	-	ns
V_{hys}	hysteresis voltage	positive hysteresis; V_{DD} = 3.0 V; V_{IC} = 1.5 V; T_{amb} = 105 °C; settings:	[3]	-	6	-	
		5 mV					mV
		10 mV		-	12	-	mV
		20 mV		-	22	-	mV
V_{hys}	hysteresis voltage	negative hysteresis; V_{DD} = 3.0 V; V_{IC} = 1.5 V; T_{amb} = 105 °C; settings:	[1][3]		7		
		5 mV		-		-	mV
		10 mV		-	13	-	mV
		20 mV		-	23	-	mV
R_{lad}	ladder resistance	-		-	1	-	MΩ

[1] C_L = 10 pF

[2] Characterized on typical samples, not tested in production.

[3] Input hysteresis is relative to the reference input channel and is software programmable.

[4] 100 mV overdrive corresponds to a square wave from 50 mV below the reference (V_{IC}) to 50 mV above the reference.

Table 30. Comparator voltage ladder dynamic characteristics

T_{amb} = −40 °C to +105 °C; V_{DD} = 1.8 V to 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{s(pu)}$	power-up settling time	to 99% of voltage ladder output value	[1]	-	17	-	µs
$t_{s(sw)}$	switching settling time	to 99% of voltage ladder output value	[1]	-	18	-	µs

[1] Characterized on typical samples, not tested in production.

14.4 I/O power consumption

I/O pins are contributing to the overall dynamic and static power consumption of the part. If pins are configured as digital inputs, a static current can flow depending on the voltage level at the pin and the setting of the internal pull-up and pull-down resistors. This current can be calculated using the parameters R_{pu} and R_{pd} given in Table 15 for a given input voltage V_I. For pins set to output, the current drive strength is given by parameters I_{OH} and I_{OL} in Table 15, but for calculating the total static current, you also need to consider any external loads connected to the pin.

I/O pins also contribute to the dynamic power consumption when the pins are switching because the V_{DD} supply provides the current to charge and discharge all internal and external capacitive loads connected to the pin in addition to powering the I/O circuitry.

The contribution from the I/O switching current I_{sw} can be calculated as follows for any given switching frequency f_{sw} if the external capacitive load (C_{ext}) is known (see Table 15 for the internal I/O capacitance):

$$I_{sw} = V_{DD} \times f_{sw} \times (C_{io} + C_{ext})$$

14.5 Termination of unused pins

Table 34 shows how to terminate pins that are **not** used in the application. In many cases, unused pins may should be connected externally or configured correctly by software to minimize the overall power consumption of the part.

Unused pins with GPIO function should be configured as outputs set to LOW with their internal pull-up disabled. To configure a GPIO pin as output and drive it LOW, select the GPIO function in the IOCON register, select output in the GPIO DIR register, and write a 0 to the GPIO PORT register for that pin. Disable the pull-up in the pin's IOCON register.

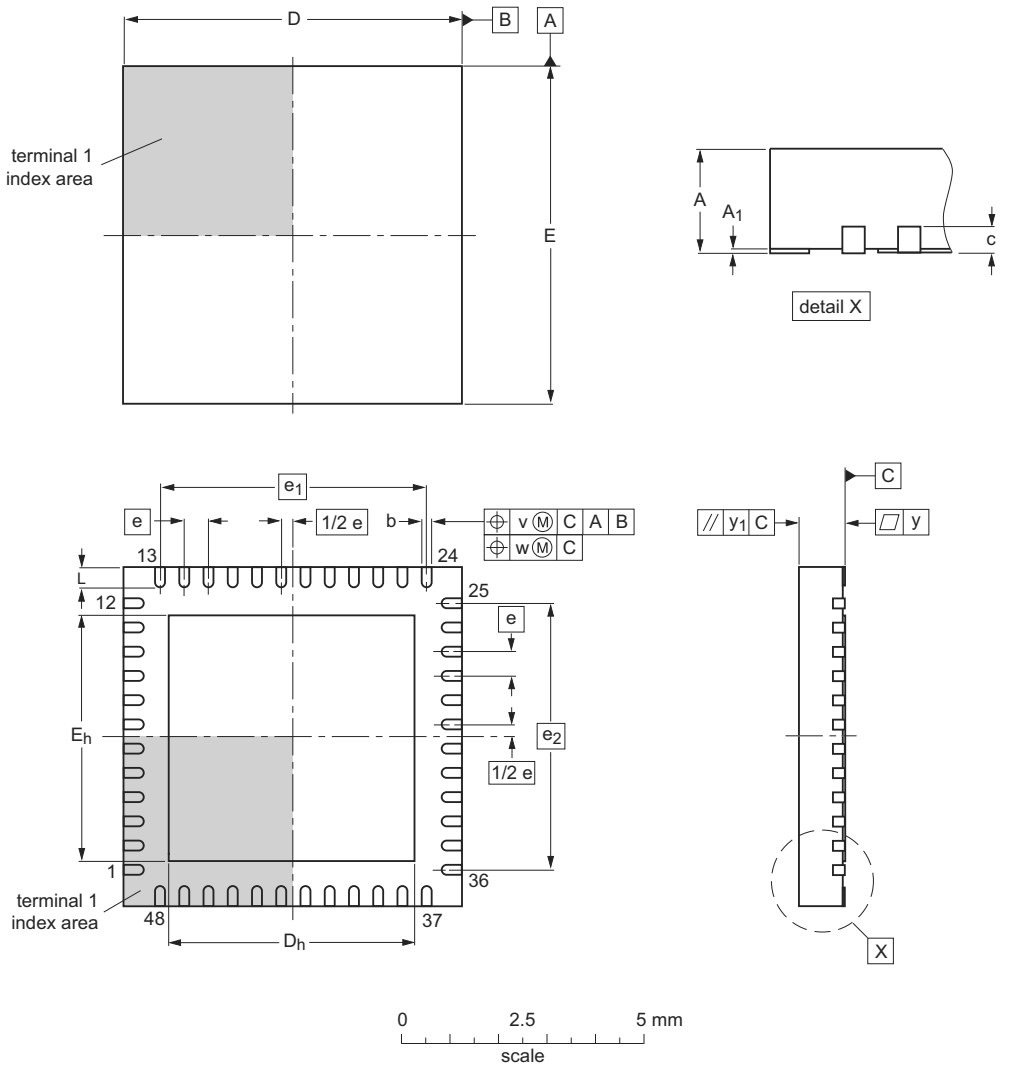
In addition, it is recommended to configure all GPIO pins that are not bonded out on smaller packages as outputs driven LOW with their internal pull-up disabled.

Table 34. Termination of unused pins

Pin	Default state[1]	Recommended termination of unused pins
$\overline{\text{RESET}}$/PIO0_5	I; PU	In an application that does not use the $\overline{\text{RESET}}$ pin or its GPIO function, the termination of this pin depends on whether deep power-down mode is used: • Deep power-down used: Connect an external pull-up resistor and keep pin in default state (input, pull-up enabled) during all other power modes. • Deep power-down not used and no external pull-up connected: can be left unconnected if internal pull-up is disabled and pin is driven LOW and configured as output by software.
all PIOn_m (not open-drain)	I; PU	Can be left unconnected if driven LOW and configured as GPIO output with pull-up disabled by software.
PIOn_m (I2C open-drain)	IA	Can be left unconnected if driven LOW and configured as GPIO output by software.
VREFP	-	Tie to VDD.
VREFN	-	Tie to VSS.

[1] I = Input, O = Output, IA = Inactive (no pull-up/pull-down enabled), F = floating, PU = Pull-Up.

HVQFN48: plastic thermal enhanced very thin quad flat package; no leads; 48 terminals; body 7 x 7 x 0.85 mm **SOT619-1**



Dimensions (mm are the original dimensions)

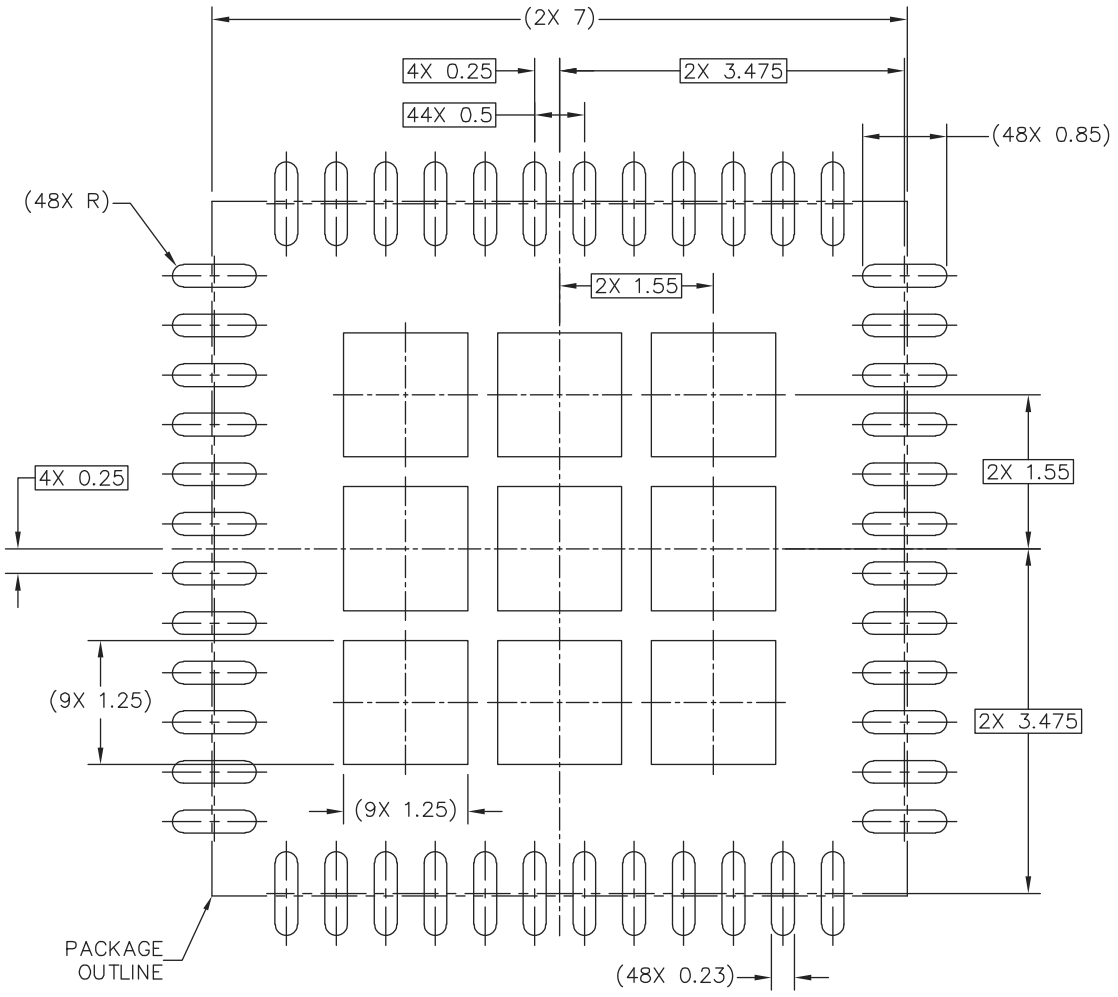
Unit[1]		A	A_1	b	C	D	D_h	E	E_h	e	e_1	e_2	L	v	w	y	y_1
	max	1.00	0.05	0.30		7.1	5.25	7.1	5.25				0.5				
mm	nom	0.85	0.02	0.21	0.2	7.0	5.10	7.0	5.10	0.5	5.5	5.5	0.4	0.1	0.05	0.05	0.1
	min	0.80	0.00	0.18		6.9	4.95	6.9	4.95				0.3				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included

sot619-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT619-1		MO-220				~~02-10-18~~ 12-11-22

Fig 43. Package outline HVQFN48 7 x 7x 0.85 mm (SOT619-1)



RECOMMENDED STENCIL THICKNESS 0.125

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

 DATE: 13 DEC 2017

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: SOT619–1	REVISION: 0	

Fig 48. Reflow soldering of the HVQFN48 package (7x7) 3 of 3

17. Abbreviations

Table 36. Abbreviations

Acronym	Description
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
BOD	BrownOut Detection
GPIO	General-Purpose Input/Output
PLL	Phase-Locked Loop
RC	Resistor-Capacitor
SPI	Serial Peripheral Interface
SMBus	System Management Bus
TEM	Transverse ElectroMagnetic
UART	Universal Asynchronous Receiver/Transmitter

18. References

[1] LPC84x User manual UM11029:

[2] LPC84x Errata sheet:

[3] I2C-bus specification *UM10204*.

[4] Technical note ADC design guidelines: http://www.nxp.com/documents/technical_note/TN00009.pdf

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