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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	30MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, Cap Sense, DMA, POR, PWM, WDT
Number of I/O	42
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	External, Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-HVQFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc844m201jhi48e

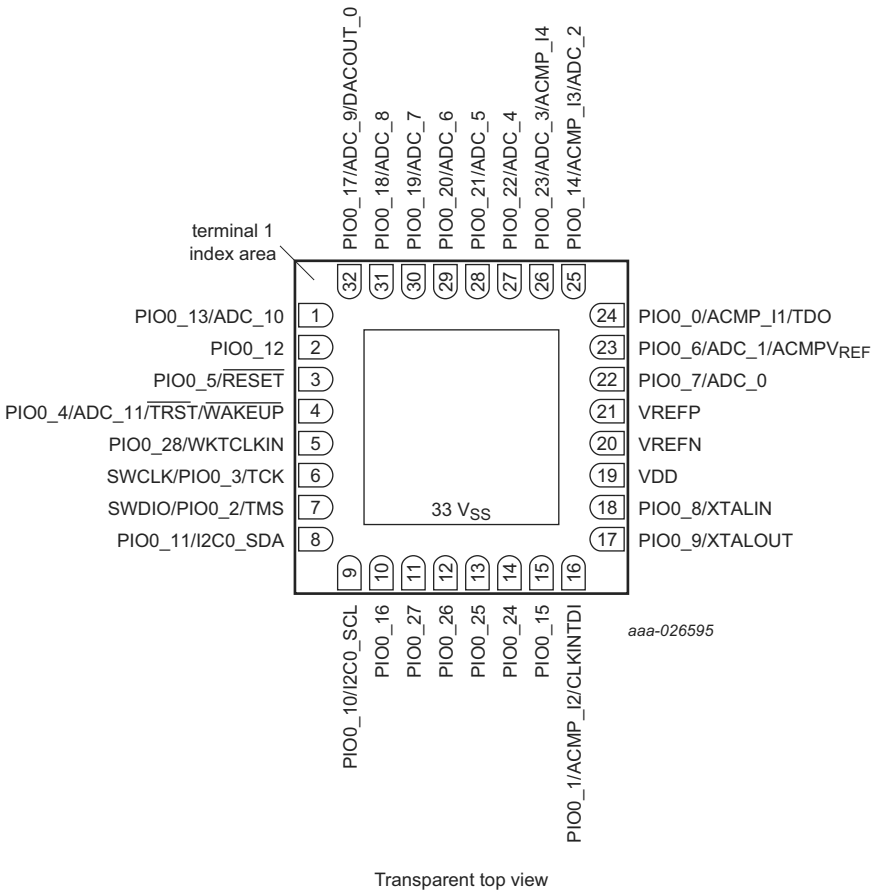


Fig 7. Pin configuration HVQFN33 package

7.2 Pin description

The pin description table shows the pin functions that are fixed to specific pins on each package. See Table 4. These fixed-pin functions are selectable through the switch matrix between GPIO and the comparator, ADC, SWD, RESET, and the XTAL pins. By default, the GPIO function is selected except on pins PIO0_2, PIO0_3, and PIO0_5. JTAG functions are available in boundary scan mode only.

Movable functions for the I^2C, USART, SPI, CTimer, SCT pins, and other peripherals can be assigned through the switch matrix to any pin that is not power or ground in place of the pin's fixed functions.

The following exceptions apply:

Do not assign more than one output to any pin. However, an output and/or one or more inputs can be assigned to a pin. Once any function is assigned to a pin, the pin's GPIO functionality is disabled.

Pin PIO0_4 triggers a wake-up from deep power-down mode. If the part must wake up from deep power-down mode via an external pin, do not assign any movable function to this pin.

Table 4. Pin description

Symbol	LQFP64	LQFP48	HVQFN48	HVQFN33		Reset state[1]	Type	Description
PIO0_31/CAPT_X0	13	9	9	-	[5]	I; PU	IO	**PIO0_31 —** General-purpose port 0 input/output 31.
								CAPT_X0 — Capacitive Touch X sensor 0.
PIO1_0/CAPT_X1	15	11	11	-	[5]	I; PU	IO	**PIO1_0 —** General-purpose port 1 input/output 0.
								CAPT_X1 — Capacitive Touch X sensor 1.
PIO1_1/CAPT_X2	18	14	14	-	[5]	I; PU	IO	**PIO1_1 —** General-purpose port 1 input/output 1.
								CAPT_X2 — Capacitive Touch X sensor 2.
PIO1_2/CAPT_X3	20	16	16	-	[5]	I; PU	IO	**PIO1_2 —** General-purpose port 1 input/output 2.
								CAPT_X3 — Capacitive Touch X sensor 3.
PIO1_3/CAPT_X4	29	21	21	-	[5]	I; PU	IO	**PIO1_3 —** General-purpose port 1 input/output 3.
								CAPT_X4 — Capacitive Touch X sensor 4.
PIO1_4/CAPT_X5	31	23	23	-	[5]	I; PU	IO	**PIO1_4 —** General-purpose port 1 input/output 4.
								CAPT_X5 — Capacitive Touch X sensor 5.
PIO1_5/CAPT_X6	35	27	27	-	[5]	I; PU	IO	**PIO1_5 —** General-purpose port 1 input/output 5.
								CAPT_X6 — Capacitive Touch X sensor 6.
PIO1_6/CAPT_X7	38	28	28	-	[5]	I; PU	IO	**PIO1_6 —** General-purpose port 1 input/output 6.
								CAPT_X7 — Capacitive Touch X sensor 7.
PIO1_7/CAPT_X8	47	35	35	-	[5]	I; PU	IO	**PIO1_7 —** General-purpose port 1 input/output 7.
								CAPT_X8 — Capacitive Touch X sensor 8.
PIO1_8/CAPT_YL	1	1	1	-	[5]	I; PU	IO	**PIO1_8 —** General-purpose port 1 input/output 8.
								CAPT_YL — Capacitive Touch Y Low.
PIO1_9/CAPT_YH	3	3	3	-	[5]	I; PU	IO	**PIO1_9 —** General-purpose port 1 input/output 9.
								CAPT_YH — Capacitive Touch Y High.
PIO1_10	64	-	-	-	[5]	I; PU	IO	**PIO1_10 —** General-purpose port 1 input/output 10.
PIO1_11	62	-	-	-	[5]	I; PU	IO	**PIO1_11 —** General-purpose port 1 input/output 11.
PIO1_12	9	-	-	-	[5]	I; PU	IO	**PIO1_12 —** General-purpose port 1 input/output 12.
PIO1_13	11	-	-	-	[5]	I; PU	IO	**PIO1_13 —** General-purpose port 1 input/output 13.
PIO1_14	22	-	-	-	[5]	I; PU	IO	**PIO1_14 —** General-purpose port 1 input/output 14.
PIO1_15	24	-	-	-	[5]	I; PU	IO	**PIO1_15 —** General-purpose port 1 input/output 15.
PIO1_16	36	-	-	-	[5]	I; PU	IO	**PIO1_16 —** General-purpose port 1 input/output 16.
PIO1_17	37	-	-	-	[5]	I; PU	IO	**PIO1_17 —** General-purpose port 1 input/output 17.
PIO1_18	43	-	-	-	[5]	I; PU	IO	**PIO1_18 —** General-purpose port 1 input/output 18.
PIO1_19	44	-	-	-	[5]	I; PU	IO	**PIO1_19 —** General-purpose port 1 input/output 19.
PIO1_20	56	-	-	-	[5]	I; PU	IO	**PIO1_20 —** General-purpose port 1 input/output 20.
PIO1_21	59	-	-	-	[5]	I; PU	IO	**PIO1_21 —** General-purpose port 1 input/output 21.
V_{DD}	7;26;39	29	29	19		-	-	Supply voltage for the I/O pad ring, the and core voltage regulator.
V_{DDA}	52	40	40					Analog supply voltage.
V_{SS}	8;25;40	30	30	33[11]		-	-	Ground.

Table 5. Movable functions (assign to pins PIO0_0 to PIO0_31, PIO1_0 to PIO1_21 through switch matrix)

Function name	Type	Description
SPIx_SSEL0	I/O	Slave select 0 for SPI0 and SPI1.
SPIx_SSEL1	I/O	Slave select 1 for SPI0 and SPI1.
SPIx_SSEL2	I/O	Slave select 2 for SPI0 and SPI1.
SPIx_SSEL3	I/O	Slave select 3 for SPI0 and SPI1.
SCT_PIN0	I	Pin input 0 to the SCT input multiplexer.
SCT_PIN1	I	Pin input 1 to the SCT input multiplexer.
SCT_PIN2	I	Pin input 2 to the SCT input multiplexer.
SCT_PIN3	I	Pin input 3 to the SCT input multiplexer.
SCT_OUT0	O	SCT output 0.
SCT_OUT1	O	SCT output 1.
SCT_OUT2	O	SCT output 2.
SCT_OUT3	O	SCT output 3.
SCT_OUT4	O	SCT output 4.
SCT_OUT5	O	SCT output 5.
I2Cx_SDA	I/O	I^2C1, I^2C2, and I^2C3 bus data input/output.
I2Cx_SCL	I/O	I^2C1, I^2C2, and I^2C3 bus clock input/output.
ACMP_O	O	Analog comparator output.
CLKOUT	O	Clock output.
GPIO_INT_BMAT	O	Output of the pattern match engine.
T0_MAT0	O	Timer Match channel 0.
T0_MAT1	O	Timer Match channel 1.
T0_MAT2	O	Timer Match channel 2.
T0_MAT3	O	Timer Match channel 3.
T0_CAP0	I	Timer Capture channel 0.
T0_CAP1	I	Timer Capture channel 1.
T0_CAP2	I	Timer Capture channel 2.

8.13.2 DMA trigger input MUX (TRIGMUX)

Each DMA trigger is connected to a programmable multiplexer which connects the trigger input to one of multiple trigger sources. Each multiplexer supports the same trigger sources: the ADC sequence interrupts, the SCT DMA request lines, and pin interrupts PININT0 and PININT1, and the outputs of the DMA triggers 0 and 1 for chaining DMA triggers.

8.14 USART0/1/2/3/4

All USART functions are movable functions and are assigned to pins through the switch matrix.

8.14.1 Features

- Maximum bit rates of 1.875 Mbit/s in asynchronous mode and 10 Mbit/s in synchronous mode for USART functions connected to all digital pins except the open-drain pins.
- 7, 8, or 9 data bits and 1 or 2 stop bits
- Synchronous mode with master or slave operation. Includes data phase selection and continuous clock option.
- Multiprocessor/multidrop (9-bit) mode with software address compare. (RS-485 possible with software address detection and transceiver direction control.)
- Parity generation and checking: odd, even, or none.
- One transmit and one receive data buffer.
- RTS/CTS for hardware signaling for automatic flow control. Software flow control can be performed using Delta CTS detect, Transmit Disable control, and any GPIO as an RTS output.
- Received data and status can optionally be read from a single register
- Break generation and detection.
- Receive data is 2 of 3 sample "voting". Status flag set when one sample differs.
- Built-in Baud Rate Generator.
- A fractional rate divider is shared among all UARTs.
- Interrupts available for Receiver Ready, Transmitter Ready, Receiver Idle, change in receiver break detect, Framing error, Parity error, Overrun, Underrun, Delta CTS detect, and receiver sample noise detected.
- Separate data and flow control loopback modes for testing.
- Baud rate clock can also be output in asynchronous mode.

8.15 SPI0/1

All SPI functions are movable functions and are assigned to pins through the switch matrix.

8.15.1 Features

- Maximum data rates of up to 30 Mbit/s in master mode and up to 18 Mbit/s in slave mode for SPI functions connected to all digital pins except the open-drain pins.

- Supports CPU PIO or DMA back-to-back transfer.
- Accept any size of data width per write: 8, 16 or 32-bit.
  - 8-bit write: 1-cycle operation.
  - 16-bit write: 2-cycle operation (8-bit x 2-cycle).
  - 32-bit write: 4-cycle operation (8-bit x 4-cycle).

8.27 Clocking and power control

8.27.1 Crystal and internal oscillators

The LPC84x include four independent oscillators:

1. The crystal oscillator (SysOsc) operating at frequencies between 1 MHz and 25 MHz.
2. Free Running Oscillator.
3. Watchdog Oscillator
4. Low Power Oscillator

Each oscillator, except the low-frequency oscillator, can be used for more than one purpose as required in a particular application.

Following reset, the LPC84x operates from the FRO until switched by software allowing the part to run without any external crystal and the bootloader code to operate at a known frequency.

See Figure 11 for an overview of the LPC84x clock generation.

8.27.1.1 Free Running Oscillator (FRO)

The FRO oscillator provides the default clock at reset and provides a clean system clock shortly after the supply pins reach operating voltage.

- This oscillator provides a selectable 18 MHz, 24 MHz, and 30 MHz outputs that can be used as a system clock. Also, these outputs can be divided down to 1.125 MHz, 1.5 MHz, 1.875 MHz, 9 MHz, 12 MHz, and 15 MHz for system clock.
- The FRO is trimmed to ±1 % accuracy over the entire voltage and temperature range of 0 C to 70 C.
- By default, the fro_oscout is 24 MHz and is divided by 2 to provide a default system (CPU) clock frequency of 12 MHz.

8.27.1.2 Crystal Oscillator (SysOsc)

The crystal oscillator can be used as the clock source for the CPU, with or without using the PLL.

The SysOsc operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the system PLL.

8.27.1.3 Internal Low-power Oscillator and Watchdog Oscillator (WDOsc)

The nominal frequency of the WDOsc is programmable between 9.4 kHz and 2.3 MHz. The frequency spread over silicon process variations is ± 40%.

The WDOsc is a dedicated oscillator for the windowed WWDT.

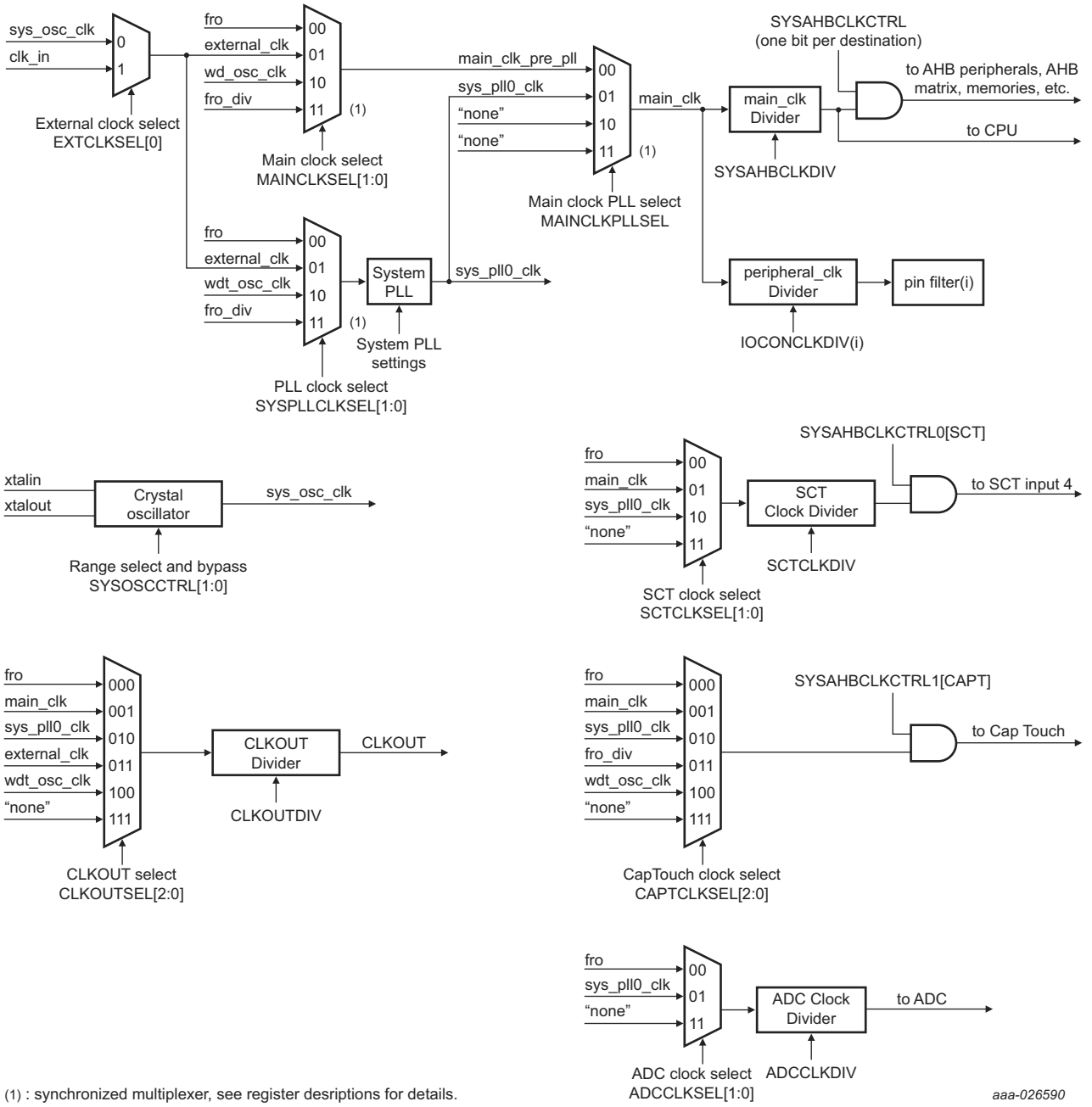


Fig 11. LPC84x clock generation

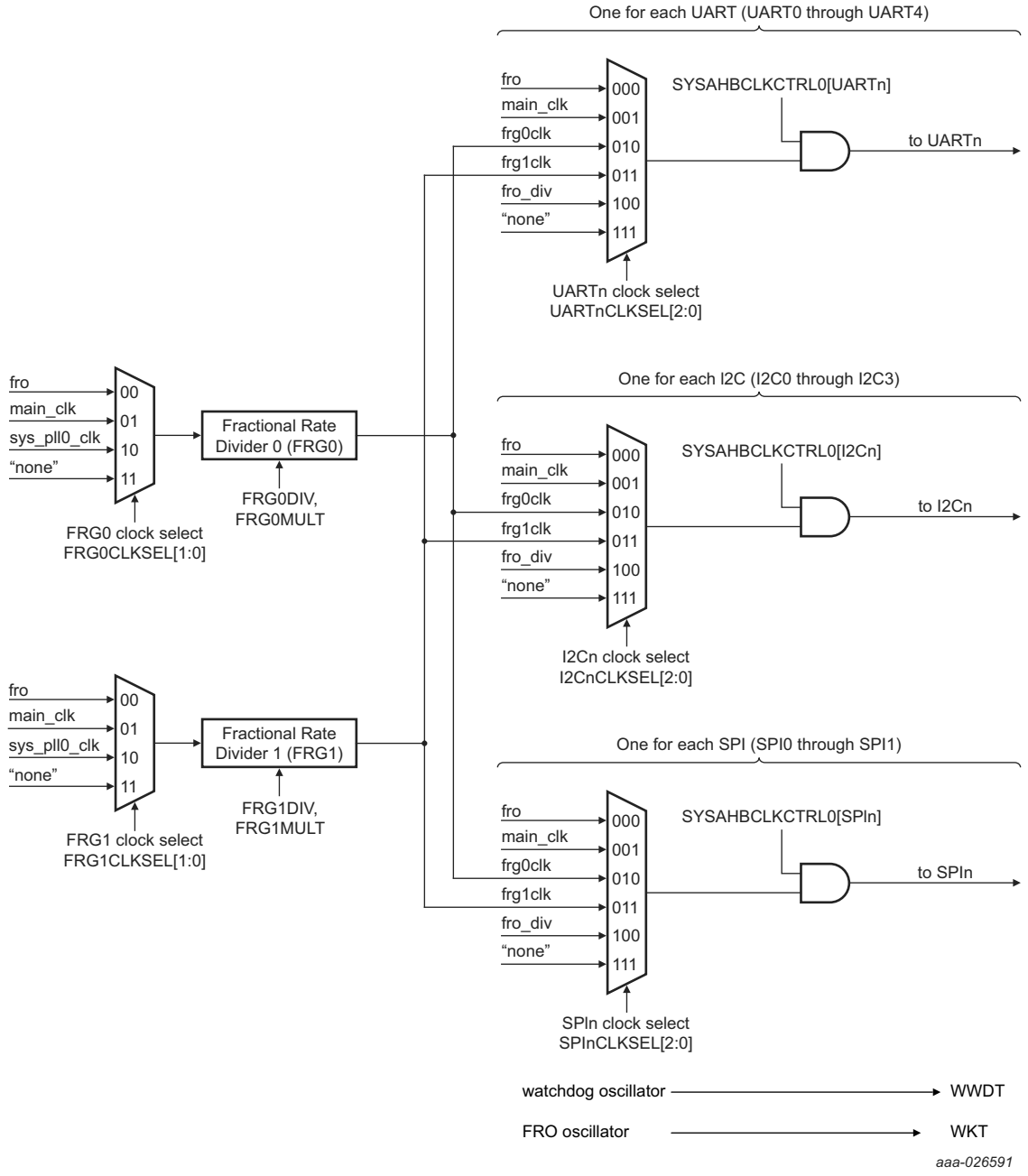


Fig 12. LPC84x clock generation (continued)

8.27.5.1 Sleep mode

When sleep mode is entered, the clock to the core is stopped. Resumption from the sleep mode does not need any special sequence but re-enabling the clock to the Arm core.

In sleep mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during sleep mode and may generate interrupts to cause the processor to resume execution. sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, and internal buses.

8.27.5.2 Deep-sleep mode

In deep-sleep mode, the LPC84x core is in sleep mode and all peripheral clocks and all clock sources are off except for the FRO and watchdog oscillator or low-power oscillator if selected. The FRO output is disabled. In addition, all analog blocks are shut down and the flash is in standby mode. In deep-sleep mode, the application can keep the watchdog oscillator and the BOD circuit running for self-timed wake-up and BOD protection.

The LPC84x can wake up from deep-sleep mode via a reset, digital pins selected as inputs to the pin interrupt block, a watchdog timer interrupt, an interrupt from Capacitive Touch, or an interrupt from the USART (if the USART is configured in synchronous slave mode), the SPI, or the I2C blocks (in slave mode).

Any interrupt used for waking up from deep-sleep mode must be enabled in one of the SYSCON wake-up enable registers and the NVIC.

Deep-sleep mode saves power and allows for short wake-up times.

8.27.5.3 Power-down mode

In power-down mode, the LPC84x is in sleep mode and all peripheral clocks and all clock sources are off except for watchdog oscillator or low-power oscillator if selected. In addition, all analog blocks and the flash are shut down. In power-down mode, the application can keep the watchdog oscillator and the BOD circuit running for self-timed wake-up and BOD protection.

The LPC84x can wake up from power-down mode via a reset, digital pins selected as inputs to the pin interrupt block, a watchdog timer interrupt, an interrupt from Capacitive Touch, or an interrupt from the USART (if the USART is configured in synchronous slave mode), the SPI, or the I2C blocks (in slave mode).

Any interrupt used for waking up from power-down mode must be enabled in one of the SYSCON wake-up enable registers and the NVIC.

Power-down mode reduces power consumption compared to deep-sleep mode at the expense of longer wake-up times.

8.27.5.4 Deep power-down mode

In deep power-down mode, power is shut off to the entire chip except for the $\overline{\text{WAKEUP}}$ pin and the self-wake-up timer. The LPC84x can wake up from deep power-down mode via the $\overline{\text{WAKEUP}}$ pin, $\overline{\text{RESET}}$ pin, or without an external signal by using the time-out of the self-wake-up timer (see Section 8.22).

8.28.3 Code security (Code Read Protection - CRP)

CRP provides different levels of security in the system so that access to the on-chip flash and use of the Serial Wire Debugger (SWD) and In-System Programming (ISP) can be restricted. Programming a specific pattern into a dedicated flash location invokes CRP. IAP commands are not affected by the CRP.

In addition, ISP entry via the ISP entry pin can be disabled without enabling CRP. For details, see the *LPC84x user manual*.

There are three levels of Code Read Protection:

1. CRP1 disables access to the chip via the SWD and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors cannot be erased.
2. CRP2 disables access to the chip via the SWD and only allows full flash erase and update using a reduced set of the ISP commands.
3. Running an application with level CRP3 selected, fully disables any access to the chip via the SWD pins and the ISP. This mode effectively disables ISP override using the ISP entry pin as well. If necessary, the application must provide a flash update mechanism using IAP calls or using a call to the reinvoke ISP command to enable flash update via the USART.

CAUTION	
	If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

In addition to the three CRP levels, sampling of the ISP entry pin for valid user code can be disabled. For details, see the *LPC84x user manual*.

8.28.4 APB interface

The APB peripherals are located on one APB bus.

8.28.5 AHBLite

The AHBLite connects the CPU bus of the Arm Cortex-M0+ to the flash memory, the main static RAM, the CRC, the DMA, the ROM, and the APB peripherals.

9. Limiting values

Table 9. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage (core and external rail)		[2]	−0.5	+4.6	V
V_{DDA}	Analog supply voltage	on pin VDDA		−0.5	+4.6	V
V_{ref}	reference voltage	on pin VREFP		−0.5	V_{DD}	V
V_I	input voltage	5 V tolerant I/O pins; $V_{DD} \geq 1.8$ V	[3][4]	−0.5	+5.5	V
		on I2C open-drain pins	[5]	−0.5	+5.5	V
		3 V tolerant I/O pin $ACMPV_{REF}$	[6]	−0.5	+3.6	V
V_{IA}	analog input voltage	on digital pins configured for an analog function	[7][8] [9]	−0.5	+4.6	V
$V_{i(xtal)}$	crystal input voltage		[2]	−0.5	+2.5	V
I_{DD}	supply current	per supply pin (LQFP64)		-	100	mA
		per supply pin (LQFP48, HVQFN48)		-	75	
		per supply pin (HVQFN33)		-	50	
I_{SS}	ground current	per ground pin (LQFP64);		-	100	mA
		per ground pin (LQFP48, HVQFN48)		-	75	
		per ground pin (HVQFN33)		-	100	
I_{latch}	I/O latch-up current	$-(0.5V_{DD}) < V_I < (1.5V_{DD})$; $T_j < 125$ °C		-	100	mA
T_{stg}	storage temperature		[10]	−65	+150	°C
$T_{j(max)}$	maximum junction temperature			-	150	°C

[3] I_{DD} measurements were performed with all pins configured as GPIO outputs driven LOW and pull-up resistors disabled.

[4] FRO enabled; system oscillator disabled; system PLL disabled.

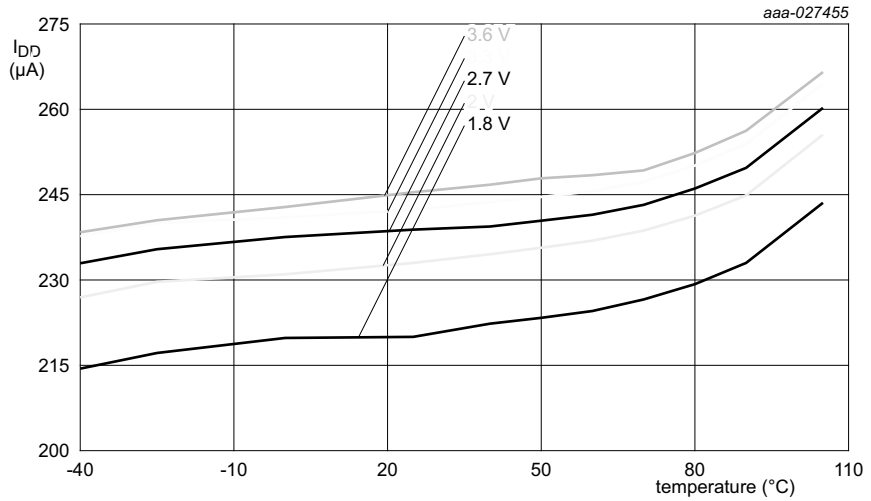
[5] BOD disabled.

[6] All peripherals disabled in the SYSAHBCLKCTRL register. Peripheral clocks disabled in system configuration block.

[7] All oscillators and analog blocks turned off.

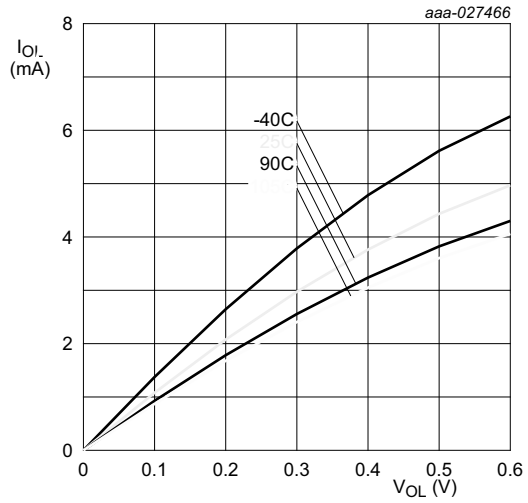
[8] $\overline{\text{WAKEUP}}$ pin pulled HIGH externally.

[9] Tested in production, VDD = 3.6 V.

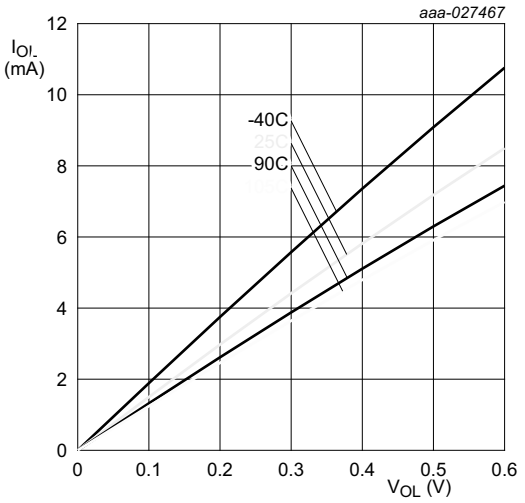


Conditions: BOD disabled; all oscillators and analog blocks disabled in the PDSLEEPCFG register (PDSLEEPCFG = 0x0000 18FF).

Fig 16. Deep-sleep mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}

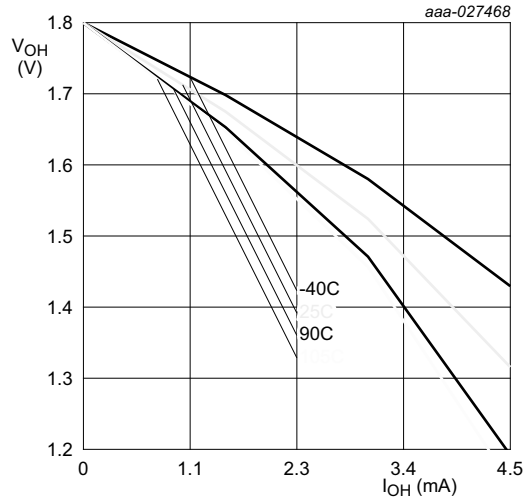


Conditions: V_{DD} = 1.8 V; standard port pins and high-drive pin PIO0_12.

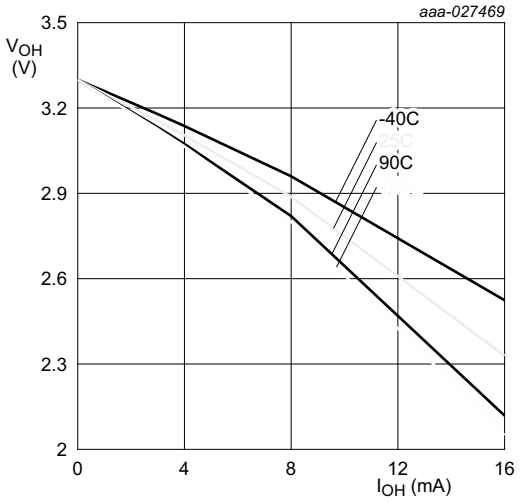


Conditions: V_{DD} = 3.3 V; standard port pins and high-drive pin PIO0_12.

Fig 25. Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}



Conditions: V_{DD} = 1.8 V; standard port pins.



Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 26. Typical HIGH-level output voltage V_{OH} versus HIGH-level output source current I_{OH}

14. Application information

14.1 Start-up behavior

Figure 36 shows the start-up timing after reset. The FRO 12 MHz oscillator provides the default clock at Reset and provides a clean system clock shortly after the supply pins reach operating voltage.

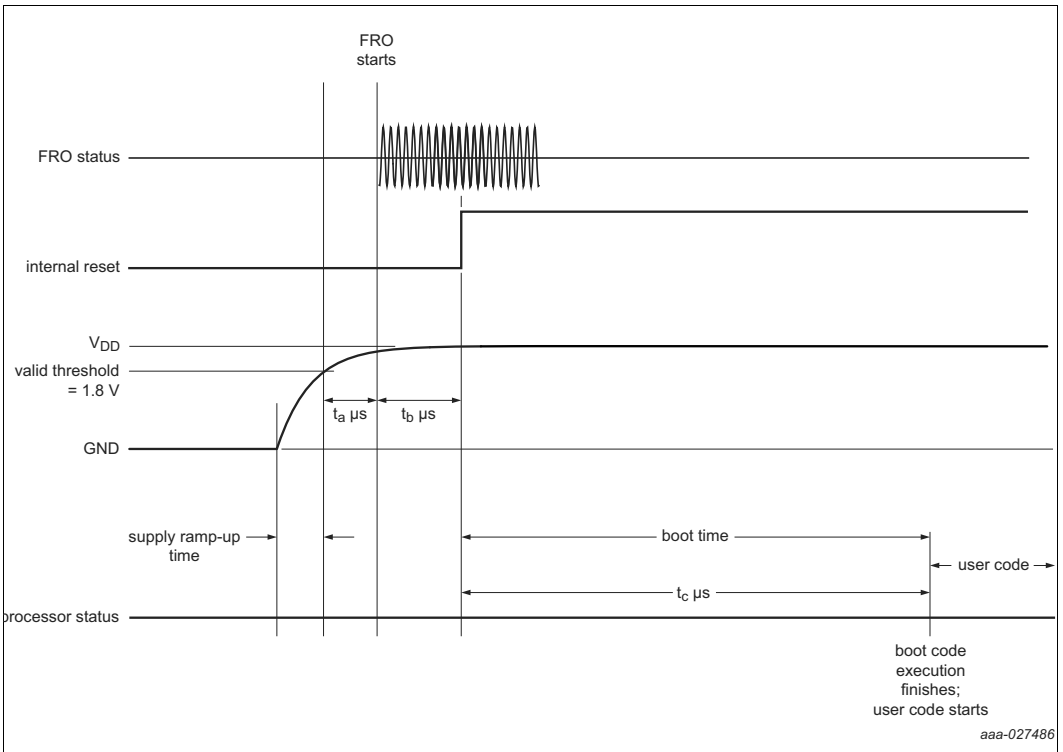


Fig 36. Start-up timing

Table 33. Typical start-up timing parameters

Parameter	Description	Value
t_a	FRO start time	≤ 26 µs
t_b	Internal reset de-asserted	101 µs
t_c	Boot time	51 µs

14.2 XTAL oscillator

In the XTAL oscillator circuit, only the crystal (XTAL) and the capacitances C_{X1} and C_{X2} need to be connected externally on XTALIN and XTALOUT. See Figure 37.

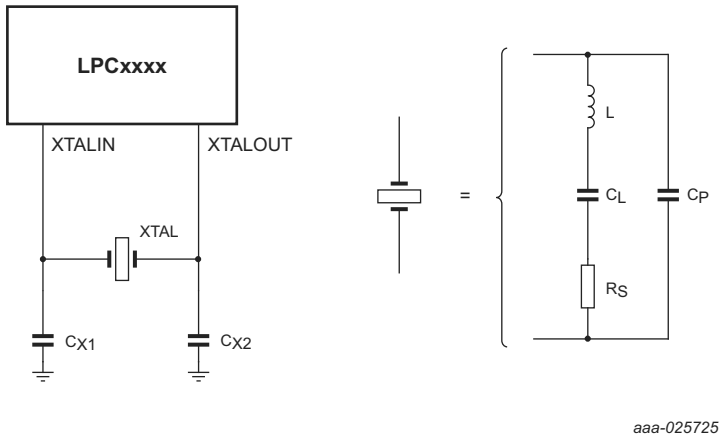


Fig 37. XTAL oscillator components

For best results, it is very critical to select a matching crystal for the on-chip oscillator. Load capacitance (CL), series resistance (RS), and drive level (DL) are important parameters to consider while choosing the crystal. After selecting the proper crystal, the external load capacitor C_{X1} and C_{X2} values can also be generally determined by the following expression:

$$C_{X1} = C_{X2} = 2C_L - (C_{Pad} + C_{Parasitic})$$

Where:

C_L - Crystal load capacitance

C_{Pad} - Pad capacitance of the XTALIN and XTALOUT pins (~3 pF).

$C_{Parasitic}$ – Parasitic or stray capacitance of external circuit.

Although $C_{Parasitic}$ can be ignored in general, the actual board layout and placement of external components influences the optimal values of external load capacitors. Therefore, it is recommended to fine tune the values of external load capacitors on actual hardware board to get the accurate clock frequency. For fine tuning, measure the clock on the XTALOUT pin and optimize the values of external load capacitors for minimum frequency deviation.

14.2.1 XTAL Printed Circuit Board (PCB) design guidelines

- Connect the crystal and external load capacitors on the PCB as close as possible to the oscillator input and output pins of the chip.
- The length of traces in the oscillation circuit should be as short as possible and must not cross other signal lines.
- Ensure that the load capacitors CX1, CX2, and CX3, in case of third overtone crystal usage, have a common ground plane.
- Loops must be made as small as possible to minimize the noise coupled in through the PCB and to keep the parasitics as small as possible.
- Lay out the ground (GND) pattern under crystal unit.
- Do not lay out other signal lines under crystal unit for multi-layered PCB.

14.2.2 XTAL input

The input voltage to the on-chip oscillators is limited to 1.95 V. If the oscillator is driven by a clock in slave mode, it is recommended to couple the input through a capacitor with C_i = 100 pF. To limit the input voltage to the specified range, choose an additional capacitor to ground C_g which attenuates the input voltage by a factor $C_i/(C_i + C_g)$. In slave mode, a minimum of 200 mV(RMS) is needed.

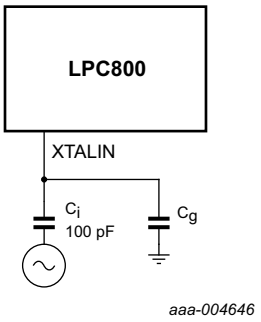


Fig 38. Slave mode operation of the on-chip oscillator

In slave mode the input clock signal should be coupled with a capacitor of 100 pF (Figure 38), with an amplitude between 200 mV (RMS) and 1000 mV (RMS). This corresponds to a square wave signal with a signal swing of between 280 mV and 1.4 V. The XTALOUT pin in this configuration can be left unconnected.

14.3 Connecting power, clocks, and debug functions

Figure 39 shows the basic board connections used to power the LPC84x, connect the external crystal, and provide debug capabilities via the serial wire port.

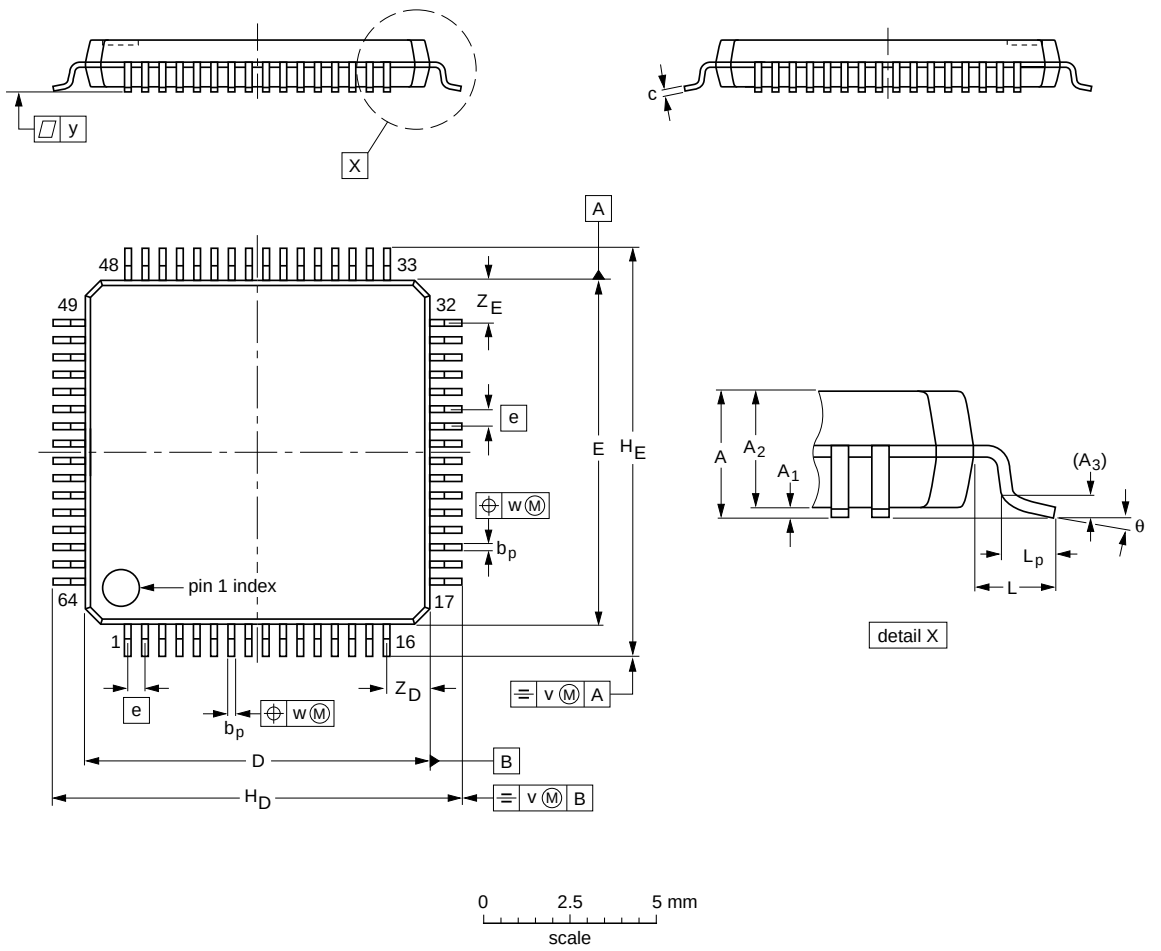
14.6 Pin states in different power modes

Table 35. Pin states in different power modes

Pin	Active	Sleep	Deep-sleep/power-down	Deep power-down
PIOn_m pins (not I2C)	As configured in the IOCON[1]. Default: internal pull-up enabled.			Floating.
Open-drain I2C-bus pins	As configured in the IOCON[1].			Floating.
$\overline{\text{RESET}}$	Reset function enabled. Default: input, internal pull-up enabled.			Reset function disabled; floating; if the part is in deep power-down mode, the $\overline{\text{RESET}}$ pin needs an external pull-up to reduce power consumption.
$\overline{\text{WAKEUP}}$	As configured in the IOCON[1]. $\overline{\text{WAKEUP}}$ function inactive.			Wake-up function enabled; can be disabled by software.

[1] Default and programmed pin states are retained in sleep, deep-sleep, and power-down modes.

LQFP64: plastic low profile quad flat package; 64 leads; body 10 x 10 x 1.4 mm **SOT314-2**



DIMENSIONS (mm are the original dimensions)

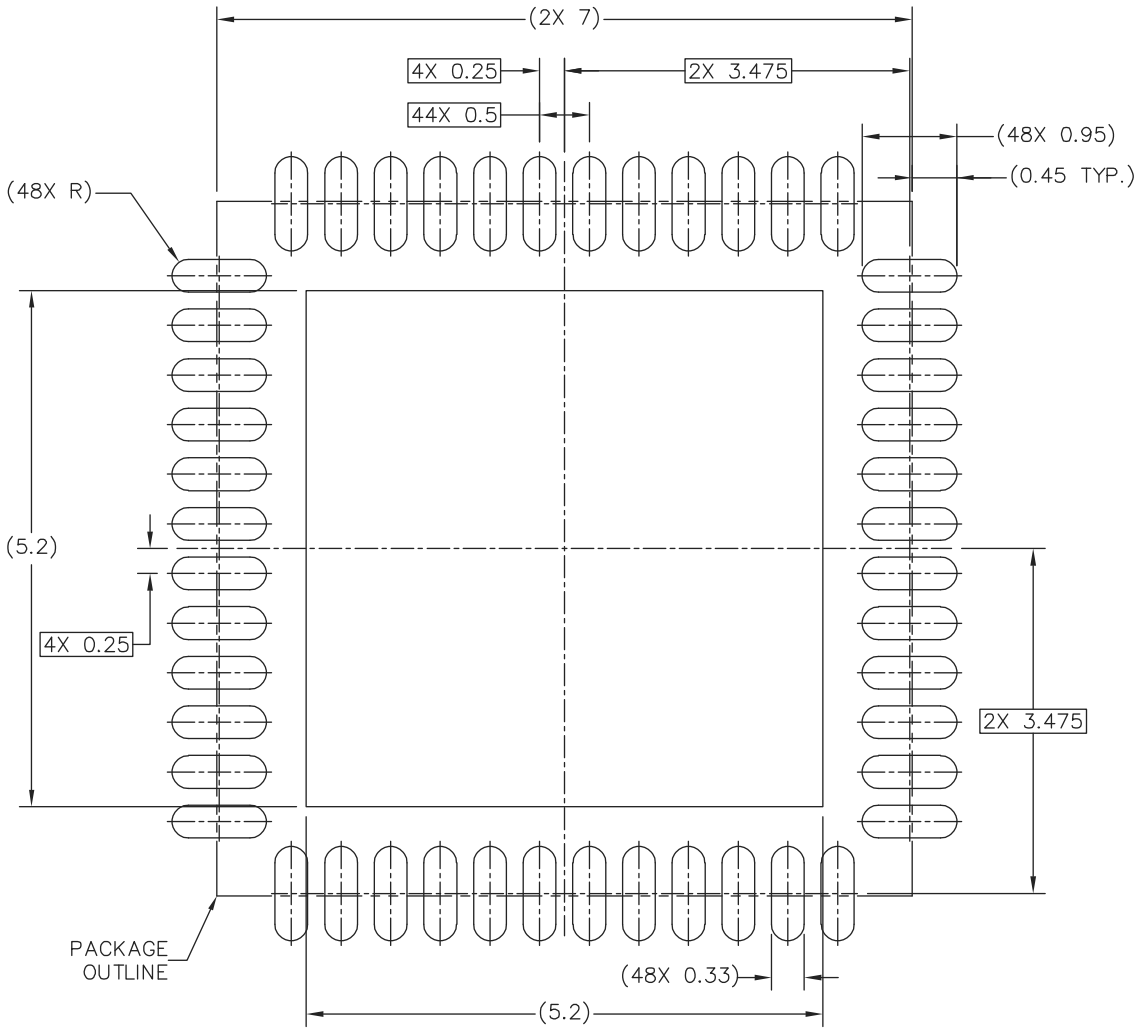
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	10.1 9.9	10.1 9.9	0.5	12.15 11.85	12.15 11.85	1	0.75 0.45	0.2	0.12	0.1	1.45 1.05	1.45 1.05	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT314-2	136E10	MS-026				~~00-01-19~~ 03-02-25

Fig 41. Package outline SOT314-2 (LQFP64)



PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

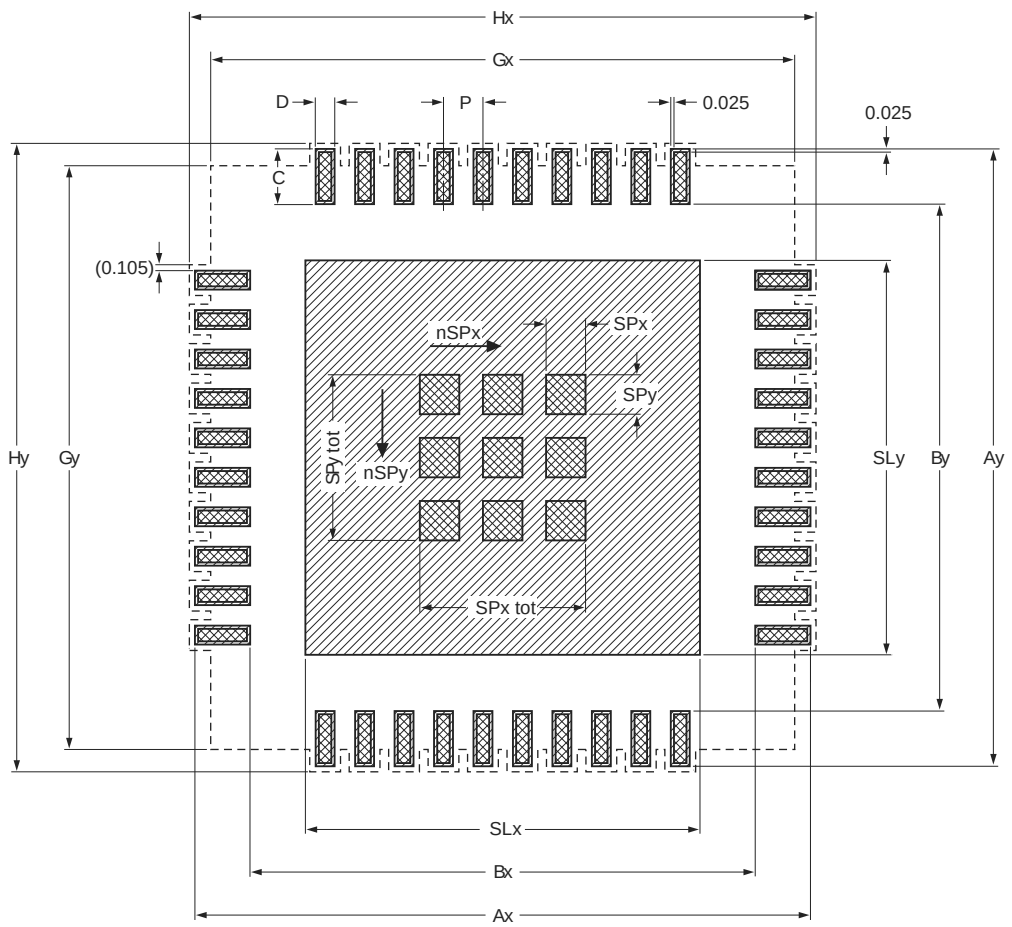
THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

 DATE: 13 DEC 2017

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: SOT619–1	REVISION: 0	

Fig 46. Reflow soldering of the HVQFN48 package (7x7) 1 of 3

Footprint information for reflow soldering of HVQFN48 package SOT619-1



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

solder paste deposit

solder land plus solder paste

occupied area

nSPx	nSPy
3	3

Dimensions in mm

P	Ax	Ay	Bx	By	C	D	SLx	SLy	SPx tot	SPy tot	SPx	SPy	Gx	Gy	Hx	Hy
0.500	8.000	8.000	6.200	6.200	0.900	0.290	5.100	5.100	3.000	3.000	0.750	0.750	7.300	7.300	8.250	8.250

Issue date ~~07-05-07~~ 09-06-15

sot619-1_fr

Fig 49. Reflow soldering of the HVQFN48 package (7x7)

22. Contents

continued >>