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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	30MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, Cap Sense, DMA, POR, PWM, WDT
Number of I/O	54
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 12x12b; D/A 2x10b
Oscillator Type	External, Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc845m301jbd64e

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC845M301JBD64	LQFP64	Plastic low profile quad flat package; 64 leads; body 10× 10 × 1.4 mm	SOT314-2
LPC845M301JBD48	LQFP48	Plastic low profile quad flat package; 48 leads; body 7× 7 × 1.4 mm	SOT313-2
LPC845M301JHI48	HVQFN48	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 48 terminals; body 7× 7 × 0.85 mm	SOT619-1
LPC845M301JHI33	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 5 × 5 × 0.85 mm	SOT617-11
LPC844M201JBD64	LQFP64	Plastic low profile quad flat package; 64 leads; body 10× 10 × 1.4 mm	SOT314-2
LPC844M201JBD48	LQFP48	Plastic low profile quad flat package; 48 leads; body 7× 7 × 1.4 mm	SOT313-2
LPC844M201JHI48	HVQFN48	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 48 terminals; body 7 × 7 × 0.85 mm	SOT619-1
LPC844M201JHI33	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 5 × 5 × 0.85 mm	SOT617-11

4.1 Ordering options

Table 2. Ordering options

Type number	Flash/KB	SRAM/KB	USART	I^2C	SPI	DAC	Capacitive Touch	GPIO	Package
LPC845M301JBD64	64	16	5	4	2	2	yes	54	LQFP64
LPC845M301JBD48	64	16	5	4	2	2	yes	42	LQFP48
LPC845M301JHI48	64	16	5	4	2	2	yes	42	HVQFN48
LPC845M301JHI33	64	16	5	4	2	1	-	29	HVQFN33
LPC844M201JBD64	64	8	2	2	2	-	-	54	LQFP64
LPC844M201JBD48	64	8	2	2	2	-	-	42	LQFP48
LPC844M201JHI48	64	8	2	2	2	-	-	42	HVQFN48
LPC844M201JHI33	64	8	2	2	2	-	-	29	HVQFN33

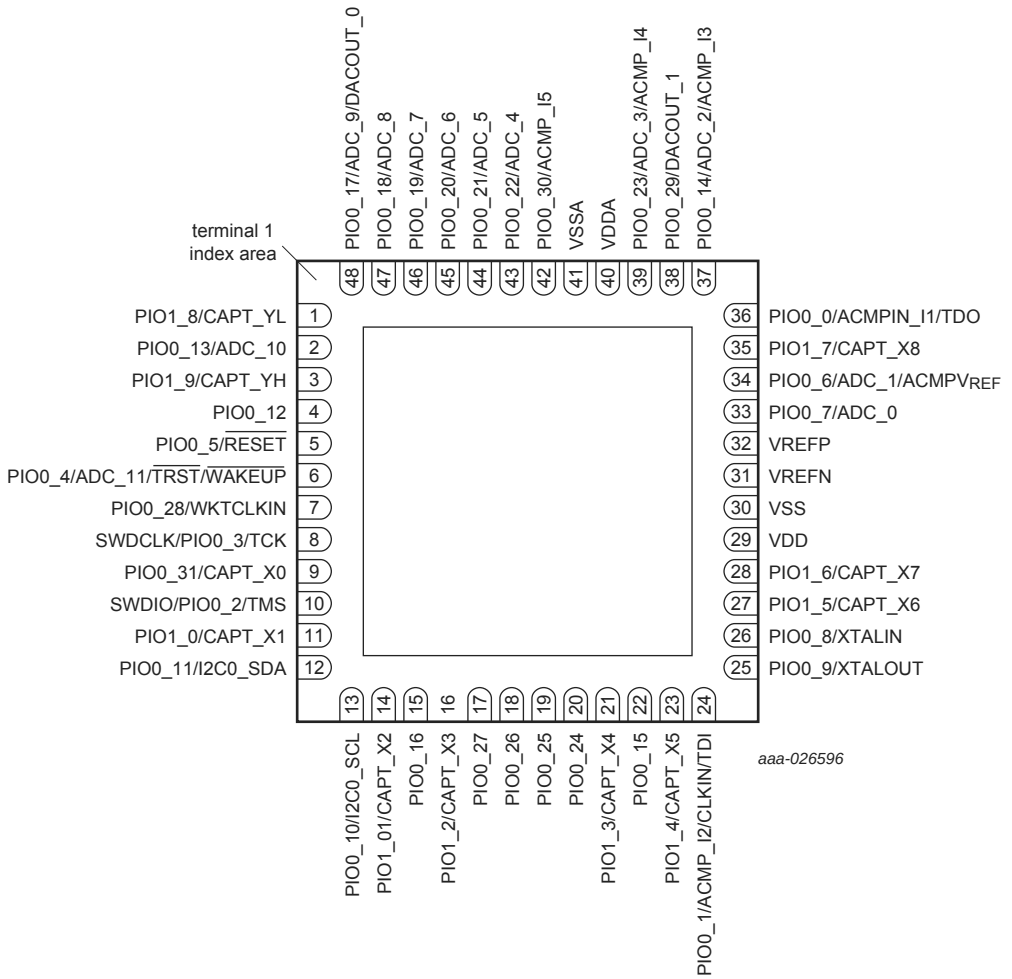


Fig 6. Pin configuration HVQFN48 package

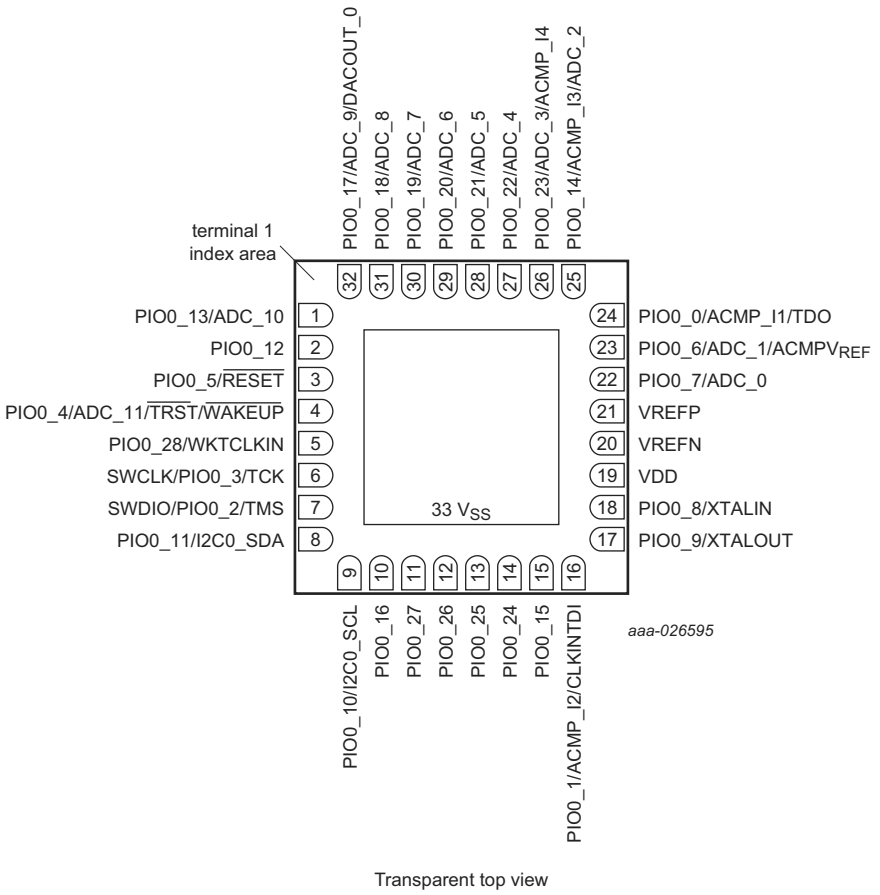


Fig 7. Pin configuration HVQFN33 package

7.2 Pin description

The pin description table shows the pin functions that are fixed to specific pins on each package. See Table 4. These fixed-pin functions are selectable through the switch matrix between GPIO and the comparator, ADC, SWD, RESET, and the XTAL pins. By default, the GPIO function is selected except on pins PIO0_2, PIO0_3, and PIO0_5. JTAG functions are available in boundary scan mode only.

Movable functions for the I^2C, USART, SPI, CTimer, SCT pins, and other peripherals can be assigned through the switch matrix to any pin that is not power or ground in place of the pin's fixed functions.

The following exceptions apply:

Do not assign more than one output to any pin. However, an output and/or one or more inputs can be assigned to a pin. Once any function is assigned to a pin, the pin's GPIO functionality is disabled.

Pin PIO0_4 triggers a wake-up from deep power-down mode. If the part must wake up from deep power-down mode via an external pin, do not assign any movable function to this pin.

Table 4. Pin description

Symbol	LQFP64	LQFP48	HVQFN48	HVQFN33		Reset state[1]	Type	Description
V_{SSA}	53	41	41					Analog ground.
VREFN	41	31	31	20		-	-	ADC negative reference voltage.
VREFP	42	32	32	21		-	-	ADC positive reference voltage. Must be equal or lower than V_{DDA}.

[1] Pin state at reset for default function: I = Input; AI = Analog Input; O = Output; PU = internal pull-up enabled (pins pulled up to full V_{DD} level); IA = inactive, no pull-up/down enabled; F = floating. For pin states in the different power modes, see Section 14.6 “Pin states in different power modes”. For termination on unused pins, see Section 14.5 “Termination of unused pins”.

[2] 5 V tolerant pin providing standard digital I/O functions with configurable modes, configurable hysteresis, and analog input. When configured as an analog input, the digital section of the pin is disabled, and the pin is not 5 V tolerant.

[3] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis. This pin is active in deep power-down mode and includes a 20 ns glitch filter (active in all power modes). In deep power-down mode, pulling the $\overline{\text{WAKEUP}}$ pin LOW wakes up the chip. The wake-up pin function can be disabled and the pin can be used for other purposes, if the WKT low-power oscillator is enabled for waking up the part from deep power-down mode. See Table 20 “Dynamic characteristics: WKTCLKIN pin” for the WKTCLKIN input.

[4] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis; includes high-current output driver.

[5] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis.

[6] True open-drain pin. I^2C-bus pins compliant with the I^2C-bus specification for I^2C standard mode, I^2C Fast-mode, and I^2C Fast-mode Plus. Do not use this pad for high-speed applications such as SPI or USART. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I2C lines. Open-drain configuration applies to all functions on this pin.

[7] See Figure 14 for the reset pad configuration. This pin includes a 20 ns glitch filter (active in all power modes). $\overline{\text{RESET}}$ functionality is available in deep power-down mode. Use the $\overline{\text{WAKEUP}}$ pin to reset the chip and wake up from deep power-down mode.

[8] 5 V tolerant pin providing standard digital I/O functions with configurable modes, configurable hysteresis, and analog I/O for the system oscillator. When configured for XTALIN and XTALOUT, the digital section of the pin is disabled, and the pin is not 5 V tolerant.

[9] The WKTCLKIN function is enabled in the DPDCTRL register in the PMU. See the LPC84x user manual.

[10] The digital part of this pin is 3 V tolerant pin due to special analog functionality. Pin provides standard digital I/O functions with configurable modes, configurable hysteresis, and an analog input. When configured as an analog input, the digital section of the pin is disabled.

[11] Thermal pad for HVQFN33.

Table 5. Movable functions (assign to pins PIO0_0 to PIO0_31, PIO1_0 to PIO1_21 through switch matrix)

Function name	Type	Description
Ux_TXD	O	Transmitter output for USART0 to USART4.
Ux_RXD	I	Receiver input for USART0 to USART4.
$\overline{\text{Ux\_RTS}}$	O	Request To Send output for USART0 to USART4.
$\overline{\text{Ux\_CTS}}$	I	Clear To Send input for USART0 to USART4.
Ux_SCLK	I/O	Serial clock input/output for USART0 to USART4 in synchronous mode.
SPIx_SCK	I/O	Serial clock for SPI0 and SPI1.
SPIx_MOSI	I/O	Master Out Slave In for SPI0 and SPI1.
SPIx_MISO	I/O	Master In Slave Out for SPI0 and SPI1.

8. Functional description

8.1 Arm Cortex-M0+ core

The Arm Cortex-M0+ core runs at an operating frequency of up to 30 MHz using a two-stage pipeline. The core revision is r0p1.

Integrated in the core are the NVIC and Serial Wire Debug with four breakpoints and two watchpoints. The Arm Cortex-M0+ core supports a single-cycle I/O enabled port for fast GPIO access.

The core includes a single-cycle multiplier and a system tick timer.

8.2 On-chip flash program memory

The LPC84x contain up to 64 KB of on-chip flash program memory. The flash memory supports a 64 Byte page size with page write and erase.

8.3 On-chip SRAM

The LPC84x contain a total of 16KB on-chip static RAM data memory in two separate SRAM blocks with one combined clock for both SRAM blocks. One 8 KB of SRAM can be used for MTB.

A bit-band module is added in series with the AHB matrix to allow atomic read-modify-write operations acting on a single bit.

8.4 FAIM memory

The LPC84x includes the FAIM memory and is used to configure the part at start-up. It is 128/256 bits in size and is used to configure the following:

- Clocks and PMU for low-power start-up.
- Low power boot at 1.5 MHz using FAIM memory.
- Pin configuration including direction and pull- up or pull-down.
- Specification of pins to use for ISP entry for each serial peripheral.
- Select whether SWCLK and SWDIO are enabled on reset.

Remark: The FAIM programming voltage range is 3.0 V ≤ Vdd ≤ 3.6 V.

8.5 On-chip ROM

The on-chip ROM contains the bootloader:

- Boot loader.
- Supports Flash In-Application Programming (IAP).
- Supports In-System Programming (ISP) through USART, SPI, and I^2C.
- On-chip ROM APIs for integer divide.
- FAIM API.
- FRO API.

8.6 Memory map

The LPC84x incorporates several distinct memory regions. Figure 8 shows the overall map of the entire address space from the user program viewpoint following reset. The interrupt vector area supports address remapping.

The Arm private peripheral bus includes the Arm core registers for controlling the NVIC, the system tick timer (SysTick), and the reduced power modes.

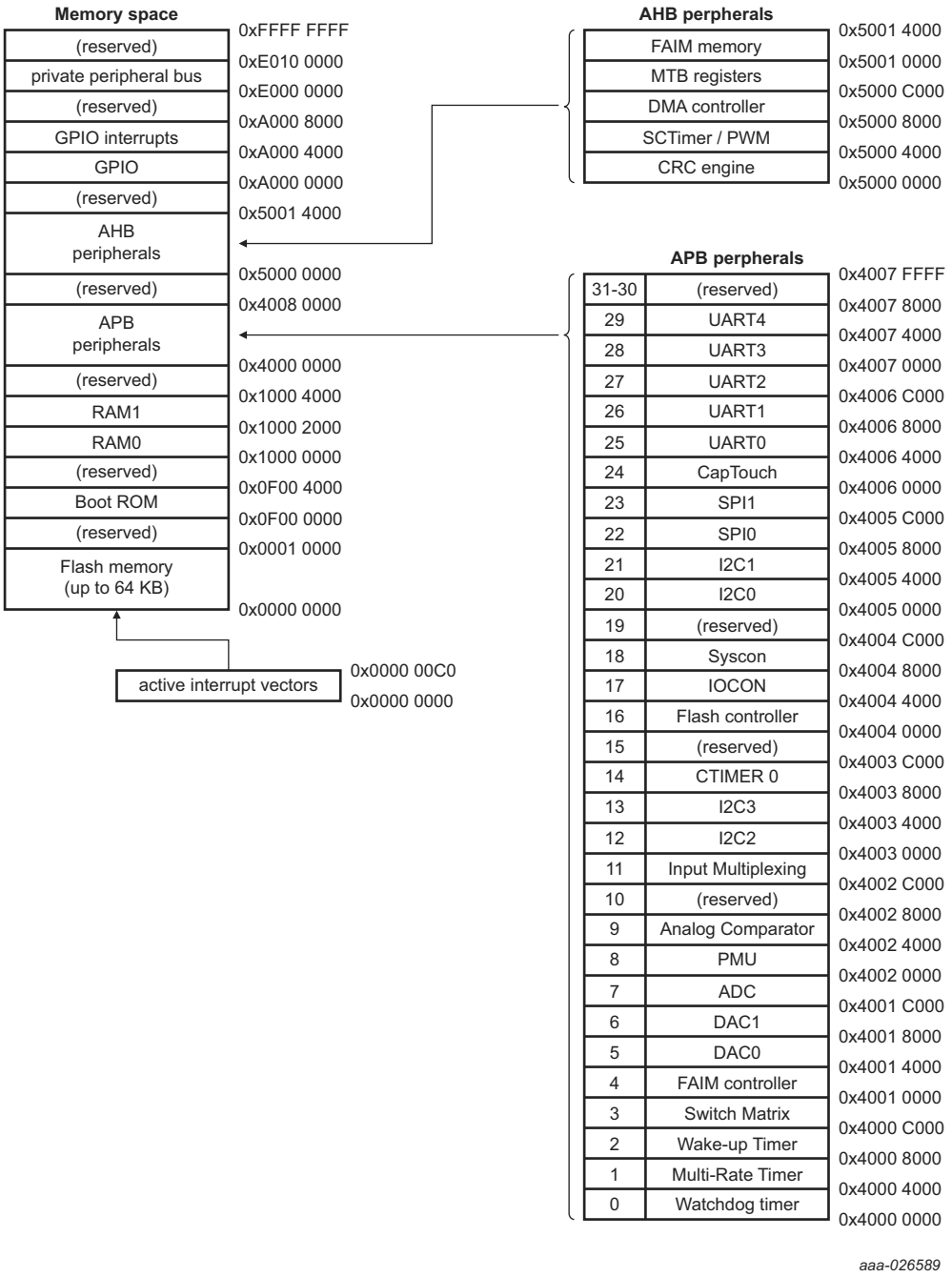


Fig 8. LPC84x AHB Memory mapping

- Data frames of 1 to 16 bits supported directly. Larger frames supported by software.
- Master and slave operation.
- Data can be transmitted to a slave without the need to read incoming data, which can be useful while setting up an SPI memory.
- Control information can optionally be written along with data, which allows very versatile operation, including “any length” frames.
- One Slave Select input/output with selectable polarity and flexible usage.

Remark: Texas Instruments SSI and National Microwire modes are not supported.

8.16 I²C-bus interface (I²C0/1/2/3)

The I²C-bus is bidirectional for inter-IC control using only two wires: a serial clock line (SCL) and a serial data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (for example, an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I²C is a multi-master bus and can be controlled by more than one bus master.

The I2C0-bus functions are fixed-pin functions. All other I2C-bus functions for I2C1/2/3 are movable functions and can be assigned through the switch matrix to any pin. However, only the true open-drain pins provide the electrical characteristics to support the full I2C-bus specification (see Ref. 3).

8.16.1 Features

- I2C0 supports Fast-mode Plus with data rates of up to 1 Mbit/s in addition to standard and fast modes on two true open-drain pins.
- True open-drain pins provide fail-safe operation: When the power to an I²C-bus device is switched off, the SDA and SCL pins connected to the I²C0-bus are floating and do not disturb the bus.
- I2C1/2/3 support standard and fast mode with data rates of up to 400 kbit/s.
- Independent Master, Slave, and Monitor functions.
- Supports both Multi-master and Multi-master with Slave functions.
- Multiple I²C slave addresses supported in hardware.
- One slave address can be selectively qualified with a bit mask or an address range in order to respond to multiple I²C bus addresses.
- 10-bit addressing supported with software assist.
- Supports SMBus.

8.17 Capacitive Touch Interface

The Capacitive Touch interface is designed to handle up to nine capacitive buttons in different sensor configurations, such as slider, rotary, and button matrix. It operates in sleep, deep sleep, and power-down modes, allowing very low power performance.

The Capacitive Touch module measures the change in capacitance of an electrode plate when an earth-ground connected object (for example, finger) is brought within close proximity.

8.18 SCTimer/PWM

The SCTimer/PWM can perform basic 16-bit and 32-bit timer/counter functions with match outputs and external and internal capture inputs. In addition, the SCTimer/PWM can employ up to eight different programmable states, which can change under the control of events, to provide complex timing patterns.

The inputs to the SCT are multiplexed between movable functions from the switch matrix and internal connections such as the ADC threshold compare interrupt, the comparator output, and the Arm core signals Arm_TXEV and DEBUG_HALTED. The signal on each SCT input is selected through the INPUT MUX.

All outputs of the SCT are movable functions and are assigned to pins through the switch matrix. One SCT output can also be selected as one of the ADC conversion triggers.

8.18.1 Features

- Each SCTimer/PWM supports:
  - Eight match/capture registers.
  - Eight events.
  - Eight states.
  - Five inputs. The fifth input is hard-wired to a clock source. Each input is configurable through an input multiplexer to use one of four external pins (connected through the switch matrix) or one of four internal sources. The maximum input signal frequency is 25 MHz.
  - Six outputs. Connected to pins through the switch matrix.
- Counter/timer features:
  - Each SCTimer is configurable as two 16-bit counters or one 32-bit counter.
  - Counters can be clocked by the system clock or selected input.
  - Configurable as up counters or up-down counters.
  - Configurable number of match and capture registers. Up to eight match and capture registers total.
  - Upon match create the following events: interrupt; stop, limit, halt the timer or change counting direction; toggle outputs.
  - Counter value can be loaded into capture register triggered by a match or input/output toggle.
- PWM features:
  - Counters can be used with match registers to toggle outputs and create time-proportioned PWM signals.
  - Up to six single-edge or dual-edge PWM outputs with independent duty cycle and common PWM cycle length.
- Event creation features:

- The following conditions define an event: a counter match condition, an input (or output) condition such as a rising or falling edge or level, a combination of match and/or input/output condition.
- Selected events can limit, halt, start, or stop a counter or change its direction.
- Events trigger state changes, output toggles, interrupts, and DMA transactions.
- Match register 0 can be used as an automatic limit.
- In bidirectional mode, events can be enabled based on the count direction.
- Match events can be held until another qualifying event occurs.

- State control features:
  - A state is defined by events that can happen in the state while the counter is running.
  - A state changes into another state as a result of an event.
  - Each event can be assigned to one or more states.
  - State variable allows sequencing across multiple counter cycles.
- One SCTimer match output can be selected as ADC hardware trigger input.

8.18.2 SCTimer/PWM input MUX (INPUT MUX)

Each input of the SCTimer/PWM is connected to a programmable multiplexer which allows to connect one of multiple internal or external sources to the input. The available sources are the same for each SCTimer/PWM input and can be selected from four pins configured through the switch matrix, the ADC threshold compare interrupt, the comparator output, and the Arm core signals Arm_TXEV and DEBUG_HALTED.

8.19 CTIMER

8.19.1 General-purpose 32-bit timers/external event counter

The LPC84x has one general-purpose 32-bit timer/counter.

The timer/counter is designed to count cycles of the system derived clock or an externally-supplied clock. It can optionally generate interrupts, generate timed DMA requests, or perform other actions at specified timer values, based on four match registers. Each timer/counter also includes two capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt.

8.19.2 Features

- A 32-bit timer/counter with a programmable 32-bit prescaler.
- Counter or timer operation.
- Up to three 32-bit captures can take a snapshot of the timer value when an input signal transitions. A capture event may also optionally generate an interrupt. The number of capture inputs for each timer that are actually available on device pins can vary by device.
- Four 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.

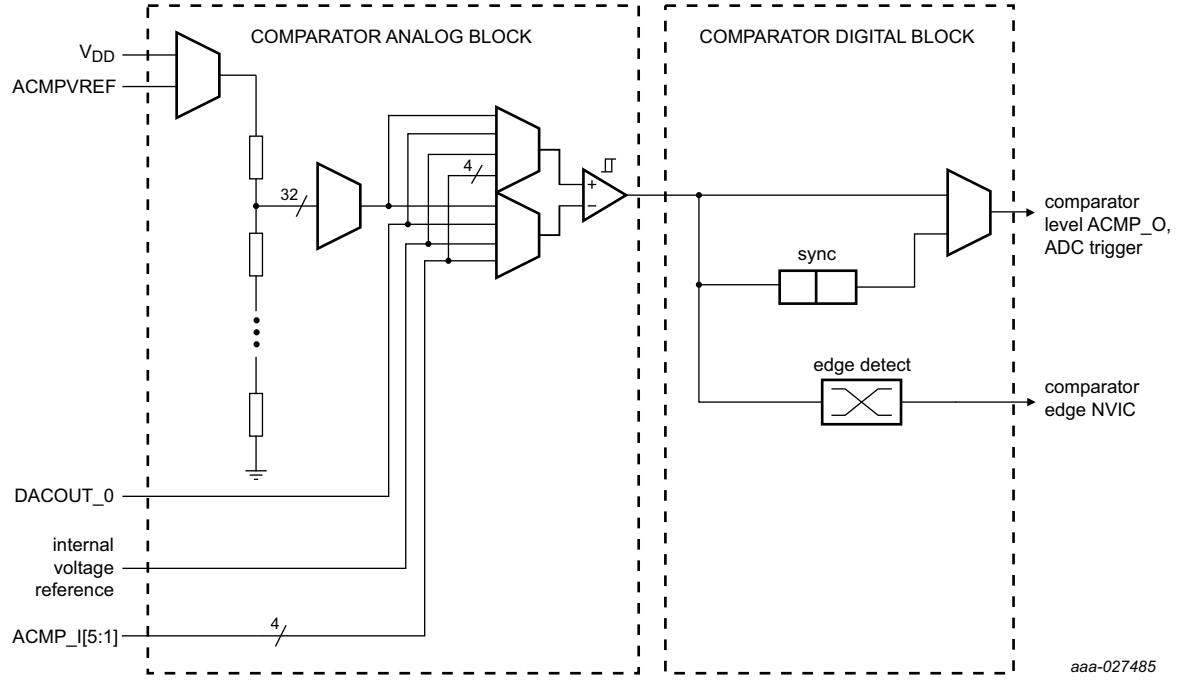


Fig 10. Comparator block diagram

8.23.1 Features

- Selectable 0 mV, 10 mV (± 5 mV), and 20 mV (± 10 mV), 40 mV (± 20 mV) input hysteresis.
- Two selectable external voltages (V_{DD} or $ACMPV_{REF}$); fully configurable on either positive or negative input channel.
- Internal voltage reference from band gap selectable on either positive or negative input channel.
- 32-stage voltage ladder with the internal reference voltage selectable on either the positive or the negative input channel.
- Voltage ladder source voltage is selectable from an external pin or the main 3.3 V supply voltage rail.
- Voltage ladder can be separately powered down for applications only requiring the comparator function.
- Interrupt output is connected to NVIC.
- Comparator level output is connected to output pin ACMP_O.
- One comparator output is internally collected to the ADC trigger input multiplexer.

8.24 Analog-to-Digital Converter (ADC)

The ADC supports a resolution of 12 bit and fast conversion rates of up to 1.2 MSamples/s. Sequences of analog-to-digital conversions can be triggered by multiple sources. Possible trigger sources are the pin triggers, the SCT output SCT_OUT3, the analog comparator output, and the Arm TXEV.

8.28.3 Code security (Code Read Protection - CRP)

CRP provides different levels of security in the system so that access to the on-chip flash and use of the Serial Wire Debugger (SWD) and In-System Programming (ISP) can be restricted. Programming a specific pattern into a dedicated flash location invokes CRP. IAP commands are not affected by the CRP.

In addition, ISP entry via the ISP entry pin can be disabled without enabling CRP. For details, see the *LPC84x user manual*.

There are three levels of Code Read Protection:

1. CRP1 disables access to the chip via the SWD and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors cannot be erased.
2. CRP2 disables access to the chip via the SWD and only allows full flash erase and update using a reduced set of the ISP commands.
3. Running an application with level CRP3 selected, fully disables any access to the chip via the SWD pins and the ISP. This mode effectively disables ISP override using the ISP entry pin as well. If necessary, the application must provide a flash update mechanism using IAP calls or using a call to the reinvoke ISP command to enable flash update via the USART.

CAUTION	
	If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

In addition to the three CRP levels, sampling of the ISP entry pin for valid user code can be disabled. For details, see the *LPC84x user manual*.

8.28.4 APB interface

The APB peripherals are located on one APB bus.

8.28.5 AHBLite

The AHBLite connects the CPU bus of the Arm Cortex-M0+ to the flash memory, the main static RAM, the CRC, the DMA, the ROM, and the APB peripherals.

11. Static characteristics

11.1 General operating conditions

Table 11. General operating conditions

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
f_{clk}	clock frequency	internal CPU/system clock		-	-	30	MHz
V_{DD}	supply voltage (core and external rail)		[3]	1.8	-	3.6	V
		FAIM programming only		3.0	-	3.6	V
		For ADC operations		2.4	-	3.6	V
		For DAC operations		2.7	-	3.6	V
V_{DDA}	analog supply voltage	For ADC operations		2.4	-	3.6	V
		For DAC operations		2.7	-	3.6	V
V_{ref}	ADC positive reference voltage	on pin VREFP		2.4	-	V_{DDA}	V
Oscillator pins							
$V_{i(xtal)}$	crystal input voltage	on pin XTALIN		−0.5	1.8	1.95	V
$V_{o(xtal)}$	crystal output voltage	on pin XTALOUT		−0.5	1.8	1.95	V
Pin capacitance							
C_{io}	input/output capacitance	pins with analog and digital functions	[2]	-	-	7.1	pF
		I^2C-bus pins	[2]	-	-	2.5	pF
		pins with digital functions only	[2]	-	-	2.8	pF

[1] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), nominal supply voltages.

[2] Including bonding pad capacitance. Based on simulation, not tested in production.

[3] The V_{DD} supply voltage must be 1.9 V or above when connecting an external crystal oscillator to the system oscillator. If the V_{DD} supply voltage is below 1.9 V, an external clock source can be fed to the XTALIN by bypassing the system oscillator or the other clock sources mentioned above can be used.

11.2 Power-up ramp conditions

Table 12. Power-up characteristics[1]

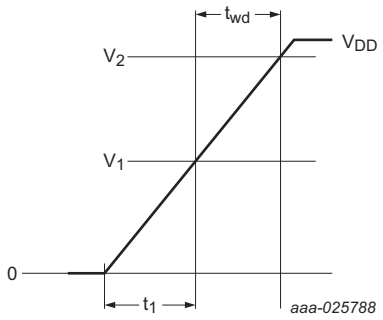
T_{amb} = −40 °C to +105 °C.

Symbol	Parameter		Min	Typ	Max	Unit
t_{wd}	Window duration (time where $V_1<V_{DD}<V_2$)		-	-	8	ms
V_1	Window low voltage	[2]	1.4	-	-	V
V_2	Window high voltage	[3]	-	-	1.8	V

[1] Assert the external reset pin until V_{DD} is > 1.8 V if the power-up characteristic specification cannot be implemented.

[2] V_{DD} to stay above V_1 for the entire duration t_{wd}.

[3] V_{DD} to stay below V_2 for the minimum duration of t_{wd}.



t_1: The time when there is no restriction on the ramp rate.

Fig 15. Power-up ramp

[3] I_{DD} measurements were performed with all pins configured as GPIO outputs driven LOW and pull-up resistors disabled.

[4] FRO enabled; system oscillator disabled; system PLL disabled.

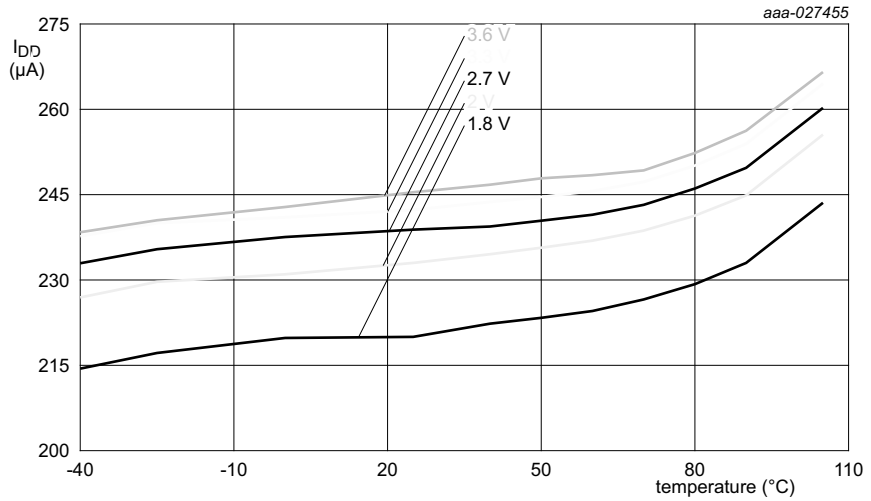
[5] BOD disabled.

[6] All peripherals disabled in the SYSAHBCLKCTRL register. Peripheral clocks disabled in system configuration block.

[7] All oscillators and analog blocks turned off.

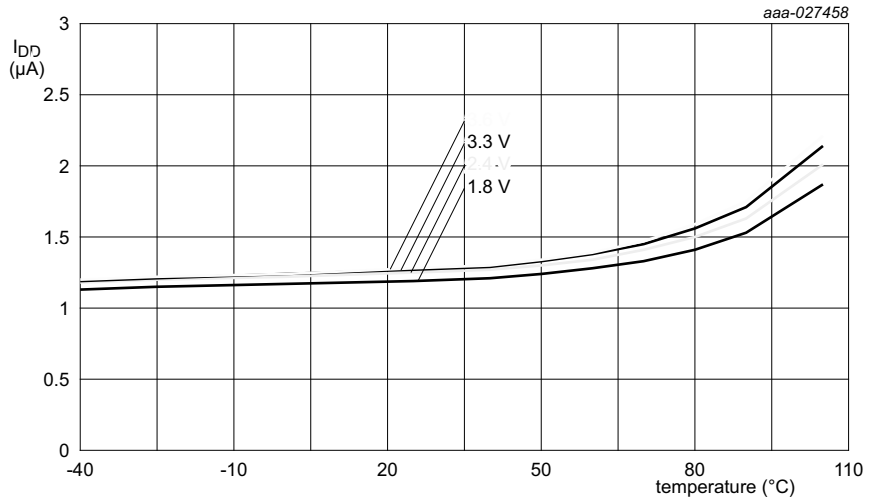
[8] $\overline{\text{WAKEUP}}$ pin pulled HIGH externally.

[9] Tested in production, VDD = 3.6 V.



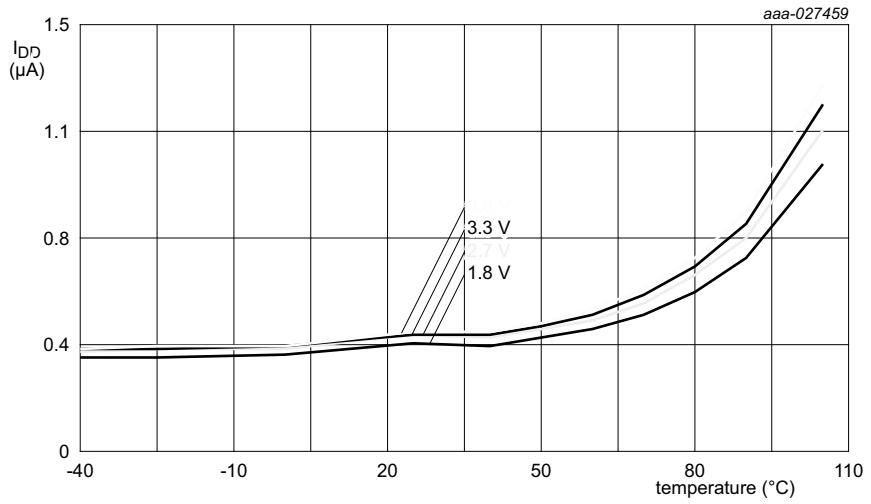
Conditions: BOD disabled; all oscillators and analog blocks disabled in the PDSLEEPCFG register (PDSLEEPCFG = 0x0000 18FF).

Fig 16. Deep-sleep mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}



WKT running with internal 10 kHz low-power oscillator.

Fig 19. Deep power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD} (internal clock)



WKT running with external 10 kHz clock. Clock input waveform: square wave with rise time and fall time of 5 ns.

Fig 20. Deep power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD} (external 10 kHz input clock)

12.8 USART interface

The actual USART bit rate depends on the delays introduced by the external trace, the external device, system clock (CCLK), and capacitive loading. Excluding delays introduced by external device and PCB, the maximum supported bit rate for USART master synchronous mode is 10 Mbit/s, and the maximum supported bit rate for USART slave synchronous mode is 10 Mbit/s.

Remark: USART functions can be assigned to all digital pins. The characteristics are valid for all digital pins except the open-drain pins PIO0_10 and PIO0_11.

Table 24. USART dynamic characteristics

T_{amb} = −40 °C to 105 °C; 1.8 V <= V_{DD} <= 3.6 V unless noted otherwise; C_L = 10 pF; input slew = 10 ns. Simulated parameters sampled at the 30 %/70 % level of the falling or rising edge; values guaranteed by design.

Symbol	Parameter	Conditions	Min	Max	Unit
USART master (in synchronous mode)					
$t_{su(D)}$	data input set-up time	3.0 V <= V_{DD} <= 3.6 V	31	-	ns
		1.8 V <= V_{DD} < 3.0 V	42		
$t_{h(D)}$	data input hold time		0	-	ns
$t_{v(Q)}$	data output valid time		0	7	ns
USART slave (in synchronous mode)					
$t_{su(D)}$	data input set-up time		5	-	ns
$t_{h(D)}$	data input hold time		5	-	ns
$t_{v(Q)}$	data output valid time	3.0 V <= V_{DD} <= 3.6 V	0	35	ns
		1.8 V <= V_{DD} < 3.0 V	0	46	ns

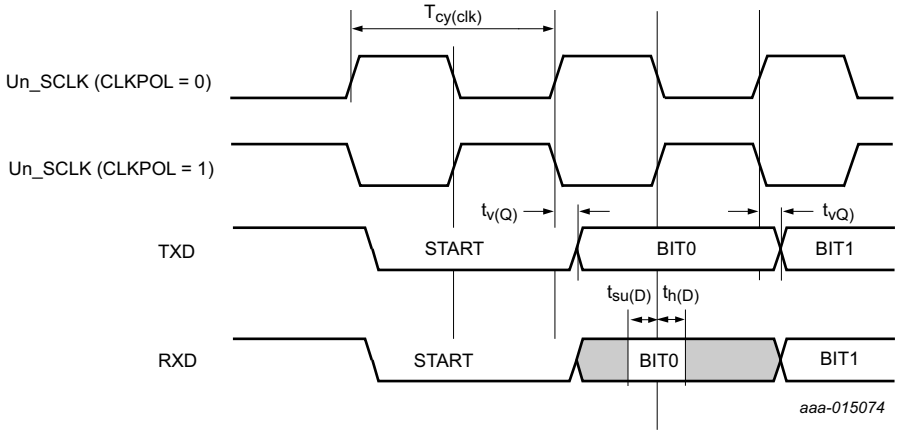


Fig 32. USART timing

13. Characteristics of analog peripherals

13.1 BOD

Table 26. BOD static characteristics[1]
T_{amb} = 25 °C.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{th}	threshold voltage	interrupt level 1					
		assertion		-	2.25	-	V
		de-assertion		-	2.38	-	V
		interrupt level 2					
		assertion		-	2.55	-	V
		de-assertion		-	2.66	-	V
		interrupt level 3					
		assertion		-	2.84	-	V
		de-assertion		-	2.92	-	V
		reset level 0					
		assertion		-	1.84	-	V
		de-assertion		-	1.97	-	V
		reset level 1					
		assertion		-	2.05	-	V
		de-assertion		-	2.18	-	V
		reset level 2					
		assertion		-	2.35	-	V
		de-assertion		-	2.47	-	V
		reset level 3					
		assertion		-	2.63	-	V
		de-assertion		-	2.76	-	V

[1] Interrupt levels are selected by writing the level value to the BOD control register BODCTRL, see *the* LPC84x *user manual*. Interrupt level 0 is reserved.

14.2 XTAL oscillator

In the XTAL oscillator circuit, only the crystal (XTAL) and the capacitances C_{X1} and C_{X2} need to be connected externally on XTALIN and XTALOUT. See Figure 37.

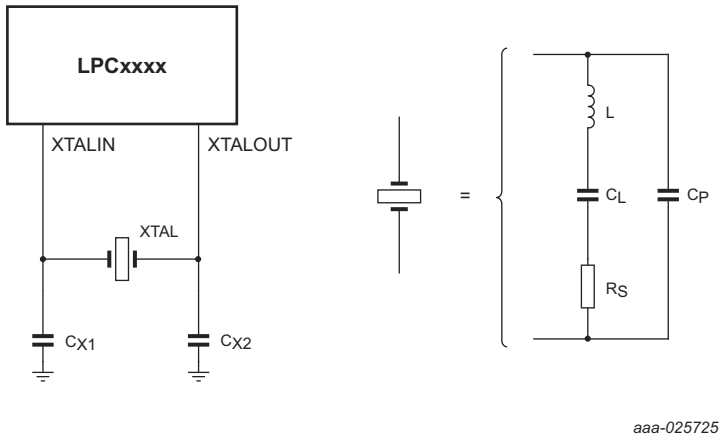


Fig 37. XTAL oscillator components

For best results, it is very critical to select a matching crystal for the on-chip oscillator. Load capacitance (CL), series resistance (RS), and drive level (DL) are important parameters to consider while choosing the crystal. After selecting the proper crystal, the external load capacitor C_{X1} and C_{X2} values can also be generally determined by the following expression:

$$C_{X1} = C_{X2} = 2C_L - (C_{Pad} + C_{Parasitic})$$

Where:

C_L - Crystal load capacitance

C_{Pad} - Pad capacitance of the XTALIN and XTALOUT pins (~3 pF).

$C_{Parasitic}$ – Parasitic or stray capacitance of external circuit.

Although $C_{Parasitic}$ can be ignored in general, the actual board layout and placement of external components influences the optimal values of external load capacitors. Therefore, it is recommended to fine tune the values of external load capacitors on actual hardware board to get the accurate clock frequency. For fine tuning, measure the clock on the XTALOUT pin and optimize the values of external load capacitors for minimum frequency deviation.

17. Abbreviations

Table 36. Abbreviations

Acronym	Description
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
BOD	BrownOut Detection
GPIO	General-Purpose Input/Output
PLL	Phase-Locked Loop
RC	Resistor-Capacitor
SPI	Serial Peripheral Interface
SMBus	System Management Bus
TEM	Transverse ElectroMagnetic
UART	Universal Asynchronous Receiver/Transmitter

18. References

[1] LPC84x User manual UM11029:

[2] LPC84x Errata sheet:

[3] I2C-bus specification *UM10204*.

[4] Technical note ADC design guidelines: http://www.nxp.com/documents/technical_note/TN00009.pdf

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