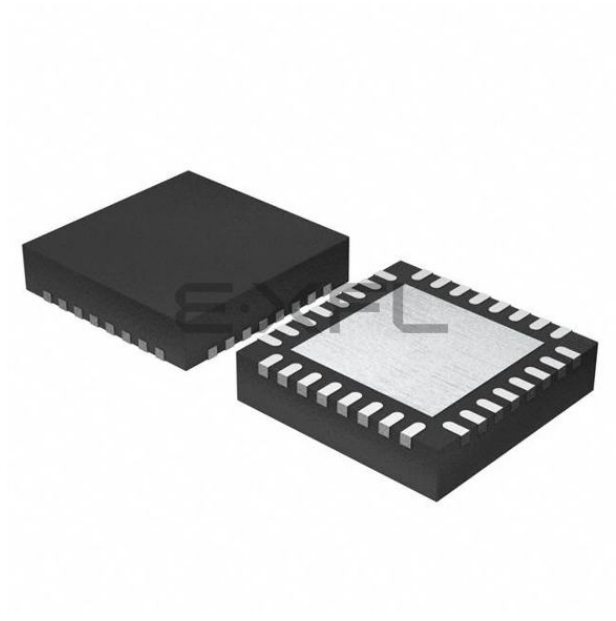

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	30MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, Cap Sense, DMA, POR, PWM, WDT
Number of I/O	29
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 12x12b; D/A 1x10b
Oscillator Type	External, Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-HVQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc845m301jhi33e

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC845M301JBD64	LQFP64	Plastic low profile quad flat package; 64 leads; body 10× 10 × 1.4 mm	SOT314-2
LPC845M301JBD48	LQFP48	Plastic low profile quad flat package; 48 leads; body 7× 7 × 1.4 mm	SOT313-2
LPC845M301JHI48	HVQFN48	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 48 terminals; body 7× 7 × 0.85 mm	SOT619-1
LPC845M301JHI33	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 5 × 5 × 0.85 mm	SOT617-11
LPC844M201JBD64	LQFP64	Plastic low profile quad flat package; 64 leads; body 10× 10 × 1.4 mm	SOT314-2
LPC844M201JBD48	LQFP48	Plastic low profile quad flat package; 48 leads; body 7× 7 × 1.4 mm	SOT313-2
LPC844M201JHI48	HVQFN48	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 48 terminals; body 7 × 7 × 0.85 mm	SOT619-1
LPC844M201JHI33	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 5 × 5 × 0.85 mm	SOT617-11

4.1 Ordering options

Table 2. Ordering options

Type number	Flash/KB	SRAM/KB	USART	I^2C	SPI	DAC	Capacitive Touch	GPIO	Package
LPC845M301JBD64	64	16	5	4	2	2	yes	54	LQFP64
LPC845M301JBD48	64	16	5	4	2	2	yes	42	LQFP48
LPC845M301JHI48	64	16	5	4	2	2	yes	42	HVQFN48
LPC845M301JHI33	64	16	5	4	2	1	-	29	HVQFN33
LPC844M201JBD64	64	8	2	2	2	-	-	54	LQFP64
LPC844M201JBD48	64	8	2	2	2	-	-	42	LQFP48
LPC844M201JHI48	64	8	2	2	2	-	-	42	HVQFN48
LPC844M201JHI33	64	8	2	2	2	-	-	29	HVQFN33

Table 4. Pin description

Symbol	LQFP64	LQFP48	HVQFN48	HVQFN33		Reset state[1]	Type	Description
PIO0_14/ ACMP_I3/ADC_2	49	37	37	25	[2]	I; PU	IO	**PIO0_14 —** General-purpose port 0 input/output 14.
							A	**ACMP_I3 —** Analog comparator common input 3.
							A	**ADC_2 —** ADC input 2.
PIO0_15	30	22	22	15	[5]	I; PU	IO	**PIO0_15 —** General-purpose port 0 input/output 15.
PIO0_16	19	15	15	10	[4]	I; PU	IO	**PIO0_16 —** General-purpose port 0 input/output 16.
PIO0_17/ADC_9/ DACOUT_0	63	48	48	32	[2]	I; PU	IO	**PIO0_17 —** General-purpose port 0 input/output 17.
							A	**ADC_9 —** ADC input 9.
							A	**DACOUT_0 —** DAC Output 0.
PIO0_18/ADC_8	61	47	47	31	[2]	I; PU	IO	**PIO0_18 —** General-purpose port 0 input/output 18.
							A	**ADC_8 —** ADC input 8.
PIO0_19/ADC_7	60	46	46	30	[2]	I; PU	IO	**PIO0_19 —** General-purpose port 0 input/output 19.
							A	**ADC_7 —** ADC input 7.
PIO0_20/ADC_6	58	45	45	29	[2]	I; PU	IO	**PIO0_20 —** General-purpose port 0 input/output 20.
							A	**ADC_6 —** ADC input 6.
PIO0_21/ADC_5	57	44	44	28	[2]	I; PU	IO	**PIO0_21 —** General-purpose port 0 input/output 21.
							A	**ADC_5 —** ADC input 5.
PIO0_22/ADC_4	55	43	43	27	[2]	I; PU	IO	**PIO0_22 —** General-purpose port 0 input/output 22.
							A	**ADC_4 —** ADC input 4.
PIO0_23/ADC_3/ ACMP_I4	51	39	39	26	[2]	I; PU	IO	**PIO0_23 —** General-purpose port 0 input/output 23.
							A	**ADC_3 —** ADC input 3.
							A	**ACMP_I4 —** Analog comparator common input 4.
PIO0_24	28	20	20	14	[5]	I; PU	IO	**PIO0_24 —** General-purpose port 0 input/output 24. In ISP mode, this is the U0_RXD pin.
PIO0_25	27	19	19	13	[5]	I; PU	IO	**PIO0_25 —** General-purpose port 0 input/output 25. In ISP mode, this pin is the U0_TXD pin.
PIO0_26	23	18	18	12	[5]	I; PU	IO	**PIO0_26 —** General-purpose port 0 input/output 26.
PIO0_27	21	17	17	11	[5]	I; PU	IO	**PIO0_27 —** General-purpose port 0 input/output 27.
PIO0_28/ WKTCLKIN	10	7	7	5	[3]	I; PU	IO	**PIO0_28 —** General-purpose port 0 input/output 28. This pin can host an external clock for the self-wake-up timer. To use the pin as a self-wake-up timer clock input, select the external clock in the wake-up timer CTRL register. The external clock input is active in all power modes, including deep power-down.
PIO0_29/ DACOUT_1	50	38	38	-	[5]	I; PU	IO	**PIO0_29 —** General-purpose port 0 input/output 29.
							A	**DACOUT_1 —** DAC output 1.
PIO0_30/ACMP_I5	54	42	42	-	[5]	I; PU	IO	**PIO0_30 —** General-purpose port 0 input/output 30.
							A	**ACMP_I5 —** Analog comparator common input 5.

Table 5. Movable functions (assign to pins PIO0_0 to PIO0_31, PIO1_0 to PIO1_21 through switch matrix)

Function name	Type	Description
SPIx_SSEL0	I/O	Slave select 0 for SPI0 and SPI1.
SPIx_SSEL1	I/O	Slave select 1 for SPI0 and SPI1.
SPIx_SSEL2	I/O	Slave select 2 for SPI0 and SPI1.
SPIx_SSEL3	I/O	Slave select 3 for SPI0 and SPI1.
SCT_PIN0	I	Pin input 0 to the SCT input multiplexer.
SCT_PIN1	I	Pin input 1 to the SCT input multiplexer.
SCT_PIN2	I	Pin input 2 to the SCT input multiplexer.
SCT_PIN3	I	Pin input 3 to the SCT input multiplexer.
SCT_OUT0	O	SCT output 0.
SCT_OUT1	O	SCT output 1.
SCT_OUT2	O	SCT output 2.
SCT_OUT3	O	SCT output 3.
SCT_OUT4	O	SCT output 4.
SCT_OUT5	O	SCT output 5.
I2Cx_SDA	I/O	I^2C1, I^2C2, and I^2C3 bus data input/output.
I2Cx_SCL	I/O	I^2C1, I^2C2, and I^2C3 bus clock input/output.
ACMP_O	O	Analog comparator output.
CLKOUT	O	Clock output.
GPIO_INT_BMAT	O	Output of the pattern match engine.
T0_MAT0	O	Timer Match channel 0.
T0_MAT1	O	Timer Match channel 1.
T0_MAT2	O	Timer Match channel 2.
T0_MAT3	O	Timer Match channel 3.
T0_CAP0	I	Timer Capture channel 0.
T0_CAP1	I	Timer Capture channel 1.
T0_CAP2	I	Timer Capture channel 2.

8. Functional description

8.1 Arm Cortex-M0+ core

The Arm Cortex-M0+ core runs at an operating frequency of up to 30 MHz using a two-stage pipeline. The core revision is r0p1.

Integrated in the core are the NVIC and Serial Wire Debug with four breakpoints and two watchpoints. The Arm Cortex-M0+ core supports a single-cycle I/O enabled port for fast GPIO access.

The core includes a single-cycle multiplier and a system tick timer.

8.2 On-chip flash program memory

The LPC84x contain up to 64 KB of on-chip flash program memory. The flash memory supports a 64 Byte page size with page write and erase.

8.3 On-chip SRAM

The LPC84x contain a total of 16KB on-chip static RAM data memory in two separate SRAM blocks with one combined clock for both SRAM blocks. One 8 KB of SRAM can be used for MTB.

A bit-band module is added in series with the AHB matrix to allow atomic read-modify-write operations acting on a single bit.

8.4 FAIM memory

The LPC84x includes the FAIM memory and is used to configure the part at start-up. It is 128/256 bits in size and is used to configure the following:

- Clocks and PMU for low-power start-up.
- Low power boot at 1.5 MHz using FAIM memory.
- Pin configuration including direction and pull- up or pull-down.
- Specification of pins to use for ISP entry for each serial peripheral.
- Select whether SWCLK and SWDIO are enabled on reset.

Remark: The FAIM programming voltage range is 3.0 V ≤ Vdd ≤ 3.6 V.

8.5 On-chip ROM

The on-chip ROM contains the bootloader:

- Boot loader.
- Supports Flash In-Application Programming (IAP).
- Supports In-System Programming (ISP) through USART, SPI, and I^2C.
- On-chip ROM APIs for integer divide.
- FAIM API.
- FRO API.

- The following conditions define an event: a counter match condition, an input (or output) condition such as a rising or falling edge or level, a combination of match and/or input/output condition.
- Selected events can limit, halt, start, or stop a counter or change its direction.
- Events trigger state changes, output toggles, interrupts, and DMA transactions.
- Match register 0 can be used as an automatic limit.
- In bidirectional mode, events can be enabled based on the count direction.
- Match events can be held until another qualifying event occurs.

- State control features:
  - A state is defined by events that can happen in the state while the counter is running.
  - A state changes into another state as a result of an event.
  - Each event can be assigned to one or more states.
  - State variable allows sequencing across multiple counter cycles.
- One SCTimer match output can be selected as ADC hardware trigger input.

8.18.2 SCTimer/PWM input MUX (INPUT MUX)

Each input of the SCTimer/PWM is connected to a programmable multiplexer which allows to connect one of multiple internal or external sources to the input. The available sources are the same for each SCTimer/PWM input and can be selected from four pins configured through the switch matrix, the ADC threshold compare interrupt, the comparator output, and the Arm core signals Arm_TXEV and DEBUG_HALTED.

8.19 CTIMER

8.19.1 General-purpose 32-bit timers/external event counter

The LPC84x has one general-purpose 32-bit timer/counter.

The timer/counter is designed to count cycles of the system derived clock or an externally-supplied clock. It can optionally generate interrupts, generate timed DMA requests, or perform other actions at specified timer values, based on four match registers. Each timer/counter also includes two capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt.

8.19.2 Features

- A 32-bit timer/counter with a programmable 32-bit prescaler.
- Counter or timer operation.
- Up to three 32-bit captures can take a snapshot of the timer value when an input signal transitions. A capture event may also optionally generate an interrupt. The number of capture inputs for each timer that are actually available on device pins can vary by device.
- Four 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.

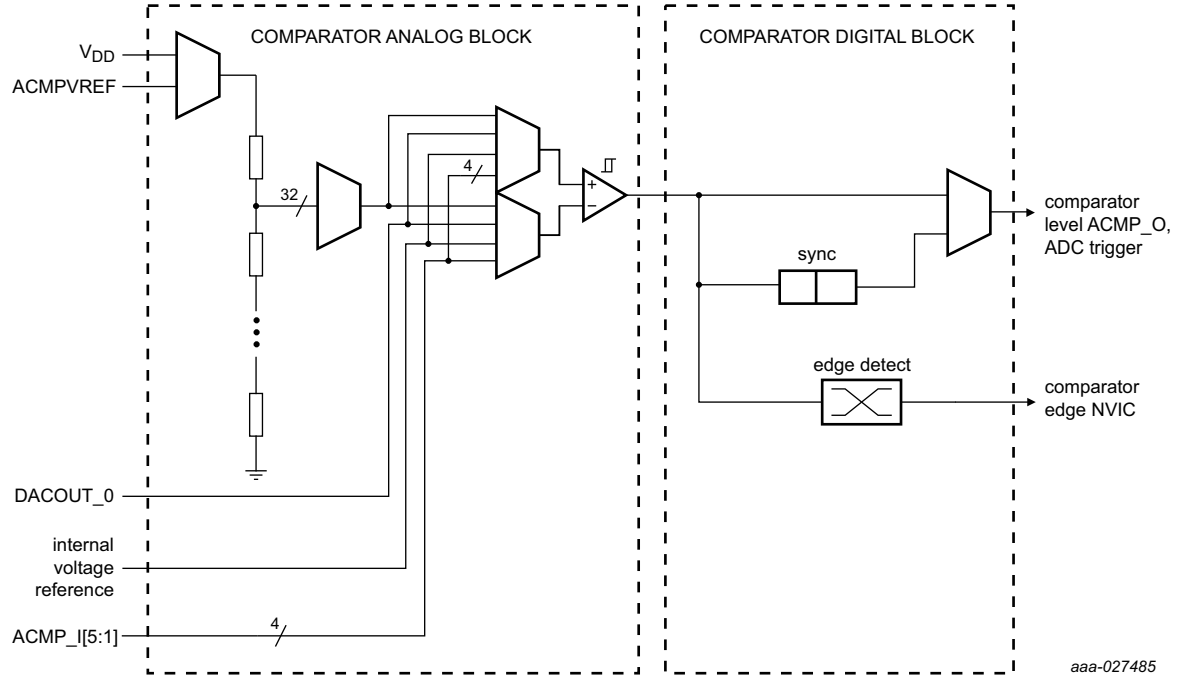


Fig 10. Comparator block diagram

8.23.1 Features

- Selectable 0 mV, 10 mV (± 5 mV), and 20 mV (± 10 mV), 40 mV (± 20 mV) input hysteresis.
- Two selectable external voltages (V_{DD} or $ACMPV_{REF}$); fully configurable on either positive or negative input channel.
- Internal voltage reference from band gap selectable on either positive or negative input channel.
- 32-stage voltage ladder with the internal reference voltage selectable on either the positive or the negative input channel.
- Voltage ladder source voltage is selectable from an external pin or the main 3.3 V supply voltage rail.
- Voltage ladder can be separately powered down for applications only requiring the comparator function.
- Interrupt output is connected to NVIC.
- Comparator level output is connected to output pin ACMP_O.
- One comparator output is internally collected to the ADC trigger input multiplexer.

8.24 Analog-to-Digital Converter (ADC)

The ADC supports a resolution of 12 bit and fast conversion rates of up to 1.2 MSamples/s. Sequences of analog-to-digital conversions can be triggered by multiple sources. Possible trigger sources are the pin triggers, the SCT output SCT_OUT3, the analog comparator output, and the Arm TXEV.

- Supports CPU PIO or DMA back-to-back transfer.
- Accept any size of data width per write: 8, 16 or 32-bit.
  - 8-bit write: 1-cycle operation.
  - 16-bit write: 2-cycle operation (8-bit x 2-cycle).
  - 32-bit write: 4-cycle operation (8-bit x 4-cycle).

8.27 Clocking and power control

8.27.1 Crystal and internal oscillators

The LPC84x include four independent oscillators:

1. The crystal oscillator (SysOsc) operating at frequencies between 1 MHz and 25 MHz.
2. Free Running Oscillator.
3. Watchdog Oscillator
4. Low Power Oscillator

Each oscillator, except the low-frequency oscillator, can be used for more than one purpose as required in a particular application.

Following reset, the LPC84x operates from the FRO until switched by software allowing the part to run without any external crystal and the bootloader code to operate at a known frequency.

See Figure 11 for an overview of the LPC84x clock generation.

8.27.1.1 Free Running Oscillator (FRO)

The FRO oscillator provides the default clock at reset and provides a clean system clock shortly after the supply pins reach operating voltage.

- This oscillator provides a selectable 18 MHz, 24 MHz, and 30 MHz outputs that can be used as a system clock. Also, these outputs can be divided down to 1.125 MHz, 1.5 MHz, 1.875 MHz, 9 MHz, 12 MHz, and 15 MHz for system clock.
- The FRO is trimmed to ±1 % accuracy over the entire voltage and temperature range of 0 C to 70 C.
- By default, the fro_oscout is 24 MHz and is divided by 2 to provide a default system (CPU) clock frequency of 12 MHz.

8.27.1.2 Crystal Oscillator (SysOsc)

The crystal oscillator can be used as the clock source for the CPU, with or without using the PLL.

The SysOsc operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the system PLL.

8.27.1.3 Internal Low-power Oscillator and Watchdog Oscillator (WDOsc)

The nominal frequency of the WDOsc is programmable between 9.4 kHz and 2.3 MHz. The frequency spread over silicon process variations is ± 40%.

The WDOsc is a dedicated oscillator for the windowed WWDT.

[3] I_{DD} measurements were performed with all pins configured as GPIO outputs driven LOW and pull-up resistors disabled.

[4] FRO enabled; system oscillator disabled; system PLL disabled.

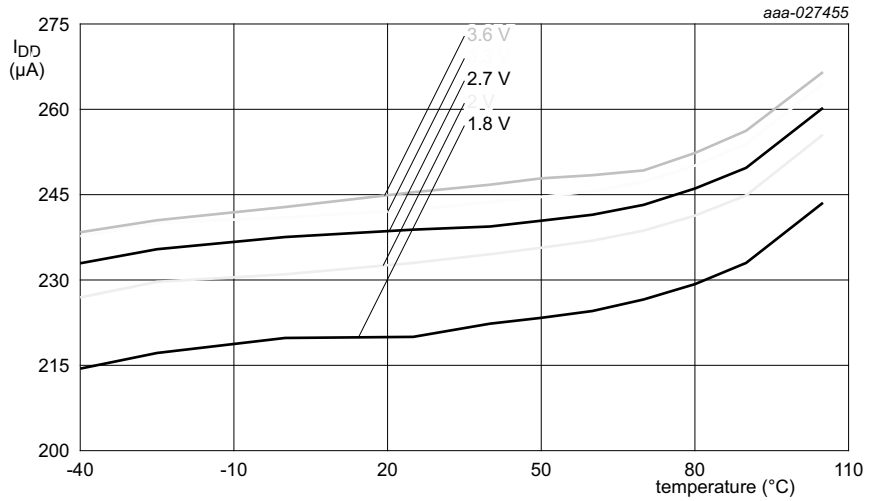
[5] BOD disabled.

[6] All peripherals disabled in the SYSAHBCLKCTRL register. Peripheral clocks disabled in system configuration block.

[7] All oscillators and analog blocks turned off.

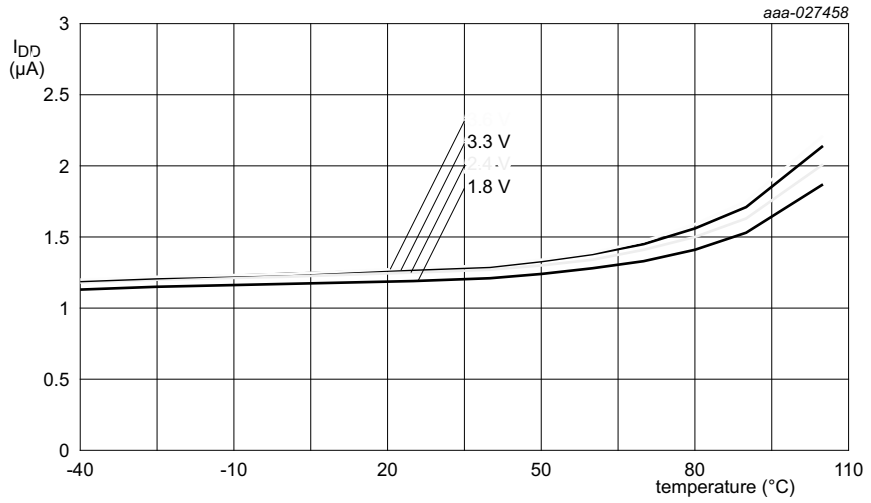
[8] $\overline{\text{WAKEUP}}$ pin pulled HIGH externally.

[9] Tested in production, VDD = 3.6 V.



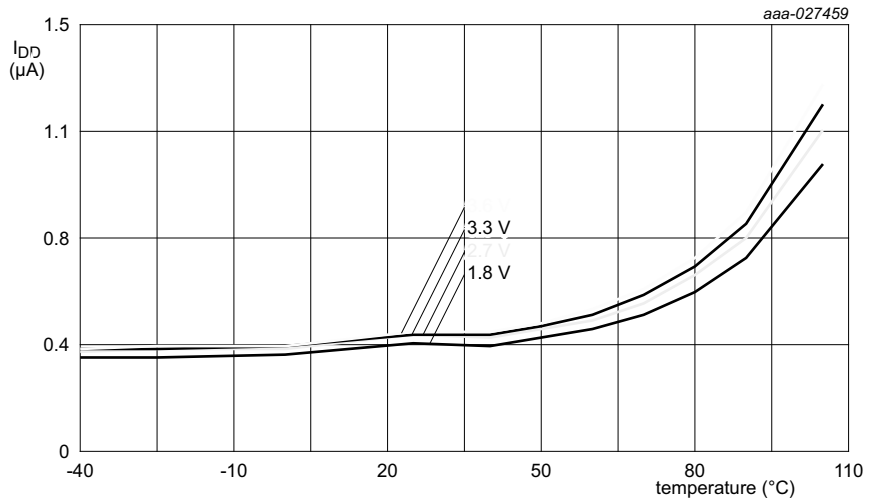
Conditions: BOD disabled; all oscillators and analog blocks disabled in the PDSLEEPCFG register (PDSLEEPCFG = 0x0000 18FF).

Fig 16. Deep-sleep mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}



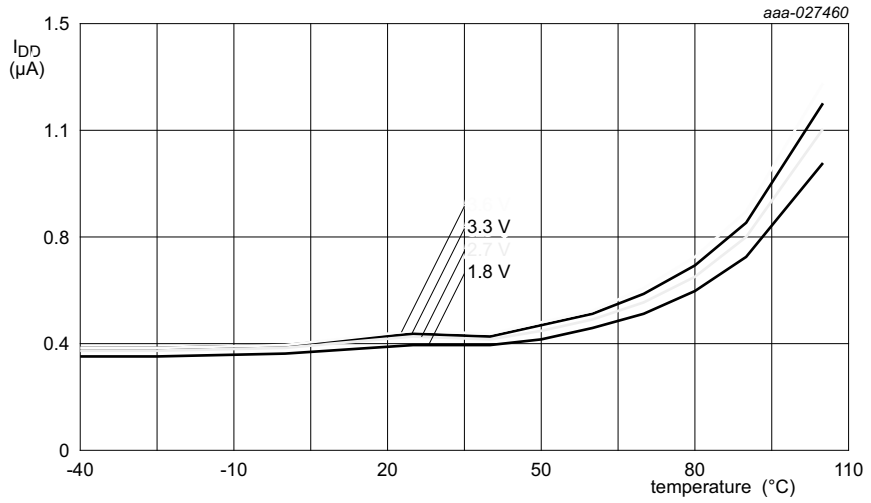
WKT running with internal 10 kHz low-power oscillator.

Fig 19. Deep power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD} (internal clock)



WKT running with external 10 kHz clock. Clock input waveform: square wave with rise time and fall time of 5 ns.

Fig 20. Deep power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD} (external 10 kHz input clock)



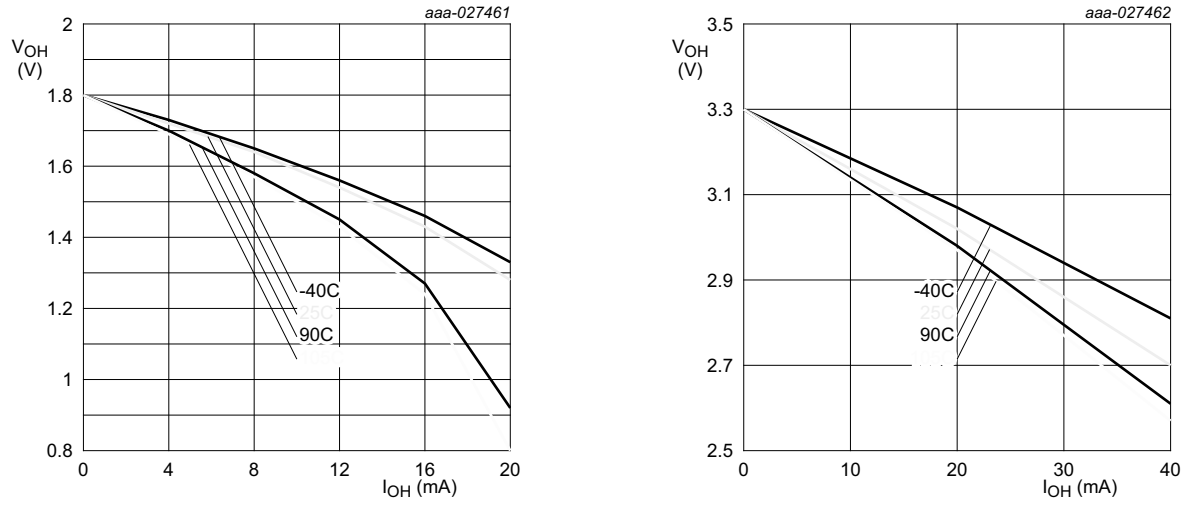
WKT running with external 32 kHz clock. Clock input waveform: square wave with rise time and fall time of 5 ns.

Fig 21. Deep power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD} (external 32 kHz input clock)

Table 14. Power consumption for individual analog and digital blocks *…continued*

Peripheral	Typical supply current in µA			Notes
	System clock frequency =			
	n/a	12 MHz	30 MHz	
USART3	-	58	142	-
USART4	-	56	137	-
Comparator ACMP	-	79	144	-
ADC	-	78	190	Digital controller only. Analog portion of the ADC disabled in the PDRUNCFG register.
	-	78	190	Combined analog and digital logic. ADC enabled in the PDRUNCFG register and LPWRMODE bit set to 1 in the ADC CTRL register (ADC in low-power mode).
	-	79	190	Combined analog and digital logic. ADC enabled in the PDRUNCFG register and LPWRMODE bit set to 0 in the ADC CTRL register (ADC powered).
DAC 0	-	46	107	-
DAC 1	-	36	88	-
Capacitive Touch	-	49	117	-
DMA	-	355	858	-
CRC	-	36	83	-

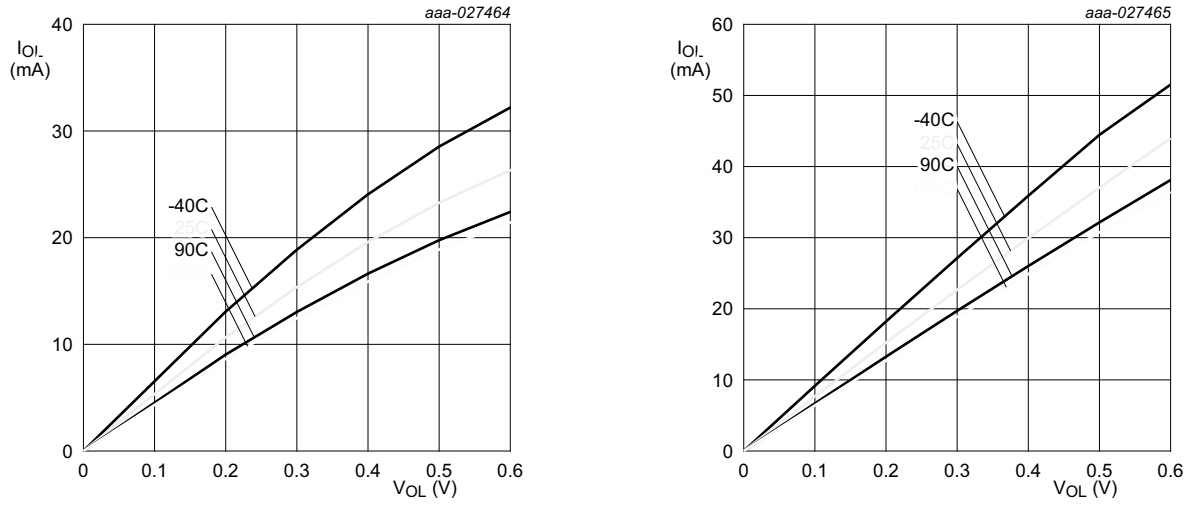
11.5.1 Electrical pin characteristics



Conditions: V_{DD} = 1.8 V; on pin PIO0_12.

Conditions: V_{DD} = 3.3 V; on pin PIO0_12.

Fig 23. High-drive output: Typical HIGH-level output voltage V_{OH} versus HIGH-level output current I_{OH}



Conditions: V_{DD} = 1.8 V; on pins PIO0_10 and PIO0_11.

Conditions: V_{DD} = 3.3 V; on pins PIO0_10 and PIO0_11.

Fig 24. I^2C-bus pins (high current sink): Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}

12.6 I²C-bus

Table 22. Dynamic characteristic: I²C-bus pins[1]

T_{amb} = −40 °C to +105 °C; values guaranteed by design.[2]

Symbol	Parameter		Conditions	Min	Max	Unit
f_{SCL}	SCL clock frequency		Standard-mode	0	100	kHz
			Fast-mode	0	400	kHz
			Fast-mode Plus; on pins PIO0_10 and PIO0_11	0	1	MHz
t_f	fall time	[4][5][6][7]	of both SDA and SCL signals	-	300	ns
			Standard-mode			
			Fast-mode	20 + 0.1 × C_b	300	ns
			Fast-mode Plus; on pins PIO0_10 and PIO0_11	-	120	ns
t_{LOW}	LOW period of the SCL clock		Standard-mode	4.7	-	µs
			Fast-mode	1.3	-	µs
			Fast-mode Plus; on pins PIO0_10 and PIO0_11	0.5	-	µs
t_{HIGH}	HIGH period of the SCL clock		Standard-mode	4.0	-	µs
			Fast-mode	0.6	-	µs
			Fast-mode Plus; on pins PIO0_10 and PIO0_11	0.26	-	µs
$t_{HD;DAT}$	data hold time	[3][4][8]	Standard-mode	0	-	µs
			Fast-mode	0	-	µs
			Fast-mode Plus; on pins PIO0_10 and PIO0_11	0	-	µs
$t_{SU;DAT}$	data set-up time	[9][10]	Standard-mode	250	-	ns
			Fast-mode	100	-	ns
			Fast-mode Plus; on pins PIO0_10 and PIO0_11	50	-	ns

[1] See the I²C-bus specification *UM10204* for details.

[2] Parameters are valid over operating temperature range unless otherwise specified.

[3] $t_{HD;DAT}$ is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.

[4] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[5] C_b = total capacitance of one bus line in pF.

[6] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[7] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

12.9 Wake-up process

Table 25. Dynamic characteristic: Typical wake-up times from low power modes
V_{DD} = 3.3 V;T_{amb} = 25 °C; using FRO (12MHz) as the system clock.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
t_{wake}	wake-up time	from sleep mode	[2][3]	-	2.4	-	µs
		from deep-sleep mode	[2]	-	2.5	-	µs
		from power-down mode	[2]	-	50	-	µs
		from deep power-down mode; WKT disabled; using $\overline{\text{RESET}}$ pin.	[4]	-	250	-	µs

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] The wake-up time measured is the time between when a GPIO input pin is triggered to wake the device up from the low power modes and from when a GPIO output pin is set in the interrupt service routine (ISR) wake-up handler. ISR is located in SRAM.

[3] FRO enabled, all peripherals off. PLL disabled.

[4] WKT disabled. Wake up from deep power-down causes the part to go through entire reset process. The wake-up time measured is the time between when the $\overline{\text{RESET}}$ pin is triggered to wake the device up and when a GPIO output pin is set in the reset handler.

13. Characteristics of analog peripherals

13.1 BOD

Table 26. BOD static characteristics[1]
T_{amb} = 25 °C.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{th}	threshold voltage	interrupt level 1					
		assertion		-	2.25	-	V
		de-assertion		-	2.38	-	V
		interrupt level 2					
		assertion		-	2.55	-	V
		de-assertion		-	2.66	-	V
		interrupt level 3					
		assertion		-	2.84	-	V
		de-assertion		-	2.92	-	V
		reset level 0					
		assertion		-	1.84	-	V
		de-assertion		-	1.97	-	V
		reset level 1					
		assertion		-	2.05	-	V
		de-assertion		-	2.18	-	V
		reset level 2					
		assertion		-	2.35	-	V
		de-assertion		-	2.47	-	V
		reset level 3					
		assertion		-	2.63	-	V
		de-assertion		-	2.76	-	V

[1] Interrupt levels are selected by writing the level value to the BOD control register BODCTRL, see *the* LPC84x *user manual*. Interrupt level 0 is reserved.

13.2 ADC

Table 27. 12-bit ADC static characteristics

T_{amb} = −40 °C to +105 °C unless noted otherwise; V_{DD} = V_{DDA} = 2.4 V to 3.6 V; VREFP = V_{DD} = V_{DDA}; VREFN = V_{SS}.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IA}	analog input voltage			0	-	V_{DDA}	V
V_{ref}	reference voltage	on pin VREFP		2.4	-	V_{DDA}	V
C_{ia}	analog input capacitance			-	-	26	pF
$f_{clk(ADC)}$	ADC clock frequency		[2]	-	-	30	MHz
f_s	sampling frequency		[2]	-	-	1.2	Msamples/s
E_D	differential linearity error		[5][4]	-	±3.0	-	LSB
$E_{L(adj)}$	integral non-linearity		[6][4]	-	±2.0	-	LSB
E_O	offset error		[7][4]	-	±3.5	-	LSB
$V_{err(fs)}$	full-scale error voltage		[8][4]	-	0.1	-	%
Z_i	input impedance	f_s = 1.2 Msamples/s	[1][9][10]	0.1	-	-	MΩ

[1] The input resistance of ADC channel 0 is higher than for all other channels. See Figure 33.

[2] In the ADC TRM register, set VRANGE = 0 (default).

[3] In the ADC TRM register, set VRANGE = 1.

[4] Based on characterization. Not tested in production.

[5] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 34.

[6] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 34.

[7] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 34.

[8] The full-scale error voltage or gain error (E_G) is the difference between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 34.

[9] T_{amb} = 25 °C; maximum sampling frequency f_s = 1.2 Msamples/s and analog input capacitance C_{ia} = 26 pF.

[10] Input impedance Z_i (See Section 13.2.1 “ADC input impedance”) is inversely proportional to the sampling frequency and the total input capacity including C_{ia} and C_{io}: $Z_i \propto 1 / (f_s \times C_i)$. See Table 13 for C_{io}.

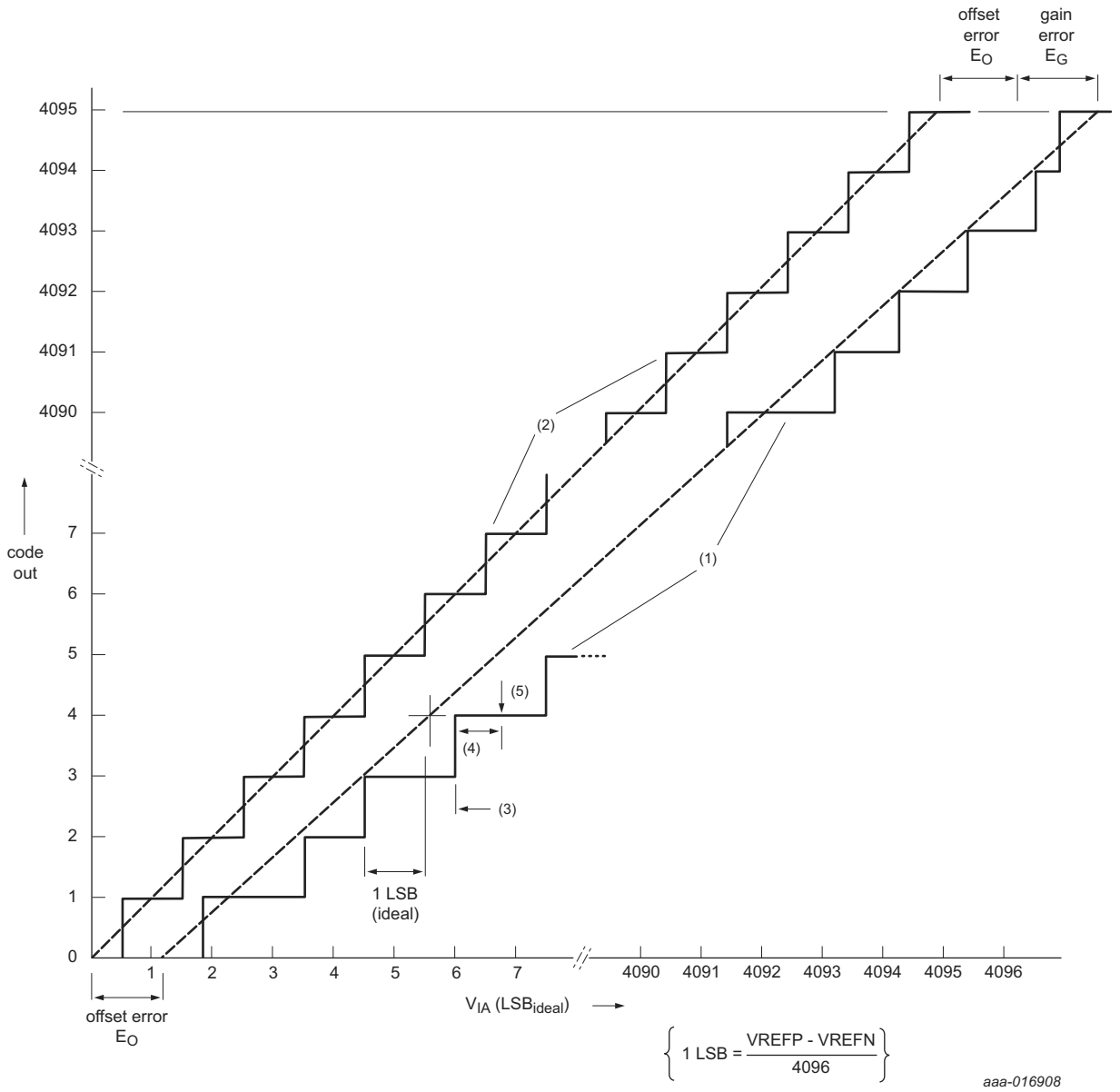


Fig 33. 12-bit ADC characteristics

Table 31. Comparator voltage ladder reference static characteristics

V_{DD} = 1.8 V to 3.6 V. T_{amb} = -40 °C to + 105°C; external or internal reference.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$E_{V(O)}$	output voltage error	decimal code = 00	[2]	-	±6	-	mV
		decimal code = 08		-	±1	-	%
		decimal code = 16		-	±1	-	%
		decimal code = 24		-	±1	-	%
		decimal code = 30		-	±1	-	%
		decimal code = 31		-	±1	-	%

[1] Characterized though limited samples. Not tested in production.

[2] All peripherals except comparator, temperature sensor, and FRO turned off.

13.4 DAC

Table 32. 10-bit DAC electrical characteristics

V_{DD} = V_{DDA} = 2.7 V to 3.6 V; T_{amb} = −40 °C to +105 °C unless otherwise specified

Symbol	Parameter		Min	Typ	Max	Unit
E_D	differential linearity error	[1][2]	-	0.4	-	LSB
$E_{L(adj)}$	integral non-linearity	[1][2]	-	6.0	-	LSB
E_O	offset error	[1][2]	-	±57.0	-	mV
E_G	gain error	[1][2]	-	±36.0	-	mV
C_L	load capacitance		-	200	-	pF
R_{OUT}	PIO0_17/DACOUT_0 pin resistance	[3]	-	90	200	Ω
R_{OUT}	PIO0_29/DACOUT_1 pin resistance	[3]	-	2	5	kΩ
V_{OUT}	Output voltage range		0.175	-	V_{DDA}-0.175	V

[1] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C) and V_{DD} = V_{DDA} = 3.6 V.

[2] Characterized through bench measurements, not tested in production.

[3] DAC output voltage depends on the voltage divider ratio of the R_{OUT} and external load resistance.

14.4 I/O power consumption

I/O pins are contributing to the overall dynamic and static power consumption of the part. If pins are configured as digital inputs, a static current can flow depending on the voltage level at the pin and the setting of the internal pull-up and pull-down resistors. This current can be calculated using the parameters R_{pu} and R_{pd} given in Table 15 for a given input voltage V_I. For pins set to output, the current drive strength is given by parameters I_{OH} and I_{OL} in Table 15, but for calculating the total static current, you also need to consider any external loads connected to the pin.

I/O pins also contribute to the dynamic power consumption when the pins are switching because the V_{DD} supply provides the current to charge and discharge all internal and external capacitive loads connected to the pin in addition to powering the I/O circuitry.

The contribution from the I/O switching current I_{sw} can be calculated as follows for any given switching frequency f_{sw} if the external capacitive load (C_{ext}) is known (see Table 15 for the internal I/O capacitance):

$$I_{sw} = V_{DD} \times f_{sw} \times (C_{io} + C_{ext})$$

14.5 Termination of unused pins

Table 34 shows how to terminate pins that are **not** used in the application. In many cases, unused pins may should be connected externally or configured correctly by software to minimize the overall power consumption of the part.

Unused pins with GPIO function should be configured as outputs set to LOW with their internal pull-up disabled. To configure a GPIO pin as output and drive it LOW, select the GPIO function in the IOCON register, select output in the GPIO DIR register, and write a 0 to the GPIO PORT register for that pin. Disable the pull-up in the pin's IOCON register.

In addition, it is recommended to configure all GPIO pins that are not bonded out on smaller packages as outputs driven LOW with their internal pull-up disabled.

Table 34. Termination of unused pins

Pin	Default state[1]	Recommended termination of unused pins
$\overline{\text{RESET}}$/PIO0_5	I; PU	In an application that does not use the $\overline{\text{RESET}}$ pin or its GPIO function, the termination of this pin depends on whether deep power-down mode is used: • Deep power-down used: Connect an external pull-up resistor and keep pin in default state (input, pull-up enabled) during all other power modes. • Deep power-down not used and no external pull-up connected: can be left unconnected if internal pull-up is disabled and pin is driven LOW and configured as output by software.
all PIOn_m (not open-drain)	I; PU	Can be left unconnected if driven LOW and configured as GPIO output with pull-up disabled by software.
PIOn_m (I2C open-drain)	IA	Can be left unconnected if driven LOW and configured as GPIO output by software.
VREFP	-	Tie to VDD.
VREFN	-	Tie to VSS.

[1] I = Input, O = Output, IA = Inactive (no pull-up/pull-down enabled), F = floating, PU = Pull-Up.

19. Revision history

Table 37. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC84X v.1.7	20180227	Product data sheet	-	LPC84X v.1.6
Modifications:	• Updated Table 17 “Dynamic characteristic: FRO”: Max values: FRO clock frequency; Condition: −20 °C ≤ T_{amb} ≤ 70 °C and FRO clock frequency; Condition: −40 °C ≤ T_{amb} ≤ 105 °C.			
LPC84X v.1.6	20180216	Product data sheet	-	LPC84X v.1.5
Modifications:	• Updated reflow soldering of the HVQFN48 package to add three figures: Figure 46 “Reflow soldering of the HVQFN48 package (7x7) 1 of 3”, Figure 47 “Reflow soldering of the HVQFN48 package (7x7) 2 of 3” and Figure 48 “Reflow soldering of the HVQFN48 package (7x7) 3 of 3”.			
LPC84X v.1.5	20171214	Product data sheet	-	LPC84X v.1.4
Modifications:	• Updated Table 25 “Dynamic characteristic: Typical wake-up times from low power modes”. • Removed remark from Section 8.17 “Capacitive Touch Interface”: **Remark:** Evaluation kits and software packages for Capacitive Touch will be available in late Q3-2017.			
LPC84X v.1.4	20171128	Product data sheet	-	LPC84X v.1.3
Modifications:	• Updated Table 17 “Dynamic characteristic: FRO”. Added conditions: −20 °C ≤ T_{amb} ≤ 70 °C and −40 °C ≤ T_{amb} ≤ 105 °C. • Updated Figure 8 “LPC84x AHB Memory mapping”. • Updated table notes: Table 15 “Static characteristics, pin characteristics”. • Updated Table 14 “Power consumption for individual analog and digital blocks”: FRO Typical supply current in µA is 89.			
LPC84X v.1.3	20170809	Product data sheet	-	LPC84X v.1.2
Modifications:	• Updated Table 9 “Limiting values”: Added max values for supply and ground pins for LQFP48, HVQFN48, and HVQFN33 packages. • Updated Table 1 “Ordering information”: Description of part number LPC844M201JHI48 and package name, HVQFN48.			
LPC84X v.1.2	20170801	Product data sheet	-	LPC84X v.1.1
Modifications:	• Updated Table 7 “Peripheral configuration in reduced power modes” and Table 8 “Wake-up sources for reduced power modes”: Cap Touch interrupt can wake up from power down mode. • Updated Table 2 “Ordering options”. LPC845M301JHI33 does not have Capacitive Touch.			
LPC84X v.1.1	20170623	Product data sheet	-	LPC84X v.1
Modifications:	• Updated Table 27 “12-bit ADC static characteristics”. • Added a remark to Section 8.17 “Capacitive Touch Interface”: Evaluation kits and software packages for Capacitive Touch will be available in late Q3-2017.			
LPC84X v.1	20170619	Product data sheet	-	-