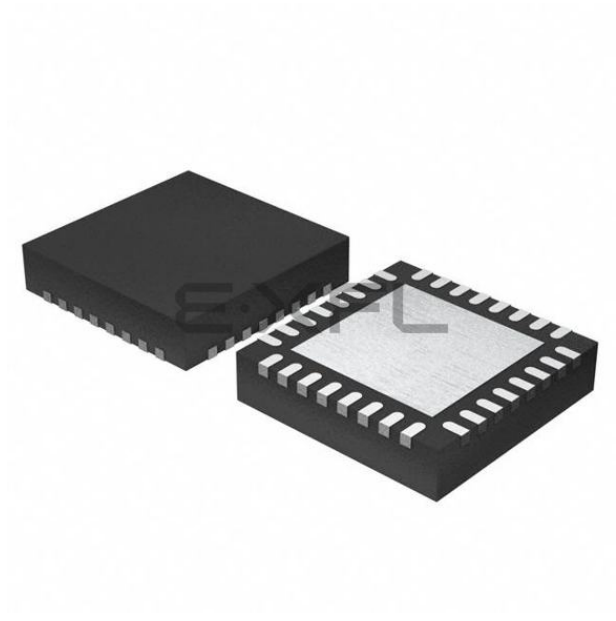


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	30MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, Cap Sense, DMA, POR, PWM, WDT
Number of I/O	29
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 12x12b; D/A 1x10b
Oscillator Type	External, Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-HVQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc845m301jhi33y

5. Marking

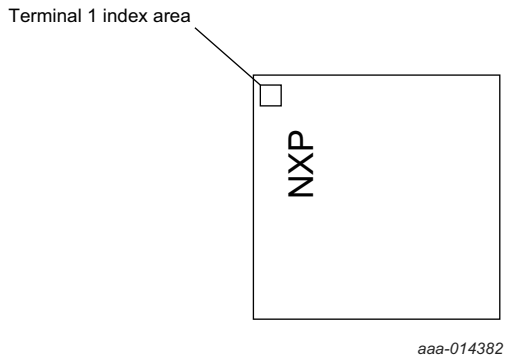


Fig 1. HVQFN48, HVQFN33 package marking

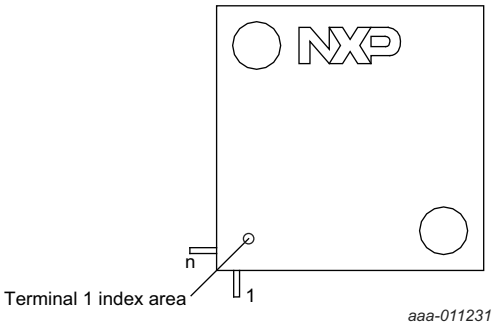


Fig 2. LQFP64, LQFP48 package marking

The LPC84x LQFP64 and LQFP48 packages have the following top-side marking:

- First line: LPC84xMy01
  - y: 3 or 2
- Second line: xxxxxx
- Third line: xxxyywwx[R]x
  - yyww: Date code with yy = year and ww = week.
  - xR = Boot code version and device revision.

The LPC84x HVQFN48 and HVQFN33 packages have the following top-side marking:

- First line: LPC84xMy01
  - y: 3 or 2
- Second line: xxxxxx
- Third line: xxxyywwx[R]x
  - yyww: Date code with yy = year and ww = week.
  - xR = Boot code version and device revision.

Table 3. Device revision table

Revision identifier (R)	Revision description
1A	Initial device revision with Boot ROM version 13.1

Table 4. Pin description

Symbol	LQFP64	LQFP48	HVQFN48	HVQFN33		Reset state[1]	Type	Description
PIO0_14/ ACMP_I3/ADC_2	49	37	37	25	[2]	I; PU	IO	**PIO0_14 —** General-purpose port 0 input/output 14.
							A	**ACMP_I3 —** Analog comparator common input 3.
							A	**ADC_2 —** ADC input 2.
PIO0_15	30	22	22	15	[5]	I; PU	IO	**PIO0_15 —** General-purpose port 0 input/output 15.
PIO0_16	19	15	15	10	[4]	I; PU	IO	**PIO0_16 —** General-purpose port 0 input/output 16.
PIO0_17/ADC_9/ DACOUT_0	63	48	48	32	[2]	I; PU	IO	**PIO0_17 —** General-purpose port 0 input/output 17.
							A	**ADC_9 —** ADC input 9.
							A	**DACOUT_0 —** DAC Output 0.
PIO0_18/ADC_8	61	47	47	31	[2]	I; PU	IO	**PIO0_18 —** General-purpose port 0 input/output 18.
							A	**ADC_8 —** ADC input 8.
PIO0_19/ADC_7	60	46	46	30	[2]	I; PU	IO	**PIO0_19 —** General-purpose port 0 input/output 19.
							A	**ADC_7 —** ADC input 7.
PIO0_20/ADC_6	58	45	45	29	[2]	I; PU	IO	**PIO0_20 —** General-purpose port 0 input/output 20.
							A	**ADC_6 —** ADC input 6.
PIO0_21/ADC_5	57	44	44	28	[2]	I; PU	IO	**PIO0_21 —** General-purpose port 0 input/output 21.
							A	**ADC_5 —** ADC input 5.
PIO0_22/ADC_4	55	43	43	27	[2]	I; PU	IO	**PIO0_22 —** General-purpose port 0 input/output 22.
							A	**ADC_4 —** ADC input 4.
PIO0_23/ADC_3/ ACMP_I4	51	39	39	26	[2]	I; PU	IO	**PIO0_23 —** General-purpose port 0 input/output 23.
							A	**ADC_3 —** ADC input 3.
							A	**ACMP_I4 —** Analog comparator common input 4.
PIO0_24	28	20	20	14	[5]	I; PU	IO	**PIO0_24 —** General-purpose port 0 input/output 24. In ISP mode, this is the U0_RXD pin.
PIO0_25	27	19	19	13	[5]	I; PU	IO	**PIO0_25 —** General-purpose port 0 input/output 25. In ISP mode, this pin is the U0_TXD pin.
PIO0_26	23	18	18	12	[5]	I; PU	IO	**PIO0_26 —** General-purpose port 0 input/output 26.
PIO0_27	21	17	17	11	[5]	I; PU	IO	**PIO0_27 —** General-purpose port 0 input/output 27.
PIO0_28/ WKTCLKIN	10	7	7	5	[3]	I; PU	IO	**PIO0_28 —** General-purpose port 0 input/output 28. This pin can host an external clock for the self-wake-up timer. To use the pin as a self-wake-up timer clock input, select the external clock in the wake-up timer CTRL register. The external clock input is active in all power modes, including deep power-down.
PIO0_29/ DACOUT_1	50	38	38	-	[5]	I; PU	IO	**PIO0_29 —** General-purpose port 0 input/output 29.
							A	**DACOUT_1 —** DAC output 1.
PIO0_30/ACMP_I5	54	42	42	-	[5]	I; PU	IO	**PIO0_30 —** General-purpose port 0 input/output 30.
							A	**ACMP_I5 —** Analog comparator common input 5.

8.9.1 Standard I/O pad configuration

Figure 9 shows the possible pin modes for standard I/O pins with analog input function:

- Digital output driver with configurable open-drain output.
- Digital input: Weak pull-up resistor (PMOS device) enabled/disabled.
- Digital input: Weak pull-down resistor (NMOS device) enabled/disabled.
- Digital input: Repeater mode enabled/disabled.
- Digital input: Programmable input digital filter selectable on all pins.
- Analog input: Selected through the switch matrix.

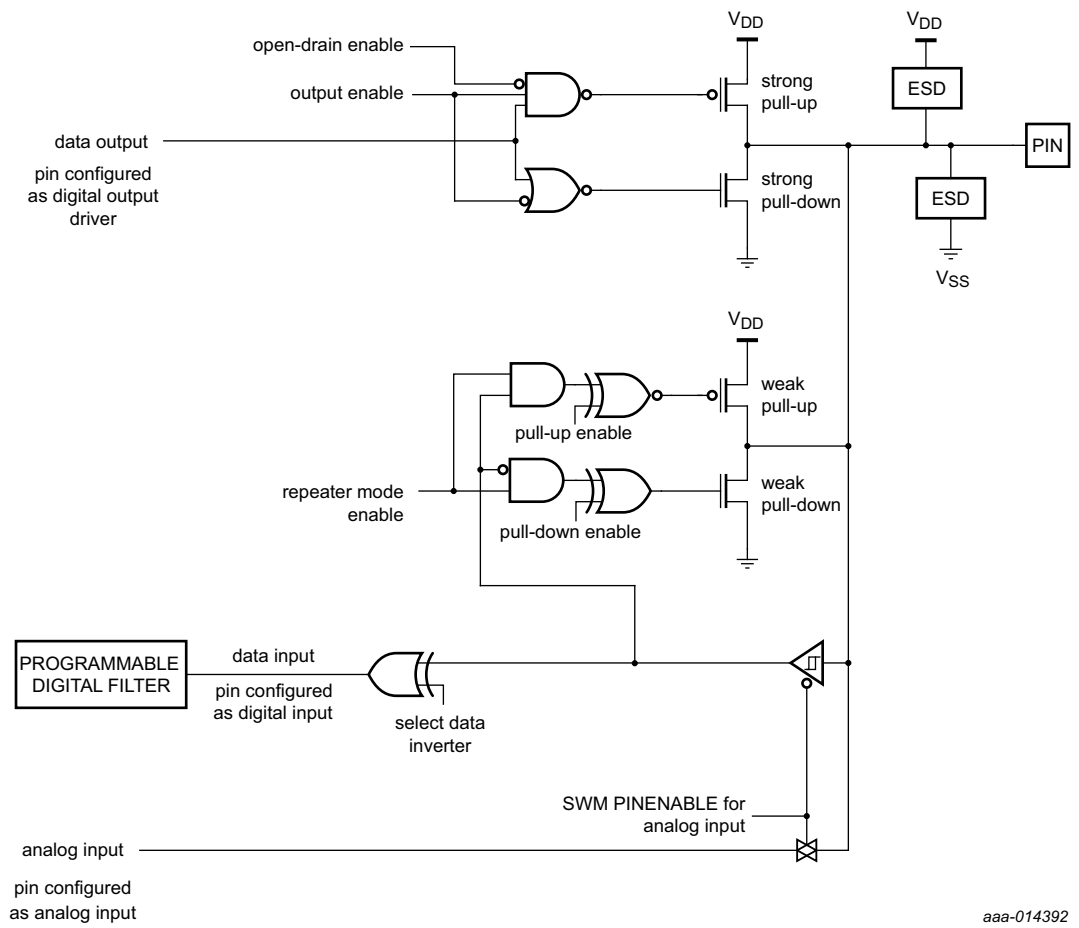


Fig 9. Standard I/O pad configuration

- The following conditions define an event: a counter match condition, an input (or output) condition such as a rising or falling edge or level, a combination of match and/or input/output condition.
- Selected events can limit, halt, start, or stop a counter or change its direction.
- Events trigger state changes, output toggles, interrupts, and DMA transactions.
- Match register 0 can be used as an automatic limit.
- In bidirectional mode, events can be enabled based on the count direction.
- Match events can be held until another qualifying event occurs.

- State control features:
  - A state is defined by events that can happen in the state while the counter is running.
  - A state changes into another state as a result of an event.
  - Each event can be assigned to one or more states.
  - State variable allows sequencing across multiple counter cycles.
- One SCTimer match output can be selected as ADC hardware trigger input.

8.18.2 SCTimer/PWM input MUX (INPUT MUX)

Each input of the SCTimer/PWM is connected to a programmable multiplexer which allows to connect one of multiple internal or external sources to the input. The available sources are the same for each SCTimer/PWM input and can be selected from four pins configured through the switch matrix, the ADC threshold compare interrupt, the comparator output, and the Arm core signals Arm_TXEV and DEBUG_HALTED.

8.19 CTIMER

8.19.1 General-purpose 32-bit timers/external event counter

The LPC84x has one general-purpose 32-bit timer/counter.

The timer/counter is designed to count cycles of the system derived clock or an externally-supplied clock. It can optionally generate interrupts, generate timed DMA requests, or perform other actions at specified timer values, based on four match registers. Each timer/counter also includes two capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt.

8.19.2 Features

- A 32-bit timer/counter with a programmable 32-bit prescaler.
- Counter or timer operation.
- Up to three 32-bit captures can take a snapshot of the timer value when an input signal transitions. A capture event may also optionally generate an interrupt. The number of capture inputs for each timer that are actually available on device pins can vary by device.
- Four 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.

8.27.5.1 Sleep mode

When sleep mode is entered, the clock to the core is stopped. Resumption from the sleep mode does not need any special sequence but re-enabling the clock to the Arm core.

In sleep mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during sleep mode and may generate interrupts to cause the processor to resume execution. sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, and internal buses.

8.27.5.2 Deep-sleep mode

In deep-sleep mode, the LPC84x core is in sleep mode and all peripheral clocks and all clock sources are off except for the FRO and watchdog oscillator or low-power oscillator if selected. The FRO output is disabled. In addition, all analog blocks are shut down and the flash is in standby mode. In deep-sleep mode, the application can keep the watchdog oscillator and the BOD circuit running for self-timed wake-up and BOD protection.

The LPC84x can wake up from deep-sleep mode via a reset, digital pins selected as inputs to the pin interrupt block, a watchdog timer interrupt, an interrupt from Capacitive Touch, or an interrupt from the USART (if the USART is configured in synchronous slave mode), the SPI, or the I2C blocks (in slave mode).

Any interrupt used for waking up from deep-sleep mode must be enabled in one of the SYSCON wake-up enable registers and the NVIC.

Deep-sleep mode saves power and allows for short wake-up times.

8.27.5.3 Power-down mode

In power-down mode, the LPC84x is in sleep mode and all peripheral clocks and all clock sources are off except for watchdog oscillator or low-power oscillator if selected. In addition, all analog blocks and the flash are shut down. In power-down mode, the application can keep the watchdog oscillator and the BOD circuit running for self-timed wake-up and BOD protection.

The LPC84x can wake up from power-down mode via a reset, digital pins selected as inputs to the pin interrupt block, a watchdog timer interrupt, an interrupt from Capacitive Touch, or an interrupt from the USART (if the USART is configured in synchronous slave mode), the SPI, or the I2C blocks (in slave mode).

Any interrupt used for waking up from power-down mode must be enabled in one of the SYSCON wake-up enable registers and the NVIC.

Power-down mode reduces power consumption compared to deep-sleep mode at the expense of longer wake-up times.

8.27.5.4 Deep power-down mode

In deep power-down mode, power is shut off to the entire chip except for the $\overline{\text{WAKEUP}}$ pin and the self-wake-up timer. The LPC84x can wake up from deep power-down mode via the $\overline{\text{WAKEUP}}$ pin, $\overline{\text{RESET}}$ pin, or without an external signal by using the time-out of the self-wake-up timer (see Section 8.22).

9. Limiting values

Table 9. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage (core and external rail)		[2]	−0.5	+4.6	V
V_{DDA}	Analog supply voltage	on pin VDDA		−0.5	+4.6	V
V_{ref}	reference voltage	on pin VREFP		−0.5	V_{DD}	V
V_I	input voltage	5 V tolerant I/O pins; $V_{DD} \geq 1.8$ V	[3][4]	−0.5	+5.5	V
		on I2C open-drain pins	[5]	−0.5	+5.5	V
		3 V tolerant I/O pin $ACMPV_{REF}$	[6]	−0.5	+3.6	V
V_{IA}	analog input voltage	on digital pins configured for an analog function	[7][8] [9]	−0.5	+4.6	V
$V_{i(xtal)}$	crystal input voltage		[2]	−0.5	+2.5	V
I_{DD}	supply current	per supply pin (LQFP64)		-	100	mA
		per supply pin (LQFP48, HVQFN48)		-	75	
		per supply pin (HVQFN33)		-	50	
I_{SS}	ground current	per ground pin (LQFP64);		-	100	mA
		per ground pin (LQFP48, HVQFN48)		-	75	
		per ground pin (HVQFN33)		-	100	
I_{latch}	I/O latch-up current	$-(0.5V_{DD}) < V_I < (1.5V_{DD})$; $T_j < 125$ °C		-	100	mA
T_{stg}	storage temperature		[10]	−65	+150	°C
$T_{j(max)}$	maximum junction temperature			-	150	°C

Table 9. Limiting values *…continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
$P_{tot(pack)}$	total power dissipation (per package)	LQFP64, based on package heat transfer, not device power consumption	[12]	-	0.66	W
		LQFP64, based on package heat transfer, not device power consumption	[13]	-	0.48	W
		LQFP48, based on package heat transfer, not device power consumption	[12]	-	0.48	W
		LQFP48, based on package heat transfer, not device power consumption	[13]	-	0.34	W
		HVQFN48, based on package heat transfer, not device power consumption	[12]	-	1.12	W
		HVQFN48, based on package heat transfer, not device power consumption	[13]	-	0.46	W
		HVQFN33, based on package heat transfer, not device power consumption	[12]	-	0.98	W
		HVQFN33, based on package heat transfer, not device power consumption	[13]	-	0.34	W
V_{esd}	electrostatic discharge voltage	human body model; all pins		-	2000	V

[1] The following applies to the limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Maximum/minimum voltage above the maximum operating voltage (see Table 13) and below ground that can be applied for a short time (< 10 ms) to a device without leading to irrecoverable failure. Failure includes the loss of reliability and shorter lifetime of the device.

[3] Applies to all 5 V tolerant I/O pins except true open-drain pins PIO0_10 and PIO0_11 and except the 3 V tolerant pin PIO0_6.

[4] Including the voltage on outputs in 3-state mode.

[5] V_{DD} present or not present. Compliant with the I^2C-bus standard. 5.5 V can be applied to this pin when V_{DD} is powered down.

[6] V_{DD} present or not present.

[7] An ADC input voltage above 3.6 V can be applied for a short time without leading to immediate, unrecoverable failure. Accumulated exposure to elevated voltages at 4.6 V must be less than 10^6 s total over the lifetime of the device. Applying an elevated voltage to the ADC inputs for a long time affects the reliability of the device and reduces its lifetime.

[8] If the comparator is configured with the common mode input $V_{IC} = V_{DD}$, the other comparator input can be up to 0.2 V above or below V_{DD} without affecting the hysteresis range of the comparator function.

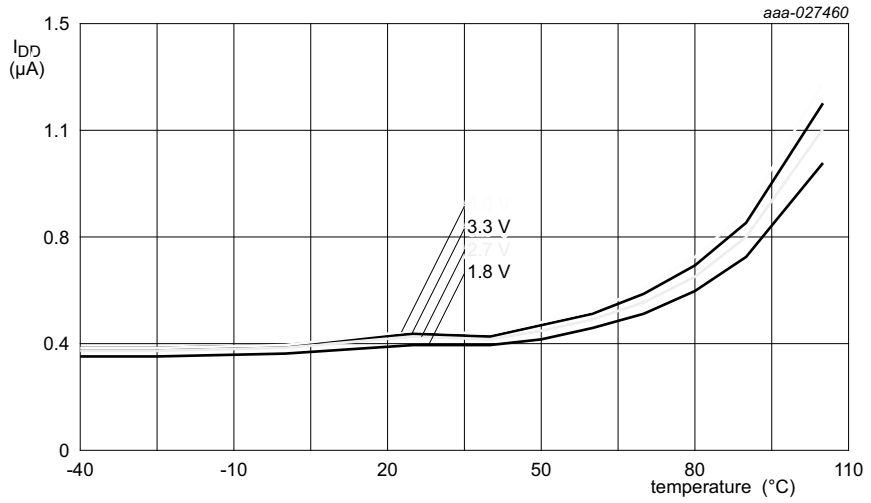
[9] It is recommended to connect an overvoltage protection diode between the analog input pin and the voltage supply pin.

[10] Dependent on package type.

[11] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

[12] JEDEC (4.5 in × 4 in); still air.

[13] Single layer (4.5 in × 3 in); still air.



WKT running with external 32 kHz clock. Clock input waveform: square wave with rise time and fall time of 5 ns.

Fig 21. Deep power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD} (external 32 kHz input clock)

11.5 Pin characteristics

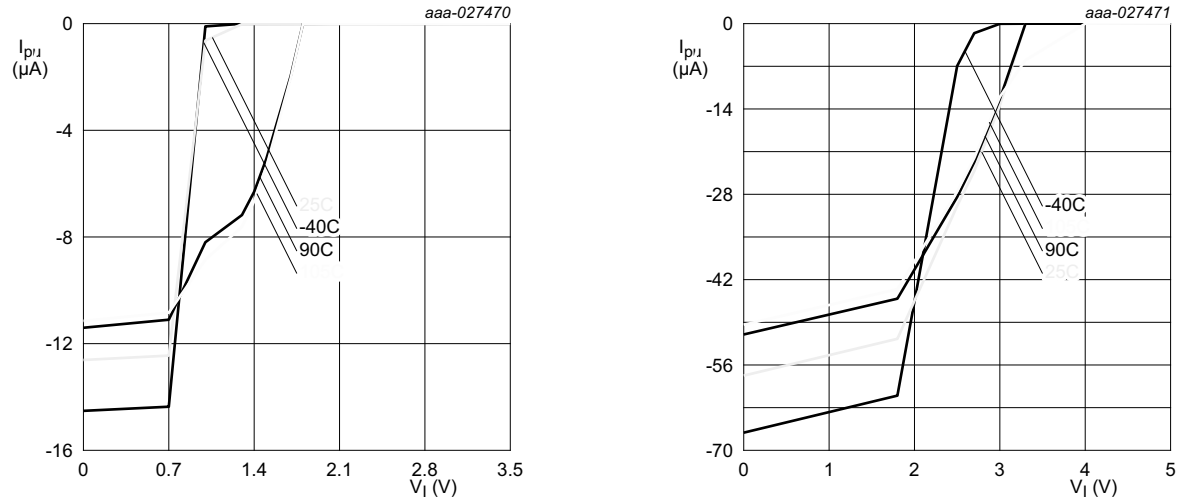
Table 15. Static characteristics, pin characteristics

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
Standard port pins configured as digital pins, RESET							
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled		-	0.5	10[2]	nA
I_{IH}	HIGH-level input current	$V_I = V_{DD}$; on-chip pull-down resistor disabled		-	0.5	10[2]	nA
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD}$; on-chip pull-up/down resistors disabled		-	0.5	10[2]	nA
V_I	input voltage	$V_{DD} \geq$ 1.8 V; 5 V tolerant pins except PIO0_6		0	-	5	V
		V_{DD} = 0 V		0	-	3.6	V
V_O	output voltage	output active		0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD}$	V
V_{hys}	hysteresis voltage			-	0.4	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = 4 mA; 2.5 V <= V_{DD} <= 3.6 V		$V_{DD} - 0.4$	-	-	V
		I_{OH} = 3 mA; 1.8 V <= V_{DD} < 2.5 V		$V_{DD} - 0.5$	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA; 2.5 V <= V_{DD} <= 3.6 V		-	-	0.5	V
		I_{OL} = 3 mA; 1.8 V <= V_{DD} < 2.5 V		-	-	0.5	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD} - 0.4$ V; 2.5 V ≤ V_{DD} ≤ 3.6 V		4	-	-	mA
		$V_{OH} = V_{DD} - 0.5$ V; 1.8 V ≤ V_{DD} < 2.5 V		3	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.5 V 2.5 V ≤ V_{DD} ≤ 3.6 V		4	-	-	mA
		1.8 V ≤ V_{DD} < 2.5 V		3	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V	[5]	-	-	45	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DD}$	[5]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V	[6]	10	50	150	µA
I_{pu}	pull-up current	V_I = 0 V; 2.0 V ≤ V_{DD} ≤ 3.6 V	[6]	15	50	85	µA
		1.8 V ≤ V_{DD} < 2.0 V		10	50	85	
		$V_{DD} < V_I$ < 5 V		0	0	0	µA
High-drive output pin configured as digital pin (PIO0_2, PIO0_3, PIO0_12, and PIO0_16)							
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled		-	0.5	10[2]	nA
I_{IH}	HIGH-level input current	$V_I = V_{DD}$; on-chip pull-down resistor disabled		-	0.5	10[2]	nA

Table 15. Static characteristics, pin characteristics *...continued*
T_{amb} = −40 °C to +105 °C, unless otherwise specified.

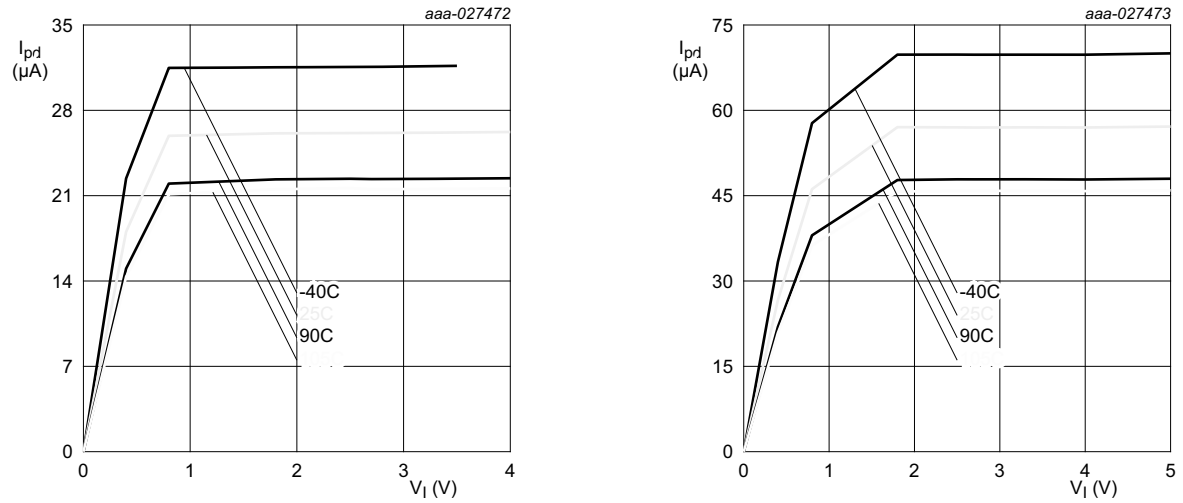
Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{OZ}	OFF-state output current	V_O = 0 V; V_O = V_{DD}; on-chip pull-up/down resistors disabled		-	0.5	10[2]	nA
V_I	input voltage	$V_{DD} \geq$ 1.8 V		0	-	5.0	V
		V_{DD} = 0 V		0	-	3.6	V
V_O	output voltage	output active		0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage			0.7V_{DD}	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.3V_{DD}	V
V_{hys}	hysteresis voltage			-	0.4	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = 20 mA; 2.5 V <= V_{DD} < 3.6 V		V_{DD} − 0.5	-	-	V
		I_{OH} = 12 mA; 1.8 V <= V_{DD} < 2.5 V		V_{DD} − 0.5	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA 2.5 V <= V_{DD} < 3.6 V		-	-	0.5	V
		I_{OL} = 3 mA 1.8 V <= V_{DD} < 2.5 V		-	-	0.5	V
I_{OH}	HIGH-level output current	V_{OH} = V_{DD} − 0.5 V; 2.5 V <= V_{DD} < 3.6 V		20	-	-	mA
		V_{OH} = V_{DD} − 0.5 V; 1.8 V <= V_{DD} < 2.5 V		12	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.5 V 2.5 V ≤ V_{DD} ≤ 3.6 V		4	-	-	mA
		1.8 V ≤ V_{DD} < 2.5 V		3	-	-	mA
I_{OLS}	LOW-level short-circuit output current	V_{OL} = V_{DD}	[5]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V	[6]	10	50	150	µA
I_{pu}	pull-up current	V_I = 0 V	[6]	−10	−50	−85	µA
		V_{DD} < V_I < 5 V		0	0	0	µA
I^2C-bus pins (PIO0_10 and PIO0_11)							
V_{IH}	HIGH-level input voltage			0.7V_{DD}	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.3V_{DD}	V
V_{hys}	hysteresis voltage			-	0.05V_{DD}	-	V
I_{OL}	LOW-level output current	V_{OL} = 0.5 V; I^2C-bus pins configured as standard mode pins 2.5 V <= V_{DD} < 3.6 V		3.5	-	-	mA
		1.8 V <= V_{DD} < 2.5 V		3	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.5 V; I^2C-bus pins configured as Fast-mode Plus pins; 2.5 V <= V_{DD} < 3.6 V		20	-	-	mA
		1.8 V <= V_{DD} < 2.5 V		16	-	-	mA



Conditions: V_{DD} = 1.8 V; standard port pins.

Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 27. Typical pull-up current I_{PU} versus input voltage V_I



Conditions: V_{DD} = 1.8 V; standard port pins.

Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 28. Typical pull-down current I_{PD} versus input voltage V_I

[8] The maximum $t_{HD;DAT}$ could be 3.45 μs and 0.9 μs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time (see *UM10204*). This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[9] $t_{SU;DAT}$ is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.

[10] A Fast-mode I^2C-bus device can be used in a Standard-mode I^2C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I^2C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

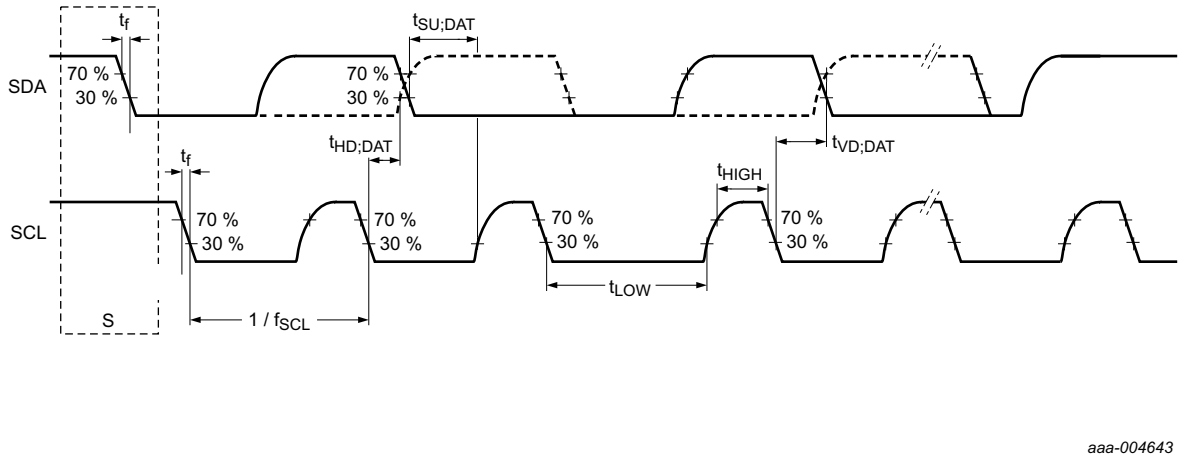


Fig 29. I^2C-bus pins clock timing

13.2.1 ADC input impedance

Figure 34 shows the ADC input impedance. In this figure:

- ADCx represents ADC input channel 0.
- ADCy represents ADC input channels 1 to 11.
- R_1 and R_{sw} are the switch-on resistance on the ADC input channel.
- If ADC input channel 0 is selected, the ADC input signal goes through $R_1 + R_{sw}$ to the sampling capacitor (C_{ia}).
- If ADC input channels 1 to 11 are selected, the ADC input signal goes through R_{sw} to the sampling capacitor (C_{ia}).
- Typical values, R_1 = 2.5 kΩ, R_{sw} = 25 Ω
- See Table 11 for C_{io}.
- See Table 27 for C_{ia}.

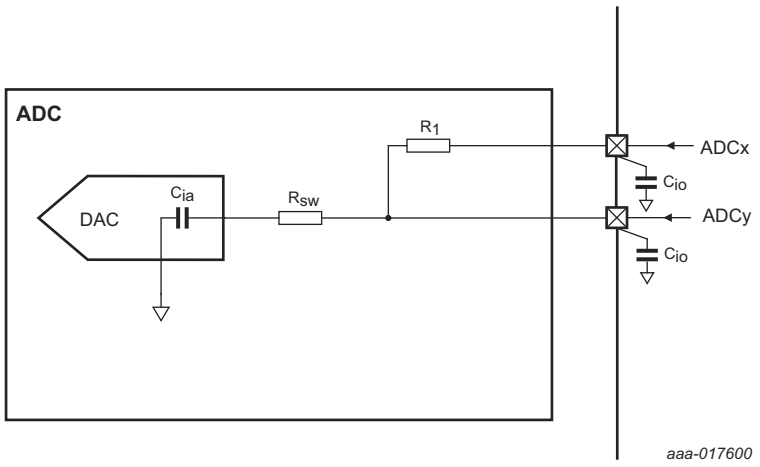


Fig 34. ADC input impedance

Table 31. Comparator voltage ladder reference static characteristics

V_{DD} = 1.8 V to 3.6 V. T_{amb} = -40 °C to + 105°C; external or internal reference.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$E_{V(O)}$	output voltage error	decimal code = 00	[2]	-	±6	-	mV
		decimal code = 08		-	±1	-	%
		decimal code = 16		-	±1	-	%
		decimal code = 24		-	±1	-	%
		decimal code = 30		-	±1	-	%
		decimal code = 31		-	±1	-	%

[1] Characterized though limited samples. Not tested in production.

[2] All peripherals except comparator, temperature sensor, and FRO turned off.

13.4 DAC

Table 32. 10-bit DAC electrical characteristics

V_{DD} = V_{DDA} = 2.7 V to 3.6 V; T_{amb} = −40 °C to +105 °C unless otherwise specified

Symbol	Parameter		Min	Typ	Max	Unit
E_D	differential linearity error	[1][2]	-	0.4	-	LSB
$E_{L(adj)}$	integral non-linearity	[1][2]	-	6.0	-	LSB
E_O	offset error	[1][2]	-	±57.0	-	mV
E_G	gain error	[1][2]	-	±36.0	-	mV
C_L	load capacitance		-	200	-	pF
R_{OUT}	PIO0_17/DACOUT_0 pin resistance	[3]	-	90	200	Ω
R_{OUT}	PIO0_29/DACOUT_1 pin resistance	[3]	-	2	5	kΩ
V_{OUT}	Output voltage range		0.175	-	V_{DDA}-0.175	V

[1] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C) and V_{DD} = V_{DDA} = 3.6 V.

[2] Characterized through bench measurements, not tested in production.

[3] DAC output voltage depends on the voltage divider ratio of the R_{OUT} and external load resistance.

14. Application information

14.1 Start-up behavior

Figure 36 shows the start-up timing after reset. The FRO 12 MHz oscillator provides the default clock at Reset and provides a clean system clock shortly after the supply pins reach operating voltage.

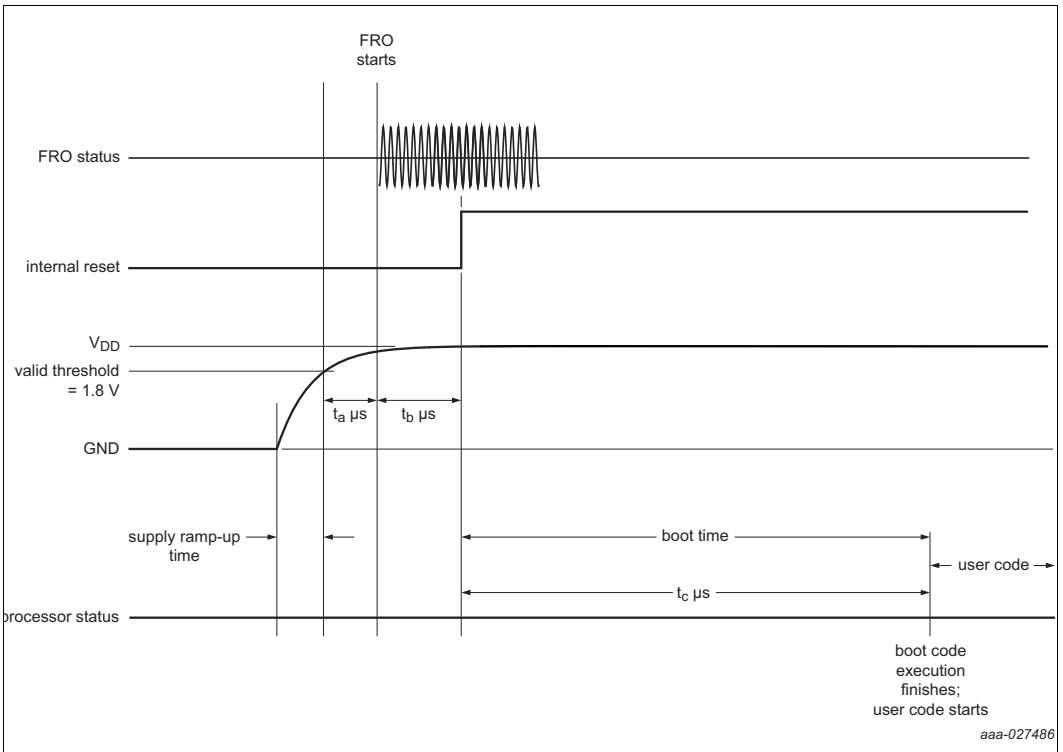


Fig 36. Start-up timing

Table 33. Typical start-up timing parameters

Parameter	Description	Value
t_a	FRO start time	≤ 26 µs
t_b	Internal reset de-asserted	101 µs
t_c	Boot time	51 µs

14.2.1 XTAL Printed Circuit Board (PCB) design guidelines

- Connect the crystal and external load capacitors on the PCB as close as possible to the oscillator input and output pins of the chip.
- The length of traces in the oscillation circuit should be as short as possible and must not cross other signal lines.
- Ensure that the load capacitors CX1, CX2, and CX3, in case of third overtone crystal usage, have a common ground plane.
- Loops must be made as small as possible to minimize the noise coupled in through the PCB and to keep the parasitics as small as possible.
- Lay out the ground (GND) pattern under crystal unit.
- Do not lay out other signal lines under crystal unit for multi-layered PCB.

14.2.2 XTAL input

The input voltage to the on-chip oscillators is limited to 1.95 V. If the oscillator is driven by a clock in slave mode, it is recommended to couple the input through a capacitor with C_i = 100 pF. To limit the input voltage to the specified range, choose an additional capacitor to ground C_g which attenuates the input voltage by a factor $C_i/(C_i + C_g)$. In slave mode, a minimum of 200 mV(RMS) is needed.

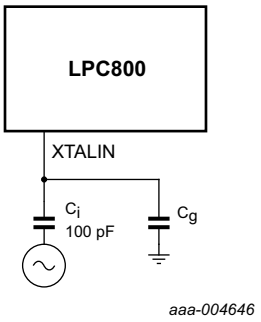


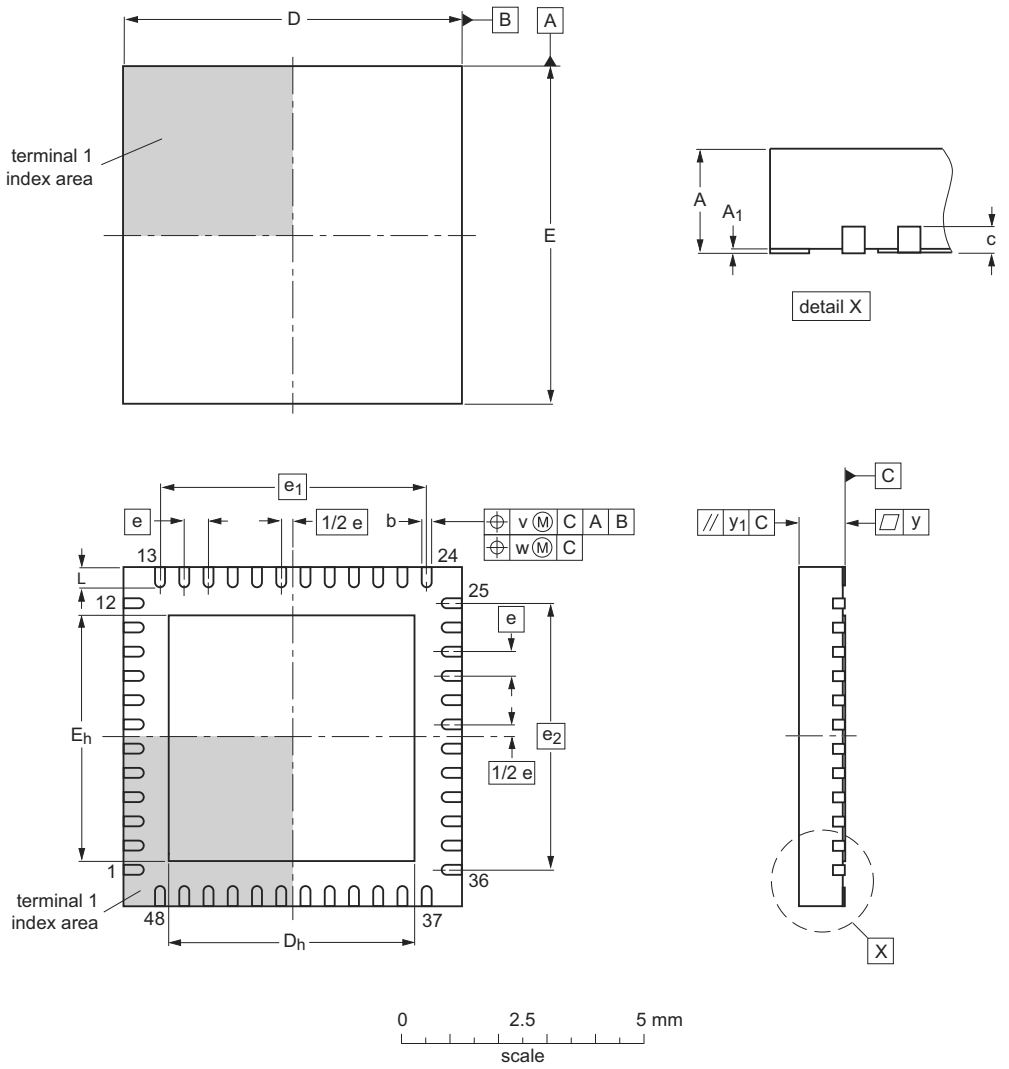
Fig 38. Slave mode operation of the on-chip oscillator

In slave mode the input clock signal should be coupled with a capacitor of 100 pF (Figure 38), with an amplitude between 200 mV (RMS) and 1000 mV (RMS). This corresponds to a square wave signal with a signal swing of between 280 mV and 1.4 V. The XTALOUT pin in this configuration can be left unconnected.

14.3 Connecting power, clocks, and debug functions

Figure 39 shows the basic board connections used to power the LPC84x, connect the external crystal, and provide debug capabilities via the serial wire port.

HVQFN48: plastic thermal enhanced very thin quad flat package; no leads; 48 terminals; body 7 x 7 x 0.85 mm **SOT619-1**



Dimensions (mm are the original dimensions)

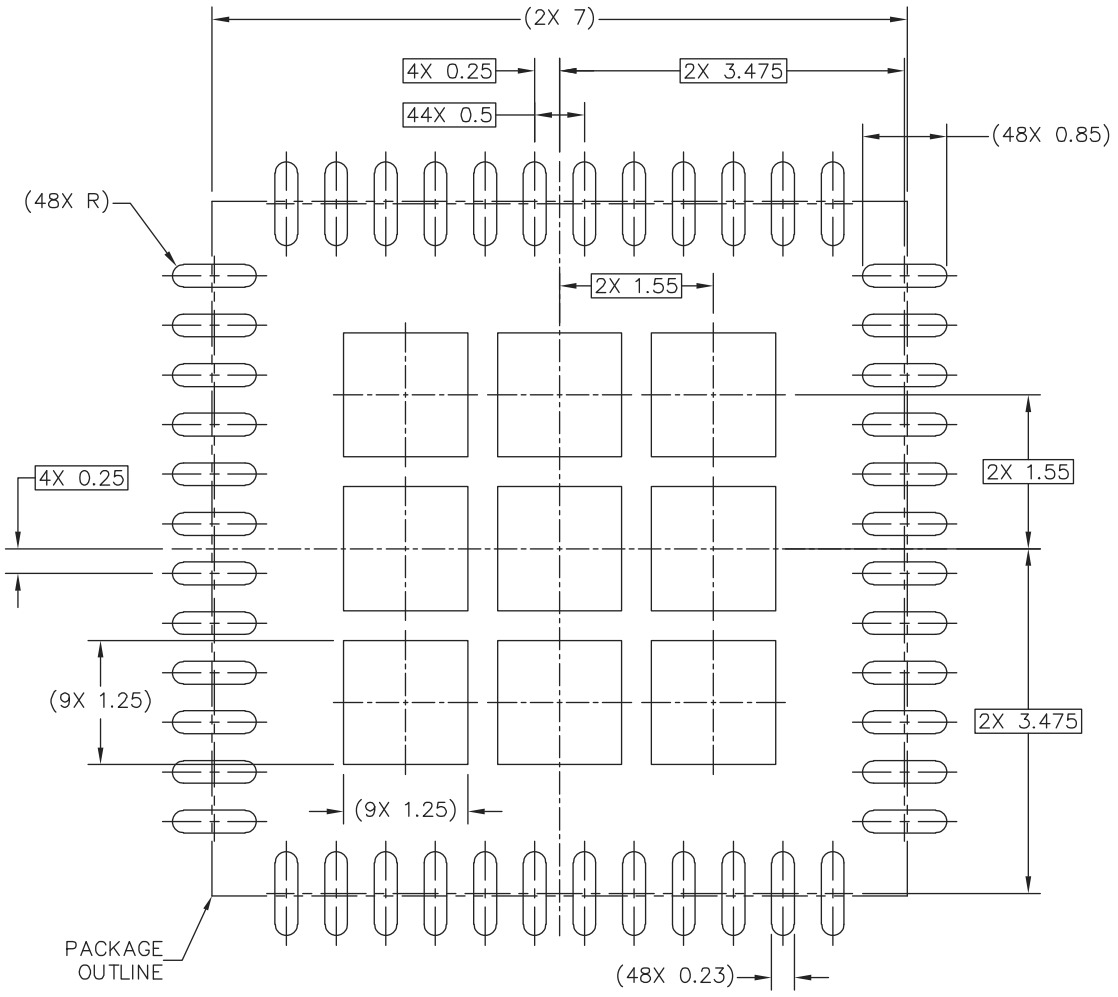
Unit[1]		A	A_1	b	C	D	D_h	E	E_h	e	e_1	e_2	L	v	w	y	y_1
	max	1.00	0.05	0.30		7.1	5.25	7.1	5.25				0.5				
mm	nom	0.85	0.02	0.21	0.2	7.0	5.10	7.0	5.10	0.5	5.5	5.5	0.4	0.1	0.05	0.05	0.1
	min	0.80	0.00	0.18		6.9	4.95	6.9	4.95				0.3				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included

sot619-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT619-1		MO-220				~~02-10-18~~ 12-11-22

Fig 43. Package outline HVQFN48 7 x 7x 0.85 mm (SOT619-1)



RECOMMENDED STENCIL THICKNESS 0.125

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

 DATE: 13 DEC 2017

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: SOT619–1	REVISION: 0	

Fig 48. Reflow soldering of the HVQFN48 package (7x7) 3 of 3

20. Legal information

20.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

20.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

20.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

20.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

I²C-bus — logo is a trademark of NXP B.V.

21. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**