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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	30MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, Cap Sense, DMA, POR, PWM, WDT
Number of I/O	42
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 12x12b; D/A 2x10b
Oscillator Type	External, Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-HVQFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc845m301jhi48e

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC845M301JBD64	LQFP64	Plastic low profile quad flat package; 64 leads; body 10× 10 × 1.4 mm	SOT314-2
LPC845M301JBD48	LQFP48	Plastic low profile quad flat package; 48 leads; body 7× 7 × 1.4 mm	SOT313-2
LPC845M301JHI48	HVQFN48	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 48 terminals; body 7× 7 × 0.85 mm	SOT619-1
LPC845M301JHI33	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 5 × 5 × 0.85 mm	SOT617-11
LPC844M201JBD64	LQFP64	Plastic low profile quad flat package; 64 leads; body 10× 10 × 1.4 mm	SOT314-2
LPC844M201JBD48	LQFP48	Plastic low profile quad flat package; 48 leads; body 7× 7 × 1.4 mm	SOT313-2
LPC844M201JHI48	HVQFN48	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 48 terminals; body 7 × 7 × 0.85 mm	SOT619-1
LPC844M201JHI33	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 5 × 5 × 0.85 mm	SOT617-11

4.1 Ordering options

Table 2. Ordering options

Type number	Flash/KB	SRAM/KB	USART	I^2C	SPI	DAC	Capacitive Touch	GPIO	Package
LPC845M301JBD64	64	16	5	4	2	2	yes	54	LQFP64
LPC845M301JBD48	64	16	5	4	2	2	yes	42	LQFP48
LPC845M301JHI48	64	16	5	4	2	2	yes	42	HVQFN48
LPC845M301JHI33	64	16	5	4	2	1	-	29	HVQFN33
LPC844M201JBD64	64	8	2	2	2	-	-	54	LQFP64
LPC844M201JBD48	64	8	2	2	2	-	-	42	LQFP48
LPC844M201JHI48	64	8	2	2	2	-	-	42	HVQFN48
LPC844M201JHI33	64	8	2	2	2	-	-	29	HVQFN33

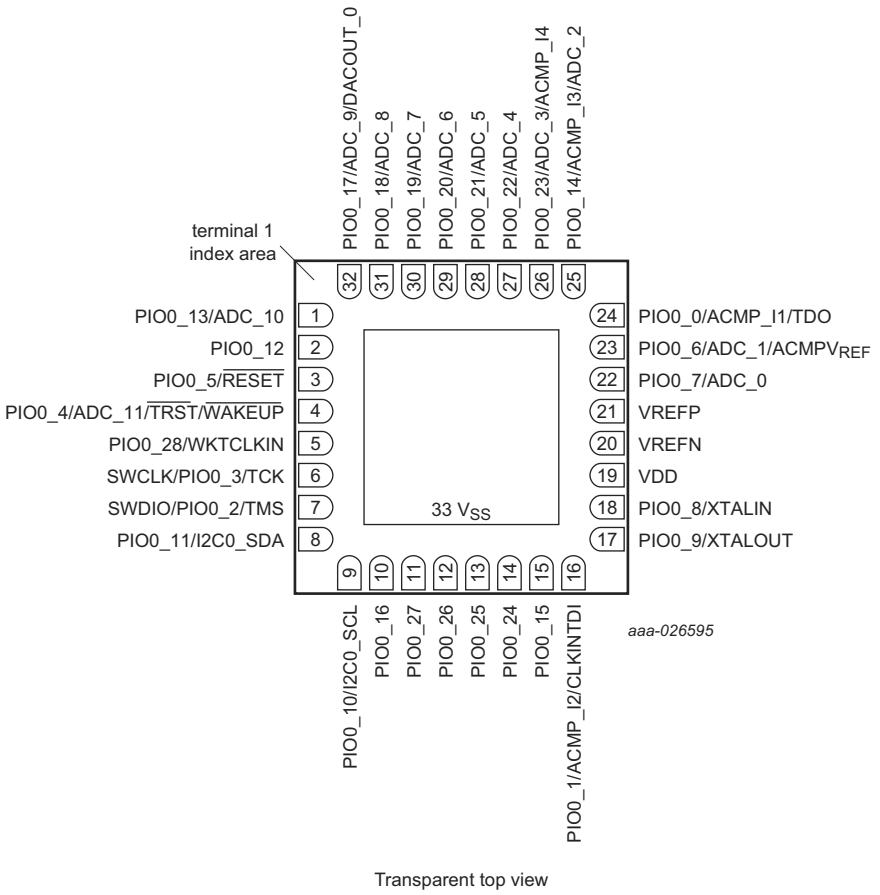


Fig 7. Pin configuration HVQFN33 package

7.2 Pin description

The pin description table shows the pin functions that are fixed to specific pins on each package. See Table 4. These fixed-pin functions are selectable through the switch matrix between GPIO and the comparator, ADC, SWD, RESET, and the XTAL pins. By default, the GPIO function is selected except on pins PIO0_2, PIO0_3, and PIO0_5. JTAG functions are available in boundary scan mode only.

Movable functions for the I^2C, USART, SPI, CTimer, SCT pins, and other peripherals can be assigned through the switch matrix to any pin that is not power or ground in place of the pin's fixed functions.

The following exceptions apply:

Do not assign more than one output to any pin. However, an output and/or one or more inputs can be assigned to a pin. Once any function is assigned to a pin, the pin's GPIO functionality is disabled.

Pin PIO0_4 triggers a wake-up from deep power-down mode. If the part must wake up from deep power-down mode via an external pin, do not assign any movable function to this pin.

Table 4. Pin description

Symbol	LQFP64	LQFP48	HVQFN48	HVQFN33		Reset state[1]	Type	Description
PIO0_14/ ACMP_I3/ADC_2	49	37	37	25	[2]	I; PU	IO	**PIO0_14 —** General-purpose port 0 input/output 14.
							A	**ACMP_I3 —** Analog comparator common input 3.
							A	**ADC_2 —** ADC input 2.
PIO0_15	30	22	22	15	[5]	I; PU	IO	**PIO0_15 —** General-purpose port 0 input/output 15.
PIO0_16	19	15	15	10	[4]	I; PU	IO	**PIO0_16 —** General-purpose port 0 input/output 16.
PIO0_17/ADC_9/ DACOUT_0	63	48	48	32	[2]	I; PU	IO	**PIO0_17 —** General-purpose port 0 input/output 17.
							A	**ADC_9 —** ADC input 9.
							A	**DACOUT_0 —** DAC Output 0.
PIO0_18/ADC_8	61	47	47	31	[2]	I; PU	IO	**PIO0_18 —** General-purpose port 0 input/output 18.
							A	**ADC_8 —** ADC input 8.
PIO0_19/ADC_7	60	46	46	30	[2]	I; PU	IO	**PIO0_19 —** General-purpose port 0 input/output 19.
							A	**ADC_7 —** ADC input 7.
PIO0_20/ADC_6	58	45	45	29	[2]	I; PU	IO	**PIO0_20 —** General-purpose port 0 input/output 20.
							A	**ADC_6 —** ADC input 6.
PIO0_21/ADC_5	57	44	44	28	[2]	I; PU	IO	**PIO0_21 —** General-purpose port 0 input/output 21.
							A	**ADC_5 —** ADC input 5.
PIO0_22/ADC_4	55	43	43	27	[2]	I; PU	IO	**PIO0_22 —** General-purpose port 0 input/output 22.
							A	**ADC_4 —** ADC input 4.
PIO0_23/ADC_3/ ACMP_I4	51	39	39	26	[2]	I; PU	IO	**PIO0_23 —** General-purpose port 0 input/output 23.
							A	**ADC_3 —** ADC input 3.
							A	**ACMP_I4 —** Analog comparator common input 4.
PIO0_24	28	20	20	14	[5]	I; PU	IO	**PIO0_24 —** General-purpose port 0 input/output 24. In ISP mode, this is the U0_RXD pin.
PIO0_25	27	19	19	13	[5]	I; PU	IO	**PIO0_25 —** General-purpose port 0 input/output 25. In ISP mode, this pin is the U0_TXD pin.
PIO0_26	23	18	18	12	[5]	I; PU	IO	**PIO0_26 —** General-purpose port 0 input/output 26.
PIO0_27	21	17	17	11	[5]	I; PU	IO	**PIO0_27 —** General-purpose port 0 input/output 27.
PIO0_28/ WKTCLKIN	10	7	7	5	[3]	I; PU	IO	**PIO0_28 —** General-purpose port 0 input/output 28. This pin can host an external clock for the self-wake-up timer. To use the pin as a self-wake-up timer clock input, select the external clock in the wake-up timer CTRL register. The external clock input is active in all power modes, including deep power-down.
PIO0_29/ DACOUT_1	50	38	38	-	[5]	I; PU	IO	**PIO0_29 —** General-purpose port 0 input/output 29.
							A	**DACOUT_1 —** DAC output 1.
PIO0_30/ACMP_I5	54	42	42	-	[5]	I; PU	IO	**PIO0_30 —** General-purpose port 0 input/output 30.
							A	**ACMP_I5 —** Analog comparator common input 5.

8.9.1 Standard I/O pad configuration

Figure 9 shows the possible pin modes for standard I/O pins with analog input function:

- Digital output driver with configurable open-drain output.
- Digital input: Weak pull-up resistor (PMOS device) enabled/disabled.
- Digital input: Weak pull-down resistor (NMOS device) enabled/disabled.
- Digital input: Repeater mode enabled/disabled.
- Digital input: Programmable input digital filter selectable on all pins.
- Analog input: Selected through the switch matrix.

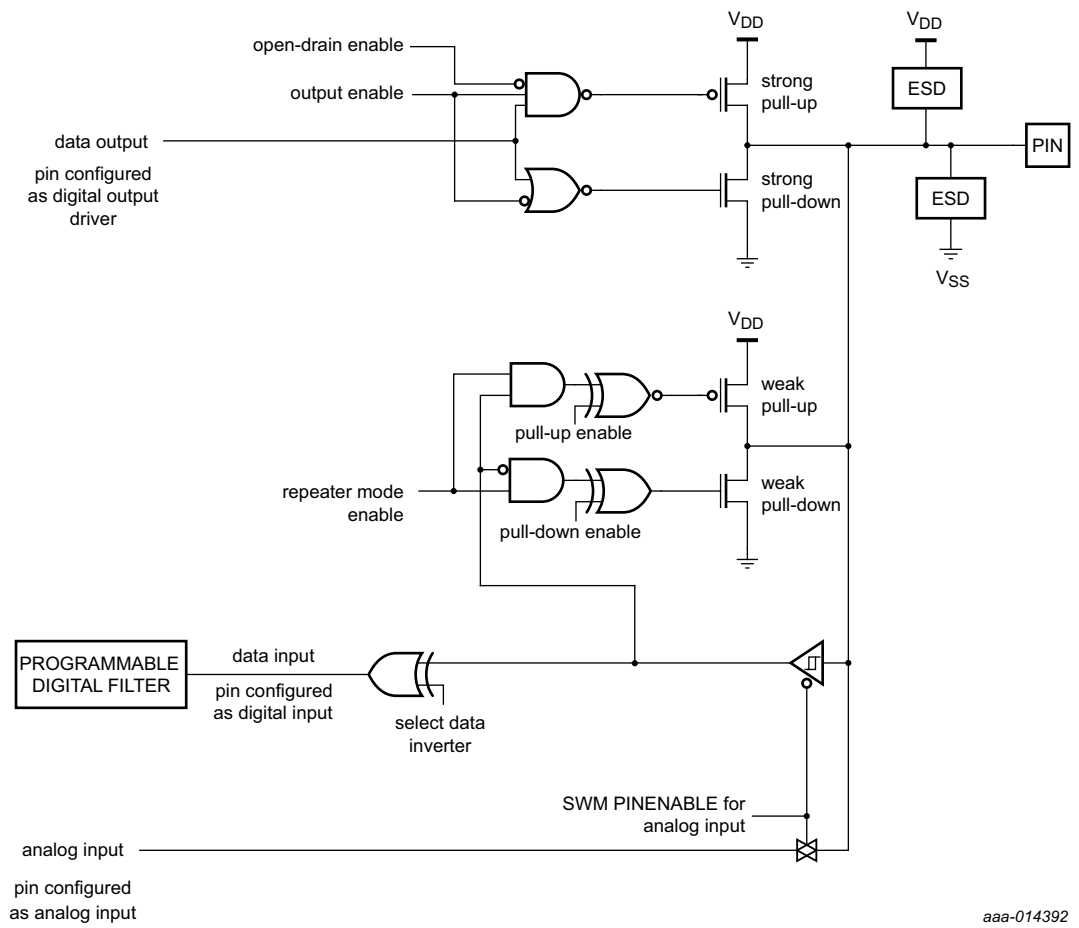


Fig 9. Standard I/O pad configuration

Any digital pin, independently of the function selected through the switch matrix, can be configured through the SYSCON block as input to the pin interrupt or pattern match engine. The registers that control the pin interrupt or pattern match engine are on the IO+ bus for fast single-cycle access.

8.12.1 Features

- Pin interrupts
  - Up to eight pins can be selected from all digital pins as edge- or level-sensitive interrupt requests. Each request creates a separate interrupt in the NVIC.
  - Edge-sensitive interrupt pins can interrupt on rising or falling edges or both.
  - Level-sensitive interrupt pins can be HIGH- or LOW-active.
  - Pin interrupts can wake up the LPC84x from sleep mode, deep-sleep mode, and power-down mode.
- Pin interrupt pattern match engine
  - Up to eight pins can be selected from all digital pins to contribute to a boolean expression. The boolean expression consists of specified levels and/or transitions on various combinations of these pins.
  - Each minterm (product term) comprising the specified boolean expression can generate its own, dedicated interrupt request.
  - Any occurrence of a pattern match can be also programmed to generate an RXEV notification to the Arm CPU. The RXEV signal can be connected to a pin.
  - The pattern match engine does not facilitate wake-up.

8.13 DMA controller

The DMA controller can access all memories and the USART, SPI, I^2C, DAC, and Capacitive Touch. DMA transfers can also be triggered by internal events like the ADC interrupts, the pin interrupts (PININT0 and PININT1), the SCTimer DMA requests, CTimer, and the DMA trigger outputs.

8.13.1 Features

- Twenty five channels with each channel connected to peripheral request inputs.
- DMA operations can be triggered by on-chip events or by two pin interrupts. Each DMA channel can select one trigger input from13 sources.
- Priority is user selectable for each channel.
- Continuous priority arbitration.
- Address cache with two entries.
- Efficient use of data bus.
- Supports single transfers up to 1,024 words.
- Address increment options allow packing and/or unpacking data.

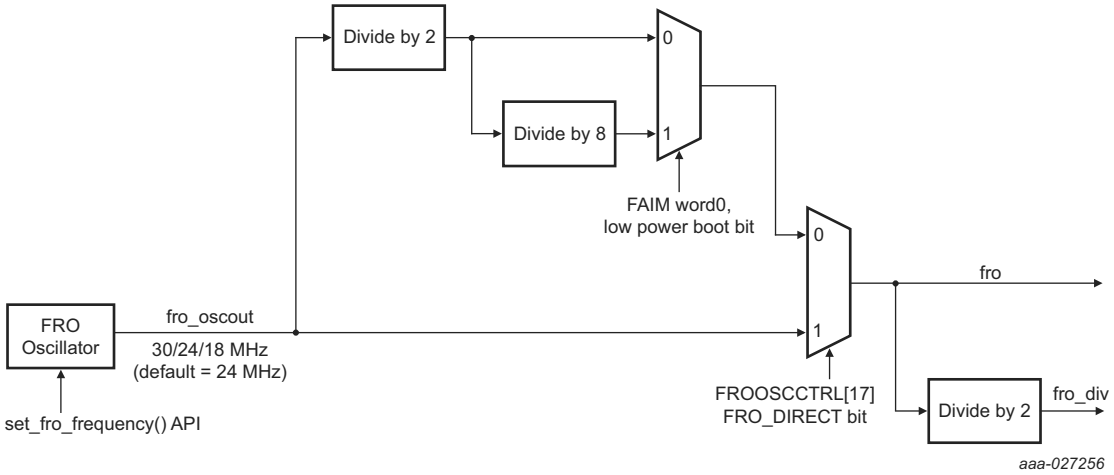


Fig 13. LPC84x FRO subsystem

Table 6. Clocking diagram signal name descriptions

Name	Description
sys_osc_clk	This is the internal clock that comes from external crystal oscillator through dedicated pins.
frg_clk	The output of the Fractional Rate Generator. The FRG and its source selection are shown in Figure 12 “LPC84x clock generation (continued)”.
fro	The output of the currently selected on-chip FRO oscillator. See UM11029 User manual.
fro_div	The FRO output. This may be either 15 MH, 12 MHz, or 9 MHz. See UM11029 User manual.
main_clk	The main clock used by the CPU and AHB bus, and potentially many others. The main clock and its source selection are shown in Figure 11 “LPC84x clock generation”.
“none”	A tied-off source that should be selected to save power when the output of the related multiplexer is not used.
sys_pll0_clk	The output of the System PLL. The System PLL and its source selection are shown in Figure 11 “LPC84x clock generation”.
wdt_osc_clk	The output of the watchdog oscillator, which has a selectable target frequency. It must also be enabled in the PDRINCFG0 register. See UM11029 User manual.
xtalin	Input of the main oscillator. If used, this is connected to an external crystal and load capacitor.
xtalout	Output of the main oscillator. If used, this is connected to an external crystal and load capacitor.
clk_in	This is the internal clock that comes from the main CLK_IN pin function. Connect that function to the pin by selecting it in the IOCON block.
external_clk	This is the internal clock that comes from the external crystal oscillator or the CLK_IN pin.

8.27.5 Power control

The LPC84x supports the Arm Cortex-M0+ sleep mode. The CPU clock rate may also be controlled as needed by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value. This allows a trade-off of power versus processing speed based on application requirements. In addition, a register is provided for shutting down the clocks to individual on-chip peripherals, allowing to fine-tune power consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Selected peripherals have their own clock divider which provides even better power control.

The LPC84x can be prevented from entering deep power-down mode by setting a lock bit in the PMU block. Locking out deep power-down mode enables the application to keep the watchdog timer or the BOD running at all times.

If the part must wake up from deep power-down mode via the $\overline{\text{WAKEUP}}$ pin or $\overline{\text{RESET}}$ pin, do not assign any movable function to this pin and must be externally pulled HIGH before entering deep power-down mode.

Table 7. Peripheral configuration in reduced power modes

Peripheral	Sleep mode	Deep-sleep mode	Power-down mode	Deep power-down mode
FRO	software configurable	on	off	off
FRO output	software configurable	off	off	off
Flash	software configurable	on	off	off
BOD	software configurable	software configurable	software configurable	off
PLL	software configurable	off	off	off
SysOsc	software configurable	off	off	off
WDosc/WWDT	software configurable	software configurable	software configurable	off
Digital peripherals	software configurable	off	off	off
WKT/low-power oscillator	software configurable	software configurable	software configurable	software configurable
ADC	software configurable	off	off	off
DAC0/1	software configurable	off	off	off
Capacitive Touch	software configurable	software configurable	software configurable	off
Comparator	software configurable	off	off	off

8.29 Emulation and debugging

Debug functions are integrated into the Arm Cortex-M0+. Serial wire debug functions are supported in addition to a standard JTAG boundary scan. The Arm Cortex-M0+ is configured to support up to four breakpoints and two watch points.

The Micro Trace Buffer is implemented on the LPC84x.

The $\overline{\text{RESET}}$ pin selects between the JTAG boundary scan ($\overline{\text{RESET}}$ = LOW) and the Arm SWD debug ($\overline{\text{RESET}}$ = HIGH). The Arm SWD debug port is disabled while the LPC84x is in reset. The JTAG boundary scan pins are selected by hardware when the part is in boundary scan mode (see Table 4).

To perform boundary scan testing, follow these steps:

1. Erase any user code residing in flash.
2. Power up the part with the $\overline{\text{RESET}}$ pin pulled HIGH externally.
3. Wait for at least 250 μs.
4. Pull the $\overline{\text{RESET}}$ pin LOW externally.
5. Perform boundary scan operations.
6. Once the boundary scan operations are completed, assert the $\overline{\text{TRST}}$ pin to enable the SWD debug mode, and release the $\overline{\text{RESET}}$ pin (pull HIGH).

Remark: The JTAG interface cannot be used for debug purposes.

11. Static characteristics

11.1 General operating conditions

Table 11. General operating conditions

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
f_{clk}	clock frequency	internal CPU/system clock		-	-	30	MHz
V_{DD}	supply voltage (core and external rail)		[3]	1.8	-	3.6	V
		FAIM programming only		3.0	-	3.6	V
		For ADC operations		2.4	-	3.6	V
		For DAC operations		2.7	-	3.6	V
V_{DDA}	analog supply voltage	For ADC operations		2.4	-	3.6	V
		For DAC operations		2.7	-	3.6	V
V_{ref}	ADC positive reference voltage	on pin VREFP		2.4	-	V_{DDA}	V
Oscillator pins							
$V_{i(xtal)}$	crystal input voltage	on pin XTALIN		−0.5	1.8	1.95	V
$V_{o(xtal)}$	crystal output voltage	on pin XTALOUT		−0.5	1.8	1.95	V
Pin capacitance							
C_{io}	input/output capacitance	pins with analog and digital functions	[2]	-	-	7.1	pF
		I^2C-bus pins	[2]	-	-	2.5	pF
		pins with digital functions only	[2]	-	-	2.8	pF

[1] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), nominal supply voltages.

[2] Including bonding pad capacitance. Based on simulation, not tested in production.

[3] The V_{DD} supply voltage must be 1.9 V or above when connecting an external crystal oscillator to the system oscillator. If the V_{DD} supply voltage is below 1.9 V, an external clock source can be fed to the XTALIN by bypassing the system oscillator or the other clock sources mentioned above can be used.

[3] I_{DD} measurements were performed with all pins configured as GPIO outputs driven LOW and pull-up resistors disabled.

[4] FRO enabled; system oscillator disabled; system PLL disabled.

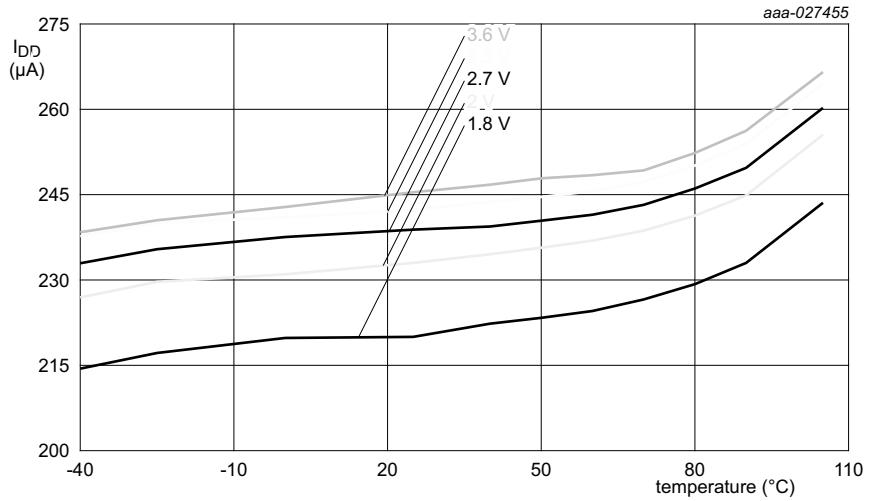
[5] BOD disabled.

[6] All peripherals disabled in the SYSAHBCLKCTRL register. Peripheral clocks disabled in system configuration block.

[7] All oscillators and analog blocks turned off.

[8] $\overline{\text{WAKEUP}}$ pin pulled HIGH externally.

[9] Tested in production, VDD = 3.6 V.



Conditions: BOD disabled; all oscillators and analog blocks disabled in the PDSLEEPCFG register (PDSLEEPCFG = 0x0000 18FF).

Fig 16. Deep-sleep mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}

Table 14. Power consumption for individual analog and digital blocks *…continued*

Peripheral	Typical supply current in µA			Notes
	System clock frequency =			
	n/a	12 MHz	30 MHz	
USART3	-	58	142	-
USART4	-	56	137	-
Comparator ACMP	-	79	144	-
ADC	-	78	190	Digital controller only. Analog portion of the ADC disabled in the PDRUNCFG register.
	-	78	190	Combined analog and digital logic. ADC enabled in the PDRUNCFG register and LPWRMODE bit set to 1 in the ADC CTRL register (ADC in low-power mode).
	-	79	190	Combined analog and digital logic. ADC enabled in the PDRUNCFG register and LPWRMODE bit set to 0 in the ADC CTRL register (ADC powered).
DAC 0	-	46	107	-
DAC 1	-	36	88	-
Capacitive Touch	-	49	117	-
DMA	-	355	858	-
CRC	-	36	83	-

Table 15. Static characteristics, pin characteristics *...continued*
T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{OZ}	OFF-state output current	V_O = 0 V; V_O = V_{DD}; on-chip pull-up/down resistors disabled		-	0.5	10[2]	nA
V_I	input voltage	$V_{DD} \geq$ 1.8 V		0	-	5.0	V
		V_{DD} = 0 V		0	-	3.6	V
V_O	output voltage	output active		0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage			0.7V_{DD}	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.3V_{DD}	V
V_{hys}	hysteresis voltage			-	0.4	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = 20 mA; 2.5 V <= V_{DD} < 3.6 V		V_{DD} − 0.5	-	-	V
		I_{OH} = 12 mA; 1.8 V <= V_{DD} < 2.5 V		V_{DD} − 0.5	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA 2.5 V <= V_{DD} < 3.6 V		-	-	0.5	V
		I_{OL} = 3 mA 1.8 V <= V_{DD} < 2.5 V		-	-	0.5	V
I_{OH}	HIGH-level output current	V_{OH} = V_{DD} − 0.5 V; 2.5 V <= V_{DD} < 3.6 V		20	-	-	mA
		V_{OH} = V_{DD} − 0.5 V; 1.8 V <= V_{DD} < 2.5 V		12	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.5 V 2.5 V ≤ V_{DD} ≤ 3.6 V		4	-	-	mA
		1.8 V ≤ V_{DD} < 2.5 V		3	-	-	mA
I_{OLS}	LOW-level short-circuit output current	V_{OL} = V_{DD}	[5]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V	[6]	10	50	150	µA
I_{pu}	pull-up current	V_I = 0 V	[6]	−10	−50	−85	µA
		V_{DD} < V_I < 5 V		0	0	0	µA
I^2C-bus pins (PIO0_10 and PIO0_11)							
V_{IH}	HIGH-level input voltage			0.7V_{DD}	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.3V_{DD}	V
V_{hys}	hysteresis voltage			-	0.05V_{DD}	-	V
I_{OL}	LOW-level output current	V_{OL} = 0.5 V; I^2C-bus pins configured as standard mode pins 2.5 V <= V_{DD} < 3.6 V		3.5	-	-	mA
		1.8 V <= V_{DD} < 2.5 V		3	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.5 V; I^2C-bus pins configured as Fast-mode Plus pins; 2.5 V <= V_{DD} < 3.6 V		20	-	-	mA
		1.8 V <= V_{DD} < 2.5 V		16	-	-	mA

12.7 SPI interfaces

The actual SPI bit rate depends on the delays introduced by the external trace, the external device, system clock (CCLK), and capacitive loading. Excluding delays introduced by external device and PCB, the maximum supported bit rate for SPI master mode is 30 Mbit/s, and the maximum supported bit rate for SPI slave mode is 1/(2 x 26 ns) = 19 Mbit/s at 3.0v ≤ VDD ≤ 3.6v and 1/(2 x 42 ns) = 12 Mbit/s at 1.8v ≤ VDD < 3.0v.

Remark: SPI functions can be assigned to all digital pins. The characteristics are valid for all digital pins except the open-drain pins PIO0_10 and PIO0_11.

Table 23. SPI dynamic characteristics

T_{amb} = −40 °C to 105 °C; C_L = 20 pF; input slew = 1 ns. Simulated parameters sampled at the 30 % and 70 % level of the rising or falling edge; values guaranteed by design. Delays introduced by the external trace or external device are not considered.

Symbol	Parameter	Conditions	Min	Max	Unit
SPI master					
t_{DS}	data set-up time	1.8 V <= V_{DD} <= 3.6 V	3	-	ns
t_{DH}	data hold time	1.8 V <= V_{DD} <= 3.6 V	0	-	ns
$t_{v(Q)}$	data output valid time	1.8 V <= V_{DD} <= 3.6 V	0	5	ns
SPI slave					
t_{DS}	data set-up time	1.8 V <= V_{DD} <= 3.6 V	4	-	ns
t_{DH}	data hold time	1.8 V <= V_{DD} <= 3.6 V	1	-	ns
$t_{v(Q)}$	data output valid time	3.0 V <= V_{DD} <= 3.6 V	0	26	ns
		1.8 V <= V_{DD} < 3.0 V	0	42	ns

12.8 USART interface

The actual USART bit rate depends on the delays introduced by the external trace, the external device, system clock (CCLK), and capacitive loading. Excluding delays introduced by external device and PCB, the maximum supported bit rate for USART master synchronous mode is 10 Mbit/s, and the maximum supported bit rate for USART slave synchronous mode is 10 Mbit/s.

Remark: USART functions can be assigned to all digital pins. The characteristics are valid for all digital pins except the open-drain pins PIO0_10 and PIO0_11.

Table 24. USART dynamic characteristics

T_{amb} = −40 °C to 105 °C; 1.8 V <= V_{DD} <= 3.6 V unless noted otherwise; C_L = 10 pF; input slew = 10 ns. Simulated parameters sampled at the 30 %/70 % level of the falling or rising edge; values guaranteed by design.

Symbol	Parameter	Conditions	Min	Max	Unit
USART master (in synchronous mode)					
$t_{su(D)}$	data input set-up time	3.0 V <= V_{DD} <= 3.6 V	31	-	ns
		1.8 V <= V_{DD} < 3.0 V	42		
$t_{h(D)}$	data input hold time		0	-	ns
$t_{v(Q)}$	data output valid time		0	7	ns
USART slave (in synchronous mode)					
$t_{su(D)}$	data input set-up time		5	-	ns
$t_{h(D)}$	data input hold time		5	-	ns
$t_{v(Q)}$	data output valid time	3.0 V <= V_{DD} <= 3.6 V	0	35	ns
		1.8 V <= V_{DD} < 3.0 V	0	46	ns

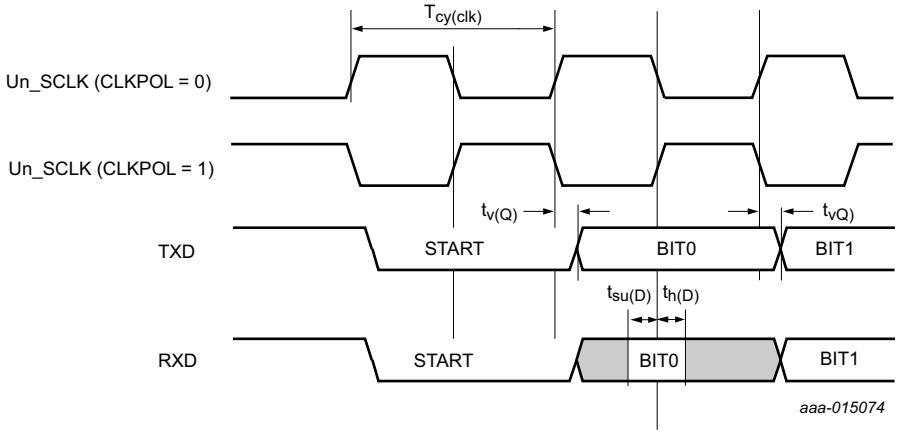


Fig 32. USART timing

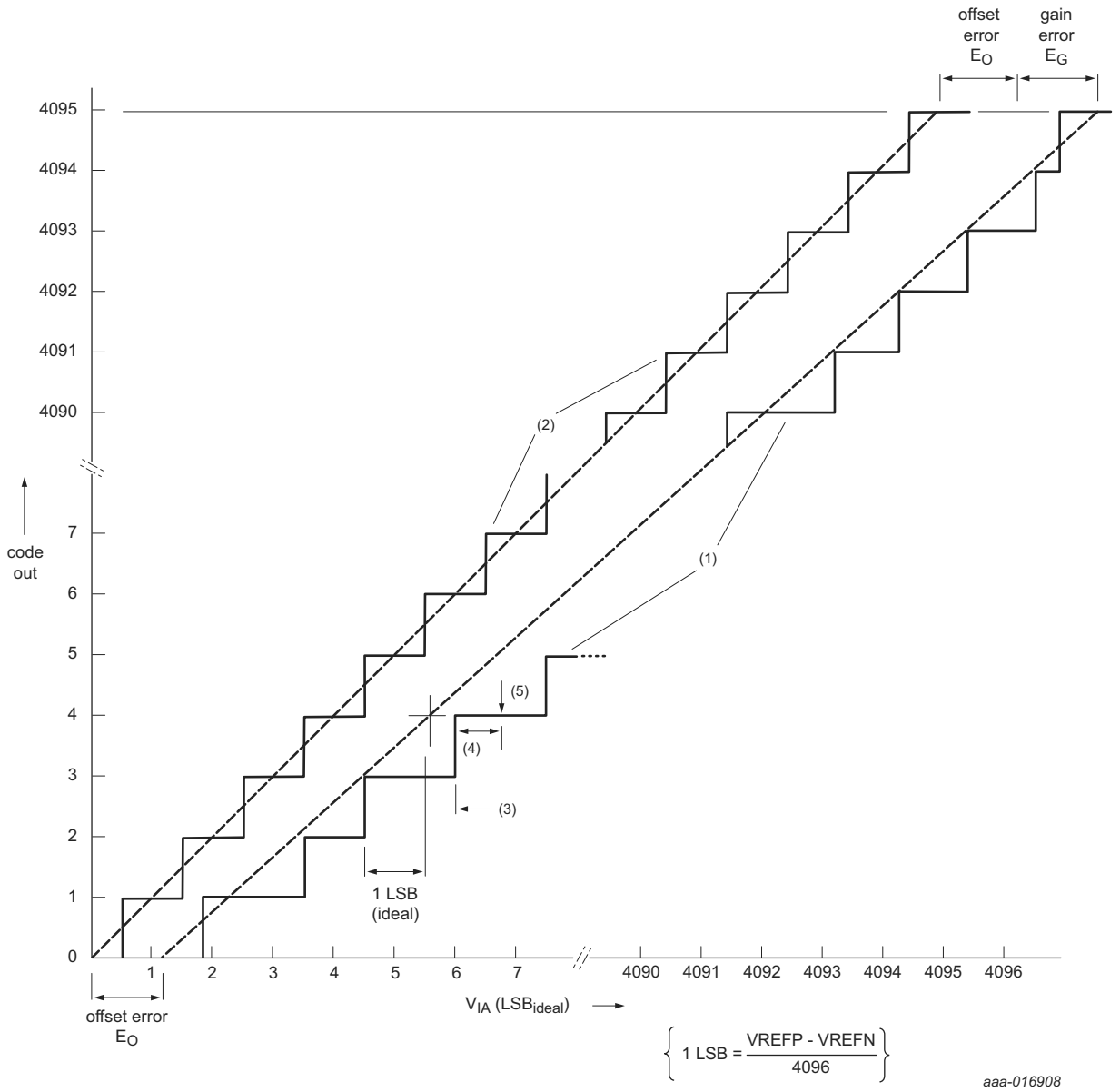


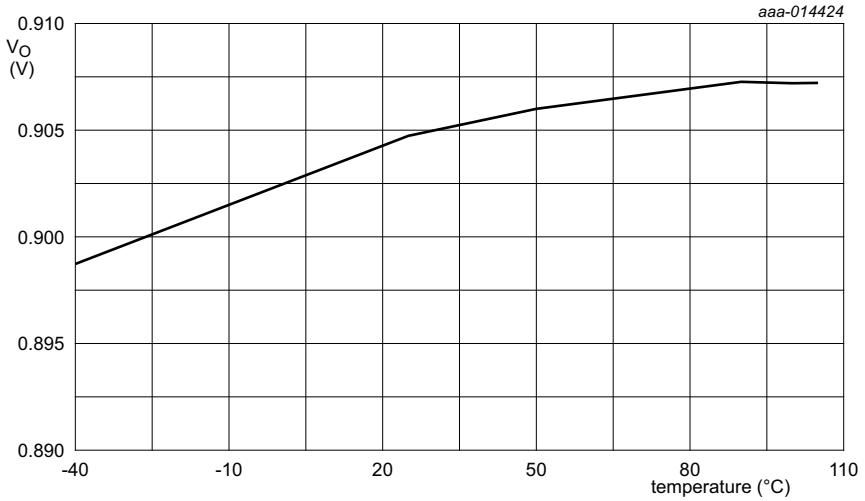
Fig 33. 12-bit ADC characteristics

13.3 Comparator and internal voltage reference

Table 28. Internal voltage reference static and dynamic characteristics

T_{amb} = −40 °C to +105 °C; V_{DD} = 3.3 V; hysteresis disabled in the comparator CTRL register.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_O	output voltage	T_{amb} = 25 °C to 105°C		860	-	940	mV
		T_{amb} = 25 °C			904		mV



V_{DD} = 3.3 V; characterized through bench measurements on typical samples.

Fig 35. Typical internal voltage reference output voltage

Table 29. Comparator characteristics

T_{amb} = −40 °C to +105 °C unless noted otherwise; V_{DD} = 1.8 V to 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{ref(cmp)}$	comparator reference voltage	pin $ACMPV_{REF}$		1.5	-	3.6	V
I_{DD}	supply current	VP > VM; T_{amb} = 25 °C; V_{DD} = 3.3 V	[2]	-	90	-	μA
		VM > VP; T_{amb} = 25 °C; V_{DD} = 3.3 V	[2]	-	60	-	μA
V_{IC}	common-mode input voltage			0	-	V_{DD}	V
DV_O	output voltage variation			0	-	V_{DD}	V
V_{offset}	offset voltage	V_{IC} = 0.1 V; V_{DD} = 3.0 V	[2]	-	3	-	mV
		V_{IC} = 1.5 V; V_{DD} = 3.0 V	[2]	-	3	-	mV
		V_{IC} = 2.9 V; V_{DD} = 3.0V	[2]	-	6	-	mV
Dynamic characteristics							
$t_{startup}$	start-up time	nominal process; V_{DD} = 3.3 V; T_{amb} = 25 °C		-	13	-	μs

14. Application information

14.1 Start-up behavior

Figure 36 shows the start-up timing after reset. The FRO 12 MHz oscillator provides the default clock at Reset and provides a clean system clock shortly after the supply pins reach operating voltage.

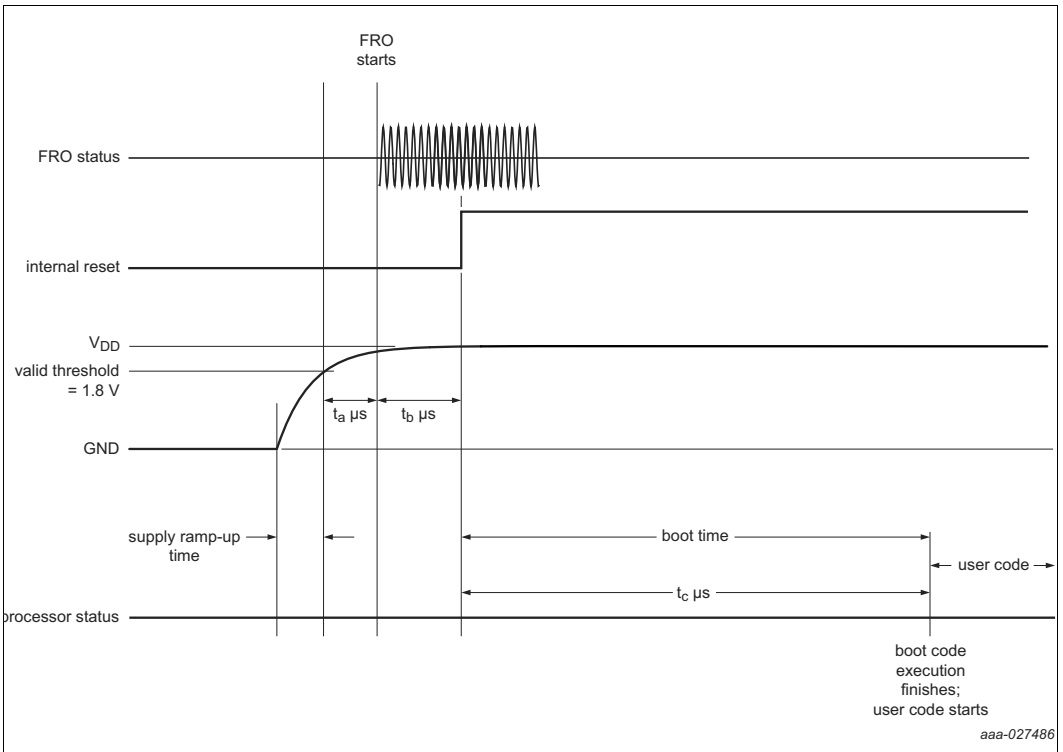


Fig 36. Start-up timing

Table 33. Typical start-up timing parameters

Parameter	Description	Value
t_a	FRO start time	≤ 26 µs
t_b	Internal reset de-asserted	101 µs
t_c	Boot time	51 µs

14.2 XTAL oscillator

In the XTAL oscillator circuit, only the crystal (XTAL) and the capacitances C_{X1} and C_{X2} need to be connected externally on XTALIN and XTALOUT. See Figure 37.

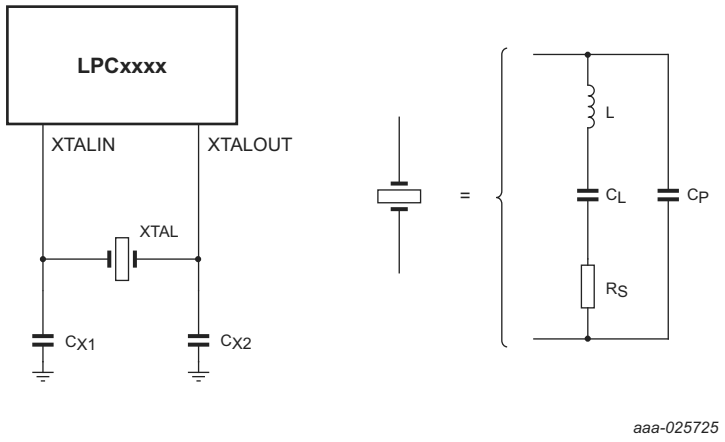


Fig 37. XTAL oscillator components

For best results, it is very critical to select a matching crystal for the on-chip oscillator. Load capacitance (CL), series resistance (RS), and drive level (DL) are important parameters to consider while choosing the crystal. After selecting the proper crystal, the external load capacitor C_{X1} and C_{X2} values can also be generally determined by the following expression:

$$C_{X1} = C_{X2} = 2C_L - (C_{Pad} + C_{Parasitic})$$

Where:

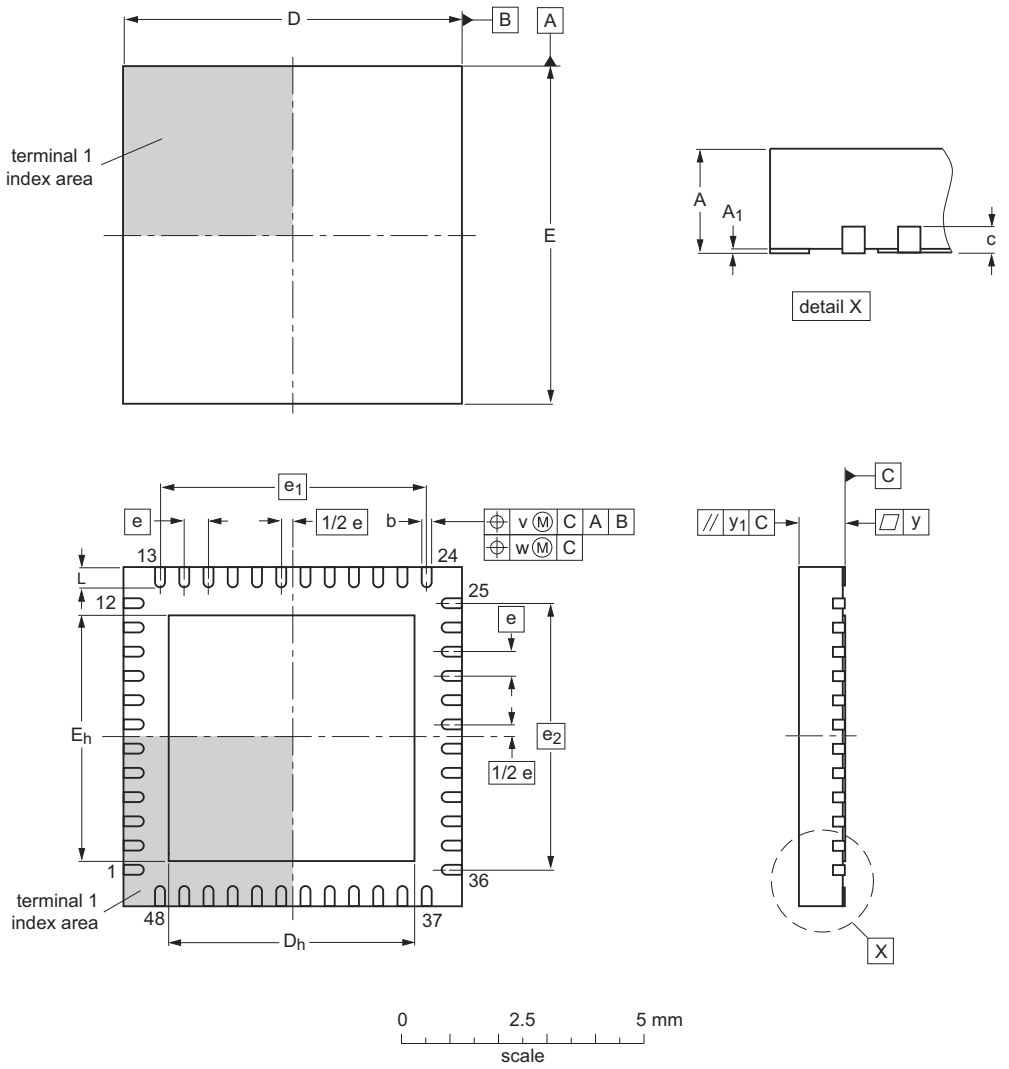
C_L - Crystal load capacitance

C_{Pad} - Pad capacitance of the XTALIN and XTALOUT pins (~3 pF).

$C_{Parasitic}$ – Parasitic or stray capacitance of external circuit.

Although $C_{Parasitic}$ can be ignored in general, the actual board layout and placement of external components influences the optimal values of external load capacitors. Therefore, it is recommended to fine tune the values of external load capacitors on actual hardware board to get the accurate clock frequency. For fine tuning, measure the clock on the XTALOUT pin and optimize the values of external load capacitors for minimum frequency deviation.

HVQFN48: plastic thermal enhanced very thin quad flat package; no leads; 48 terminals; body 7 x 7 x 0.85 mm **SOT619-1**



Dimensions (mm are the original dimensions)

Unit[1]		A	A_1	b	C	D	D_h	E	E_h	e	e_1	e_2	L	v	w	y	y_1
	max	1.00	0.05	0.30		7.1	5.25	7.1	5.25				0.5				
mm	nom	0.85	0.02	0.21	0.2	7.0	5.10	7.0	5.10	0.5	5.5	5.5	0.4	0.1	0.05	0.05	0.1
	min	0.80	0.00	0.18		6.9	4.95	6.9	4.95				0.3				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included

sot619-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT619-1		MO-220				~~02-10-18~~ 12-11-22

Fig 43. Package outline HVQFN48 7 x 7x 0.85 mm (SOT619-1)

20. Legal information

20.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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