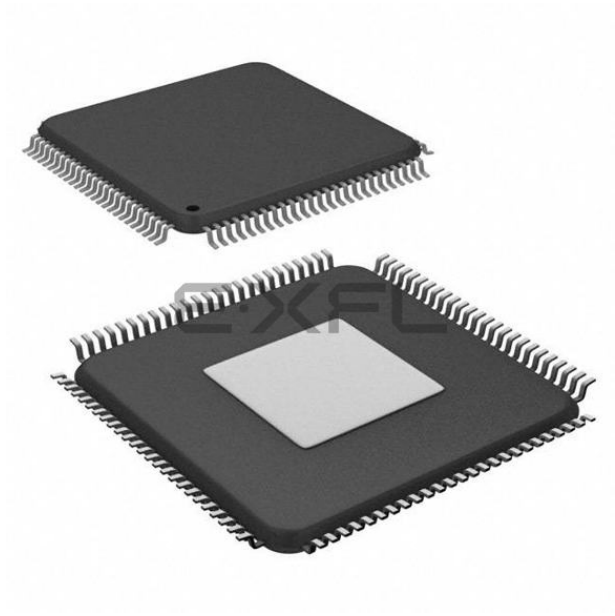
Infineon Technologies - XC2268I136F128LAAKXUMA1 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C166SV2
Core Size	16/32-Bit
Speed	128MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	76
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	90K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-100-8
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xc2268i136f128laakxuma1

Table of Contents

16/32-Bit Single-Chip Microcontroller with 32-Bit Performance

XC2268I (XC2000 Family)

1 Summary of Features

For a quick overview and easy reference, the features of the XC2268I are summarized here.

- High-performance CPU with five-stage pipeline and MPU
  - 7.8 ns instruction cycle at 128 MHz CPU clock (single-cycle execution)
  - One-cycle 32-bit addition and subtraction with 40-bit result
  - One-cycle multiplication (16 × 16 bit)
  - Background division (32 / 16 bit) in 21 cycles
  - One-cycle multiply-and-accumulate (MAC) instructions
  - Enhanced Boolean bit manipulation facilities
  - Zero-cycle jump execution
  - Additional instructions to support HLL and operating systems
  - Register-based design with multiple variable register banks
  - Fast context switching support with two additional local register banks
  - 16 Kbytes of two-way set-associative Instruction Cache (ICache)
  - 16 Mbytes total linear address space for code and data
  - 1024 Bytes on-chip special function register area (C166 Family compatible)
  - Integrated Memory Protection Unit (MPU)
- Interrupt system with 16 priority levels providing 112 interrupt nodes
  - Selectable external inputs for interrupt generation and wake-up
  - Fastest sample-rate 7.8 ns
- Sixteen-channel interrupt-driven single-cycle data transfer with Peripheral Event Controller (PEC), 24-bit pointers cover total address space
- Clock generation from internal or external clock sources, using on-chip PLL or prescaler
- Hardware CRC-Checker with Programmable Polynomial to Supervise On-Chip Memory Areas
- On-chip memory modules
  - 8 Kbytes on-chip stand-by RAM (SBRAM)
  - 2 Kbytes on-chip dual-port RAM (DPRAM)
  - 24 Kbytes on-chip data SRAM (DSRAM)
  - Up to 64 Kbytes on-chip program/data SRAM (PSRAM)
  - Up to 1 088 Kbytes on-chip program memory (Flash memory)
  - Memory content protection through Error Correction Code (ECC)
- On-Chip Peripheral Modules

2 General Device Information

The XC2268I series (16/32-Bit Single-Chip Microcontroller with 32-Bit Performance) is a part of the Infineon XC2000 Family of full-feature single-chip CMOS microcontrollers. These devices extend the functionality and performance of the C166 Family in terms of instructions (MAC unit), peripherals, and speed. They combine high CPU performance (up to 128 million instructions per second) with extended peripheral functionality and enhanced IO capabilities. Optimized peripherals can be adapted flexibly to meet the application requirements. These derivatives utilize clock generation via PLL and internal or external clock sources. On-chip memory modules include program Flash, program RAM, and data RAM.

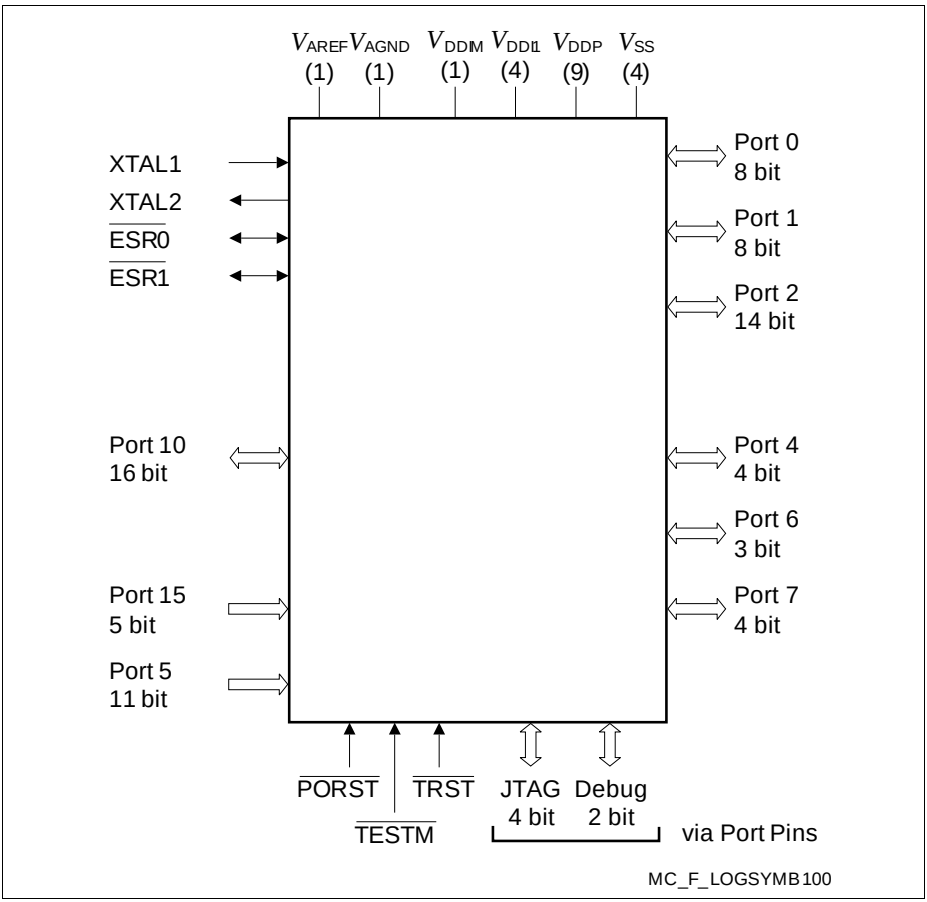

Figure 1 XC2268I Logic Symbol

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
9	P7.4	O0 / I	St/B	**Bit 4 of Port 7, General Purpose Input/Output**
	EMUX2	O1	St/B	**External Analog MUX Control Output 2 (ADC1)**
	U0C1_DOUT	O2	St/B	**USIC0 Channel 1 Shift Data Output**
	U0C1_SCLKOUT	O3	St/B	**USIC0 Channel 1 Shift Clock Output**
	CCU62_CCPOS2A	I	St/B	**CCU62 Position Input 2**
	TCK_C	IH	St/B	**DAP0/JTAG Clock Input** If JTAG pos. C is selected during start-up, an internal pull-up device will hold this pin high when nothing is driving it. If DAP pos. 2 is selected during start-up, an internal pull-down device will hold this pin low when nothing is driving it.
	U0C0_DX0D	I	St/B	**USIC0 Channel 0 Shift Data Input**
	U0C1_DX1E	I	St/B	**USIC0 Channel 1 Shift Clock Input**
11	P6.0	O0 / I	DA/A	**Bit 0 of Port 6, General Purpose Input/Output**
	EMUX0	O1	DA/A	**External Analog MUX Control Output 0 (ADC0)**
	TxDC2	O2	DA/A	**CAN Node 2 Transmit Data Output**
	$\overline{\text{BRKOUT}}$	O3	DA/A	**OCDS Break Signal Output**
	ADCx_REQGTyG	I	DA/A	**External Request Gate Input for ADC0/1**
	U1C1_DX0E	I	DA/A	**USIC1 Channel 1 Shift Data Input**
	ADC1_CH15	I	DA/A	**Analog Input Channel 15 for ADC1**
12	P6.1	O0 / I	DA/A	**Bit 1 of Port 6, General Purpose Input/Output**
	EMUX1	O1	DA/A	**External Analog MUX Control Output 1 (ADC0)**
	T3OUT	O2	DA/A	**GPT12E Timer T3 Toggle Latch Output**
	U1C1_DOUT	O3	DA/A	**USIC1 Channel 1 Shift Data Output**
	ADCx_REQTRyE	I	DA/A	**External Request Trigger Input for ADC0/1**
	RxDC2E	I	DA/A	**CAN Node 2 Receive Data Input**
	ESR1_6	I	DA/A	**ESR1 Trigger Input 6**
	ADC1_CH14	I	DA/A	**Analog Input Channel 14 for ADC1**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
41	P2.2	O0 / I	St/B	**Bit 2 of Port 2, General Purpose Input/Output**
	TxDC1	O1	St/B	**CAN Node 1 Transmit Data Output**
	CCU63_CC62	O2	St/B	**CCU63 Channel 2 Output**
	AD15	OH / IH	St/B	**External Bus Interface Address/Data Line 15**
	CCU63_CC62INB	I	St/B	**CCU63 Channel 2 Input**
	ESR2_5	I	St/B	**ESR2 Trigger Input 5**
	ERU_1A0	I	St/B	**External Request Unit Channel 1 Input A0**
42	P4.0	O0 / I	St/B	**Bit 0 of Port 4, General Purpose Input/Output**
	CC2_CC24	O3 / I	St/B	**CAPCOM2 CC24IO Capture Inp./ Compare Out.**
	$\overline{CS0}$	OH	St/B	**External Bus Interface Chip Select 0 Output**
43	P2.3	O0 / I	St/B	**Bit 3 of Port 2, General Purpose Input/Output**
	U0C0_DOUT	O1	St/B	**USIC0 Channel 0 Shift Data Output**
	CCU63_COUT63	O2	St/B	**CCU63 Channel 3 Output**
	CC2_CC16	O3 / I	St/B	**CAPCOM2 CC16IO Capture Inp./ Compare Out.**
	A16	OH	St/B	**External Bus Interface Address Line 16**
	ESR2_0	I	St/B	**ESR2 Trigger Input 0**
	U0C0_DX0E	I	St/B	**USIC0 Channel 0 Shift Data Input**
	U0C1_DX0D	I	St/B	**USIC0 Channel 1 Shift Data Input**
	RxDC0A	I	St/B	**CAN Node 0 Receive Data Input**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
66	P2.10	O0 / I	St/B	**Bit 10 of Port 2, General Purpose Input/Output**
	U0C1_DOUT	O1	St/B	**USIC0 Channel 1 Shift Data Output**
	U0C0_SELO 3	O2	St/B	**USIC0 Channel 0 Select/Control 3 Output**
	CC2_CC23	O3 / I	St/B	**CAPCOM2 CC23IO Capture Inp./ Compare Out.**
	A23	OH	St/B	**External Bus Interface Address Line 23**
	U0C1_DX0E	I	St/B	**USIC0 Channel 1 Shift Data Input**
	CAPINA	I	St/B	**GPT12E Register CAPREL Capture Input**
	U3C1_DX0A	I	St/B	**USIC3 Channel 1 Shift Data Input**
67	P10.3	O0 / I	St/B	**Bit 3 of Port 10, General Purpose Input/Output**
	CCU60_COU T60	O2	St/B	**CCU60 Channel 0 Output**
	AD3	OH / IH	St/B	**External Bus Interface Address/Data Line 3**
	U0C0_DX2A	I	St/B	**USIC0 Channel 0 Shift Control Input**
	U0C1_DX2A	I	St/B	**USIC0 Channel 1 Shift Control Input**
	U3C0_DX0A	I	St/B	**USIC3 Channel 0 Shift Data Input**
68	P0.5	O0 / I	St/B	**Bit 5 of Port 0, General Purpose Input/Output**
	U1C1_SCLK OUT	O1	St/B	**USIC1 Channel 1 Shift Clock Output**
	U1C0_SELO 2	O2	St/B	**USIC1 Channel 0 Select/Control 2 Output**
	CCU61_COU T62	O3	St/B	**CCU61 Channel 2 Output**
	A5	OH	St/B	**External Bus Interface Address Line 5**
	U1C1_DX1A	I	St/B	**USIC1 Channel 1 Shift Clock Input**
	U1C0_DX1C	I	St/B	**USIC1 Channel 0 Shift Clock Input**
	RXDC3E	I	St/B	**CAN Node 3 Receive Data Input**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
69	P10.4	O0 / I	St/B	**Bit 4 of Port 10, General Purpose Input/Output**
	U0C0_SELO 3	O1	St/B	**USIC0 Channel 0 Select/Control 3 Output**
	CCU60_COU T61	O2	St/B	**CCU60 Channel 1 Output**
	U3C0_DOUT	O3	St/B	**USIC3 Channel 0 Shift Data Output**
	AD4	OH / IH	St/B	**External Bus Interface Address/Data Line 4**
	U0C0_DX2B	I	St/B	**USIC0 Channel 0 Shift Control Input**
	U0C1_DX2B	I	St/B	**USIC0 Channel 1 Shift Control Input**
	ESR1_9	I	St/B	**ESR1 Trigger Input 9**
70	P10.5	O0 / I	St/B	**Bit 5 of Port 10, General Purpose Input/Output**
	U0C1_SCLK OUT	O1	St/B	**USIC0 Channel 1 Shift Clock Output**
	CCU60_COU T62	O2	St/B	**CCU60 Channel 2 Output**
	U2C0_DOUT	O3	St/B	**USIC2 Channel 0 Shift Data Output**
	AD5	OH / IH	St/B	**External Bus Interface Address/Data Line 5**
	U0C1_DX1B	I	St/B	**USIC0 Channel 1 Shift Clock Input**
71	P0.6	O0 / I	St/B	**Bit 6 of Port 0, General Purpose Input/Output**
	U1C1_DOUT	O1	St/B	**USIC1 Channel 1 Shift Data Output**
	TxDC1	O2	St/B	**CAN Node 1 Transmit Data Output**
	CCU61_COU T63	O3	St/B	**CCU61 Channel 3 Output**
	A6	OH	St/B	**External Bus Interface Address Line 6**
	U1C1_DX0A	I	St/B	**USIC1 Channel 1 Shift Data Input**
	CCU61_CTR APA	I	St/B	**CCU61 Emergency Trap Input**
	U1C1_DX1B	I	St/B	**USIC1 Channel 1 Shift Clock Input**

Up to 64 Kbytes of on-chip Program SRAM (PSRAM) are provided to store user code or data. The PSRAM is accessed via the PMU and is optimized for code fetches. A section of the PSRAM with programmable size can be write-protected.

Note: The actual size of the PSRAM depends on the quoted device type.

3.3 Central Processing Unit (CPU)

The core of the CPU consists of a 5-stage execution pipeline with a 2-stage instruction-fetch pipeline, a 16-bit arithmetic and logic unit (ALU), a 32-bit/40-bit multiply and accumulate unit (MAC), a register-file providing three register banks, and dedicated SFRs. The ALU features a multiply-and-divide unit, a bit-mask generator, and a barrel shifter.

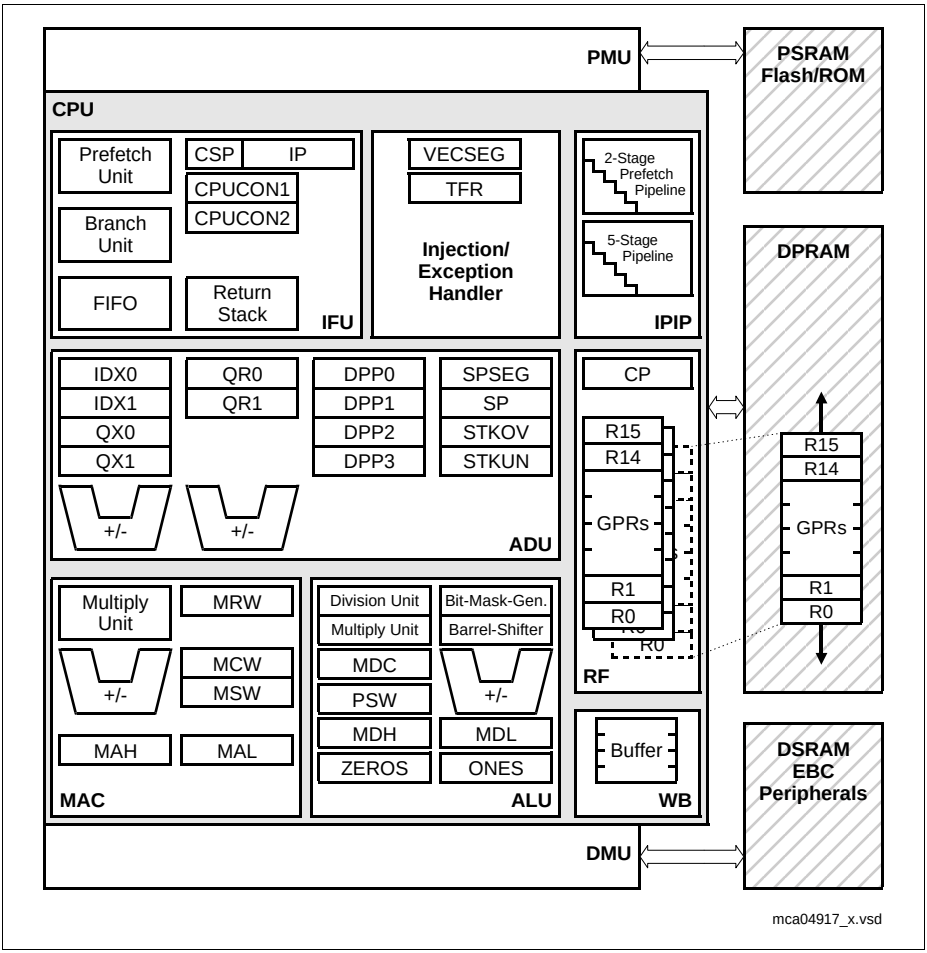

Figure 3 CPU Block Diagram

3.20 Instruction Set Summary

Table 11 lists the instructions of the XC2268I.
The addressing modes that can be used with a specific instruction, the function of the instructions, parameters for conditional execution of instructions, and the opcodes for each instruction can be found in the **"Instruction Set Manual"**.

This document also provides a detailed description of each instruction.

Table 11 Instruction Set Summary

Mnemonic	Description	Bytes
ADD(B)	Add word (byte) operands	2 / 4
ADDC(B)	Add word (byte) operands with Carry	2 / 4
SUB(B)	Subtract word (byte) operands	2 / 4
SUBC(B)	Subtract word (byte) operands with Carry	2 / 4
MUL(U)	(Un)Signed multiply direct GPR by direct GPR (16- × 16-bit)	2
DIV(U)	(Un)Signed divide register MDL by direct GPR (16-/16-bit)	2
DIVL(U)	(Un)Signed long divide reg. MD by direct GPR (32-/16-bit)	2
CPL(B)	Complement direct word (byte) GPR	2
NEG(B)	Negate direct word (byte) GPR	2
AND(B)	Bitwise AND, (word/byte operands)	2 / 4
OR(B)	Bitwise OR, (word/byte operands)	2 / 4
XOR(B)	Bitwise exclusive OR, (word/byte operands)	2 / 4
BCLR/BSET	Clear/Set direct bit	2
BMOV(N)	Move (negated) direct bit to direct bit	4
BAND/BOR/BXOR	AND/OR/XOR direct bit with direct bit	4
BCMP	Compare direct bit to direct bit	4
BFLDH/BFLDL	Bitwise modify masked high/low byte of bit-addressable direct word memory with immediate data	4
CMP(B)	Compare word (byte) operands	2 / 4
CMPD1/2	Compare word data to GPR and decrement GPR by 1/2	2 / 4
CMPI1/2	Compare word data to GPR and increment GPR by 1/2	2 / 4
PRIOR	Determine number of shift cycles to normalize direct word GPR and store result in direct word GPR	2
SHL/SHR	Shift left/right direct word GPR	2

4.4 System Parameters

The following parameters specify several aspects which are important when integrating the XC2268I into an application system.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply.

Table 24 Various System Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Short-term deviation of internal clock source frequency[1]	Δf_{INT} CC	-1	–	1	%	$\Delta T_J \leq 10$ °C
Internal clock source frequency	f_{INT} CC	4.8	5.0	5.2	MHz	
Wakeup clock source frequency[2]	f_{WU} CC	400	–	700	kHz	FREQSEL= 00
		210	–	390	kHz	FREQSEL= 01
		140	–	260	kHz	FREQSEL= 10
		110	–	200	kHz	FREQSEL= 11
Startup time from power-on with code execution from Flash	t_{SPO} CC	1.9	2.5	3.7	ms	f_{WU} = 500 kHz
Startup time from standby mode with code execution from Flash	t_{SSB} CC	3.1	4.0	5.2	ms	f_{WU} = 140 kHz
		1.9	2.4	3.6	ms	f_{WU} = 500 kHz
Startup time from stopover mode with code execution from PSRAM	t_{SSO} CC	11 / f_{WU}[3]	–	12 / f_{WU}[3]	µs	
Core voltage (PVC) supervision level	V_{PVC} CC	V_{LV} - 0.03	V_{LV}	V_{LV} + 0.07[4]	V	[5]
Supply watchdog (SWD) supervision level	V_{SWD} CC	V_{LV} - 0.10[6]	V_{LV}	V_{LV} + 0.15	V	Lower voltage range[5]
		V_{LV} - 0.15	V_{LV}	V_{LV} + 0.15	V	Upper voltage range[5]

1) The short-term frequency deviation refers to a timeframe of a few hours and is measured relative to the current frequency at the beginning of the respective timeframe. This parameter is useful to determine a time span for re-triggering a LIN synchronization.
2) This parameter is tested for the fastest and the slowest selection. The medium selections are not subject to production test - verified by design/characterization
3) f_{WU} in MHz
4) This value includes a hysteresis of approximately 50 mV for rising voltage.
5) V_{LV} = selected PVC/SWD voltage level
6) The limit V_{LV} - 0.10 V is valid for the OK1 level. The limit for the OK2 level is V_{LV} - 0.15 V.

Conditions for t_{SPO} Timing Measurement

The time required for the transition from **Power-On** to **Base** mode is called t_{SPO}. It is measured under the following conditions:

Precondition: The pad supply is valid, i.e. V_{DDPB} is above 3.0 V and remains above 3.0 V even though the XC2268I is starting up. See also V_{DDPB} requirements in **Table 13**.

Start condition: Power-on reset is removed ($\overline{\text{PORST}}$ = 1).

End condition: External pin toggle caused by first user instruction executed from FLASH after startup.

Conditions for t_{SSB} Timing Measurement

The time required for the transition from **Standby** to **Base** mode is called t_{SSB}. It is measured under the following conditions:

Precondition: The **Standby** mode has been entered using the procedure defined in the Programmer's Guide.

Start condition: Pin toggle on $\overline{\text{ESR}}$ pin triggering the startup sequence.

End condition: External pin toggle caused by first user instruction executed from FLASH after startup.

Conditions for t_{SSO} Timing Measurement

The time required for the transition from **Stopover** to **Stopover Waked-Up** mode is called t_{SSO}. It is measured under the following conditions:

Precondition: The **Stopover** mode has been entered using the procedure defined in the Programmer's Guide.

Start condition: Pin toggle on $\overline{\text{ESR}}$ pin triggering the startup sequence.

End condition: External pin toggle caused by first user instruction executed from PSRAM after startup.

4.6 AC Parameters

These parameters describe the dynamic behavior of the XC2268I.

4.6.1 Testing Waveforms

These values are used for characterization and production testing (except pin XTAL1).

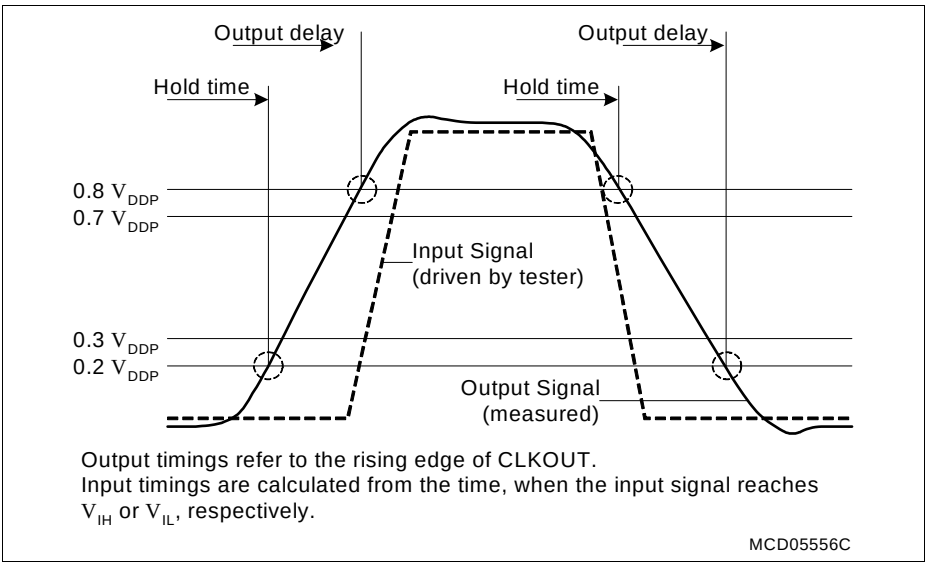

Figure 14 Input Output Waveforms

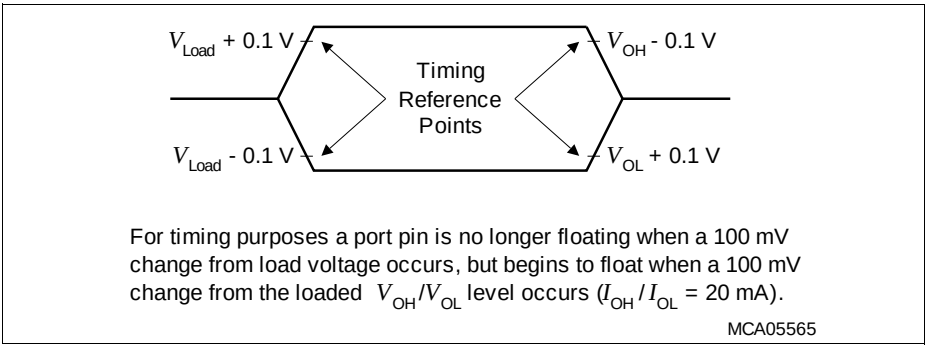

Figure 15 Floating Waveforms

4.6.2 Definition of Internal Timing

The internal operation of the XC2268I is controlled by the internal system clock f_{SYS}.

Because the system clock signal f_{SYS} can be generated from a number of internal and external sources using different mechanisms, the duration of the system clock periods (TCSs) and their variation (as well as the derived external timing) depend on the mechanism used to generate f_{SYS}. This must be considered when calculating the timing for the XC2268I.

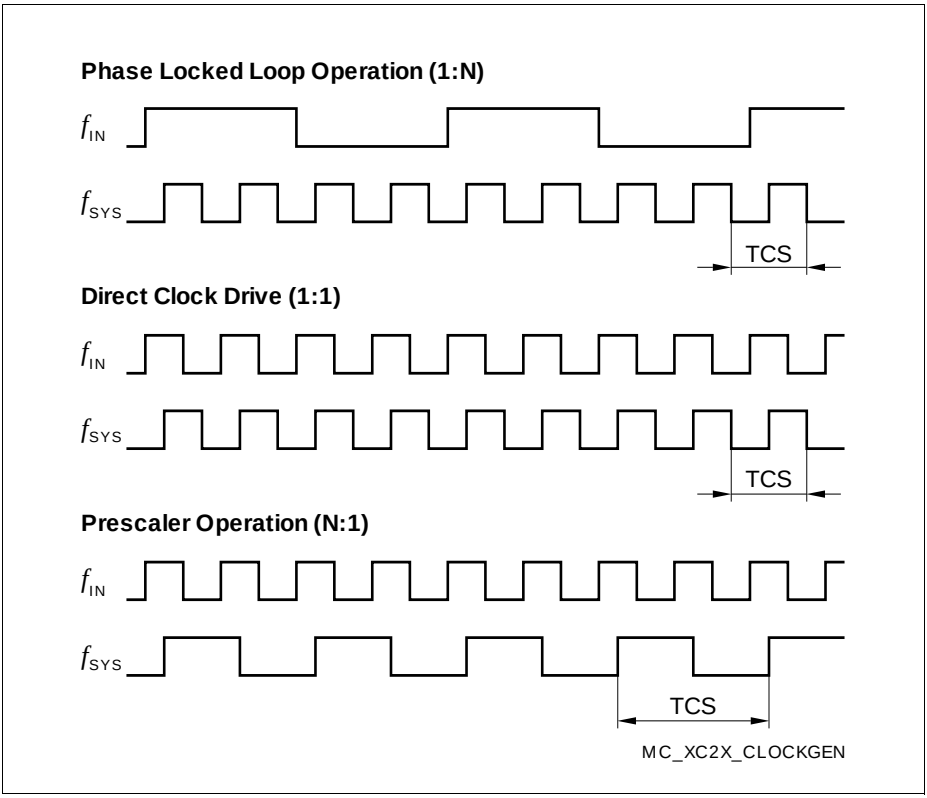

Figure 16 Generation Mechanisms for the System Clock

*Note: The example of PLL operation shown in **Figure 16** uses a PLL factor of 1:4; the example of prescaler operation uses a divider factor of 2:1.*

The specification of the external timing (AC Characteristics) depends on the period of the system clock (TCS).

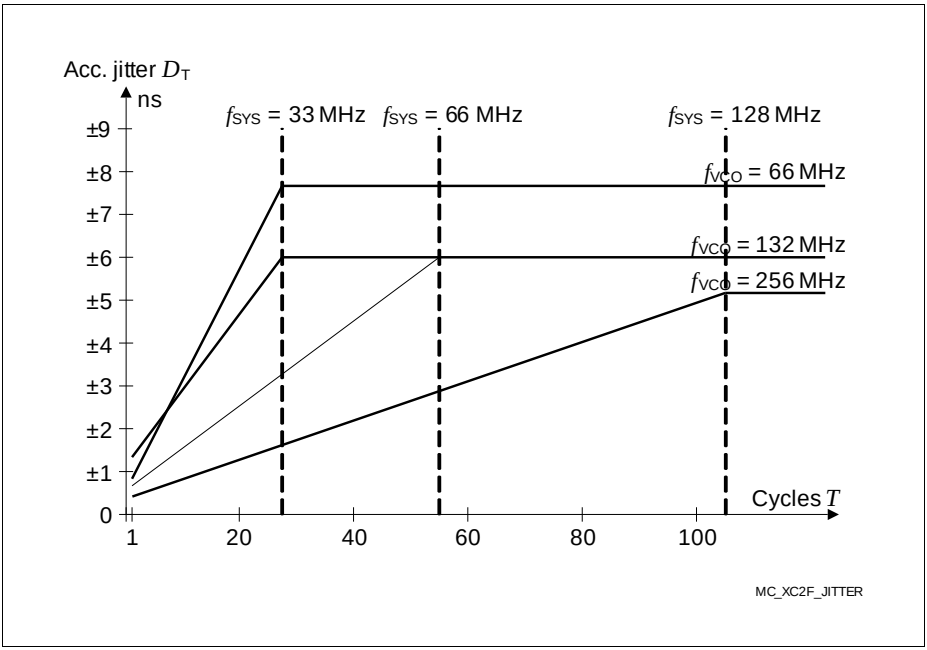

Figure 17 Approximated Accumulated PLL Jitter

Note: The specified PLL jitter values are valid if the capacitive load per pin does not exceed C_L = 20 pF.
The maximum peak-to-peak noise on the pad supply voltage (measured between V_{DDPB} pin 100 and V_{SS} pin 1) is limited to a peak-to-peak voltage of V_{PP} = 50 mV. This can be achieved by appropriate blocking of the supply voltage as close as possible to the supply pins and using PCB supply and ground planes.

Note: The term CLKOUT refers to the reference clock output signal which is generated by selecting f_{SYS} as the source signal for the clock output signal EXTCLK on pin P2.8 and by enabling the high-speed clock driver on this pin.

Variable Memory Cycles

External bus cycles of the XC2268I are executed in five consecutive cycle phases (AB, C, D, E, F). The duration of each cycle phase is programmable (via the TCONCSx registers) to adapt the external bus cycles to the respective external module (memory, peripheral, etc.).

The duration of the access phase can optionally be controlled by the external module using the READY handshake input.

This table provides a summary of the phases and the ranges for their length.

Table 33 Programmable Bus Cycle Phases (see timing diagrams)

Bus Cycle Phase	Parameter	Valid Values	Unit
Address setup phase, the standard duration of this phase (1 … 2 TCS) can be extended by 0 … 3 TCS if the address window is changed	tpAB	1 … 2 (5)	TCS
Command delay phase	tpC	0 … 3	TCS
Write Data setup/MUX Tristate phase	tpD	0 … 1	TCS
Access phase	tpE	1 … 32	TCS
Address/Write Data hold phase	tpF	0 … 3	TCS

Note: The bandwidth of a parameter (from minimum to maximum value) covers the whole operating range (temperature, voltage) as well as process variations. Within a given device, however, this bandwidth is smaller than the specified range. This is also due to interdependencies between certain parameters. Some of these interdependencies are described in additional notes (see standard timing).

Note: Operating Conditions apply; C_L = 20 pF.

Table 34 EBC External Bus Timing for Upper Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output valid delay for $\overline{RD}$, $\overline{WR}$(L/H)	t_{10} CC	–	7	13	ns	
Output valid delay for $\overline{BHE}$, ALE	t_{11} CC	–	7	14	ns	
Address output valid delay for A23 ... A0	t_{12} CC	–	8	14	ns	
Address output valid delay for AD15 ... AD0 (MUX mode)	t_{13} CC	–	8	15	ns	
Output valid delay for $\overline{CS}$	t_{14} CC	–	7	13	ns	
Data output valid delay for AD15 ... AD0 (write data, MUX mode)	t_{15} CC	–	8	15	ns	
Data output valid delay for D15 ... D0 (write data, DEMUX mode)	t_{16} CC	–	8	15	ns	
Output hold time for $\overline{RD}$, $\overline{WR}$(L/H)	t_{20} CC	-2	6	8	ns	
Output hold time for $\overline{BHE}$, ALE	t_{21} CC	-2	6	10	ns	
Address output hold time for AD15 ... AD0	t_{23} CC	-3	6	8	ns	
Output hold time for $\overline{CS}$	t_{24} CC	-3	6	11	ns	
Data output hold time for D15 ... D0 and AD15 ... AD0	t_{25} CC	-3	6	8	ns	
Input setup time for READY, D15 ... D0, AD15 ... AD0	t_{30} SR	25	15	–	ns	
Input hold time READY, D15 ... D0, AD15 ... AD0[1)]	t_{31} SR	0	-7	–	ns	

1) Read data are latched with the same internal clock edge that triggers the address change and the rising edge of RD. Address changes before the end of RD have no impact on (demultiplexed) read cycles. Read data can change after the rising edge of RD.

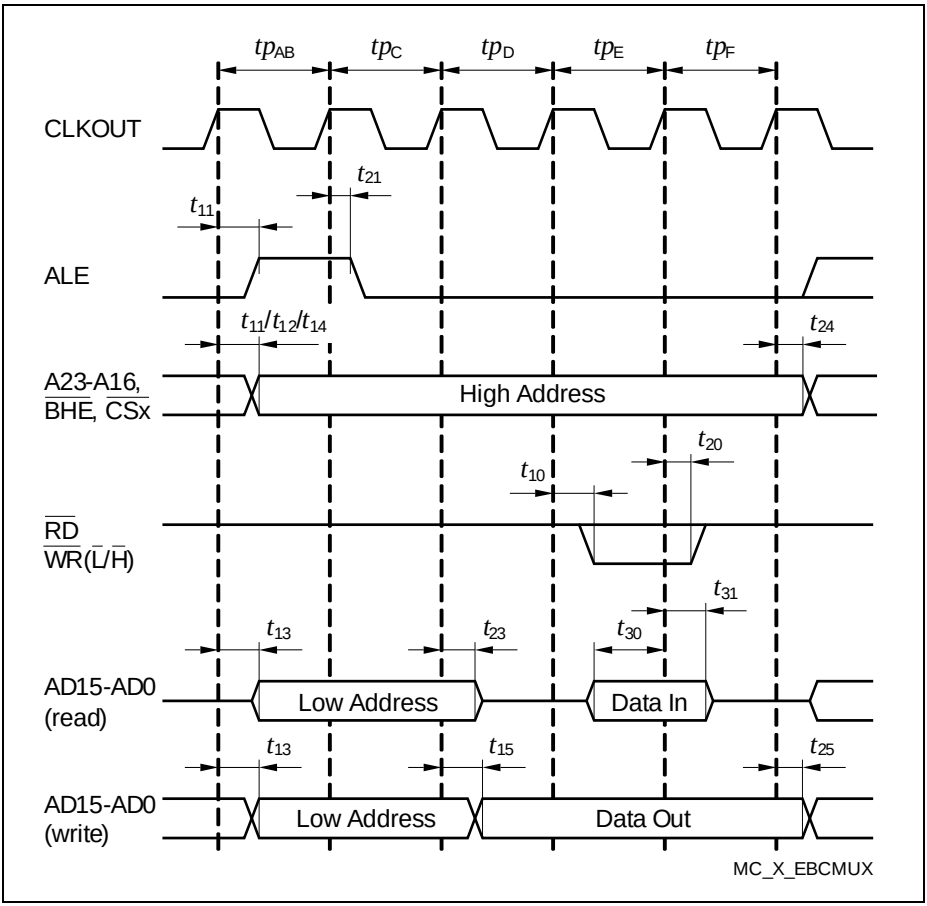

Figure 20 Multiplexed Bus Cycle

Table 37 USIC SSC Master Mode Timing for Lower Voltage Range (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Receive data input setup time to SCLKOUT receive edge	t_4 SR	40	–	–	ns	
Data input DX0 hold time from SCLKOUT receive edge	t_5 SR	-5	–	–	ns	

1) $t_{SYS} = 1 / f_{SYS}$

Table 38 USIC SSC Slave Mode Timing for Upper Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Select input DX2 setup to first clock input DX1 transmit edge[1)]	t_{10} SR	7	–	–	ns	
Select input DX2 hold after last clock input DX1 receive edge[1)]	t_{11} SR	7	–	–	ns	
Receive data input setup time to shift clock receive edge[1)]	t_{12} SR	7	–	–	ns	
Data input DX0 hold time from clock input DX1 receive edge[1)]	t_{13} SR	5	–	–	ns	
Data output DOUT valid time	t_{14} CC	7	–	33	ns	

1) These input timings are valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).

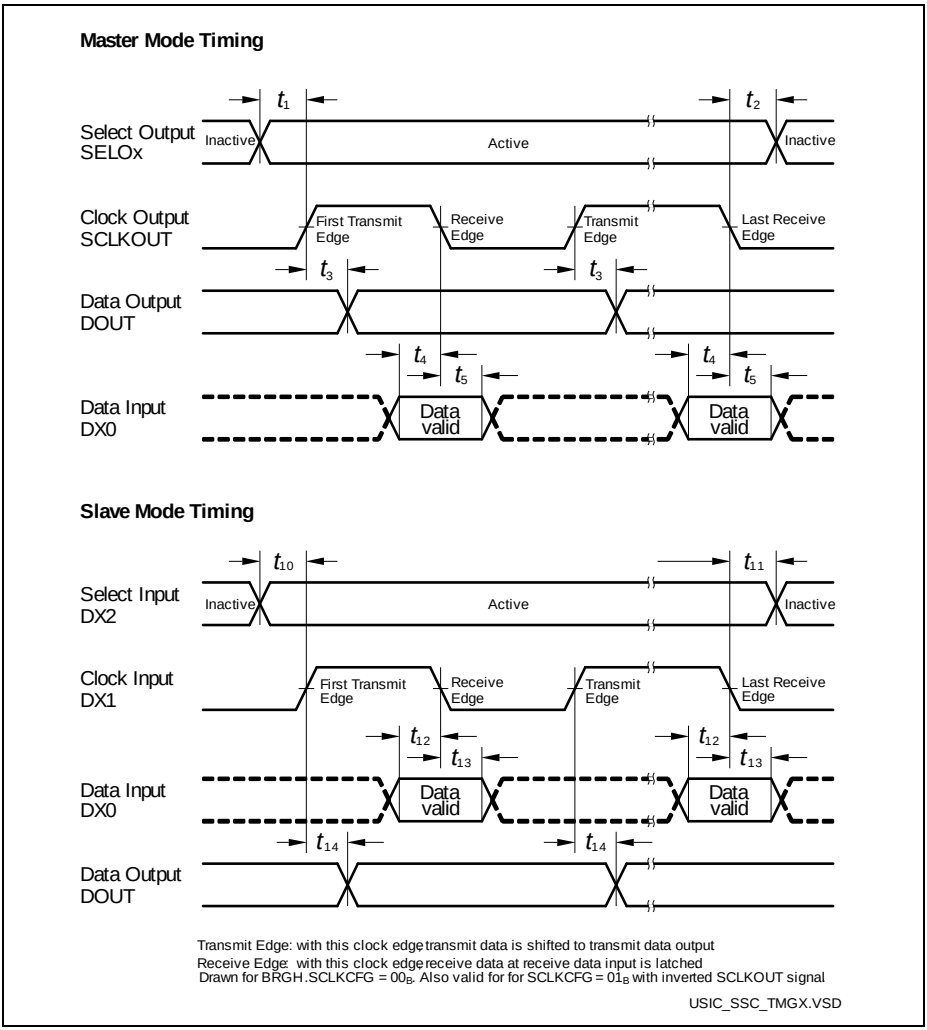

Figure 23 USIC - SSC Master/Slave Mode Timing

Note: This timing diagram shows a standard configuration where the slave select signal is low-active and the serial clock signal is not shifted and not inverted.