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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	HCS12
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, I²C, SCI, SPI
Peripherals	PWM, WDT
Number of I/O	59
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 5.25V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-QFP
Supplier Device Package	80-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s12dg128cfuer

Version Number	Revision Date	Effective Date	Author	Description of Changes
V02.02	08 Mar 2002	08 Mar 2002		Changed XCLKS to PE7 in Table 2-2 Updated device part numbers in Figure 2-1 Updated BDM clock in Figure 3-1 Removed SIM description in overview & n_{UPOSC} spec in Table A-15 Updated electrical spec of VDD & VDDPLL (Table A-4), IOL/IOH (Table A-6), C_{INS} (Table A-9), C_{IN} (Table A-6 & A-15), Updated interrupt pulse timing variables in Table A-6 Updated device part numbers in Figure 2-1 Added document numbers on cover page and Table 0-2
V02.03	14 Mar 2002	14 Mar 2002		Cleaned up Fig. 1-1, 2-1 Updated Section 1.5 descriptions Corrected PE assignment in Table 2-2, Fig. 2-5,6,7. Corrected NVM sizes in Sections 16, 17 Added I_{REF} spec for 1ATD in Table A-8 Added Blank Check in A.3.1.5 and Table A-11 Updated CRG spec in Table A-15
V02.04	16 Aug 2002	16 Aug 2002		Added: Pull-up columns to signal table, Example for PLL Filter calculation, Thermal values for junction to board and package, BGND pin pull-up Part Order Information Global Register Table Chip Configuration Summary Device specific info on CRG Modified: Reduced Wait and Run IDD values Mode of Operation chapter Changed leakage current for ADC inputs down to +-1uA Minor modification of PLL frequency/ voltage gain values Corrected: Pin names/functions on 80 pin packages Interrupt vector table enable register inconsistencies PCB layout for 80QFP VREGEN position
V02.05	12 Sep 2002	12 Sep 2002		Corrected: Register address mismatches in 1.5.1
V02.06	06 Nov 2002	06 Nov 2002		Removed document order no. from Revision History pages Renamed "Preface" section to "Derivative Differences and Document references". Added details for derivatives missing CAN0/1/4, BDLC, IIC and/or Byteflight Added 2L40K mask set in section 1.6 Added OSC User Guide in Preface, “Document References” Added oscillator clock connection to BDM in S12_CORE in fig 3-1 Corrected several register and bit names in “Local Enable” column of Table 5.1 Interrupt Vector Locations Section HCS12 Core Block Description: mentioned alternate clock of BDM to be equivalent to oscillator clock Added new section: “Oscillator (OSC) Block Description” Corrected in footnote of Table "PLL Characteristics": fOSC = 4MHz

List of Tables

- **Port H**
  In order to avoid floating nodes the ports should be either configured as outputs by setting the data direction register (DDRH at Base+$0262) to $FF, or enabling the pull resistors by writing a $FF to the pull enable register (PERH at Base+$0264).
- **Port J[1:0]**
  Port J pull-up resistors are enabled out of reset on all four pins (7:6 and 1:0). Therefore care must be taken not to disable the pull enables on PJ[1:0] by clearing the bits PERJ1 and PERJ0 at Base+$026C.
- **Port K**
  Port K pull-up resistors are enabled out of reset, i.e. Bit 7 = PUKE = 1 in the register PUCR at Base+$000C. Therefore care must be taken not to clear this bit.
- **Port M[7:6]**
  PM7:6 must be configured as outputs or their pull resistors must be enabled to avoid floating inputs.
- **Port P6**
  PP6 must be configured as output or its pull resistor must be enabled to avoid a floating input.
- **Port S[7:4]**
  PS7:4 must be configured as outputs or their pull resistors must be enabled to avoid floating inputs.
- **PAD[15:8] (ATD1 channels)**
  Out of reset the ATD1 is disabled preventing current flows in the pins. Do not modify the ATD1 registers!

- **Pins not available in 80 pin QFP package for MC9S12DB128, SC515846, and SC102202**
  - **Port H**
    In order to avoid floating nodes the ports should be either configured as outputs by setting the data direction register (DDRH at Base+$0262) to $FF, or enabling the pull resistors by writing a $FF to the pull enable register (PERH at Base+$0264).
  - **Port J[7:6, 1:0]**
    Port J pull-up resistors are enabled out of reset on all four pins (7:6 and 1:0). Therefore care must be taken not to disable the pull enables on PJ[7:6, 1:0] by clearing the bits PERJ7, PERJ6, PERJ1 and PERJ0 at Base+$026C.
  - **Port K**
    Port K pull-up resistors are enabled out of reset, i.e. Bit 7 = PUKE = 1 in the register PUCR at Base+$000C. Therefore care must be taken not to clear this bit.
  - **Port M[1:0]**
    PM1:0 must be configured as outputs or their pull resistors must be enabled to avoid floating inputs.
  - **Port P6**
    PP6 must be configured as output or its pull resistor must be enabled to avoid a floating input.

Section 1 Introduction

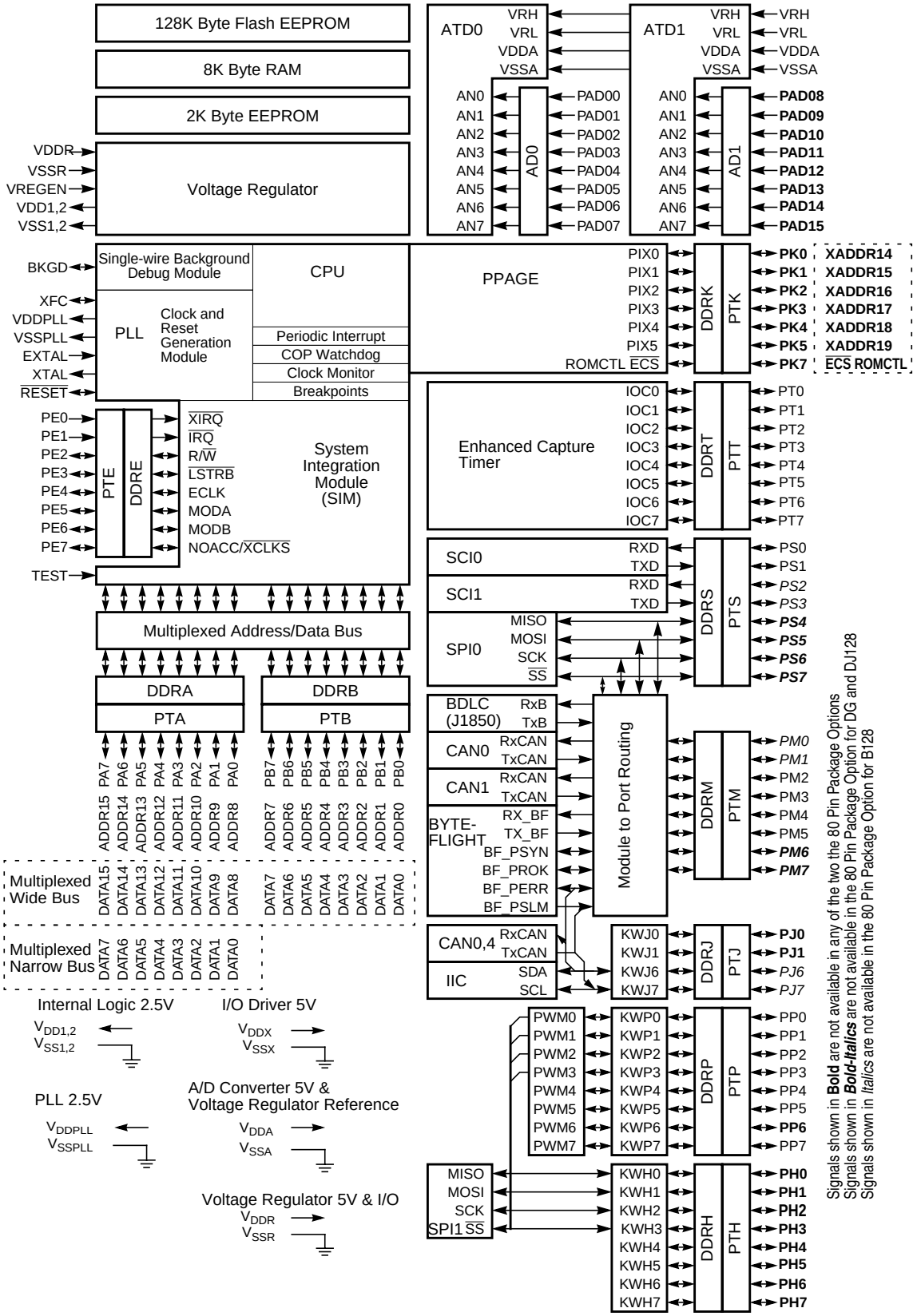
1.1 Overview

The MC9S12DT128 microcontroller unit (MCU) is a 16-bit device composed of standard on-chip peripherals including a 16-bit central processing unit (HCS12 CPU), 128K bytes of Flash EEPROM, 8K bytes of RAM, 2K bytes of EEPROM, two asynchronous serial communications interfaces (SCI), two serial peripheral interfaces (SPI), an 8-channel IC/OC enhanced capture timer, two 8-channel, 10-bit analog-to-digital converters (ADC), an 8-channel pulse-width modulator (PWM), a digital Byte Data Link Controller (BDLC), 29 discrete digital I/O channels (Port A, Port B, Port K and Port E), 20 discrete digital I/O lines with interrupt and wakeup capability, three CAN 2.0 A, B software compatible modules (MSCAN12), a Byteflight module and an Inter-IC Bus. The MC9S12DT128 has full 16-bit data paths throughout. However, the external bus can operate in an 8-bit narrow mode so single 8-bit wide memory can be interfaced for lower cost systems. The inclusion of a PLL circuit allows power consumption and performance to be adjusted to suit operational requirements.

1.2 Features

- HCS12 Core
  - 16-bit HCS12 CPU
    i. Upward compatible with M68HC11 instruction set
    ii. Interrupt stacking and programmer’s model identical to M68HC11
    iii. 20-bit ALU
    iv. Instruction queue
    v. Enhanced indexed addressing
  - MEBI (Multiplexed External Bus Interface)
  - MMC (Module Mapping Control)
  - INT (Interrupt control)
  - BKP (Breakpoints)
  - BDM (Background Debug Module)
- CRG (Clock and Reset Generator)
  - Choice of low current Colpitts oscillator or standard Pierce Oscillator
  - PLL
  - COP watchdog
  - real time interrupt
  - clock monitor
- 8-bit and 4-bit ports with interrupt functionality

Figure 1-1 MC9S12DT128 Block Diagram



1.5.1 Detailed Register Map

$0000 - $000F MEBI map 1 of 3 (HCS12 Multiplexed External Bus Interface)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0000	PORTA	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0001	PORTB	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0002	DDRA	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0003	DDRB	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0004	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0005	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0006	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0007	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0008	PORTE	Read:	Bit 7	6	5	4	3	2	Bit 1	Bit 0
		Write:								
$0009	DDRE	Read:	Bit 7	6	5	4	3	Bit 2	0	0
		Write:								
$000A	PEAR	Read:	NOACCE	0	PIPOE	NECLK	LSTRE	RDWE	0	0
		Write:								
$000B	MODE	Read:	MODC	MODB	MODA	0	IVIS	0	EMK	EME
		Write:								
$000C	PUCR	Read:	PUPKE	0	0	PUPEE	0	0	PUPBE	PUPAE
		Write:								
$000D	RDRIV	Read:	RDPK	0	0	RDPE	0	0	RDPB	RDPA
		Write:								
$000E	EBICTL	Read:	0	0	0	0	0	0	0	ESTR
		Write:								
$000F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0010 - $0014 MMC map 1 of 4 (HCS12 Module Mapping Control)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0010	INITRM	Read:	RAM15	RAM14	RAM13	RAM12	RAM11	0	0	RAMHAL
		Write:								
$0011	INITRG	Read:	0	REG14	REG13	REG12	REG11	0	0	0
		Write:								
$0012	INITEE	Read:	EE15	EE14	EE13	EE12	EE11	0	0	EEON
		Write:								
$0013	MISC	Read:	0	0	0	0	EXSTR1	EXSTR0	ROMHM	ROMON
		Write:								
$0014	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0080 - $009F ATD0 (Analog to Digital Converter 10 Bit 8 Channel)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0092	ATD0DR1H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$0093	ATD0DR1L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$0094	ATD0DR2H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$0095	ATD0DR2L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$0096	ATD0DR3H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$0097	ATD0DR3L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$0098	ATD0DR4H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$0099	ATD0DR4L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$009A	ATD0DR5H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$009B	ATD0DR5L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$009C	ATD0DR6H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$009D	ATD0DR6L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$009E	ATD0DR7H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$009F	ATD0DR7L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								

$00A0 - $00C7 PWM (Pulse Width Modulator 8 Bit 8 Channel)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00A0	PWME	Read:	PWME7	PWME6	PWME5	PWME4	PWME3	PWME2	PWME1	PWME0
		Write:								
$00A1	PWMPOL	Read:	PPOL7	PPOL6	PPOL5	PPOL4	PPOL3	PPOL2	PPOL1	PPOL0
		Write:								
$00A2	PWMCLK	Read:	PCLK7	PCLK6	PCLK5	PCLK4	PCLK3	PCLK2	PCLK1	PCLK0
		Write:								
$00A3	PWMPRCLK	Read:	0	PCKB2	PCKB1	PCKB0	0	PCKA2	PCKA1	PCKA0
		Write:								
$00A4	PWMCAE	Read:	CAE7	CAE6	CAE5	CAE4	CAE3	CAE2	CAE1	CAE0
		Write:								
$00A5	PWMCTL	Read:	CON67	CON45	CON23	CON01	PSWAI	PFRZ	0	0
		Write:								
$00A6	PWMTST Test Only	Read:	0	0	0	0	0	0	0	0
		Write:								
$00A7	PWMPRSC Test Only	Read:	0	0	0	0	0	0	0	0
		Write:								
$00A8	PWMSCLA	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								

$00A0 - $00C7 PWM (Pulse Width Modulator 8 Bit 8 Channel)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00A9	PWMSCLB	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00AA	PWMSCNTA Test Only	Read:	0	0	0	0	0	0	0	0
		Write:								
$00AB	PWMSCNTB Test Only	Read:	0	0	0	0	0	0	0	0
		Write:								
$00AC	PWMCNT0	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:	0	0	0	0	0	0	0	0
$00AD	PWMCNT1	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:	0	0	0	0	0	0	0	0
$00AE	PWMCNT2	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:	0	0	0	0	0	0	0	0
$00AF	PWMCNT3	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:	0	0	0	0	0	0	0	0
$00B0	PWMCNT4	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:	0	0	0	0	0	0	0	0
$00B1	PWMCNT5	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:	0	0	0	0	0	0	0	0
$00B2	PWMCNT6	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:	0	0	0	0	0	0	0	0
$00B3	PWMCNT7	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:	0	0	0	0	0	0	0	0
$00B4	PWMPER0	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00B5	PWMPER1	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00B6	PWMPER2	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00B7	PWMPER3	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00B8	PWMPER4	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00B9	PWMPER5	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00BA	PWMPER6	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00BB	PWMPER7	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00BC	PWMDTY0	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00BD	PWMDTY1	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00BE	PWMDTY2	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00BF	PWMDTY3	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00C0	PWMDTY4	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00C1	PWMDTY5	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0

$0300 - $035F Byteflight

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0315	BFFIDRMR	Read:	FIDRMR 7	FIDRMR 6	FIDRMR 5	FIDRMR 5	FIDRMR 4	FIDRMR 3	FIDRMR 2	FIDRMR 1
		Write:								
$0316	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0317	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0318	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0319	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$031A	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$031B	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$031C	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$031D	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$031E	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$031F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0320	BFTIDENT	Read:	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
		Write:								
$0321	BFTLEN	Read:					LEN3	LEN2	LEN1	LEN0
		Write:								
$0322 - $032D	BFTDATA0-BFTDATA11	Read:	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0
		Write:								
$032E - $032F	Reserved	Read:								
		Write:								
$0330	BFRIDENT	Read:	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
		Write:								
$0331	BFRLEN	Read:					LEN3	LEN2	LEN1	LEN0
		Write:								
$0332 - $033D	BFRDATA0-BFRDATA11	Read:	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA 0
		Write:								
$033E- $033F	Reserved	Read:								
		Write:								
$0340	BFFIDENT	Read:	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
		Write:								
$0341	BFFLEN	Read:					LEN3	LEN2	LEN1	LEN0
		Write:								
$0342 - $034D	BFFDATA0-BFFDATA11	Read:	DATA 7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0
		Write:								
$034E - $034F	Reserved	Read:								
		Write:								
$0350 - $035F	BFBUFCTL0 - BFBUFCTL15	Read:	IFLG	IENA	LOCK	ABTAK	ABTRQ	0	0	CFG
		Write:								

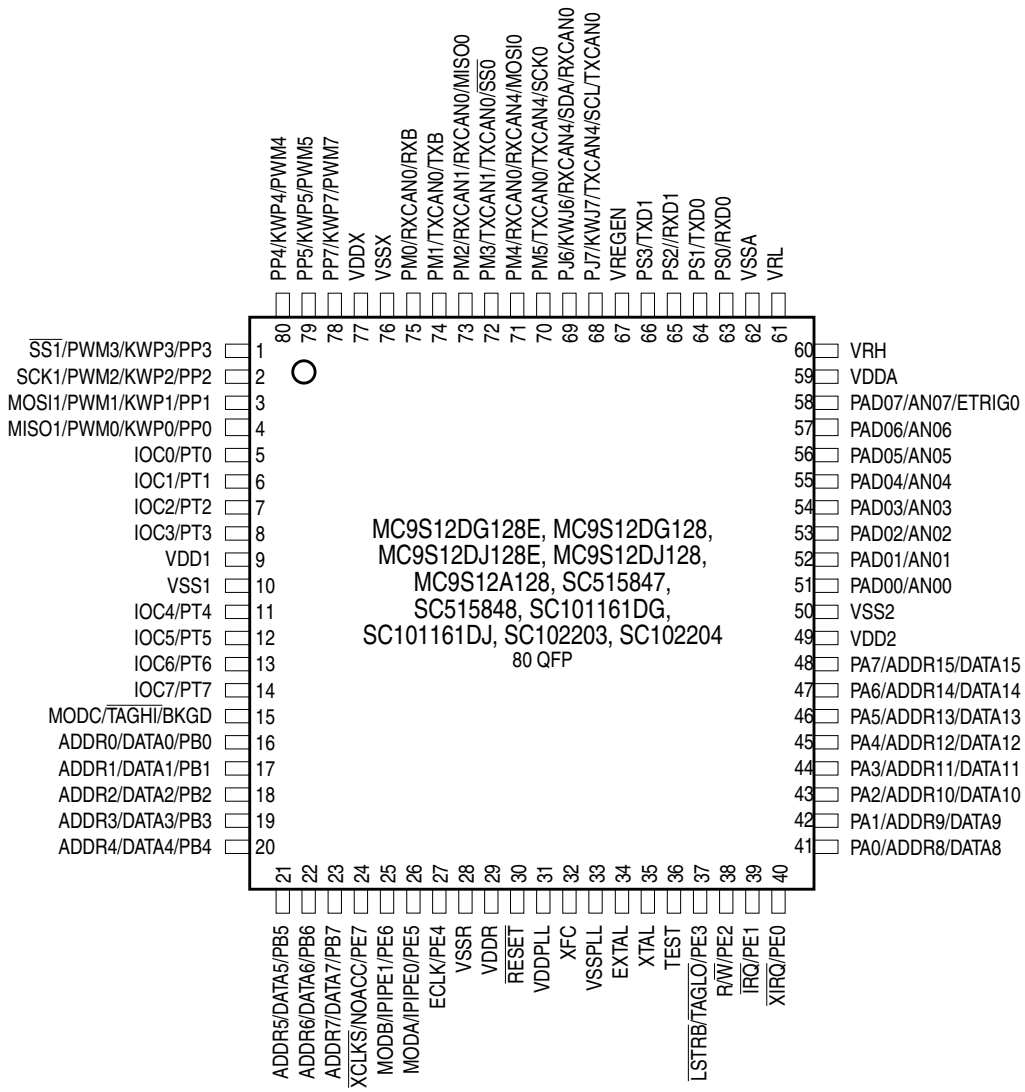


Figure 2-2 Pin Assignments in 80 QFP for MC9S12DG128E, MC9S12DG128, MC9S12DJ128E, MC9S12DJ128, MC9S12A128, SC515847, SC515848, SC101161DG, SC101161DJ, SC102203, and SC102204 Bondout

2.3.6 PAD[15] / AN1[7] / ETRIG1 — Port AD Input Pin [15]

PAD15 is a general purpose input pin and analog input of the analog to digital converter ATD1. It can act as an external trigger input for the ATD1.

2.3.7 PAD[14:8] / AN1[6:0] — Port AD Input Pins [14:8]

PAD14 - PAD8 are general purpose input pins and analog inputs of the analog to digital converter ATD1.

2.3.8 PAD[7] / AN0[7] / ETRIG0 — Port AD Input Pin [7]

PAD7 is a general purpose input pin and analog input of the analog to digital converter ATD0. It can act as an external trigger input for the ATD0.

2.3.9 PAD[6:0] / AN0[6:0] — Port AD Input Pins [6:0]

PAD6 - PAD8 are general purpose input pins and analog inputs of the analog to digital converter ATD0.

2.3.10 PA[7:0] / ADDR[15:8] / DATA[15:8] — Port A I/O Pins

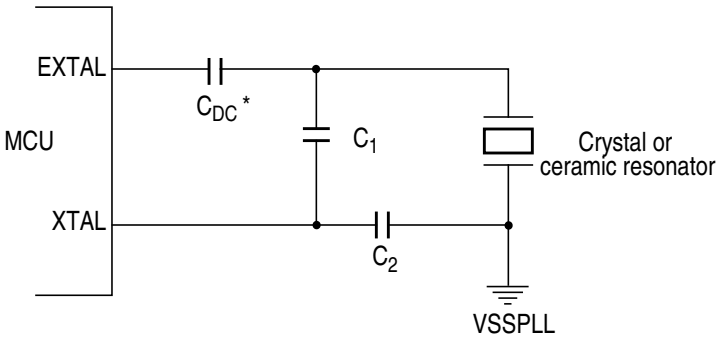
PA7-PA0 are general purpose input or output pins. In MCU expanded modes of operation, these pins are used for the multiplexed external address and data bus.

2.3.11 PB[7:0] / ADDR[7:0] / DATA[7:0] — Port B I/O Pins

PB7-PB0 are general purpose input or output pins. In MCU expanded modes of operation, these pins are used for the multiplexed external address and data bus.

2.3.12 PE7 / NOACC / $\overline{\text{XCLKS}}$ — Port E I/O Pin 7

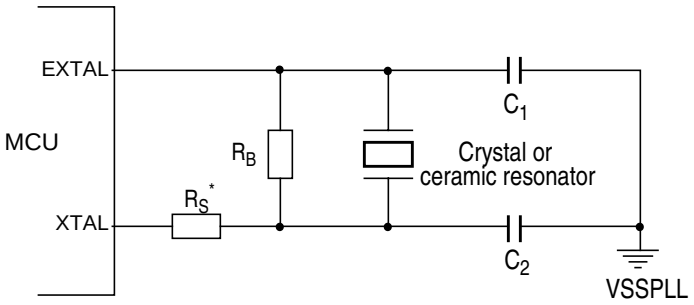
PE7 is a general purpose input or output pin. During MCU expanded modes of operation, the NOACC signal, when enabled, is used to indicate that the current bus cycle is an unused or “free” cycle. This signal will assert when the CPU is not using the bus.
The $\overline{\text{XCLKS}}$ is an input signal which controls whether a crystal in combination with the internal Colpitts (low power) oscillator is used or whether Pierce oscillator/external clock circuitry is used. The state of this pin is latched at the rising edge of $\overline{\text{RESET}}$. If the input is a logic low the EXTAL pin is configured for an external clock drive. If input is a logic high an oscillator circuit is configured on EXTAL and XTAL. Since this pin is an input with a pull-up device during reset, if the pin is left floating, the default configuration is an oscillator circuit on EXTAL and XTAL.



* Due to the nature of a translated ground Colpitts oscillator a DC voltage bias is applied to the crystal

Please contact the crystal manufacturer for crystal DC bias conditions and recommended capacitor value C_{DC}.

Figure 2-5 Colpitts Oscillator Connections (PE7=1)



* Rs can be zero (shorted) when used with higher frequency crystals. Refer to manufacturer's data.

Figure 2-6 Pierce Oscillator Connections (PE7=0)

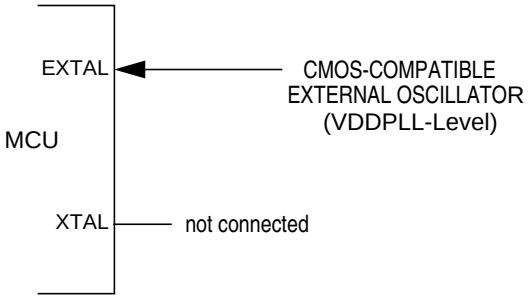


Figure 2-7 External Clock Connections (PE7=0)

Mnemonic	Pin Number 112-pin QFP	Nominal Voltage	Description
VDDR	41	5.0V	External power and ground, supply to pin drivers and internal voltage regulator.
VSSR	40	0V	
VDDX	107	5.0V	External power and ground, supply to pin drivers.
VSSX	106	0V	
VDDA	83	5.0V	Operating voltage and ground for the analog-to-digital converters and the reference for the internal voltage regulator, allows the supply voltage to the A/D to be bypassed independently.
VSSA	86	0V	
VRL	85	0V	Reference voltages for the analog-to-digital converter.
VRH	84	5.0V	
VDDPLL	43	2.5V	Provides operating voltage and ground for the Phased-Locked Loop. This allows the supply voltage to the PLL to be bypassed independently. Internal power and ground generated by internal regulator.
VSSPLL	45	0V	
VREGEN	97	5V	Internal Voltage Regulator enable/disable

NOTE: *All VSS pins must be connected together in the application.*

2.4.1 VDDX,VSSX — Power & Ground Pins for I/O Drivers

External power and ground for I/O drivers. Because fast signal transitions place high, short-duration current demands on the power supply, use bypass capacitors with high-frequency characteristics and place them as close to the MCU as possible. Bypass requirements depend on how heavily the MCU pins are loaded.

2.4.2 VDDR, VSSR — Power & Ground Pins for I/O Drivers & for Internal Voltage Regulator

External power and ground for I/O drivers and input to the internal voltage regulator. Because fast signal transitions place high, short-duration current demands on the power supply, use bypass capacitors with high-frequency characteristics and place them as close to the MCU as possible. Bypass requirements depend on how heavily the MCU pins are loaded.

2.4.3 VDD1, VDD2, VSS1, VSS2 — Internal Logic Power Supply Pins

Power is supplied to the MCU through VDD and VSS. Because fast signal transitions place high, short-duration current demands on the power supply, use bypass capacitors with high-frequency characteristics and place them as close to the MCU as possible. This 2.5V supply is derived from the internal voltage regulator. There is no static load on those pins allowed. The internal voltage regulator is turned off, if VREGEN is tied to ground.

NOTE: *No load allowed except for bypass capacitors.*

4.3.3 Unsecuring the Microcontroller

In order to unsecure the microcontroller, the internal FLASH and EEPROM must be erased. This can be done through an external program in expanded mode or via a .sequence of BDM commands. Unsecuring is also possible via the Backdoor Key Access. Refer to Flash Block Guide for details.

Once the user has erased the FLASH and EEPROM, the part can be reset into special single chip mode. This invokes a program that verifies the erasure of the internal FLASH and EEPROM. Once this program completes, the user can erase and program the FLASH security bits to the unsecured state. This is generally done through the BDM, but the user could also change to expanded mode (by writing the mode bits through the BDM) and jumping to an external program (again through BDM commands). Note that if the part goes through a reset before the security bits are reprogrammed to the unsecure state, the part will be secured again.

4.4 Low Power Modes

The microcontroller features three main low power modes. Consult the respective Block User Guide for information on the module behavior in Stop, Pseudo Stop, and Wait Mode. An important source of information about the clock system is the Clock and Reset Generator User Guide (CRG).

4.4.1 Stop

Executing the CPU STOP instruction stops all clocks and the oscillator thus putting the chip in fully static mode. Wake up from this mode can be done via reset or external interrupts.

4.4.2 Pseudo Stop

This mode is entered by executing the CPU STOP instruction. In this mode the oscillator is still running and the Real Time Interrupt (RTI) or Watchdog (COP) sub module can stay active. Other peripherals are turned off. This mode consumes more current than the full STOP mode, but the wake up time from this mode is significantly shorter.

4.4.3 Wait

This mode is entered by executing the CPU WAI instruction. In this mode the CPU will not execute instructions. The internal CPU signals (address and databus) will be fully static. All peripherals stay active. For further power consumption the peripherals can individually turn off their local clocks.

4.4.4 Run

Although this is not a low power mode, unused peripheral modules should not be enabled in order to save power.

$FFCA, $FFCB	Modulus Down Counter underflow	I-Bit	MCCTL (MCZI)	$CA
$FFC8, $FFC9	Pulse Accumulator B Overflow	I-Bit	PBCTL (PBOVI)	$C8
$FFC6, $FFC7	CRG PLL lock	I-Bit	PLLCR (LOCKIE)	$C6
$FFC4, $FFC5	CRG Self Clock Mode	I-Bit	PLLCR (SCMIE)	$C4
$FFC2, $FFC3	BDLC	I-Bit	DLCBCR1 (IE)	$C2
$FFC0, $FFC1	IIC Bus	I-Bit	IBCR (IBIE)	$C0
$FFBE, $FFBF	SPI1	I-Bit	SPICR1 (SPIE, SPTIE)	$BE
$FFBC, $FFBD	Reserved			
$FFBA, $FFBB	EEPROM	I-Bit	ECNFG (CCIE, CBEIE)	$BA
$FFB8, $FFB9	FLASH	I-Bit	FCNFG (CCIE, CBEIE)	$B8
$FFB6, $FFB7	CAN0 wake-up	I-Bit	CANRIER (WUPIE)	$B6
$FFB4, $FFB5	CAN0 errors	I-Bit	CANRIER (CSCIE, OVRIE)	$B4
$FFB2, $FFB3	CAN0 receive	I-Bit	CANRIER (RXFIE)	$B2
$FFB0, $FFB1	CAN0 transmit	I-Bit	CANTIER (TXEIE[2:0])	$B0
$FFAE, $FFAF	CAN1 wake-up	I-Bit	CANRIER (WUPIE)	$AE
$FFAC, $FFAD	CAN1 errors	I-Bit	CANRIER (CSCIE, OVRIE)	$AC
$FFAA, $FFAB	CAN1 receive	I-Bit	CANRIER (RXFIE)	$AA
$FFA8, $FFA9	CAN1 transmit	I-Bit	CANTIER (TXEIE[2:0])	$A8
$FFA6, $FFA7	BF Receive FIFO not empty	I-Bit	BFRIER (RCVFIE)	$A6
$FFA4, $FFA5	BF receive	I-Bit	BFBUFCTL[15:0] (IENA)	$A4
$FFA2, $FFA3	BF Synchronization	I-Bit	BFRIER (SYNAIE, SYNNIE)	$A2
$FFA0, $FFA1	BF general	I-Bit	BFBUFCTL[15:0] (IENA), BFGIER (OVRNIE, ERRIE, SYNEIE, SYNLIE, ILLPIE, LOCKIE, WAKEIE) BFRIER (SLMMIE)	$A0
$FF98, $FF9F	Reserved			
$FF96, $FF97	CAN4 wake-up	I-Bit	CANRIER (WUPIE)	$96
$FF94, $FF95	CAN4 errors	I-Bit	CANRIER (CSCIE, OVRIE)	$94
$FF92, $FF93	CAN4 receive	I-Bit	CANRIER (RXFIE)	$92
$FF90, $FF91	CAN4 transmit	I-Bit	CANTIER (TXEIE[2:0])	$90
$FF8E, $FF8F	Port P Interrupt	I-Bit	PIEP (PIEP7-0)	$8E
$FF8C, $FF8D	PWM Emergency Shutdown	I-Bit	PWMSDN (PWMIE)	$8C
$FF80 to $FF8B	Reserved			

5.3 Effects of Reset

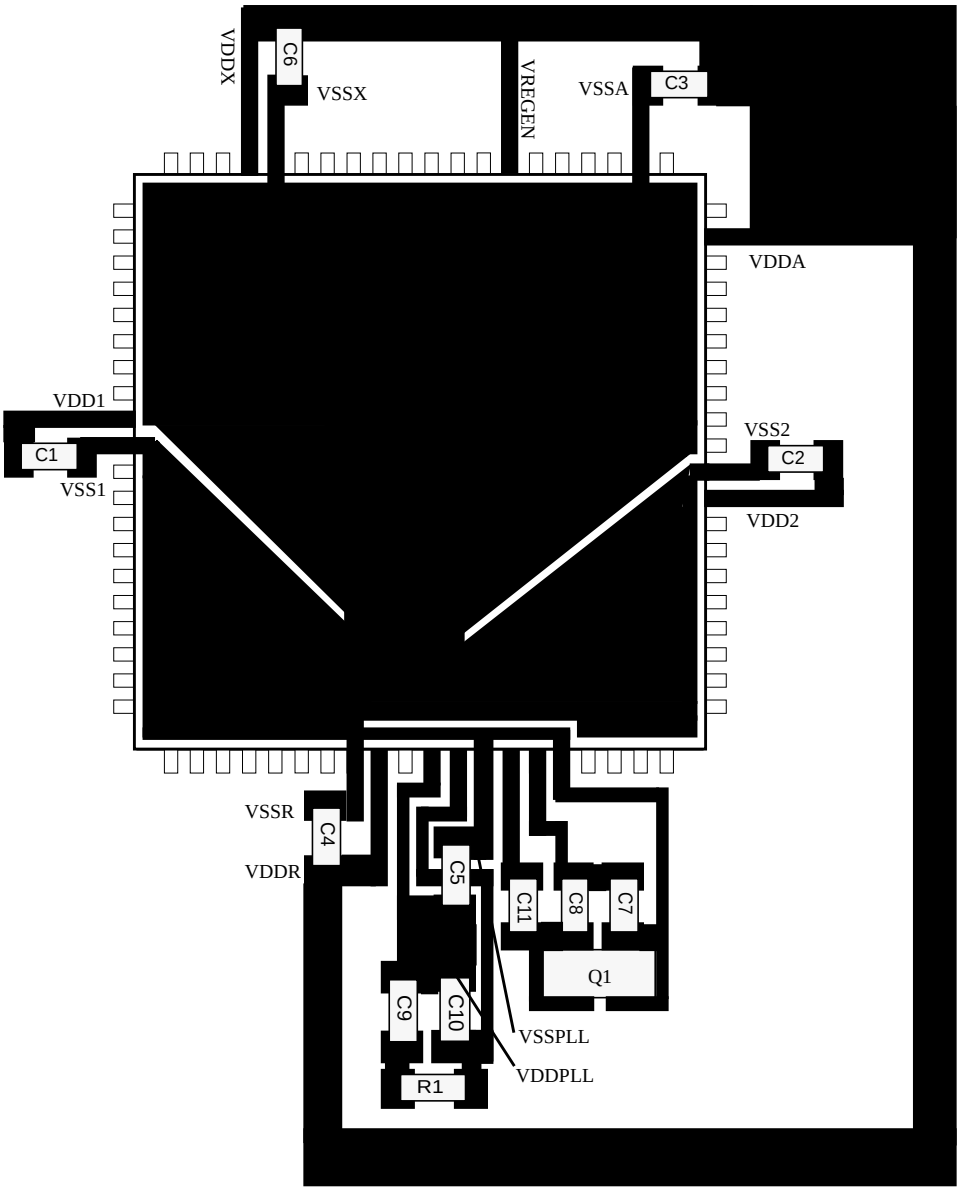
When a reset occurs, MCU registers and control bits are changed to known start-up states. Refer to the respective module Block User Guides for register reset states.

5.3.1 I/O pins

Refer to the HCS12 Multiplexed External Bus Interface (MEBI) Block Guide for mode dependent pin configuration of port A, B, E and K out of reset.

Refer to the PIM Block User Guide for reset configurations of all peripheral module ports.

Figure 23-2 Recommended PCB Layout for 80QFP (MC9S12DG128E, MC9S12DG128, MC9S12DJ128E, MC9S12DJ128, MC9S12A128, SC515847, SC515848, SC101161DG, SC101161DJ, SC102203, and SC102204) Colpitts Oscillator



A.1.10.1 Measurement Conditions

All measurements are without output loads. Unless otherwise noted the currents are measured in single chip mode, internal voltage regulator enabled and at 25MHz bus frequency using a 4MHz oscillator in Colpitts mode. Production testing is performed using a square wave signal at the EXTAL input.

A.1.10.2 Additional Remarks

In expanded modes the currents flowing in the system are highly dependent on the load at the address, data and control signals as well as on the duty cycle of those signals. No generally applicable numbers can be given. A very good estimate is to take the single chip currents and add the currents due to the external loads.

Table A-7 Supply Current Characteristics

Conditions are shown in **(Table A-4)** unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Run supply currents Single Chip, Internal regulator enabled	I_{DD5}			55	mA
2	P P	Wait Supply current All modules enabled, PLL on only RTI enabled (1)	I_{DDW}			30 5	mA
3	 C P C C P C P C P	Pseudo Stop Current (RTI and COP disabled) 1, 2 -40°C 27°C 70°C 85°C “C” Temp Option 100°C 105°C “V” Temp Option 120°C 125°C “M” Temp Option 140°C	I_{DDPS}		 370 400 450 550 600 650 800 850 1200	 500 1600 2100 5000	µA
4	 C C C C C C C	Pseudo Stop Current (RTI and COP enabled) (1), (2) -40°C 27°C 70°C 85°C 105°C 125°C 140°C	I_{DDPS}		 570 600 650 750 850 1200 1500		µA
5	 C P C C P C P C P	Stop Current (2) -40°C 27°C 70°C 85°C “C” Temp Option 100°C 105°C “V” Temp Option 120°C 125°C “M” Temp Option 140°C	I_{DDS}		 12 25 100 130 160 200 350 400 600	 100 1200 1700 5000	µA

Appendix B Package Information

B.1 General

This section provides the physical dimensions of the MC9S12DT128 packages.