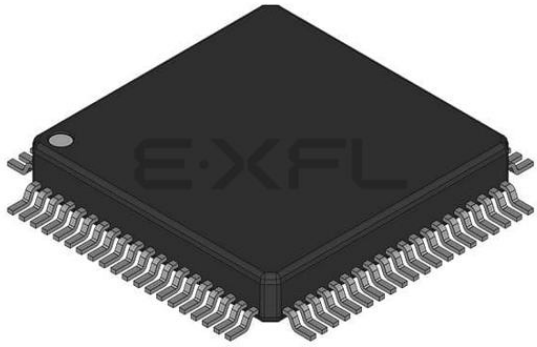

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	HCS12
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, I²C, SCI, SPI
Peripherals	PWM, WDT
Number of I/O	59
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 5.25V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	80-QFP
Supplier Device Package	80-QFP (14x14)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9s12dg128mfue

Version Number	Revision Date	Effective Date	Author	Description of Changes
V02.07	29 Jan 2003	29 Jan 2003		Added 3L40K mask set in section 1.6 Corrected register entries in section 1.5.1 “Detailed Memory Map” Updated description for ROMCTL in section 2.3.31 Updated section 4.3.3 “Unsecuring the Microcontroller” Corrected and updated device-specific information for OSC (section 8.1) & Byteflight (section 15.1) Updated footnote in Table A-4 “Operating Conditions” Changed reference of VDDM to VDDR in section A.1.8 Removed footnote on input leakage current in Table A-6 “5V I/O Characteristics”
V02.08	26 Feb 2003	26 Feb 2003		Added part numbers MC9S12DT128E, MC9S12DG128E, and MC9S12DJ128E in “Preface” and related part number references Removed mask sets 0L40K and 2L40K from Table 1-3
V02.09	15 Oct 2003	15 Oct 2003		Replaced references to HCS12 Core Guide by the individual HCS12 Block guides in Table 0-2, section 1.5.1, and section 6; updated Fig.3-1 “Clock Connections” to show the individual HCS12 blocks Corrected PIM module name and document order number in Table 0-2 “Document References” Corrected ECT pulse accumulators description in section 1.2 “Features” Corrected KWP5 pin name in Fig 2-1 112LQFP pin assignments Corrected pull resistor CTRL/reset states for PE7 and PE4-PE0 in Table 2.1 “Signal Properties” Mentioned “S12LRAE” bootloader in Flash section 17 Corrected footnote on clamp of TEST pin under Table A-1 “Absolute Maximum Ratings” Corrected minimum bus frequency to 0.25MHz in Table A-4 “Operating Conditions” Replaced “burst programming” by “row programming” in A.3 “NVM, Flash and EEPROM” Corrected blank check time for EEPROM in Table A-11 “NVM Timing Characteristics” Corrected operating frequency in Table A-18 “SPI Master/Slave Mode Timing Characteristics
V02.10	6 Feb 2004	6 Feb 2004		Added A128 information in “Derivative Differences”, 2.1 “Device Pinout”, 2.2 “Signal Properties Summary”, Fig 23-2 & Fig 23-4 Added lead-free package option (PVE) in Table 0-2 “Derivative Differences for MC9S12DB128” and Fig 0-1 “Order Partnumber Example” Added an “AEC qualified” row in the “Derivative Differences” tables 0-1 & 0-2.
V02.11	3 May 2004	3 May 2004		Added part numbers SC515846, SC515847, SC515848, and SC515849 in “Derivative Differences” tables 0-1 & 0-2, section 2, and section 23. Corrected and added maskset 4L40K in tables 0-1 & 0-2 and section 1.6. Corrected BDLC module availability in DB128 80QFP part in “Derivative Differences” table 0-2.

- Do not write or read Byteflight registers (after reset: address range $0300 - $035F), if using a derivative without Byteflight registers (see **(Table 0-1)** and **(Table 0-2)**).

- **Interrupts**
  - Fill the four CAN0 interrupt vectors ($FFB0 - $FFB7) according to your coding policies for unused interrupts, if using a derivative without CAN0 (see **(Table 0-1)** and **(Table 0-2)**).
  - Fill the four CAN1 interrupt vectors ($FFA8 - $FFAF) according to your coding policies for unused interrupts, if using a derivative without CAN1 (see **(Table 0-1)** and **(Table 0-2)**).
  - Fill the four CAN4 interrupt vectors ($FF90 - $FF97) according to your coding policies for unused interrupts, if using a derivative without CAN4 (see **(Table 0-1)** and **(Table 0-2)**).
  - Fill the BDLC interrupt vector ($FFC2, $FFC3) according to your coding policies for unused interrupts, if using a derivative without BDLC (see **(Table 0-1)** and **(Table 0-2)**).
  - Fill the IIC interrupt vector ($FFC0, $FFC1) according to your coding policies for unused interrupts, if using a derivative without IIC (see **(Table 0-1)** and **(Table 0-2)**).
  - Fill the four Byteflight interrupt vectors ($FFA0 - $FFA7) according to your coding policies for unused interrupts, if using a derivative without Byteflight (see **(Table 0-1)** and **(Table 0-2)**).

- **Ports**
  - The CAN0 pin functionality (TXCAN0, RXCAN0) is not available on port PJ7, PJ6, PM5, PM4, PM3, PM2, PM1 and PM0, if using a derivative without CAN0 (see **(Table 0-1)** and **(Table 0-2)**).
  - The CAN1 pin functionality (TXCAN1, RXCAN1) is not available on port PM3 and PM2, if using a derivative without CAN1 (see **(Table 0-1)** and **(Table 0-2)**).
  - The CAN4 pin functionality (TXCAN4, RXCAN4) is not available on port PJ7, PJ6, PM7, PM6, PM5 and PM4, if using a derivative without CAN4 (see **(Table 0-1)** and **(Table 0-2)**).
  - The BDLC pin functionality (TXB, RXB) is not available on port PM1 and PM0, if using a derivative without BDLC (see **(Table 0-1)** and **(Table 0-2)**).
  - The IIC pin functionality (SCL, SCA) is not available on port PJ7 and PJ6, if using a derivative without IIC (see **(Table 0-1)** and **(Table 0-2)**).
  - The Byteflight pin functionality (BF_PSLM, BF_PERR, BF_PROK, BF_PSYN, TX_BF, RX_BF) is not available on port PM7, PM6, PM5, PM4, PM3 and PM2, if using a derivative without Byteflight (see **(Table 0-1)** and **(Table 0-2)**).
  - Do not write MODRR1 and MODRR0 Bit of Module Routing Register (PIM_9DTB128 Block User Guide), if using a derivative without CAN0 (see **(Table 0-1)** and **(Table 0-2)**).
  - Do not write MODRR3 and MODRR2 Bit of Module Routing Register (PIM_9DTB128 Block User Guide), if using a derivative without CAN4 (see **(Table 0-1)** and **(Table 0-2)**).

- **Pins not available in 80 pin QFP package for MC9S12DG128E, MC9S12DG128, MC9S12DJ128E, MC9S12DJ128, MC9S12A128, SC515847, SC515848, SC101161DG, SC101161DJ, SC102203, and SC102204**

1.4 Block Diagram

Figure 1-1 shows a block diagram of the MC9S12DT128 device.

1.5 Device Memory Map

(Table 1-1) and **(Figure 1-2)** show the device memory map of the MC9S12DT128 after reset. Note that after reset the EEPROM ($0000 – $07FF) is hidden by the register space ($0000 - $03FF) and the RAM ($0000 - $1FFF). The bottom 1K Bytes of RAM ($0000 - $03FF) are hidden by the register space.

Table 1-1 Device Memory Map

Address	Module	Size (Bytes)
$0000 – $0017	CORE (Ports A, B, E, Modes, Inits, Test)	24
$0018 – $0019	Reserved	2
$001A – $001B	Device ID register (PARTID)	2
$001C – $001F	CORE (MEMSIZ, IRQ, HPRIO)	4
$0020 – $0027	Reserved	8
$0028 – $002F	CORE (Background Debug Module)	8
$0030 – $0033	CORE (PPAGE, Port K)	4
$0034 – $003F	Clock and Reset Generator (PLL, RTI, COP)	12
$0040 – $007F	Enhanced Capture Timer 16-bit 8 channels	64
$0080 – $009F	Analog to Digital Converter 10-bit 8 channels (ATD0)	32
$00A0 – $00C7	Pulse Width Modulator 8-bit 8 channels (PWM)	40
$00C8 – $00CF	Serial Communications Interface (SCI0)	8
$00D0 – $00D7	Serial Communications Interface (SCI1)	8
$00D8 – $00DF	Serial Peripheral Interface (SPI0)	8
$00E0 – $00E7	Inter IC Bus	8
$00E8 – $00EF	Byte Level Data Link Controller (BDLC)	8
$00F0 – $00F7	Serial Peripheral Interface (SPI1)	8
$00F8 – $00FF	Reserved	8
$0100 – $010F	Flash Control Register	16
$0110 – $011B	EEPROM Control Register	12
$011C – $011F	Reserved	4
$0120 – $013F	Analog to Digital Converter 10-bit 8 channels (ATD1)	32
$0140 – $017F	Motorola Scalable CAN (CAN0)	64
$0180 – $01BF	Motorola Scalable CAN (CAN1)	64
$01C0 – $01FF	Reserved	64
$0200 – $023F	Reserved	64
$0240 – $027F	Port Integration Module (PIM)	64
$0280 – $02BF	Motorola Scalable CAN (CAN4)	64
$02C0 – $02FF	Reserved	64
$0300 – $035F	Byteflight (BF)	96
$0360 – $03FF	Reserved	160
$0000 – $07FF	EEPROM array	2048
$0000 – $1FFF	RAM array	8192
$4000 – $7FFF	Fixed Flash EEPROM array incl. 0.5K, 1K, 2K or 4K Protected Sector at start	16384
$8000 – $BFFF	Flash EEPROM Page Window	16384

$0040 - $007F ECT (Enhanced Capture Timer 16 Bit 8 Channels)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$004A	TCTL3	Read:	EDG7B	EDG7A	EDG6B	EDG6A	EDG5B	EDG5A	EDG4B	EDG4A
		Write:								
$004B	TCTL4	Read:	EDG3B	EDG3A	EDG2B	EDG2A	EDG1B	EDG1A	EDG0B	EDG0A
		Write:								
$004C	TIE	Read:	C7I	C6I	C5I	C4I	C3I	C2I	C1I	C0I
		Write:								
$004D	TSCR2	Read:	TOI	0	0	0	TCRE	PR2	PR1	PR0
		Write:								
$004E	TFLG1	Read:	C7F	C6F	C5F	C4F	C3F	C2F	C1F	C0F
		Write:								
$004F	TFLG2	Read:	TOF	0	0	0	0	0	0	0
		Write:								
$0050	TC0 (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$0051	TC0 (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0052	TC1 (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$0053	TC1 (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0054	TC2 (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$0055	TC2 (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0056	TC3 (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$0057	TC3 (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0058	TC4 (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$0059	TC4 (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$005A	TC5 (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$005B	TC5 (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$005C	TC6 (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$005D	TC6 (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$005E	TC7 (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$005F	TC7 (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0060	PACTL	Read:	0	PAEN	PAMOD	PEDGE	CLK1	CLK0	PAOVI	PAI
		Write:								
$0061	PAFLG	Read:	0	0	0	0	0	0	PAOVF	PAIF
		Write:								
$0062	PACN3 (hi)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								

$0040 - $007F ECT (Enhanced Capture Timer 16 Bit 8 Channels)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0063	PACN2 (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0064	PACN1 (hi)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0065	PACN0 (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0066	MCCTL	Read:	MCZI	MODMC	RDMCL	0	0	MCEN	MCPR1	MCPR0
		Write:				ICLAT	FLMC			
$0067	MCFLG	Read:	MCZF	0	0	0	POLF3	POLF2	POLF1	POLF0
		Write:								
$0068	ICPAR	Read:	0	0	0	0	PA3EN	PA2EN	PA1EN	PA0EN
		Write:								
$0069	DLYCT	Read:	0	0	0	0	0	0	DLY1	DLY0
		Write:								
$006A	ICOVW	Read:	NOVW7	NOVW6	NOVW5	NOVW4	NOVW3	NOVW2	NOVW1	NOVW0
		Write:								
$006B	ICSYS	Read:	SH37	SH26	SH15	SH04	TFMOD	PACMX	BUFEN	LATQ
		Write:								
$006C	Reserved	Read:								
		Write:								
$006D	TIMTST Test Only	Read:	0	0	0	0	0	0	TCBYP	0
		Write:								
$006E	Reserved	Read:								
		Write:								
$006F	Reserved	Read:								
		Write:								
$0070	PBCTL	Read:	0	PBEN	0	0	0	0	PBOVI	0
		Write:								
$0071	PBFLG	Read:	0	0	0	0	0	0	PBOVF	0
		Write:								
$0072	PA3H	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0073	PA2H	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0074	PA1H	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0075	PA0H	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0076	MCCNT (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$0077	MCCNT (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0078	TC0H (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$0079	TC0H (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$007A	TC1H (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$007B	TC1H (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								

$00A0 - $00C7 PWM (Pulse Width Modulator 8 Bit 8 Channel)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00A9	PWMSCLB	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00AA	PWMSCNTA Test Only	Read:	0	0	0	0	0	0	0	0
		Write:								
$00AB	PWMSCNTB Test Only	Read:	0	0	0	0	0	0	0	0
		Write:								
$00AC	PWMCNT0	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:	0	0	0	0	0	0	0	0
$00AD	PWMCNT1	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:	0	0	0	0	0	0	0	0
$00AE	PWMCNT2	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:	0	0	0	0	0	0	0	0
$00AF	PWMCNT3	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:	0	0	0	0	0	0	0	0
$00B0	PWMCNT4	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:	0	0	0	0	0	0	0	0
$00B1	PWMCNT5	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:	0	0	0	0	0	0	0	0
$00B2	PWMCNT6	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:	0	0	0	0	0	0	0	0
$00B3	PWMCNT7	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:	0	0	0	0	0	0	0	0
$00B4	PWMPER0	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00B5	PWMPER1	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00B6	PWMPER2	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00B7	PWMPER3	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00B8	PWMPER4	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00B9	PWMPER5	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00BA	PWMPER6	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00BB	PWMPER7	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00BC	PWMDTY0	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00BD	PWMDTY1	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00BE	PWMDTY2	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00BF	PWMDTY3	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00C0	PWMDTY4	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00C1	PWMDTY5	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0

$00A0 - $00C7 PWM (Pulse Width Modulator 8 Bit 8 Channel)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00C2	PWMDTY6	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00C3	PWMDTY7	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00C4	PWMSDN	Read: Write:	PWMIF	PWMIE	PWMRSTRT	PWMLVL	0	PWM7IN	PWM7INL	PWM7ENA
$00C5	Reserved	Read: Write:	0	0	0	0	0	0	0	0
$00C6	Reserved	Read: Write:	0	0	0	0	0	0	0	0
$00C7	Reserved	Read: Write:	0	0	0	0	0	0	0	0

$00C8 - $00CF SCI0 (Asynchronous Serial Interface)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00C8	SCI0BDH	Read: Write:	0	0	0	SBR12	SBR11	SBR10	SBR9	SBR8
$00C9	SCI0BDL	Read: Write:	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0
$00CA	SCI0CR1	Read: Write:	LOOPS	SCISWAI	RSRC	M	WAKE	ILT	PE	PT
$00CB	SCI0CR2	Read: Write:	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
$00CC	SCI0SR1	Read: Write:	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF
$00CD	SCI0SR2	Read: Write:	0	0	0	0	0	BRK13	TXDIR	RAF
$00CE	SCI0DRH	Read: Write:	R8	T8	0	0	0	0	0	0
$00CF	SCI0DRL	Read: Write:	R7	R6	R5	R4	R3	R2	R1	R0
			T7	T6	T5	T4	T3	T2	T1	T0

$00D0 - $00D7 SCI1 (Asynchronous Serial Interface)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00D0	SCI1BDH	Read: Write:	0	0	0	SBR12	SBR11	SBR10	SBR9	SBR8
$00D1	SCI1BDL	Read: Write:	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0
$00D2	SCI1CR1	Read: Write:	LOOPS	SCISWAI	RSRC	M	WAKE	ILT	PE	PT
$00D3	SCI1CR2	Read: Write:	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
$00D4	SCI1SR1	Read: Write:	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF

$0240 - $027F PIM (Port Integration Module)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0259	PTIP	Read:	PTIP7	PTIP6	PTIP5	PTIP4	PTIP3	PTIP2	PTIP1	PTIP0
		Write:								
$025A	DDRP	Read:	DDRP7	DDRP7	DDRP5	DDRP4	DDRP3	DDRP2	DDRP1	DDRP0
		Write:								
$025B	RDRP	Read:	RDRP7	RDRP6	RDRP5	RDRP4	RDRP3	RDRP2	RDRP1	RDRP0
		Write:								
$025C	PERP	Read:	PERP7	PERP6	PERP5	PERP4	PERP3	PERP2	PERP1	PERP0
		Write:								
$025D	PPSP	Read:	PPSP7	PPSP6	PPSP5	PPSP4	PPSP3	PPSP2	PPSP1	PPSS0
		Write:								
$025E	PIEP	Read:	PIEP7	PIEP6	PIEP5	PIEP4	PIEP3	PIEP2	PIEP1	PIEP0
		Write:								
$025F	PIFP	Read:	PIFP7	PIFP6	PIFP5	PIFP4	PIFP3	PIFP2	PIFP1	PIFP0
		Write:								
$0260	PTH	Read:	PTH7	PTH6	PTH5	PTH4	PTH3	PTH2	PTH1	PTH0
		Write:								
$0261	PTIH	Read:	PTIH7	PTIH6	PTIH5	PTIH4	PTIH3	PTIH2	PTIH1	PTIH0
		Write:								
$0262	DDRH	Read:	DDRH7	DDRH7	DDRH5	DDRH4	DDRH3	DDRH2	DDRH1	DDRH0
		Write:								
$0263	RDRH	Read:	RDRH7	RDRH6	RDRH5	RDRH4	RDRH3	RDRH2	RDRH1	RDRH0
		Write:								
$0264	PERH	Read:	PERH7	PERH6	PERH5	PERH4	PERH3	PERH2	PERH1	PERH0
		Write:								
$0265	PPSH	Read:	PPSH7	PPSH6	PPSH5	PPSH4	PPSH3	PPSH2	PPSH1	PPSH0
		Write:								
$0266	PIEH	Read:	PIEH7	PIEH6	PIEH5	PIEH4	PIEH3	PIEH2	PIEH1	PIEH0
		Write:								
$0267	PIFH	Read:	PIFH7	PIFH6	PIFH5	PIFH4	PIFH3	PIFH2	PIFH1	PIFH0
		Write:								
$0268	PTJ	Read:	PTJ7	PTJ6	0	0	0	0	PTJ1	PTJ0
		Write:								
$0269	PTIJ	Read:	PTIJ7	PTIJ6	0	0	0	0	PTIJ1	PTIJ0
		Write:								
$026A	DDRJ	Read:	DDRJ7	DDRJ7	0	0	0	0	DDRJ1	DDRJ0
		Write:								
$026B	RDRJ	Read:	RDRJ7	RDRJ6	0	0	0	0	RDRJ1	RDRJ0
		Write:								
$026C	PERJ	Read:	PERJ7	PERJ6	0	0	0	0	PERJ1	PERJ0
		Write:								
$026D	PPSJ	Read:	PPSJ7	PPSJ6	0	0	0	0	PPSJ1	PPSJ0
		Write:								
$026E	PIEJ	Read:	PIEJ7	PIEJ6	0	0	0	0	PIEJ1	PIEJ0
		Write:								
$026F	PIFJ	Read:	PIFJ7	PIFJ6	0	0	0	0	PIFJ1	PIFJ0
		Write:								
$0270 - $027F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

2.3.36 PM4 / BF_PSYN / RXCAN0 / RXCAN4/ MOSI0 — Port M I/O Pin 4

PM4 is a general purpose input or output pin. It can be configured as the correct synchronisation pulse reception/transmission output pulse pin of Byteflight. It can be configured as the receive pin RXCAN of the Motorola Scalable Controller Area Network controllers 0 or 4 (CAN0 or CAN4). It can be configured as the master output (during master mode) or slave input pin (during slave mode) MOSI for the Serial Peripheral Interface 0 (SPI0).

2.3.37 PM3 / TX_BF / TXCAN1 / TXCAN0 / $\overline{SS0}$ — Port M I/O Pin 3

PM3 is a general purpose input or output pin. It can be configured as the transmit pinTX_BF of Byteflight. It can be configured as the transmit pin TXCAN of the Motorola Scalable Controller Area Network controllers 1 or 0 (CAN1 or CAN0). It can be configured as the slave select pin $\overline{SS}$ of the Serial Peripheral Interface 0 (SPI0).

2.3.38 PM2 / RX_BF / RXCAN1 / RXCAN0 / MISO0 — Port M I/O Pin 2

PM2 is a general purpose input or output pin. It can be configured as the receive pin RX_BF of Byteflight. It can be configured as the receive pin RXCAN of the Motorola Scalable Controller Area Network controllers 1 or 0 (CAN1 or CAN0). It can be configured as the master input (during master mode) or slave output pin (during slave mode) MISO for the Serial Peripheral Interface 0 (SPI0).

2.3.39 PM1 / TXCAN0 / TXB — Port M I/O Pin 1

PM1 is a general purpose input or output pin. It can be configured as the transmit pin TXCAN of the Motorola Scalable Controller Area Network controller 0 (CAN0). It can be configured as the transmit pin TXB of the BDLC.

2.3.40 PM0 / RXCAN0 / RXB — Port M I/O Pin 0

PM0 is a general purpose input or output pin. It can be configured as the receive pin RXCAN of the Motorola Scalable Controller Area Network controller 0 (CAN0). It can be configured as the receive pin RXB of the BDLC.

2.3.41 PP7 / KWP7 / PWM7 — Port P I/O Pin 7

PP7 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 7 output.

2.3.42 PP6 / KWP6 / PWM6 — Port P I/O Pin 6

PP6 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 6 output.

Mnemonic	Pin Number 112-pin QFP	Nominal Voltage	Description
VDDR	41	5.0V	External power and ground, supply to pin drivers and internal voltage regulator.
VSSR	40	0V	
VDDX	107	5.0V	External power and ground, supply to pin drivers.
VSSX	106	0V	
VDDA	83	5.0V	Operating voltage and ground for the analog-to-digital converters and the reference for the internal voltage regulator, allows the supply voltage to the A/D to be bypassed independently.
VSSA	86	0V	
VRL	85	0V	Reference voltages for the analog-to-digital converter.
VRH	84	5.0V	
VDDPLL	43	2.5V	Provides operating voltage and ground for the Phased-Locked Loop. This allows the supply voltage to the PLL to be bypassed independently. Internal power and ground generated by internal regulator.
VSSPLL	45	0V	
VREGEN	97	5V	Internal Voltage Regulator enable/disable

NOTE: *All VSS pins must be connected together in the application.*

2.4.1 VDDX,VSSX — Power & Ground Pins for I/O Drivers

External power and ground for I/O drivers. Because fast signal transitions place high, short-duration current demands on the power supply, use bypass capacitors with high-frequency characteristics and place them as close to the MCU as possible. Bypass requirements depend on how heavily the MCU pins are loaded.

2.4.2 VDDR, VSSR — Power & Ground Pins for I/O Drivers & for Internal Voltage Regulator

External power and ground for I/O drivers and input to the internal voltage regulator. Because fast signal transitions place high, short-duration current demands on the power supply, use bypass capacitors with high-frequency characteristics and place them as close to the MCU as possible. Bypass requirements depend on how heavily the MCU pins are loaded.

2.4.3 VDD1, VDD2, VSS1, VSS2 — Internal Logic Power Supply Pins

Power is supplied to the MCU through VDD and VSS. Because fast signal transitions place high, short-duration current demands on the power supply, use bypass capacitors with high-frequency characteristics and place them as close to the MCU as possible. This 2.5V supply is derived from the internal voltage regulator. There is no static load on those pins allowed. The internal voltage regulator is turned off, if VREGEN is tied to ground.

NOTE: *No load allowed except for bypass capacitors.*

2.4.4 VDDA, VSSA — Power Supply Pins for ATD and VREG

VDDA, VSSA are the power supply and ground input pins for the voltage regulator and the analog to digital converter. It also provides the reference for the internal voltage regulator. This allows the supply voltage to the ATD and the reference voltage to be bypassed independently.

2.4.5 VRH, VRL — ATD Reference Voltage Input Pins

VRH and VRL are the reference voltage input pins for the analog to digital converter.

2.4.6 VDDPLL, VSSPLL — Power Supply Pins for PLL

Provides operating voltage and ground for the Oscillator and the Phased-Locked Loop. This allows the supply voltage to the Oscillator and PLL to be bypassed independently.This 2.5V voltage is generated by the internal voltage regulator.

NOTE: *No load allowed except for bypass capacitors.*

2.4.7 VREGEN — On Chip Voltage Regulator Enable

Enables the internal 5V to 2.5V voltage regulator. If this pin is tied low, VDD1,2 and VDDPLL must be supplied externally.

6.4 HCS12 Interrupt (INT) Block Description

Consult the INT Block Guide for information on the HCS12 Interrupt module.

6.5 HCS12 Background Debug Module (BDM) Block Description

Consult the BDM Block Guide for information on the HCS12 Background Debug module.

6.5.1 Device-specific information

When the BDM Block Guide refers to *alternate clock* this is equivalent to *oscillator clock*.

6.6 HCS12 Breakpoint (BKP) Block Description

Consult the BKP Block Guide for information on the HCS12 Breakpoint module.

Section 7 Clock and Reset Generator (CRG) Block Description

Consult the CRG Block User Guide for information about the Clock and Reset Generator module.

7.1 Device-specific information

The Low Voltage Reset feature of the CRG is not available on this device.

Section 8 Oscillator (OSC) Block Description

Consult the OSC Block User Guide for information about the Oscillator module.

8.1 Device-specific information

The $\overline{\text{XCLKS}}$ input signal is active low (see **2.3.12 PE / NOACC / $\overline{\text{XCLKS}}$ — Port E I/O Pin 7**).

Section 9 Enhanced Capture Timer (ECT) Block Description

A.1.5 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only. A functional operation under or outside those maxima is not guaranteed. Stress beyond those limits may affect the reliability or cause permanent damage of the device.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS5} or V_{DD5}).

Table A-1 Absolute Maximum Ratings[1]

Num	Rating	Symbol	Min	Max	Unit
1	I/O, Regulator and Analog Supply Voltage	V_{DD5}	-0.3	6.0	V
2	Digital Logic Supply Voltage [2]	V_{DD}	-0.3	3.0	V
3	PLL Supply Voltage [(2)]	V_{DDPLL}	-0.3	3.0	V
4	Voltage difference VDDX to VDDR and VDDA	Δ_{VDDX}	-0.3	0.3	V
5	Voltage difference VSSX to VSSR and VSSA	Δ_{VSSX}	-0.3	0.3	V
6	Digital I/O Input Voltage	V_{IN}	-0.3	6.0	V
7	Analog Reference	$V_{RH,}$ V_{RL}	-0.3	6.0	V
8	XFC, EXTAL, XTAL inputs	V_{ILV}	-0.3	3.0	V
9	TEST input	V_{TEST}	-0.3	10.0	V
10	Instantaneous Maximum Current Single pin limit for all digital I/O pins [3]	I_D	-25	+25	mA
11	Instantaneous Maximum Current Single pin limit for XFC, EXTAL, XTAL[4]	I_{DL}	-25	+25	mA
12	Instantaneous Maximum Current Single pin limit for TEST [5]	I_{DT}	-0.25	0	mA
13	Storage Temperature Range	T_{stg}	– 65	155	°C

NOTES:
1. Beyond absolute maximum ratings device might be damaged.
2. The device contains an internal voltage regulator to generate the logic and PLL supply out of the I/O supply. The absolute maximum ratings apply when the device is powered from an external source.
3. All digital I/O pins are internally clamped to V_{SSX} and V_{DDX}, V_{SSR} and V_{DDR} or V_{SSA} and V_{DDA}.
4. Those pins are internally clamped to V_{SSPLL} and V_{DDPLL}.
5. This pin is clamped low to V_{SSX}, but not clamped high. This pin must be tied low in applications.

A.1.6 ESD Protection and Latch-up Immunity

All ESD testing is in conformity with CDF-AEC-Q100 Stress test qualification for Automotive Grade Integrated Circuits. During the device qualification ESD stresses were performed for the Human Body Model (HBM), the Machine Model (MM) and the Charge Device Model.

A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table A-2 ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series Resistance	R1	1500	Ohm
	Storage Capacitance	C	100	pF
	Number of Pulse per pin positive negative	–	– 3 3	
Machine	Series Resistance	R1	0	Ohm
	Storage Capacitance	C	200	pF
	Number of Pulse per pin positive negative	–	– 3 3	
Latch-up	Minimum input voltage limit		–2.5	V
	Maximum input voltage limit		7.5	V

Table A-3 ESD and Latch-Up Protection Characteristics

Num	C	Rating	Symbol	Min	Max	Unit
1	C	Human Body Model (HBM)	V_{HBM}	2000	–	V
2	C	Machine Model (MM)	V_{MM}	200	–	V
3	C	Charge Device Model (CDM)	V_{CDM}	500	–	V
4	C	Latch-up Current at 125°C positive negative	I_{LAT}	+100 –100	–	mA
5	C	Latch-up Current at 27°C positive negative	I_{LAT}	+200 –200	–	mA

A.1.7 Operating Conditions

This chapter describes the operating conditions of the device. Unless otherwise noted those conditions apply to all the following data.

NOTE: *Please refer to the temperature rating of the device (C, V, M) with regards to the ambient temperature T_A and the junction temperature T_J. For power dissipation*

calculations refer to ***Section A.1.8 Power Dissipation and Thermal Characteristics****.*

Table A-4 Operating Conditions

Rating	Symbol	Min	Typ	Max	Unit
I/O, Regulator and Analog Supply Voltage	V_{DD5}	4.5	5	5.25	V
Digital Logic Supply Voltage [1]	V_{DD}	2.35	2.5	2.75	V
PLL Supply Voltage [1]	V_{DDPLL}	2.25	2.5	2.75	V
Voltage Difference VDDX to VDDR and VDDA	Δ_{VDDX}	-0.1	0	0.1	V
Voltage Difference VSSX to VSSR and VSSA	Δ_{VSSX}	-0.1	0	0.1	V
Bus Frequency	f_{bus}	0.25[2]	-	25	MHz
MC9S12DT128**C** Operating Junction Temperature Range	T_J	-40	-	100	°C
Operating Ambient Temperature Range [3]	T_A	-40	27	85	°C
MC9S12DT128**V** Operating Junction Temperature Range	T_J	-40	-	120	°C
Operating Ambient Temperature Range [3]	T_A	-40	27	105	°C
MC9S12DT128**M** Operating Junction Temperature Range	T_J	-40	-	140	°C
Operating Ambient Temperature Range [3]	T_A	-40	27	125	°C

NOTES:
1. The device contains an internal voltage regulator to generate the logic and PLL supply out of the I/O supply. The given operating range applies when this regulator is disabled and the device is powered from an external source.
2. Some blocks e.g. ATD (conversion) and NVMs (program/erase) require higher bus frequencies for proper operation.
3. Please refer to **Section A.1.8 Power Dissipation and Thermal Characteristics** for more details about the relation between ambient temperature T_A and device junction temperature T_J.

A.1.8 Power Dissipation and Thermal Characteristics

Power dissipation and thermal characteristics are closely related. The user must assure that the maximum operating junction temperature is not exceeded. The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \bullet \Theta_{JA})$$

T_J = Junction Temperature, [°C]

T_A = Ambient Temperature, [°C]

A.3 NVM, Flash and EEPROM

NOTE: *Unless otherwise noted the abbreviation NVM (Non Volatile Memory) is used for both Flash and EEPROM.*

A.3.1 NVM timing

The time base for all NVM program or erase operations is derived from the oscillator. A minimum oscillator frequency f_{NVMOSC} is required for performing program or erase operations. The NVM modules do not have any means to monitor the frequency and will not prevent program or erase operation at frequencies above or below the specified minimum. Attempting to program or erase the NVM modules at a lower frequency a full program or erase transition is not assured.

The Flash and EEPROM program and erase operations are timed using a clock derived from the oscillator using the FCLKDIV and ECLKDIV registers respectively. The frequency of this clock must be set within the limits specified as f_{NVMOP}.

The minimum program and erase times shown in **(Table A-11)** are calculated for maximum f_{NVMOP} and maximum f_{bus}. The maximum times are calculated for minimum f_{NVMOP} and a f_{bus} of 2MHz.

A.3.1.1 Single Word Programming

The programming time for single word programming is dependant on the bus frequency as a well as on the frequency f_{NVMOP} and can be calculated according to the following formula.

$$t_{swpgm} = 9 \cdot \frac{1}{f_{NVMOP}} + 25 \cdot \frac{1}{f_{bus}}$$

A.3.1.2 Row Programming

This applies only to the Flash where up to 32 words in a row can be programmed consecutively by keeping the command pipeline filled. The time to program a consecutive word can be calculated as:

$$t_{bwpgm} = 4 \cdot \frac{1}{f_{NVMOP}} + 9 \cdot \frac{1}{f_{bus}}$$

The time to program a whole row is:

$$t_{brpgm} = t_{swpgm} + 31 \cdot t_{bwpgm}$$

Row programming is more than 2 times faster than single word programming.

A.3.1.3 Sector Erase

Erasing a 512 byte Flash sector or a 4 byte EEPROM sector takes: