Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HCS12
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, I²C, SCI, SPI
Peripherals	PWM, WDT
Number of I/O	91
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 5.25V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s12dg128mpver

Version Number	Revision Date	Effective Date	Author	Description of Changes
V02.02	08 Mar 2002	08 Mar 2002		Changed XCLKS to PE7 in Table 2-2 Updated device part numbers in Figure 2-1 Updated BDM clock in Figure 3-1 Removed SIM description in overview & n_{UPOSC} spec in Table A-15 Updated electrical spec of VDD & VDDPLL (Table A-4), IOL/IOH (Table A-6), C_{INS} (Table A-9), C_{IN} (Table A-6 & A-15), Updated interrupt pulse timing variables in Table A-6 Updated device part numbers in Figure 2-1 Added document numbers on cover page and Table 0-2
V02.03	14 Mar 2002	14 Mar 2002		Cleaned up Fig. 1-1, 2-1 Updated Section 1.5 descriptions Corrected PE assignment in Table 2-2, Fig. 2-5,6,7. Corrected NVM sizes in Sections 16, 17 Added I_{REF} spec for 1ATD in Table A-8 Added Blank Check in A.3.1.5 and Table A-11 Updated CRG spec in Table A-15
V02.04	16 Aug 2002	16 Aug 2002		Added: Pull-up columns to signal table, Example for PLL Filter calculation, Thermal values for junction to board and package, BGND pin pull-up Part Order Information Global Register Table Chip Configuration Summary Device specific info on CRG Modified: Reduced Wait and Run IDD values Mode of Operation chapter Changed leakage current for ADC inputs down to +-1uA Minor modification of PLL frequency/ voltage gain values Corrected: Pin names/functions on 80 pin packages Interrupt vector table enable register inconsistencies PCB layout for 80QFP VREGEN position
V02.05	12 Sep 2002	12 Sep 2002		Corrected: Register address mismatches in 1.5.1
V02.06	06 Nov 2002	06 Nov 2002		Removed document order no. from Revision History pages Renamed "Preface" section to "Derivative Differences and Document references". Added details for derivatives missing CAN0/1/4, BDLC, IIC and/or Byteflight Added 2L40K mask set in section 1.6 Added OSC User Guide in Preface, “Document References” Added oscillator clock connection to BDM in S12_CORE in fig 3-1 Corrected several register and bit names in “Local Enable” column of Table 5.1 Interrupt Vector Locations Section HCS12 Core Block Description: mentioned alternate clock of BDM to be equivalent to oscillator clock Added new section: “Oscillator (OSC) Block Description” Corrected in footnote of Table "PLL Characteristics": fOSC = 4MHz

Modules	MC9S12DB128 SC515846[4] SC102202[6]	MC9S12DB128 SC515846[4] SC102202[6]
Package Code	PV/PVE	FU
Mask set	3L40K, 0L94R, 4L40K[4], 5L40K[6], 2L94R	3L40K, 0L94R, 4L40K[4], 5L40K[6], 2L94R
Temp Options	M, V, C/M, V	M, V, C
AEC qualified	Yes	Yes
Notes	An errata exists contact Sales Office	An errata exists contact Sales Office

NOTE:
1. ✓: Available for this device, ✕: Not available for this device.
2. 80 Pin bond-out for MC9S12DG128E, MC9S12DG128, MC9S12DJ128E, MC9S12DJ128, MC9S12A128, SC515847, SC515848, SC101161DG, SC101161DJ, SC102203, and SC102204 is the same; MC9S12DB128, SC515846, and SC102202 have a different bond-out.
3. Part numbers MC9S12DT128E, MC9S12DG128E, and MC9S12DJ128E are associated with the mask set 1L40K.
4. Part numbers SC515846, SC515847, SC515848, and SC515849 are associated with the mask set 4L40K.
5. Part numbers SC101161DT, SC101161DG, SC101161DJ are associated with the mask set 1L59W.
6. Part numbers SC102202, SC102203, SC102204, and SC102205 are associated with the mask set 5L40K which is not for volume production.

The following figure provides an ordering number example for the MC9S12D128 devices.

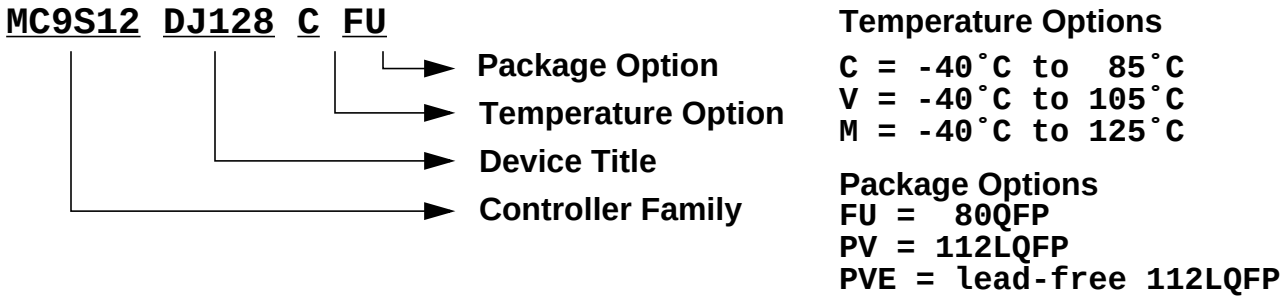


Figure 0-1 Order Partnumber Example

The following items should be considered when using a derivative.

- **Registers**
  - Do not write or read CAN0 registers (after reset: address range $0140 - $017F), if using a derivative without CAN0 (see **(Table 0-1)** and **(Table 0-2)**).
  - Do not write or read CAN1 registers (after reset: address range $0180 - $01BF), if using a derivative without CAN1 (see **(Table 0-1)** and **(Table 0-2)**).
  - Do not write or read CAN4 registers (after reset: address range $0280 - $02BF), if using a derivative without CAN4 (see **(Table 0-1)** and **(Table 0-2)**).
  - Do not write or read BDLC registers (after reset: address range $00E8 - $00EF), if using a derivative without BDLC (see **(Table 0-1)** and **(Table 0-2)**).
  - Do not write or read IIC registers (after reset: address range $00E0 - $00E7), if using a derivative without IIC (see **(Table 0-1)** and **(Table 0-2)**).

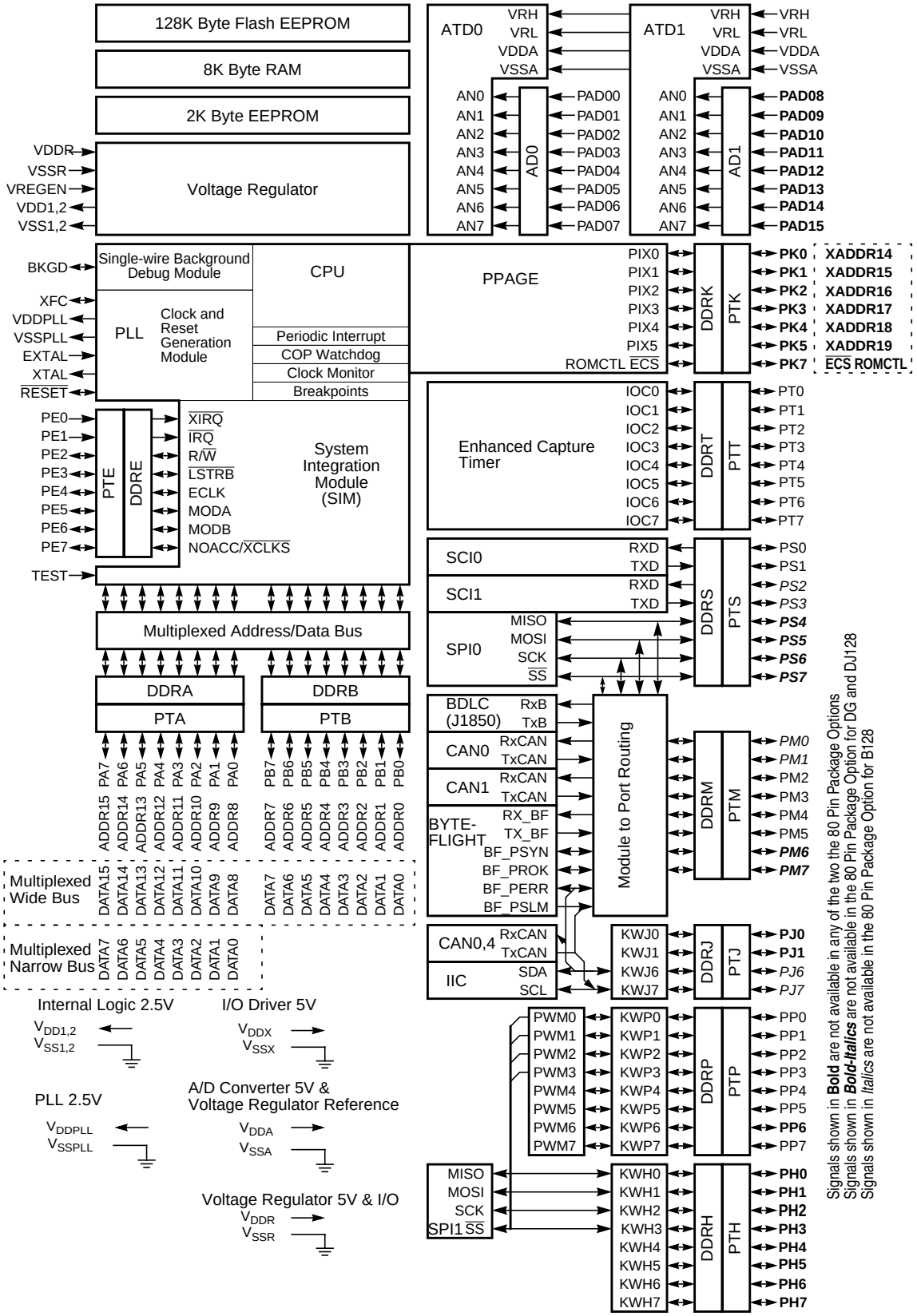
- Do not write or read Byteflight registers (after reset: address range $0300 - $035F), if using a derivative without Byteflight registers (see **(Table 0-1)** and **(Table 0-2)**).

- **Interrupts**
  - Fill the four CAN0 interrupt vectors ($FFB0 - $FFB7) according to your coding policies for unused interrupts, if using a derivative without CAN0 (see **(Table 0-1)** and **(Table 0-2)**).
  - Fill the four CAN1 interrupt vectors ($FFA8 - $FFAF) according to your coding policies for unused interrupts, if using a derivative without CAN1 (see **(Table 0-1)** and **(Table 0-2)**).
  - Fill the four CAN4 interrupt vectors ($FF90 - $FF97) according to your coding policies for unused interrupts, if using a derivative without CAN4 (see **(Table 0-1)** and **(Table 0-2)**).
  - Fill the BDLC interrupt vector ($FFC2, $FFC3) according to your coding policies for unused interrupts, if using a derivative without BDLC (see **(Table 0-1)** and **(Table 0-2)**).
  - Fill the IIC interrupt vector ($FFC0, $FFC1) according to your coding policies for unused interrupts, if using a derivative without IIC (see **(Table 0-1)** and **(Table 0-2)**).
  - Fill the four Byteflight interrupt vectors ($FFA0 - $FFA7) according to your coding policies for unused interrupts, if using a derivative without Byteflight (see **(Table 0-1)** and **(Table 0-2)**).

- **Ports**
  - The CAN0 pin functionality (TXCAN0, RXCAN0) is not available on port PJ7, PJ6, PM5, PM4, PM3, PM2, PM1 and PM0, if using a derivative without CAN0 (see **(Table 0-1)** and **(Table 0-2)**).
  - The CAN1 pin functionality (TXCAN1, RXCAN1) is not available on port PM3 and PM2, if using a derivative without CAN1 (see **(Table 0-1)** and **(Table 0-2)**).
  - The CAN4 pin functionality (TXCAN4, RXCAN4) is not available on port PJ7, PJ6, PM7, PM6, PM5 and PM4, if using a derivative without CAN4 (see **(Table 0-1)** and **(Table 0-2)**).
  - The BDLC pin functionality (TXB, RXB) is not available on port PM1 and PM0, if using a derivative without BDLC (see **(Table 0-1)** and **(Table 0-2)**).
  - The IIC pin functionality (SCL, SCA) is not available on port PJ7 and PJ6, if using a derivative without IIC (see **(Table 0-1)** and **(Table 0-2)**).
  - The Byteflight pin functionality (BF_PSLM, BF_PERR, BF_PROK, BF_PSYN, TX_BF, RX_BF) is not available on port PM7, PM6, PM5, PM4, PM3 and PM2, if using a derivative without Byteflight (see **(Table 0-1)** and **(Table 0-2)**).
  - Do not write MODRR1 and MODRR0 Bit of Module Routing Register (PIM_9DTB128 Block User Guide), if using a derivative without CAN0 (see **(Table 0-1)** and **(Table 0-2)**).
  - Do not write MODRR3 and MODRR2 Bit of Module Routing Register (PIM_9DTB128 Block User Guide), if using a derivative without CAN4 (see **(Table 0-1)** and **(Table 0-2)**).

- **Pins not available in 80 pin QFP package for MC9S12DG128E, MC9S12DG128, MC9S12DJ128E, MC9S12DJ128, MC9S12A128, SC515847, SC515848, SC101161DG, SC101161DJ, SC102203, and SC102204**

Figure 1-1 MC9S12DT128 Block Diagram



$00D0 - $00D7 SCI1 (Asynchronous Serial Interface)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00D5	SCI1SR2	Read:	0	0	0	0	0	BRK13	TXDIR	RAF
		Write:								
$00D6	SCI1DRH	Read:	R8	T8	0	0	0	0	0	0
		Write:								
$00D7	SCI1DRL	Read:	R7	R6	R5	R4	R3	R2	R1	R0
		Write:	T7	T6	T5	T4	T3	T2	T1	T0

$00D8 - $00DF SPI0 (Serial Peripheral Interface)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00D8	SPI0CR1	Read:	SPIE	SPE	SPTIE	MSTR	CPOL	CPHA	SSOE	LSBFE
		Write:								
$00D9	SPI0CR2	Read:	0	0	0	MODFEN	BIDIROE	0	SPISWAI	SPC0
		Write:								
$00DA	SPI0BR	Read:	0	SPPR2	SPPR1	SPPR0	0	SPR2	SPR1	SPR0
		Write:								
$00DB	SPI0SR	Read:	SPIF	0	SPTEF	MODF	0	0	0	0
		Write:								
$00DC	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$00DD	SPI0DR	Read:	Bit7	6	5	4	3	2	1	Bit0
		Write:								
$00DE	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$00DF	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$00E0 - $00E7 IIC (Inter IC Bus)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00E0	IBAD	Read:	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	0
		Write:								
$00E1	IBFD	Read:	IBC7	IBC6	IBC5	IBC4	IBC3	IBC2	IBC1	IBC0
		Write:								
$00E2	IBCR	Read:	IBEN	IBIE	MS/$\overline{SL}$	TX/$\overline{RX}$	TXAK	0	0	IBSWAI
		Write:						RSTA		
$00E3	IBSR	Read:	TCF	IAAS	IBB	IBAL	0	SRW	IBIF	RXAK
		Write:								
$00E4	IBDR	Read:	D7	D6	D5	D4	D3	D2	D1	D 0
		Write:								
$00E5	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$00E6	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$00E7	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

Table 1-2 Detailed MSCAN Foreground Receive and Transmit Buffer Layout

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$xxxC	CANRxDLR	Read:					DLC3	DLC2	DLC1	DLC0
		Write:								
$xxxD	Reserved	Read:								
		Write:								
$xxxE	CANxRTSRH	Read:	TSR15	TSR14	TSR13	TSR12	TSR11	TSR10	TSR9	TSR8
		Write:								
$xxxF	CANxRTSRL	Read:	TSR7	TSR6	TSR5	TSR4	TSR3	TSR2	TSR1	TSR0
		Write:								
$xx10	Extended ID CANxTIDR0	Read:	ID28	ID27	ID26	ID25	ID24	ID23	ID22	ID21
		Write:								
	Standard ID	Read:	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3
		Write:								
$xx11	Extended ID CANxTIDR1	Read:	ID20	ID19	ID18	SRR=1	IDE=1	ID17	ID16	ID15
		Write:								
	Standard ID	Read:	ID2	ID1	ID0	RTR	IDE=0			
		Write:								
$xx12	Extended ID CANxTIDR2	Read:	ID14	ID13	ID12	ID11	ID10	ID9	ID8	ID7
		Write:								
	Standard ID	Read:								
		Write:								
$xx13	Extended ID CANxTIDR3	Read:	ID6	ID5	ID4	ID3	ID2	ID1	ID0	RTR
		Write:								
	Standard ID	Read:								
		Write:								
$xx14- $xx1B	CANxTDSR0 - CANxTDSR7	Read:	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
		Write:								
$xx1C	CANxTDLR	Read:					DLC3	DLC2	DLC1	DLC0
		Write:								
$xx1D	CONxTTBPR	Read:	PRIO7	PRIO6	PRIO5	PRIO4	PRIO3	PRIO2	PRIO1	PRIO0
		Write:								
$xx1E	CANxTTSRH	Read:	TSR15	TSR14	TSR13	TSR12	TSR11	TSR10	TSR9	TSR8
		Write:								
$xx1F	CANxTTSRL	Read:	TSR7	TSR6	TSR5	TSR4	TSR3	TSR2	TSR1	TSR0
		Write:								

$0180 - $01BF CAN1 (Motorola Scalable CAN - MSCAN)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0180	CAN1CTL0	Read:	RXFRM	RXACT	CSWAI	SYNCH	TIME	WUPE	SLPRQ	INITRQ
		Write:								
$0181	CAN1CTL1	Read:	CANE	CLKSRC	LOOPB	LISTEN	0	WUPM	SLPAK	INITAK
		Write:								
$0182	CAN1BTR0	Read:	SJW1	SJW0	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0
		Write:								
$0183	CAN1BTR1	Read:	SAMP	TSEG22	TSEG21	TSEG20	TSEG13	TSEG12	TSEG11	TSEG10
		Write:								
$0184	CAN1RFLG	Read:	WUPIF	CSCIF	RSTAT1	RSTAT0	TSTAT1	TSTAT0	OVRIF	RXF
		Write:								

Pin Name Function 1	Pin Name Function 2	Pin Name Function 3	Pin Name Function 4	Pin Name Function 5	Powered by	Internal Pull Resistor		Description
						CTRL	Reset State	
PH6	**KWH6**	**---**	**—**	**—**	**VDDR**	**PERH/ PPSH**	**Disabled**	**Port H I/O, Interrupt**
PH5	**KWH5**	**---**	**—**	**—**	**VDDR**	**PERH/ PPSH**	**Disabled**	**Port H I/O, Interrupt**
PH4	**KWH4**	**---**	**—**	**—**	**VDDR**	**PERH/ PPSH**	**Disabled**	**Port H I/O, Interrupt**
PH3	**KWH3**	**$\overline{SS1}$**	**—**	**—**	**VDDR**	**PERH/ PPSH**	**Disabled**	**Port H I/O, Interrupt, $\overline{SS}$ of SPI1**
PH2	**KWH2**	**SCK1**	**—**	**—**	**VDDR**	**PERH/ PPSH**	**Disabled**	**Port H I/O, Interrupt, SCK of SPI1**
PH1	**KWH1**	**MOSI1**	**—**	**—**	**VDDR**	**PERH/ PPSH**	**Disabled**	**Port H I/O, Interrupt, MOSI of SPI1**
PH0	**KWH0**	**MISO1**	**—**	**—**	**VDDR**	**PERH/ PPSH**	**Disabled**	**Port H I/O, Interrupt, MISO of SPI1**
PJ7	*KWJ7*	*TXCAN4*	*SCL*	*TXCAN0*	*VDDX*	*PERJ/ PPSJ*	*Up*	*Port J I/O, Interrupt, TX of CAN4, SCL of IIC*
PJ6	*KWJ6*	*RXCAN4*	*SDA*	*RXCAN0*	*VDDX*	*PERJ/ PPSJ*	*Up*	*Port J I/O, Interrupt, RX of CAN4, SDA of IIC*
PJ[1:0]	**KWJ[1:0]**	**—**	**—**	**—**	**VDDX**	**PERJ/ PPSJ**	**Up**	**Port J I/O, Interrupts**
PK7	**$\overline{ECS}$**	**ROMCTL**	—	—	**VDDX**	**PUCR/ PUPKE**	**Up**	**Port K I/O, Emulation Chip Select, ROM Control**
PK[5:0]	**XADDR[19:14]**	—	—	—	**VDDX**	**PUCR/ PUPKE**	**Up**	**Port K I/O, Extended Addresses**
PM7	***BF_PSLM***	***TXCAN4***	**—**	**—**	***VDDX***	***PERM/ PPSM***	***Disabled***	***Port M I/O, BF slot mismatch pulse, TX of CAN4***
PM6	***BF_PERR***	***RXCAN4***	**—**	**—**	***VDDX***	***PERM/ PPSM***	***Disabled***	***Port M I/O, BF illegal pulse/message format error pulse, RX of CAN4***
PM5	BF_PROK	TXCAN0	TXCAN4	SCK0	VDDX	PERM/ PPSM	Disabled	Port M I/O, BF reception ok pulse, TX of CAN0, CAN4, SCK of SPI0
PM4	BF_PSYN	RXCAN0	RXCAN4	MOSI0	VDDX	PERM/ PPSM	Disabled	Port M I/O, BF sync pulse (Rx/Tx) OK pulse o/p, RX of CAN0, CAN4, MOSI of SPI0
PM3	TX_BF	TXCAN1	TXCAN0	$\overline{SS0}$	VDDX	PERM/ PPSM	Disabled	Port M I/O, TX of BF, CAN1, CAN0, $\overline{SS}$ of SPI0
PM2	RX_BF	RXCAN1	RXCAN0	MISO0	VDDX	PERM/ PPSM	Disabled	Port M I/O, RX of BF, CAN1, CAN0, MISO of SPI0

2.3 Detailed Signal Descriptions

2.3.1 EXTAL, XTAL — Oscillator Pins

EXTAL and XTAL are the crystal driver and external clock pins. On reset all the device clocks are derived from the EXTAL input frequency. XTAL is the crystal output.

2.3.2 $\overline{\text{RESET}}$ — External Reset Pin

An active low bidirectional control signal, it acts as an input to initialize the MCU to a known start-up state, and an output when an internal MCU function causes a reset.

2.3.3 TEST — Test Pin

This input only pin is reserved for test.

NOTE: *The TEST pin must be tied to VSS in all applications.*

2.3.4 XFC — PLL Loop Filter Pin

PLL loop filter. Please ask your Freescale representative for the interactive application note to compute PLL loop filter elements. Any current leakage on this pin must be avoided.

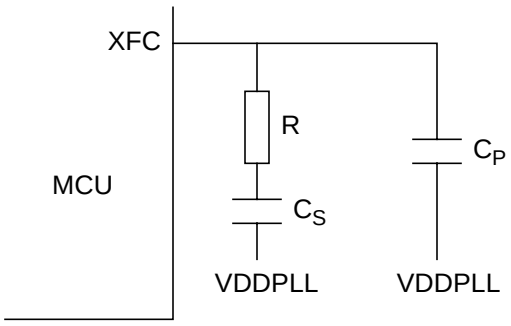


Figure 2-4 PLL Loop Filter Connections

2.3.5 BKGD / $\overline{\text{TAGHI}}$ / MODC — Background Debug, Tag High, and Mode Pin

The BKGD/$\overline{\text{TAGHI}}$/MODC pin is used as a pseudo-open-drain pin for the background debug communication. In MCU expanded modes of operation when instruction tagging is on, an input low on this pin during the falling edge of E-clock tags the high half of the instruction word being read into the instruction queue. It is used as a MCU operating mode select pin during reset. The state of this pin is latched to the MODC bit at the rising edge of $\overline{\text{RESET}}$. This pin has a permanently enabled pull-up device.

2.3.6 PAD[15] / AN1[7] / ETRIG1 — Port AD Input Pin [15]

PAD15 is a general purpose input pin and analog input of the analog to digital converter ATD1. It can act as an external trigger input for the ATD1.

2.3.7 PAD[14:8] / AN1[6:0] — Port AD Input Pins [14:8]

PAD14 - PAD8 are general purpose input pins and analog inputs of the analog to digital converter ATD1.

2.3.8 PAD[7] / AN0[7] / ETRIG0 — Port AD Input Pin [7]

PAD7 is a general purpose input pin and analog input of the analog to digital converter ATD0. It can act as an external trigger input for the ATD0.

2.3.9 PAD[6:0] / AN0[6:0] — Port AD Input Pins [6:0]

PAD6 - PAD8 are general purpose input pins and analog inputs of the analog to digital converter ATD0.

2.3.10 PA[7:0] / ADDR[15:8] / DATA[15:8] — Port A I/O Pins

PA7-PA0 are general purpose input or output pins. In MCU expanded modes of operation, these pins are used for the multiplexed external address and data bus.

2.3.11 PB[7:0] / ADDR[7:0] / DATA[7:0] — Port B I/O Pins

PB7-PB0 are general purpose input or output pins. In MCU expanded modes of operation, these pins are used for the multiplexed external address and data bus.

2.3.12 PE7 / NOACC / $\overline{\text{XCLKS}}$ — Port E I/O Pin 7

PE7 is a general purpose input or output pin. During MCU expanded modes of operation, the NOACC signal, when enabled, is used to indicate that the current bus cycle is an unused or “free” cycle. This signal will assert when the CPU is not using the bus.
The $\overline{\text{XCLKS}}$ is an input signal which controls whether a crystal in combination with the internal Colpitts (low power) oscillator is used or whether Pierce oscillator/external clock circuitry is used. The state of this pin is latched at the rising edge of $\overline{\text{RESET}}$. If the input is a logic low the EXTAL pin is configured for an external clock drive. If input is a logic high an oscillator circuit is configured on EXTAL and XTAL. Since this pin is an input with a pull-up device during reset, if the pin is left floating, the default configuration is an oscillator circuit on EXTAL and XTAL.

Table 4-3 Voltage Regulator VREGEN

VREGEN	Description
1	Internal Voltage Regulator enabled
0	Internal Voltage Regulator disabled, VDD1,2 and VDDPLL must be supplied externally with 2.5V

4.3 Security

The device will make available a security feature preventing the unauthorized read and write of the memory contents. This feature allows:

- Protection of the contents of FLASH,
- Protection of the contents of EEPROM,
- Operation in single-chip mode, No BDM possible
- Operation from external memory with internal FLASH and EEPROM disabled.

The user must be reminded that part of the security must lie with the user's code. An extreme example would be user's code that dumps the contents of the internal program. This code would defeat the purpose of security. At the same time the user may also wish to put a back door in the user's program. An example of this is the user downloads a key through the SCI which allows access to a programming routine that updates parameters stored in EEPROM.

4.3.1 Securing the Microcontroller

Once the user has programmed the FLASH and EEPROM (if desired), the part can be secured by programming the security bits located in the FLASH module. These non-volatile bits will keep the part secured through resetting the part and through powering down the part.

The security byte resides in a portion of the Flash array.

Check the Flash Block User Guide for more details on the security configuration.

4.3.2 Operation of the Secured Microcontroller

4.3.2.1 Normal Single Chip Mode

This will be the most common usage of the secured part. Everything will appear the same as if the part was not secured with the exception of BDM operation. The BDM operation will be blocked.

4.3.2.2 Executing from External Memory

The user may wish to execute from external space with a secured microcontroller. This is accomplished by resetting directly into expanded mode. The internal FLASH and EEPROM will be disabled. BDM operations will be blocked.

NOTE: *For devices assembled in 80-pin QFP packages all non-bonded out pins should be configured as outputs after reset in order to avoid current drawn from floating inputs. Refer to* ***Table 2-1*** *for affected pins.*

5.3.2 Memory

Refer to **Table 1-1** for locations of the memories depending on the operating mode after reset.

The RAM array is not automatically initialized out of reset.

Figure 23-3 Recommended PCB Layout for 112LQFP Pierce Oscillator

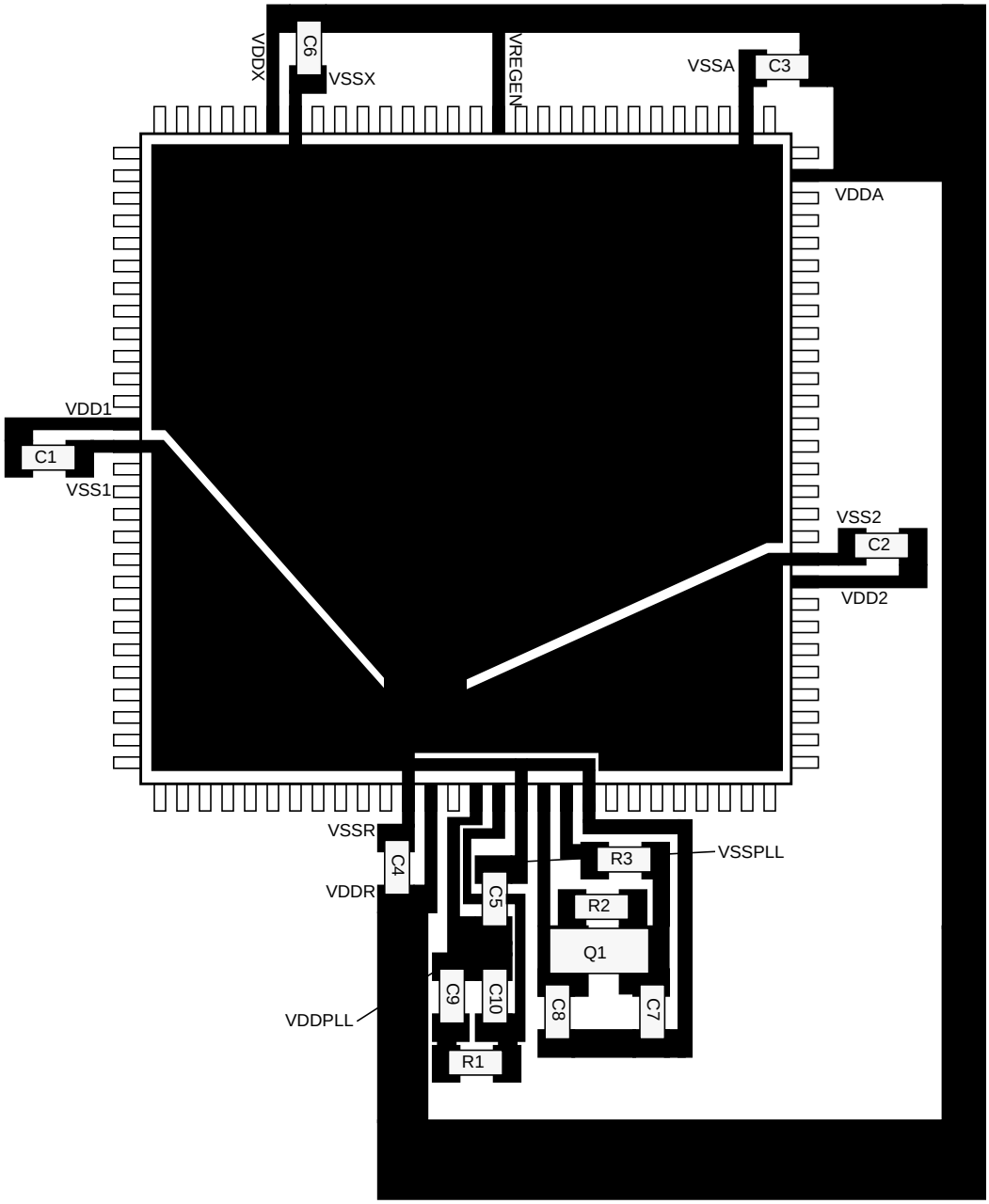
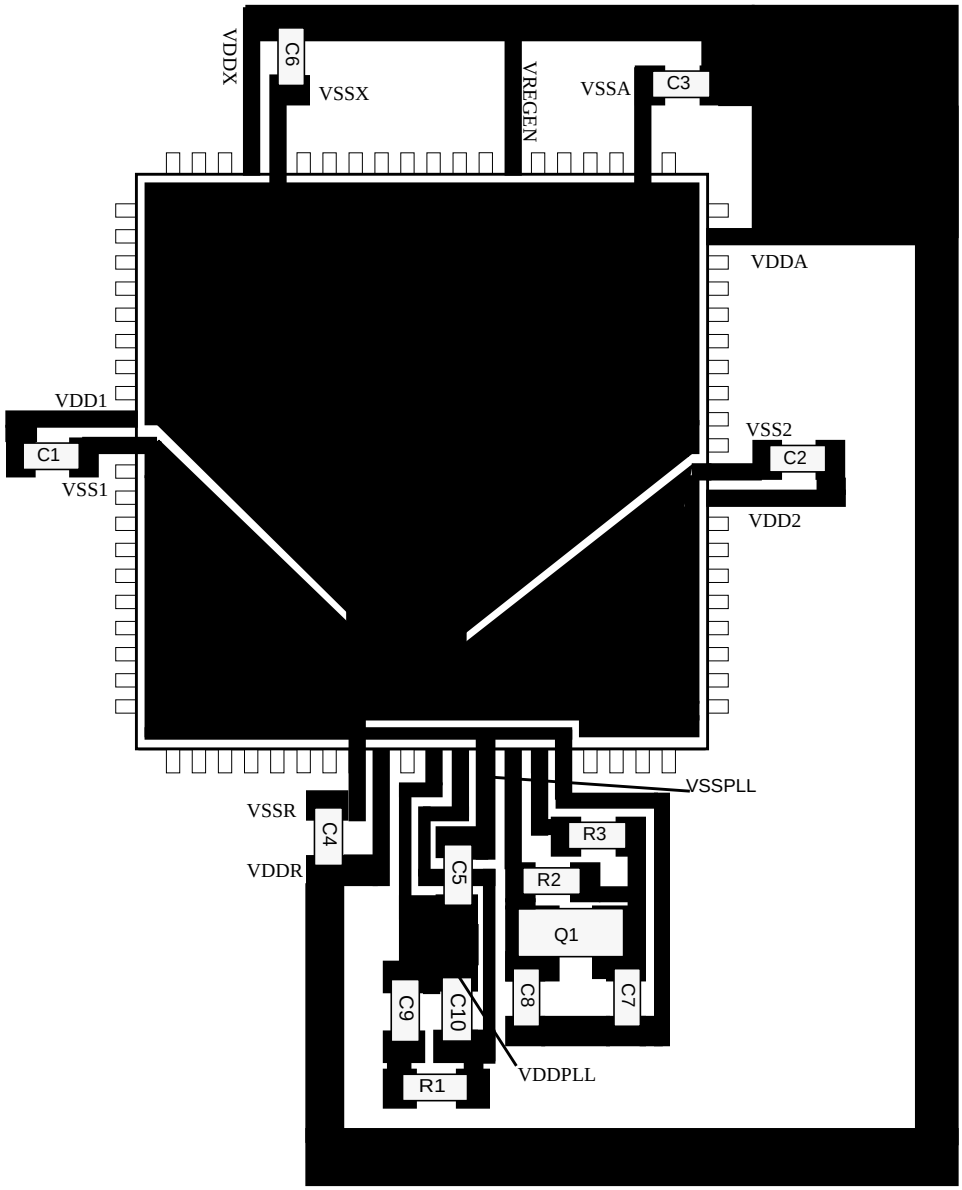


Figure 23-4 Recommended PCB Layout for 80QFP (MC9S12DG128E, MC9S12DG128, MC9S12DJ128E, MC9S12DJ128, MC9S12A128, SC515847, SC515848, SC101161DG, SC101161DJ, SC102203, and SC102204) Pierce Oscillator



A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table A-2 ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series Resistance	R1	1500	Ohm
	Storage Capacitance	C	100	pF
	Number of Pulse per pin positive negative	–	– 3 3	
Machine	Series Resistance	R1	0	Ohm
	Storage Capacitance	C	200	pF
	Number of Pulse per pin positive negative	–	– 3 3	
Latch-up	Minimum input voltage limit		–2.5	V
	Maximum input voltage limit		7.5	V

Table A-3 ESD and Latch-Up Protection Characteristics

Num	C	Rating	Symbol	Min	Max	Unit
1	C	Human Body Model (HBM)	V_{HBM}	2000	–	V
2	C	Machine Model (MM)	V_{MM}	200	–	V
3	C	Charge Device Model (CDM)	V_{CDM}	500	–	V
4	C	Latch-up Current at 125°C positive negative	I_{LAT}	+100 –100	–	mA
5	C	Latch-up Current at 27°C positive negative	I_{LAT}	+200 –200	–	mA

A.1.7 Operating Conditions

This chapter describes the operating conditions of the device. Unless otherwise noted those conditions apply to all the following data.

NOTE: *Please refer to the temperature rating of the device (C, V, M) with regards to the ambient temperature T_A and the junction temperature T_J. For power dissipation*

Table A-6 5V I/O Characteristics

Conditions are shown in **(Table A-4)** unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Input High Voltage	V_{IH}	$0.65*V_{DD5}$	–		V
	T	Input High Voltage	V_{IH}	–	–	V_{DD5} + 0.3	
2	P	Input Low Voltage	V_{IL}	–	–	$0.35*V_{DD5}$	V
	T	Input Low Voltage	V_{IL}	V_{SS5} – 0.3	–	–	V
3	C	Input Hysteresis	V_{HYS}		250		mV
4	P	Input Leakage Current (pins in high ohmic input mode) $V_{in} = V_{DD5}$ or V_{SS5}	I_{in}	-1.0	–	1.0	µA
5	C P	Output High Voltage (pins in output mode) Partial Drive I_{OH} = –2.0mA Full Drive I_{OH} = –10.0mA	V_{OH}	V_{DD5} – 0.8	–	–	V
6	C P	Output Low Voltage (pins in output mode) Partial Drive I_{OL} = +2.0mA Full Drive I_{OL} = +10.0mA	V_{OL}	–	–	0.8	V
7	P	Internal Pull Up Device Current, tested at V_{IL} Max.	I_{PUL}	–	–	–130	µA
8	C	Internal Pull Up Device Current, tested at V_{IH} Min.	I_{PUH}	–10	–	–	µA
9	P	Internal Pull Down Device Current, tested at V_{IH} Min.	I_{PDH}	–	–	130	µA
10	C	Internal Pull Down Device Current, tested at V_{IL} Max.	I_{PDL}	10	–	–	µA
11	D	Input Capacitance	C_{in}		6	–	pF
12	T	Injection current[1] Single Pin limit Total Device Limit. Sum of all injected currents	I_{ICS} I_{ICP}	 –2.5 –25	–	 2.5 25	mA
13	P	Port H, J, P Interrupt Input Pulse filtered [2]	t_{PULSE}			3	µs
14	P	Port H, J, P Interrupt Input Pulse passed [2]	t_{PULSE}	10			µs

NOTES:
1. Refer to **Section A.1.4 Current Injection**, for more details
2. Parameter only applies in STOP or Pseudo STOP mode.

A.1.10 Supply Currents

This section describes the current consumption characteristics of the device as well as the conditions for the measurements.

Table A-12 NVM Reliability Characteristics[1]

Conditions are shown in **(Table A-4)** unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Flash Reliability Characteristics							
1	C	Data retention after 10,000 program/erase cycles at an average junction temperature of $T_{Javg} \leq 85°C$	t_{FLRET}	15	100[2]	—	Years
2	C	Data retention with <100 program/erase cycles at an average junction temperature $T_{Javg} \leq 85°C$		20	100[2]	—	
3	C	Number of program/erase cycles ($-40°C \leq T_J \leq 0°C$)	n_{FL}	10,000	—	—	Cycles
4	C	Number of program/erase cycles ($0°C \leq T_J \leq 140°C$)		10,000	100,000[3]	—	
EEPROM Reliability Characteristics							
5	C	Data retention after up to 100,000 program/erase cycles at an average junction temperature of $T_{Javg} \leq 85°C$	t_{EEPRET}	15	100[2]	—	Years
6	C	Data retention with <100 program/erase cycles at an average junction temperature $T_{Javg} \leq 85°C$		20	100[2]	—	
7	C	Number of program/erase cycles ($-40°C \leq T_J \leq 0°C$)	n_{EEP}	10,000	—	—	Cycles
8	C	Number of program/erase cycles ($0°C < T_J \leq 140°C$)		100,000	300,000[3]	—	

NOTES:

1. T_{Javg} will not exeed 85°C considering a typical temperature profile over the lifetime of a consumer, industrial or automotive application.
2. Typical data retention values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale defines Typical Data Retention, please refer to Engineering Bulletin EB618.
3. Spec table quotes typical endurance evaluated at 25°C for this product family, typical endurance at various temperature can be estimated using the graph below. For additional information on how Freescale defines Typical Endurance, please refer to Engineering Bulletin EB619.

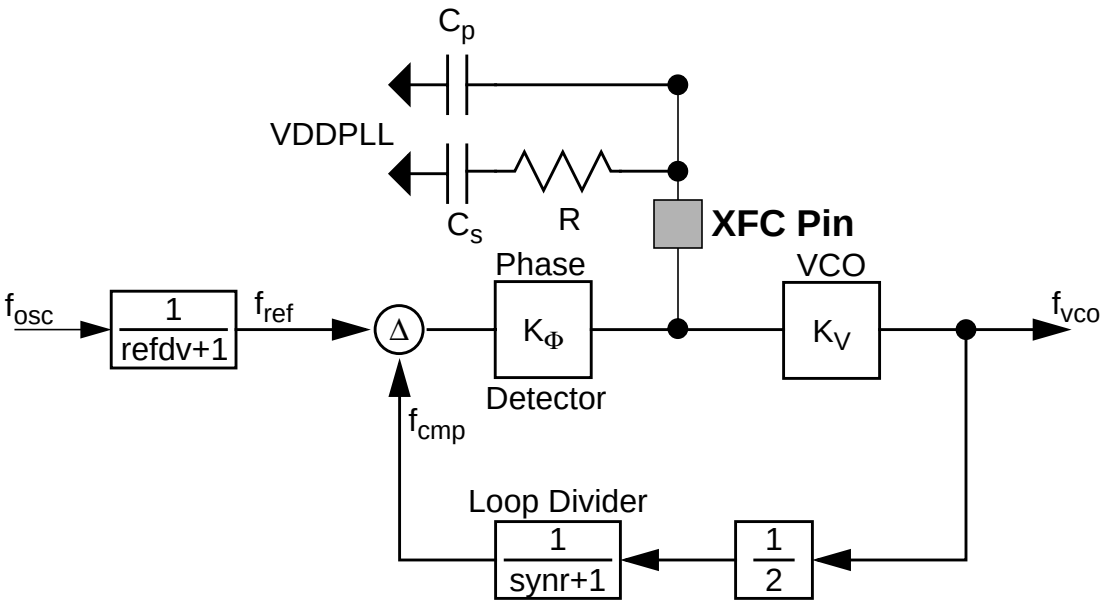


Figure A-3 Basic PLL functional diagram

The following procedure can be used to calculate the resistance and capacitance values using typical values for K_1, f_1 and i_{ch} from **(Table A-16)**.

The grey boxes show the calculation for f_{VCO} = 50MHz and f_{ref} = 1MHz. E.g., these frequencies are used for f_{OSC} = 4MHz and a 25MHz bus clock.

The VCO Gain at the desired VCO frequency is approximated by:

$$K_V = K_1 \cdot e^{\frac{(f_1 - f_{vco})}{K_1 \cdot 1V}} = -100 \cdot e^{\frac{(60-50)}{-100}} = -90.48\text{MHz/V}$$

The phase detector relationship is given by:

$$K_\Phi = -|i_{ch}| \cdot K_V \qquad = 316.7\text{Hz}/\Omega$$

i_{ch} is the current in tracking mode.

The loop bandwidth f_C should be chosen to fulfill the Gardner's stability criteria by <u>at least</u> a factor of 10, typical values are 50. $\zeta = 0.9$ ensures a good transient response.

$$f_C < \frac{2 \cdot \zeta \cdot f_{ref}}{\pi \cdot \left(\zeta + \sqrt{1 + \zeta^2}\right)} \cdot \frac{1}{10} \rightarrow f_C < \frac{f_{ref}}{4 \cdot 10}; (\zeta = 0.9)$$

$$f_C < 25\text{kHz}$$

A.7.2 Slave Mode

Figure A-8 and **Figure A-9** illustrate the slave mode timing. Timing values are shown in **(Table A-19)**.

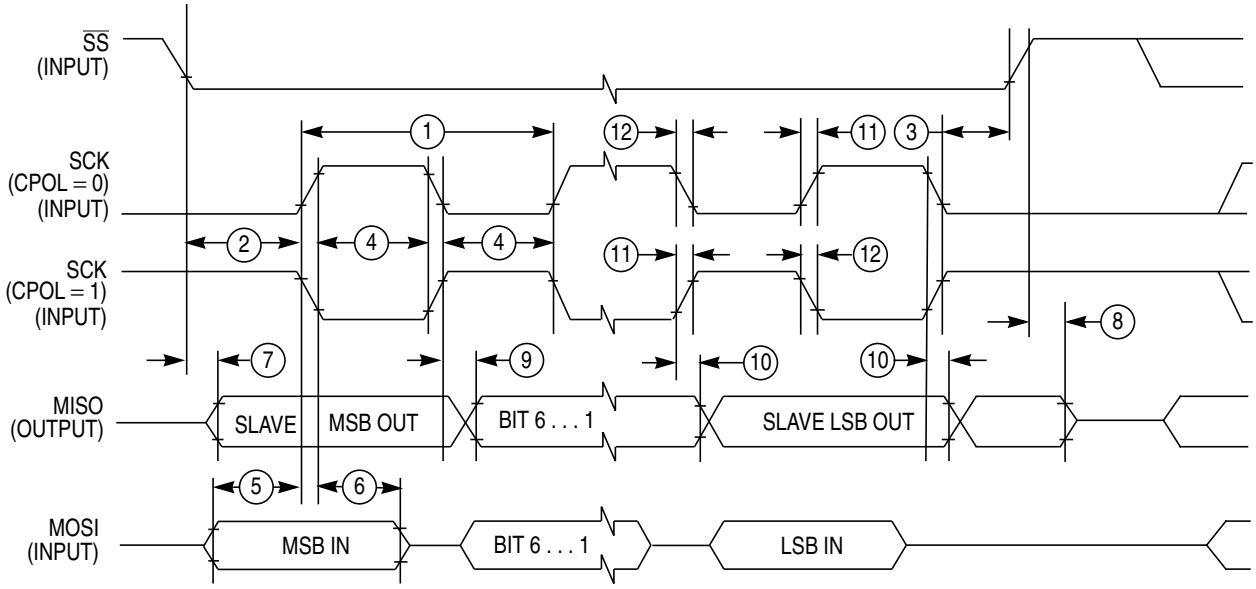


Figure A-8 SPI Slave Timing (CPHA = 0)

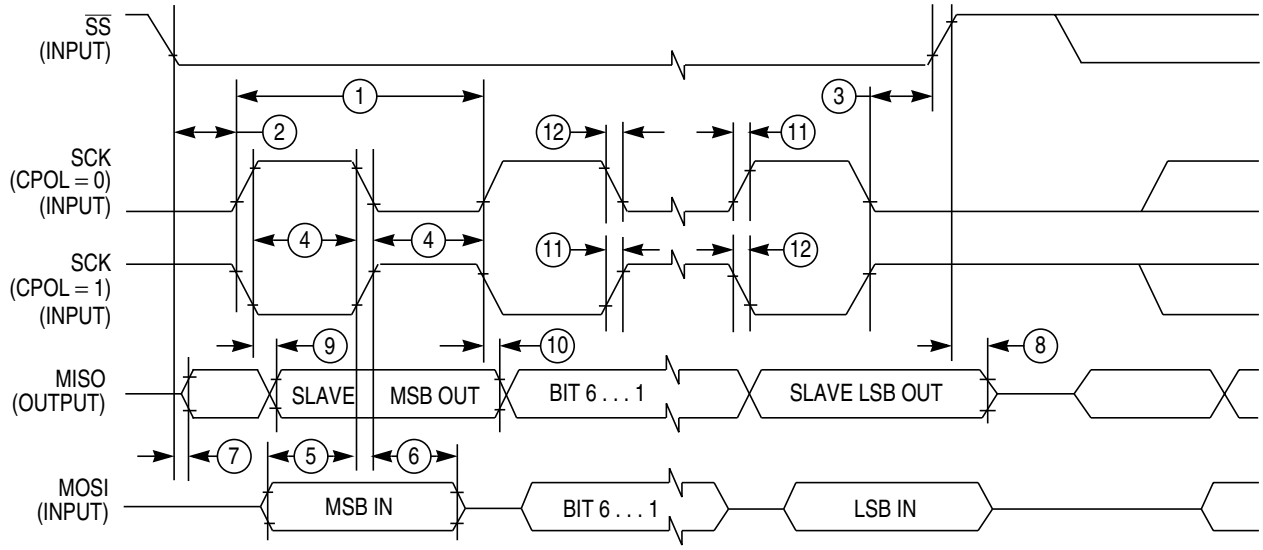


Figure A-9 SPI Slave Timing (CPHA =1)