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Applications of "<u>Embedded - Microcontrollers</u>"

Details	
Product Status	Active
Core Processor	HCS12
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, I ² C, SCI, SPI
Peripherals	PWM, WDT
Number of I/O	91
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 5.25V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s12dg128vpve

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

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Derivative Differences and Document References

Derivative Differences

(Table 0-1) and **(Table 0-2)** show the availability of peripheral modules on the various derivatives. For details about the compatibility within the MC9S12D-Family refer also to engineering bulletin EB386.

Table 0-1 Derivative Differences¹

Modules	MC9S12DT128E ³ MC9S12DT128 SC515849 ⁴ SC101161DT ⁵ SC102205 ⁶	MC9S12DG128E ³ MC9S12DG128 SC515847 ⁴ SC101161DG ⁵ SC102203 ⁶	MC9S12DJ128E ³ MC9S12DJ128 SC515848 ⁴ SC101161DJ ⁵ SC102204 ⁶	MC9S12A128
# of CANs	3	2	2	0
CAN4	✓	✓	✓	X
CAN1	✓	X	X	X
CAN0	✓	✓	✓	X
J1850/BDLC	×	X	✓	X
IIC	✓	✓	✓	✓
Byteflight	X	X	X	X
Package	112 LQFP	112 LQFP/80 QFP ²	112 LQFP/80 QFP ²	112 LQFP/80 QFP ²
Package Code	PV	PV/FU	PV/FU	PV/FU
Mask set	1L40K ³ , 3L40K, 0L94R, 4L40K ⁴ , 1L59W ⁵ , 5L40K ⁶ , 2L94R	1L40K ³ , 3L40K, 0L94R, 4L40K ⁴ , 1L59W ⁵ , 5L40K ⁶ , 2L94R	1L40K ³ , 3L40K, 0L94R, 4L40K ⁴ , 1L59W ⁵ , 5L40K ⁶ , 2L94R	3L40K, 0L94R, 2L94R, 1L59W
Temp Options	M, V, C	M, V, C	M, V, C	С
AEC qualified	Yes	Yes	Yes	No
Notes	An errata exists contact Sales Office	An errata exists contact Sales Office	An errata exists contact Sales Office	An errata exists contact Sales Office

Table 0-2 Derivative Differences for MC9S12DB128¹

Modules	MC9S12DB128 SC515846 ⁴ SC102202 ⁶	MC9S12DB128 SC515846 ⁴ SC102202 ⁶
# of CANs	2	0
CAN4	✓	X
CAN1	X	X
CAN0	✓	X
J1850/BDLC	X	X
IIC	X	X
Byteflight	✓	✓
Package	112 LQFP	80 QFP ²

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- Digital filtering
- Programmable rising or falling edge trigger
- Memory
 - 128K Flash EEPROM
 - 2K byte EEPROM
 - 8K byte RAM
- Two 8-channel Analog-to-Digital Converters
 - 10-bit resolution
 - External conversion trigger capability
- Three 1M bit per second, CAN 2.0 A, B software compatible modules
 - Five receive and three transmit buffers
 - Flexible identifier filter programmable as 2 x 32 bit, 4 x 16 bit or 8 x 8 bit
 - Four separate interrupt channels for Rx, Tx, error and wake-up
 - Low-pass filter wake-up function
 - Loop-back for self test operation
- Enhanced Capture Timer
 - 16-bit main counter with 7-bit prescaler
 - 8 programmable input capture or output compare channels
 - Four 8-bit or two 16-bit pulse accumulators
- 8 PWM channels
 - Programmable period and duty cycle
 - 8-bit 8-channel or 16-bit 4-channel
 - Separate control for each pulse width and duty cycle
 - Center-aligned or left-aligned outputs
 - Programmable clock select logic with a wide range of frequencies
 - Fast emergency shutdown input
 - Usable as interrupt inputs
- Serial interfaces
 - Two asynchronous Serial Communications Interfaces (SCI)
 - Two Synchronous Serial Peripheral Interface (SPI)
 - Byteflight
- Byte Data Link Controller (BDLC)

\$0040 - \$007F

ECT (Enhanced Capture Timer 16 Bit 8 Channels)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
¢007C	TC2L (bi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
\$007C	TC2H (hi)	Write:								
\$007D	TC2H (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
φοστ	10211 (10)	Write:								
\$007E	TC3H (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
ψ007L	10311 (111)	Write:								
\$007F	TC3H (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								

\$0080 - \$009F

ATD0 (Analog to Digital Converter 10 Bit 8 Channel)

S0080	Address	Name	ı	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
S0080			Read.								0
\$0081 ATDOCTL1 Read: Write: ADPU AFFC AWAI ETRIGLE ETRIGP ETRIG ASCIE \$0082 ATDOCTL2 Write: ADPU AFFC AWAI ETRIGLE ETRIGP ETRIG ASCIE \$0083 ATDOCTL3 Read: Write: SRESS SMP1 SMP0 PRS4 PRS3 PRS2 PRS1 FROM SMR SCAN MULT \$0084 ATDOCTL5 Read: Write: SRESS SMP1 SMP0 PRS4 PRS3 PRS2 PRS1 FROM SMR SCAN MULT \$0085 ATDOCTL5 Write: SCF OFFOR SCAN MULT \$0086 ATDOSTATO Write: SCF OFFOR SCAN MULT \$0087 Reserved Read: Write: SMR SMR SCAN MULT \$0088 ATDOTESTO Read: Write: SMR SMR SCAN MULT \$0089 ATDOTEST1 Read: Write: SMR SMR SCAN MULT \$0080 ARSERVED READ: Write: SMR SCAN MULT \$0080 ATDOSTAT1 WRITE: SMR SCAN MULT \$0080 ATDOSTAT1 Read: Write: SMR SCAN MULT \$0080 ATDOSTAT1 WRITE: SMR SCAN MULT \$	\$0080	ATD0CTL0		0		0	U	0	U		U
\$0082 ATDOCTL2 Write: \$0083 ATDOCTL3 Read: Write: \$0084 ATDOCTL4 Read: Write: \$0085 ATDOCTL5 Write: \$0086 ATDOCTL5 Write: \$0086 ATDOCTL5 Write: \$0087 Reserved Read: Write: \$0088 ATDOTEST0 Write: \$0088 ATDOTEST1 Read: Write: \$0089 ATDOTEST1 Read: Write: \$0080 ATDOSTAT1 Read: Write: \$0080 Reserved Read: Write: \$0080 ATDODIEN Read: Write: \$0080 ATDODIEN Read: Write: \$0080 ATDODIEN Read: Write: \$0080 ATDOSTAT1 Read: Write: \$0080 Reserved Read: Write: \$0080 ATDOSTAT1 Read: Write: \$0080 ATDOSTAT1 Read: Write: \$0080 Reserved Read: Write: \$0080 ATDOSTAT1 Read: Write: \$0080 ATDOSTAT1 Read: Write: \$0080 Reserved Read: Write: \$0080 ATDOSTAT1 Read	¢0001	ATDOCTI 1		0	0	0	0	0	0	0	0
\$0082 ATDOCTL2 Write: \$0083 ATDOCTL3 Read: \$0084 ATDOCTL4 Write: \$0085 ATDOCTL5 Write: \$0086 ATDOSTATO Write: \$0088 ATDOTESTO Write: \$008	\$000 I	AIDUCILI	Write:								
\$0084 ATD0CTL4 Read: Write: Read: Write: Read: Write: SCF Write: S	\$0082	ATD0CTL2		ADPU	AFFC	AWAI	ETRIGLE	ETRIGP	ETRIG	ASCIE	ASCIF
\$0084 ATDOCTL4 Write: \$0085 ATDOCTL5 Read: Write: \$0086 ATDOSTATO Read: Write: \$0087 Reserved Read: Write: \$0088 ATDOTESTO Read: Write: \$0089 ATDOTEST1 Read: Write: \$0080 ATDOSTAT1 Read: Write: \$0080 Reserved Read: O O O O O O O O O O O O O O O O O O O	\$0083	ATD0CTL3		0	S8C	S4C	S2C	S1C	FIFO	FRZ1	FRZ0
\$0086 ATD0STAT0 Read: Write: SCF Write: SCF Write: SCF Write: SCF Write: S0087 Reserved Write: S0088 ATD0TEST0 Read: 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	\$0084	ATD0CTL4		SRES8	SMP1	SMP0	PRS4	PRS3	PRS2	PRS1	PRS0
\$0086 AlDOSIAIO Write: SCF EIORF FIFOR	\$0085	ATD0CTL5		DJM	DSGN	SCAN	MULT	0	СС	СВ	CA
\$0087 Reserved Write: \$0088 ATD0TEST0 Read: \$0089 ATD0TEST1 Read: \$0080 Reserved Write: \$0080 ATD0TEST1 Read: \$0080 Reserved Write: \$0080 Reserved Write: \$0080 ATD0STAT1 Read: \$0080 ATD0STAT1 Read: \$0080 ATD0STAT1 Read: \$0080 Reserved Read: \$0000 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	\$0086	ATD0STAT0		SCF	0	ETORF	FIFOR	0	CC2	CC1	CC0
\$0088 ATDOTESTO Read: 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	\$0087	Reserved	,	0	0	0	0	0	0	0	0
\$0089 ATDOTEST1 Read: 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	\$0088	ATD0TEST0	Read:	0	0	0	0	0	0	0	0
\$008A Reserved	\$0089	ATD0TEST1	Read:	0	0	0	0	0	0	0	SC
\$008B ATD0STAT1 Read: CCF7 CCF6 CCF5 CCF4 CCF3 CCF2 CCF1 CCF1 CCF3 CCF2 CCF1 CCF1 CCF3 CCF2 CCF1 CCF1 CCF3 CCF2 CCF1 CCF1 CCF1 CCF1 CCF1 CCF1 CCF1	\$008A	Reserved	Read:	0	0	0	0	0	0	0	0
\$008C Reserved Read: 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	\$008B	ATD0STAT1	Read:	CCF7	CCF6	CCF5	CCF4	CCF3	CCF2	CCF1	CCF0
\$008D ATD0DIEN Read: Write: Read: 0 0 0 0 0 0 0 0	\$008C	Reserved	Read:	0	0	0	0	0	0	0	0
\$008E Reserved Read: 0 0 0 0 0 0 0	\$008D	ATD0DIEN	Read:	Bit 7	6	5	4	3	2	1	Bit 0
Write:	\$008E	Reserved		0	0	0	0	0	0	0	0
	\$008F	PORTAD0	Read:	Bit7	6	5	4	3	2	1	BIT 0
	\$0090	ATD0DR0H	Read:	Bit15	14	13	12	11	10	9	Bit8
\$0091 ATD0DR0L Read: Bit7 Bit6 0 0 0 0 0 0 Write:	\$0091	ATD0DR0L	Read:	Bit7	Bit6	0	0	0	0	0	0

Section 2 Signal Description

This section describes signals that connect off-chip. It includes a pinout diagram, a table of signal properties, and detailed discussion of signals. It is built from the signal description sections of the Block User Guides of the individual IP blocks on the device.

2.1 Device Pinout

The MC9S12DT128 and its derivatives are available in a 112-pin low profile quad flat pack (LQFP) and in a 80-pin quad flat pack (QFP). Most pins perform two or more functions, as described in the Signal Descriptions. **Figure 2-1**, **Figure 2-2**, and **Figure 2-3** show the pin assignments for different packages.

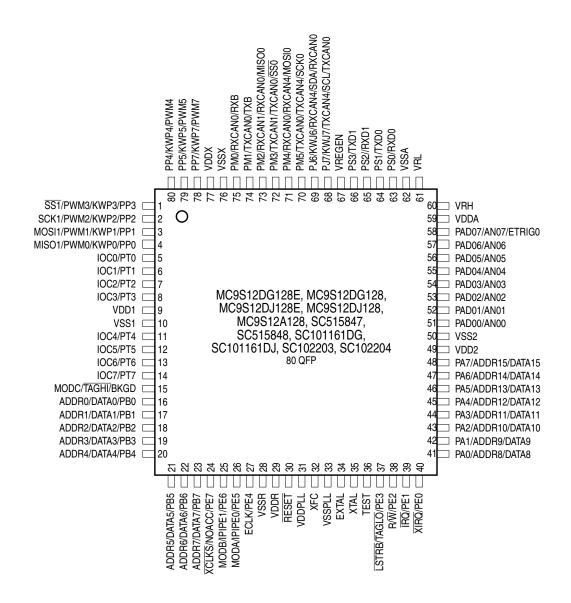


Figure 2-2 Pin Assignments in 80 QFP for MC9S12DG128E, MC9S12DG128, MC9S12DJ128E, MC9S12DJ128, MC9S12A128, SC515847, SC515848, SC101161DG, SC101161DJ, SC102203, and SC102204 Bondout

Device User Guide — 9S12DT128DGV2/D V02.17

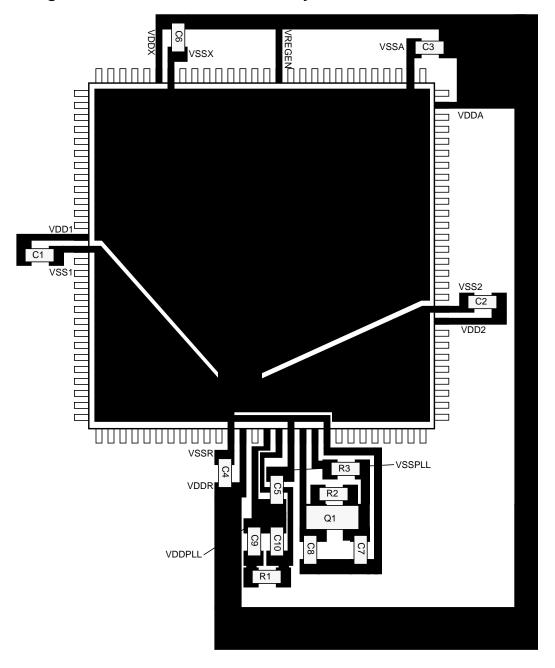


Figure 23-3 Recommended PCB Layout for 112LQFP Pierce Oscillator

Figure 23-4 Recommended PCB Layout for 80QFP (MC9S12DG128E, MC9S12DG128, MC9S12DJ128E, MC9S12DJ128, MC9S12A128, SC515847, SC515848, SC101161DG, SC101161DJ, SC102203, and SC102204) Pierce Oscillator

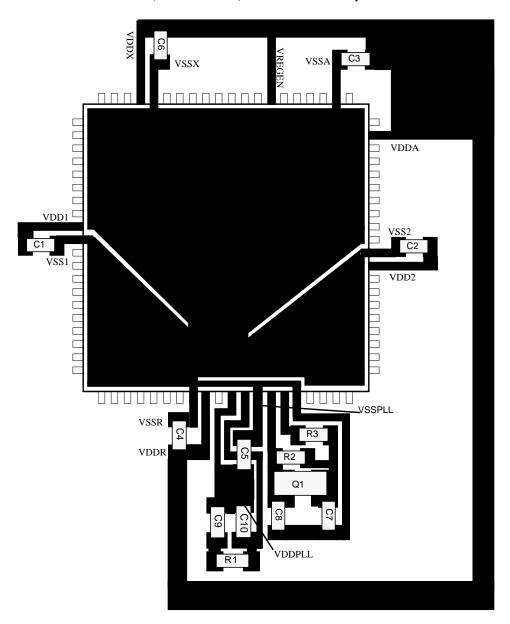
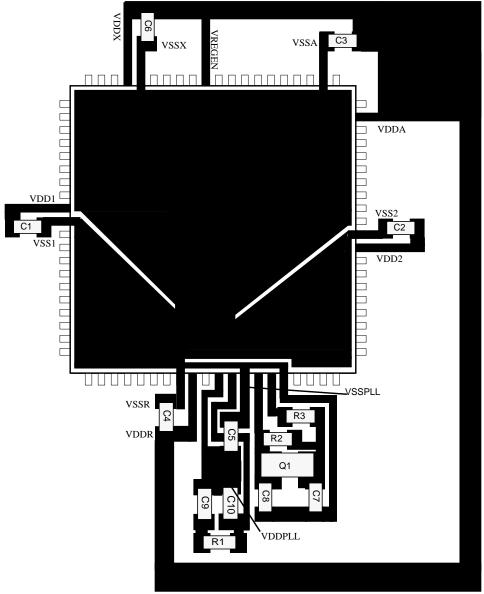


Figure 23-5 Recommended PCB Layout for 80QFP (MC9S12DB128, SC515846, and SC102202) Pierce Oscillator



Appendix A Electrical Characteristics

A.1 General

This introduction is intended to give an overview on several common topics like power supply, current injection etc.

A.1.1 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate.

P:

Those parameters are guaranteed during production testing on each individual device.

C:

Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations. They are regularly verified by production monitors.

T:

Those parameters are achieved by design characterization on a small sample size from typical devices. All values shown in the typical column are within this category.

D:

Those parameters are derived mainly from simulations.

A.1.2 Power Supply

The MC9S12DT128 utilizes several pins to supply power to the I/O ports, A/D converter, oscillator, PLL and internal logic.

The VDDA, VSSA pair supplies the A/D converter and the resistor ladder of the internal voltage regulator.

The VDDX, VSSX, VDDR and VSSR pairs supply the I/O pins, VDDR supplies also the internal voltage regulator.

VDD1, VSS1, VDD2 and VSS2 are the supply pins for the digital logic, VDDPLL, VSSPLL supply the oscillator and the PLL.

VSS1 and VSS2 are internally connected by metal.

VDDA, VDDX, VDDR as well as VSSA, VSSX, VSSR are connected by anti-parallel diodes for ESD protection.

Table A-6 5V I/O Characteristics

Num	С	Rating	Symbol	Min	Тур	Max	Unit
1	Р	Input High Voltage	V _{IH}	0.65*V _{DD5}	-		V
	Т	Input High Voltage	V _{IH}	-	-	V _{DD5} + 0.3	
2	Р	Input Low Voltage	V _{IL}	-	-	0.35*V _{DD5}	V
	Т	Input Low Voltage	V _{IL}	V _{SS5} - 0.3	-	_	V
3	С	Input Hysteresis	V _{HYS}		250		mV
4	Р	Input Leakage Current (pins in high ohmic input mode) $V_{in} = V_{DD5}$ or V_{SS5}	I _{in}	-1.0	-	1.0	μΑ
5	C P	Output High Voltage (pins in output mode) Partial Drive $I_{OH} = -2.0mA$ Full Drive $I_{OH} = -10.0mA$	V _{OH}	V _{DD5} – 0.8	-	-	V
6	C P	Output Low Voltage (pins in output mode) Partial Drive I _{OL} = +2.0mA Full Drive I _{OL} = +10.0mA	V _{OL}	-	-	0.8	V
7	Р	Internal Pull Up Device Current, tested at V _{IL} Max.	I _{PUL}	-	_	-130	μА
8	С	Internal Pull Up Device Current, tested at V _{IH} Min.	I _{PUH}	-10	_	_	μА
9	Р	Internal Pull Down Device Current, tested at V _{IH} Min.	I _{PDH}	-	_	130	μΑ
10	С	Internal Pull Down Device Current, tested at V _{IL} Max.	I _{PDL}	10	-	_	μА
11	D	Input Capacitance	C _{in}		6	_	pF
12	Т	Injection current ¹ Single Pin limit Total Device Limit. Sum of all injected currents	I _{ICS}	-2.5 -25	-	2.5 25	mA
13	Р	Port H, J, P Interrupt Input Pulse filtered ²	t _{PULSE}			3	μs
14	Р	Port H, J, P Interrupt Input Pulse passed ²	t _{PULSE}	10			μs

NOTES:

- 1. Refer to Section A.1.4 Current Injection, for more details
- 2. Parameter only applies in STOP or Pseudo STOP mode.

A.1.10 Supply Currents

This section describes the current consumption characteristics of the device as well as the conditions for the measurements.

A.2.3 ATD accuracy

(Table A-10) specifies the ATD conversion performance excluding any errors due to current injection, input capacitance and source resistance.

Table A-10 ATD Conversion Performance

Conditions are shown in (Table A-4) unless otherwise noted

 $V_{REF} = V_{RH} - V_{RL} = 5.12V$. Resulting to one 8 bit count = 20mV and one 10 bit count = 5mV

 $f_{ATDCIK} = 2.0MHz$

Num	С	Rating	Symbol	Min	Тур	Max	Unit
1	Р	10-Bit Resolution	LSB		5		mV
2	Р	10-Bit Differential Nonlinearity	DNL	-1		1	Counts
3	Р	10-Bit Integral Nonlinearity	INL	-2.5	±1.5	2.5	Counts
4	Р	10-Bit Absolute Error ¹	AE	-3	±2.0	3	Counts
5	Р	8-Bit Resolution	LSB		20		mV
6	Р	8-Bit Differential Nonlinearity	DNL	-0.5		0.5	Counts
7	Р	8-Bit Integral Nonlinearity	INL	-1.0	±0.5	1.0	Counts
8	Р	8-Bit Absolute Error ⁽¹⁾	AE	-1.5	±1.0	1.5	Counts

NOTES:

For the following definitions see also **Figure A-1**.

Differential Non-Linearity (DNL) is defined as the difference between two adjacent switching steps.

$$DNL(i) = \frac{V_i - V_{i-1}}{1LSB} - 1$$

The Integral Non-Linearity (INL) is defined as the sum of all DNLs:

$$INL(n) = \sum_{i=1}^{n} DNL(i) = \frac{V_n - V_0}{1LSB} - n$$

^{1.} These values include the quantization error which is inherently 1/2 count for any A/D converter.

A.3.2 NVM Reliability

The reliability of the NVM blocks is guaranteed by stress test during qualification, constant process monitors and burn-in to screen early life failures.

The failure rates for data retention and program/erase cycling are specified at the operating conditions noted.

The program/erase cycle count on the sector is incremented every time a sector or mass erase event is executed.

The state of the s

40

60

Operating Temperature T_J [°C]

80

100

120

140

Figure A-2 Typical Endurance vs Temperature

Flash
----- EEPROM

50

0

-40

-20

0

20

And finally the frequency relationship is defined as

$$n = \frac{f_{VCO}}{f_{ref}} = 2 \cdot (synr + 1) = 50$$

With the above values the resistance can be calculated. The example is shown for a loop bandwidth f_C =10KHz:

$$R = \frac{2 \cdot \pi \cdot n \cdot f_{C}}{K_{\Phi}} = 2 \pi^{*} 50^{*} 10 \text{kHz} / (316.7 \text{Hz}/\Omega) = 9.9 \text{k}\Omega = \sim 10 \text{k}\Omega$$

The capacitance C_s can now be calculated as:

$$C_s = \frac{2 \cdot \zeta^2}{\pi \cdot f_C \cdot R} \approx \frac{0.516}{f_C \cdot R}; (\zeta = 0.9)$$
 = 5.19nF =~ 4.7nF

The capacitance C_p should be chosen in the range of:

$$C_s/20 \le C_p \le C_s/10$$
 $C_p = 470pF$

A.5.3.2 Jitter Information

The basic functionality of the PLL is shown in **Figure A-3**. With each transition of the clock f_{cmp} , the deviation from the reference clock f_{ref} is measured and input voltage to the VCO is adjusted accordingly. The adjustment is done continuously with no abrupt changes in the clock output frequency. Noise, voltage, temperature and other factors cause slight variations in the control loop resulting in a clock jitter. This jitter affects the real minimum and maximum clock periods as illustrated in **Figure A-4**.

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A.7.2 Slave Mode

Figure A-8 and Figure A-9 illustrate the slave mode timing. Timing values are shown in (Table A-19).

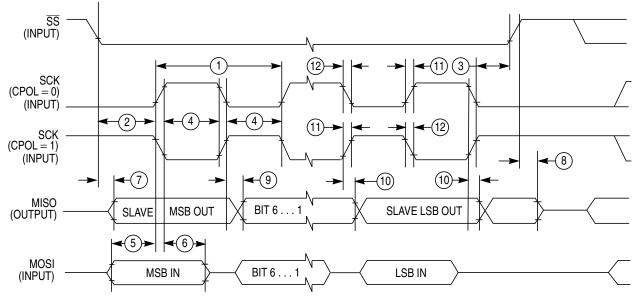


Figure A-8 SPI Slave Timing (CPHA = 0)

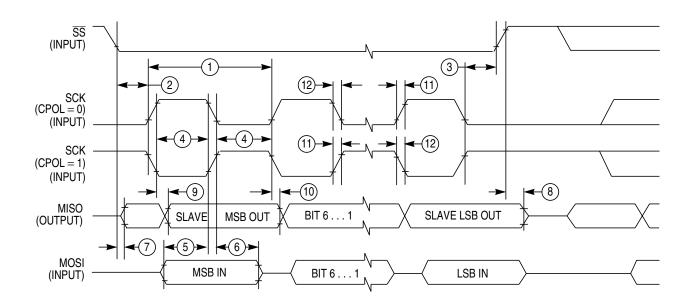


Figure A-9 SPI Slave Timing (CPHA =1)

A.8 External Bus Timing

A timing diagram of the external multiplexed-bus is illustrated in **Figure A-10** with the actual timing values shown on table **(Table A-20)**. All major bus signals are included in the diagram. While both a data write and data read cycle are shown, only one or the other would occur on a particular bus cycle.

A.8.1 General Multiplexed Bus Timing

The expanded bus timings are highly dependent on the load conditions. The timing parameters shown assume a balanced load across all outputs.